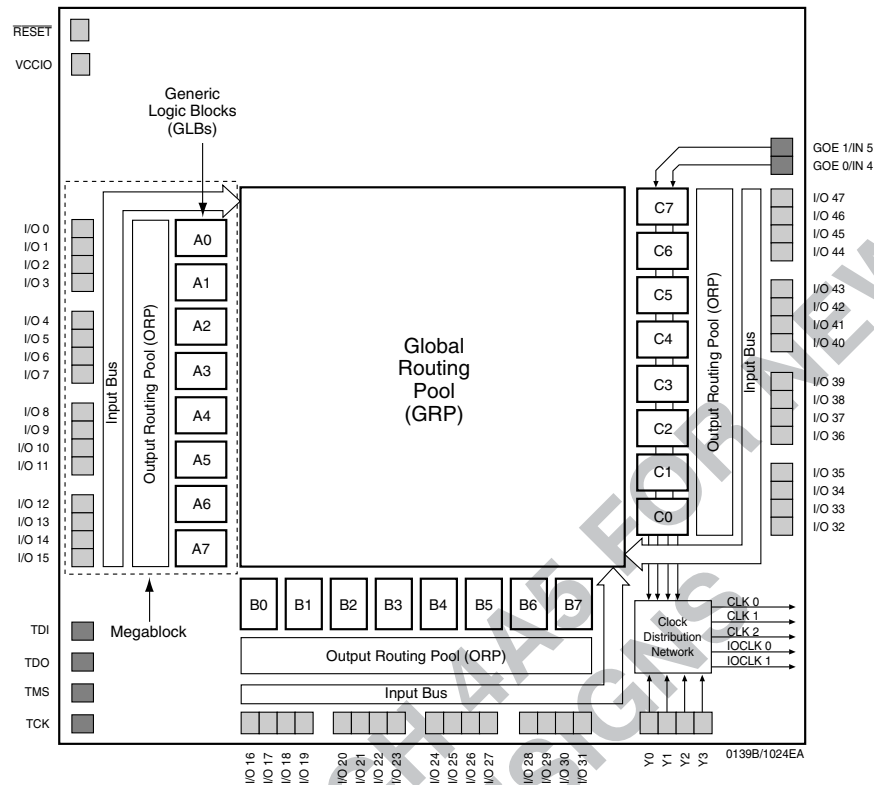


Functional Block Diagram

Figure 1. ispLSI 1024EA Functional Block Diagram



The device also has 48 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise. By connecting the VCCIO pin to a common 5V or 3.3V power supply, I/O output levels can be matched to 5V or 3.3V-compatible voltages.

Eight GLBs, 16 I/O cells, dedicated inputs (if available) and one ORP are connected together to make a Megablock (Figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. Each ispLSI 1024EA device contains three Megablocks.

The GRP has, as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

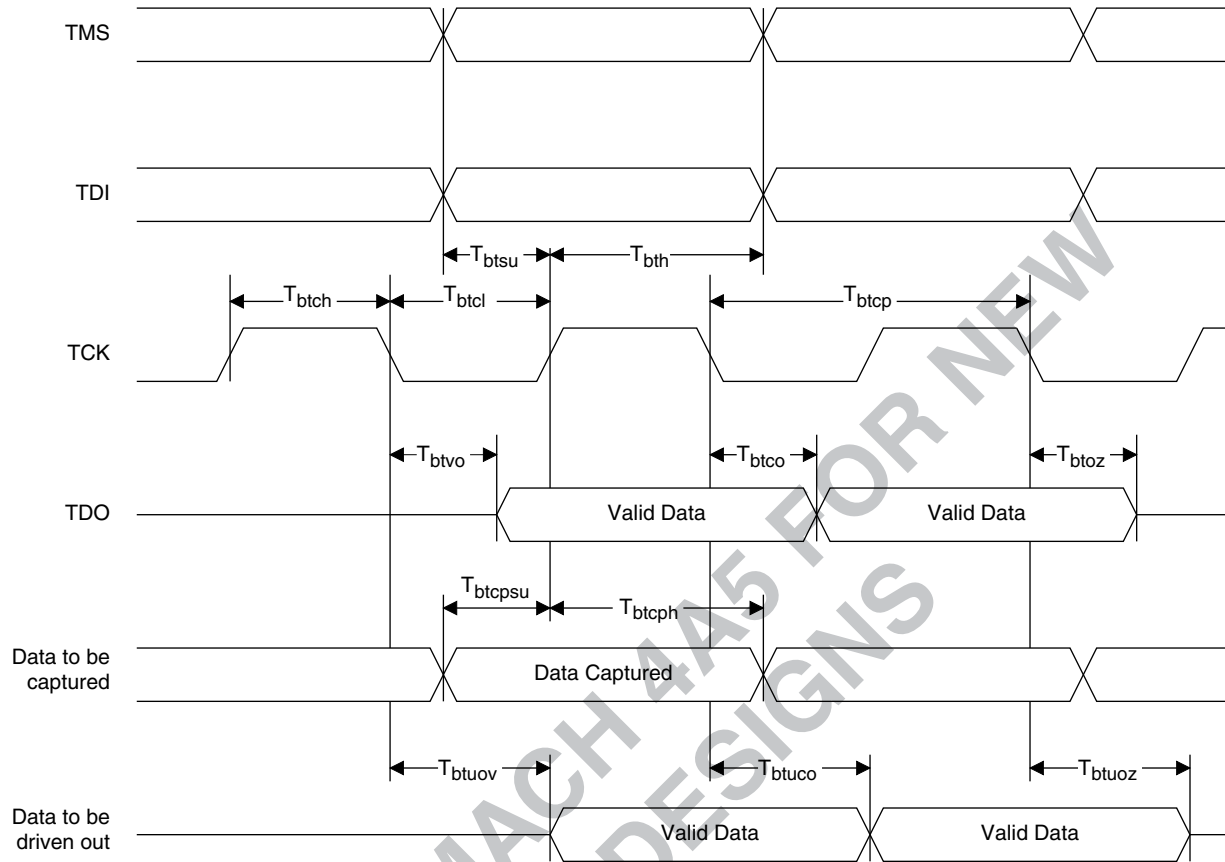
Clocks in the ispLSI 1024EA device are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (C0 on the ispLSI 1024EA device). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Programmable Open-Drain Outputs

In addition to the standard output configuration, the outputs of the ispLSI 1024EA are individually programmable, either as a standard totem-pole output or an open-drain output. The totem-pole output drives the specified Voh and Vol levels, whereas the open-drain output drives only the specified Vol. The Voh level on the open-drain output depends on the external loading and pull-up. This output configuration is controlled by a programmable fuse. The default configuration when the device is in bulk erased state is totem-pole configuration. The open-drain/totem-pole option is selectable through the Lattice software tools.

Boundary Scan

Figure 2. Boundary Scan Waveforms and Timing Specifications



| Symbol | Parameter | Min | Max | Units |
|-------------|--|-----|-----|-------|
| t_{btcp} | TCK [BSCAN test] clock pulse width | 100 | – | ns |
| t_{btch} | TCK [BSCAN test] pulse width high | 50 | – | ns |
| t_{btcl} | TCK [BSCAN test] pulse width low | 50 | – | ns |
| t_{btsu} | TCK [BSCAN test] setup time | 20 | – | ns |
| t_{bth} | TCK [BSCAN test] hold time | 25 | – | ns |
| t_{rf} | TCK [BSCAN test] rise and fall time | 50 | – | mV/ns |
| t_{btco} | TAP controller falling edge of clock to valid output | – | 25 | ns |
| t_{btoz} | TAP controller falling edge of clock to data output disable | – | 25 | ns |
| t_{btvo} | TAP controller falling edge of clock to data output enable | – | 25 | ns |
| t_{btcpu} | BSCAN test Capture register setup time | 40 | – | ns |
| t_{btcpu} | BSCAN test Capture register hold time | 25 | – | ns |
| t_{btuo} | BSCAN test Update reg, falling edge of clock to valid output | – | 50 | ns |
| t_{btuo} | BSCAN test Update reg, falling edge of clock to output disable | – | 50 | ns |
| t_{btuo} | BSCAN test Update reg, falling edge of clock to output enable | – | 50 | ns |

Absolute Maximum Ratings ¹

Supply Voltage V_{CC} -0.5 to +7.0V
 Input Voltage Applied -2.5 to $V_{CC} + 1.0V$
 Off-State Output Voltage Applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Case Temp. with Power Applied -55 to 125°C
 Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

| SYMBOL | PARAMETER | | MIN. | MAX. | UNITS |
|------------|--------------------------------|---|------|--------------|-------|
| V_{CC} | Supply Voltage | Commercial $T_A = 0^\circ C$ to $+70^\circ C$ | 4.75 | 5.25 | V |
| V_{CCIO} | Supply Voltage: Output Drivers | 5V | 4.75 | 5.25 | V |
| | | 3.3V | 3.0 | 3.6 | V |
| V_{IL} | Input Low Voltage | | 0 | 0.8 | V |
| V_{IH} | Input High Voltage | | 2.0 | $V_{CC} + 1$ | V |

Table 2-0005/1024EA

Capacitance ($T_A = 25^\circ C$, $f = 1.0$ MHz)

| SYMBOL | PARAMETER | TYPICAL | UNITS | TEST CONDITIONS |
|--------|---|---------|-------|------------------------------------|
| C_1 | Dedicated Input, I/O, Y1, Y2, Y3, Clock Capacitance (Commercial/Industrial) | 8 | pf | $V_{CC} = 5.0V$, $V_{PIN} = 2.0V$ |
| C_2 | Y0 Clock Capacitance | 10 | pf | $V_{CC} = 5.0V$, $V_{PIN} = 2.0V$ |

Table 2-0006/1024EA

Erase/Reprogram Specifications

| PARAMETER | MINIMUM | MAXIMUM | UNITS |
|------------------------|---------|---------|--------|
| Erase/Reprogram Cycles | 10000 | — | Cycles |

Table 2-0008/1024EA

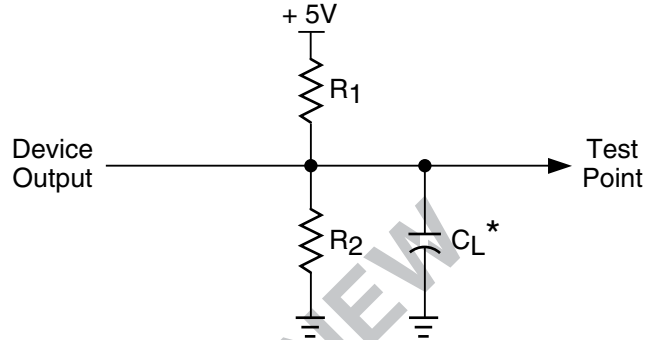
Switching Test Conditions

| | |
|-------------------------------------|--------------|
| Input Pulse Levels | GND to 3.0V |
| Input Rise and Fall Time 10% to 90% | 1.5ns |
| Input Timing Reference Levels | 1.5V |
| Output Timing Reference Levels | 1.5V |
| Output Load | See Figure 3 |

3-state levels are measured 0.5V from steady-state active level.

Table 2-0003/1024EA

Figure 3. Test Load



*CL includes Test Fixture and Probe Capacitance.

0213a

Output Load Conditions (see Figure 3)

| TEST CONDITION | | R1 | R2 | CL |
|----------------|-----------------------------------|------|------|------|
| A | | 470Ω | 390Ω | 35pF |
| B | Active High | ∞ | 390Ω | 35pF |
| | Active Low | 470Ω | 390Ω | 35pF |
| C | Active High to Z at $V_{OH}-0.5V$ | ∞ | 390Ω | 5pF |
| | Active Low to Z at $V_{OL}+0.5V$ | 470Ω | 390Ω | 5pF |

Table 2-0004/1024EA

DC Electrical Characteristics

Over Recommended Operating Conditions

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP. ³ | MAX. | UNITS |
|---------------------------------------|-----------------------------------|--|------|-------------------|------|-------|
| V_{OL} | Output Low Voltage | $I_{OL} = 8 \text{ mA}$ | — | — | 0.4 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -2 \text{ mA}, V_{CCIO} = 3.0V$ | 2.4 | — | — | V |
| | | $I_{OH} = -4 \text{ mA}, V_{CCIO} = 4.75V$ | 2.4 | — | — | V |
| I_{IL} | Input or I/O Low Leakage Current | $0V \leq V_{IN} \leq V_{IL} \text{ (Max.)}$ | — | — | -10 | μA |
| I_{IH} | Input or I/O High Leakage Current | $(V_{CCIO} - 0.2)V \leq V_{IN} \leq V_{CCIO}$ | — | — | 10 | μA |
| | | $V_{CCIO} \leq V_{IN} \leq 5.25V$ | — | — | 10 | μA |
| I_{IL-PU} | I/O Active Pull-Up Current | $0V \leq V_{IN} \leq V_{IL}$ | — | — | -200 | μA |
| I_{OS}¹ | Output Short Circuit Current | $V_{CCIO} = 5.0V \text{ or } 3.3V, V_{OUT} = 0.5V$ | — | — | -240 | mA |
| I_{CC}^{2,4,5} | Operating Power Supply Current | $V_{IL} = 0.0V, V_{IH} = 3.0V$ $f_{TOGGLE} = 1 \text{ MHz}$ | — | 152 | — | mA |

Table 2-0007/1024EA

- One output at a time for a maximum duration of one second. $V_{OUT} = 0.5V$ was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
- Measured using eight 16-bit counters.
- Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$.
- Unused inputs held at 0.0V.
- Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and the Thermal Management section of the Lattice Semiconductor Data Book CD-ROM to estimate maximum I_{CC} .

External Timing Parameters

Over Recommended Operating Conditions

| PARAMETER | TEST COND. ⁴ | # ² | DESCRIPTION ¹ | -200 | | -125 | | -100 | | UNITS |
|-------------------------|-------------------------|----------------|--|------|------|------|------|------|------|-------|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{pd1} | A | 1 | Data Propagation Delay, 4PT Bypass, ORP Bypass | — | 4.5 | — | 7.5 | — | 10.0 | ns |
| t _{pd2} | A | 2 | Data Propagation Delay, Worst Case Path | — | 6.0 | — | 10.0 | — | 12.5 | ns |
| f _{max} (Int.) | A | 3 | Clock Frequency with Internal Feedback ³ | 200 | — | 125 | — | 100 | — | MHz |
| f _{max} (Ext.) | — | 4 | Clock Frequency with External Feedback ($\frac{1}{t_{su2} + t_{co1}}$) | 143 | — | 100 | — | 77 | — | MHz |
| f _{max} (Tog.) | — | 5 | Clock Frequency, Max. Toggle ($\frac{1}{t_{wh} + t_{wl}}$) | 250 | — | 167 | — | 125 | — | MHz |
| t _{su1} | — | 6 | GLB Reg. Setup Time before Clock, 4 PT Bypass | 3.0 | — | 4.5 | — | 6.0 | — | ns |
| t _{co1} | A | 7 | GLB Reg. Clock to Output Delay, ORP Bypass | — | 3.5 | — | 4.5 | — | 6.0 | ns |
| t _{h1} | — | 8 | GLB Reg. Hold Time after Clock, 4 PT Bypass | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| t _{su2} | — | 9 | GLB Reg. Setup Time before Clock | 3.5 | — | 5.5 | — | 7.0 | — | ns |
| t _{co2} | — | 10 | GLB Reg. Clock to Output Delay | — | 4.0 | — | 5.5 | — | 7.0 | ns |
| t _{h2} | — | 11 | GLB Reg. Hold Time after Clock | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| t _{r1} | A | 12 | Ext. Reset Pin to Output Delay | — | 5.5 | — | 10.0 | — | 13.5 | ns |
| t _{rw1} | — | 13 | Ext. Reset Pulse Duration | 3.5 | — | 5.0 | — | 6.5 | — | ns |
| t _{ptoen} | B | 14 | Input to Output Enable | — | 7.0 | — | 12.0 | — | 15.0 | ns |
| t _{ptoedis} | C | 15 | Input to Output Disable | — | 7.0 | — | 12.0 | — | 15.0 | ns |
| t _{goeen} | B | 16 | Global OE Output Enable | — | 4.5 | — | 7.0 | — | 9.0 | ns |
| t _{goedis} | C | 17 | Global OE Output Disable | — | 4.5 | — | 7.0 | — | 9.0 | ns |
| t _{wh} | — | 18 | External Synchronous Clock Pulse Duration, High | 2.0 | — | 3.0 | — | 4.0 | — | ns |
| t _{wl} | — | 19 | External Synchronous Clock Pulse Duration, Low | 2.0 | — | 3.0 | — | 4.0 | — | ns |
| t _{su3} | — | 20 | I/O Reg. Setup Time before Ext. Sync Clock (Y2, Y3) | 3.0 | — | 3.0 | — | 3.5 | — | ns |
| t _{h3} | — | 21 | I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3) | 0.0 | — | 0.0 | — | 0.0 | — | ns |

1. Unless noted otherwise, all parameters use a GRP load of four GLBs, 20 PTXOR path, ORP and Y0 clock. Table 2-0030A/1024EA v.2.5
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Internal Timing Parameters¹

| PARAM. | # ² | DESCRIPTION | -200 | | -125 | | -100 | | UNITS |
|----------------------|----------------|--|------|------|------|------|------|------|-------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Inputs | | | | | | | | | |
| t _{iobp} | 22 | I/O Register Bypass | — | 0.3 | — | 0.3 | — | 0.4 | ns |
| t _{iolat} | 23 | I/O Latch Delay | — | 4.0 | — | 4.0 | — | 4.0 | ns |
| t _{iosu} | 24 | I/O Register Setup Time before Clock | 3.0 | — | 3.0 | — | 3.4 | — | ns |
| t _{ioh} | 25 | I/O Register Hold Time after Clock | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| t _{ioco} | 26 | I/O Register Clock to Out Delay | — | 4.0 | — | 4.6 | — | 5.0 | ns |
| t _{ior} | 27 | I/O Register Reset to Out Delay | — | 4.0 | — | 4.6 | — | 5.0 | ns |
| t _{din} | 28 | Dedicated Input Delay | — | 1.1 | — | 1.9 | — | 2.2 | ns |
| GRP | | | | | | | | | |
| t _{grp1} | 29 | GRP Delay, 1 GLB Load | — | 1.3 | — | 1.7 | — | 2.1 | ns |
| t _{grp4} | 30 | GRP Delay, 4 GLB Loads | — | 1.5 | — | 1.9 | — | 2.3 | ns |
| t _{grp8} | 31 | GRP Delay, 8 GLB Loads | — | 1.7 | — | 2.1 | — | 2.5 | ns |
| t _{grp16} | 32 | GRP Delay, 16 GLB Loads | — | 2.1 | — | 2.5 | — | 2.9 | ns |
| t _{grp24} | 33 | GRP Delay, 24 GLB Loads | — | 2.5 | — | 2.9 | — | 3.3 | ns |
| GLB | | | | | | | | | |
| t _{4ptbpc} | 34 | 4 ProductTerm Bypass Path Delay (Combinatorial) | — | 1.7 | — | 3.4 | — | 4.9 | ns |
| t _{4ptbpr} | 35 | 4 Product Term Bypass Path Delay (Registered) | — | 1.8 | — | 3.1 | — | 3.8 | ns |
| t _{1ptxor} | 36 | 1 ProductTerm/XOR Path Delay | — | 1.9 | — | 3.6 | — | 4.3 | ns |
| t _{20ptxor} | 37 | 20 Product Term/XOR Path Delay | — | 1.9 | — | 3.6 | — | 4.3 | ns |
| t _{xoradj} | 38 | XOR Adjacent Path Delay ³ | — | 1.9 | — | 3.6 | — | 4.3 | ns |
| t _{gbp} | 39 | GLB Register Bypass Delay | — | 0.6 | — | 1.2 | — | 2.1 | ns |
| t _{gsu} | 40 | GLB Register Setup Time before Clock | 0.2 | — | 0.3 | — | 1.4 | — | ns |
| t _{gh} | 41 | GLB Register Hold Time after Clock | 1.0 | — | 3.5 | — | 4.0 | — | ns |
| t _{gco} | 42 | GLB Register Clock to Output Delay | — | 1.4 | — | 1.4 | — | 1.7 | ns |
| t _{gro} | 43 | GLB Register Reset to Output Delay | — | 3.8 | — | 4.9 | — | 5.0 | ns |
| t _{ptre} | 44 | GLB Product Term Reset to Register Delay | — | 2.5 | — | 3.8 | — | 4.5 | ns |
| t _{ptoe} | 45 | GLB Product Term Output Enable to I/O Cell Delay | — | 2.1 | — | 5.7 | — | 7.2 | ns |
| t _{ptck} | 46 | GLB Product Term Clock Delay | 1.5 | 2.5 | 2.8 | 3.9 | 3.5 | 4.7 | ns |
| t _{gfb} | 47 | GLB Feedback Delay | — | 0.0 | — | 0.3 | — | 0.3 | ns |
| ORP | | | | | | | | | |
| t _{orp} | 48 | ORP Delay | — | 0.8 | — | 1.3 | — | 1.4 | ns |
| t _{orpbp} | 49 | ORP Bypass Delay | — | 0.1 | — | 0.2 | — | 0.4 | ns |

1. Internal Timing Parameters are not tested and are for reference only.

2. Refer to Timing Model in this data sheet for further details.

3. The XOR adjacent path can only be used by hard macros.

Table 2-0036A/1024EA
v.2.5

Internal Timing Parameters¹

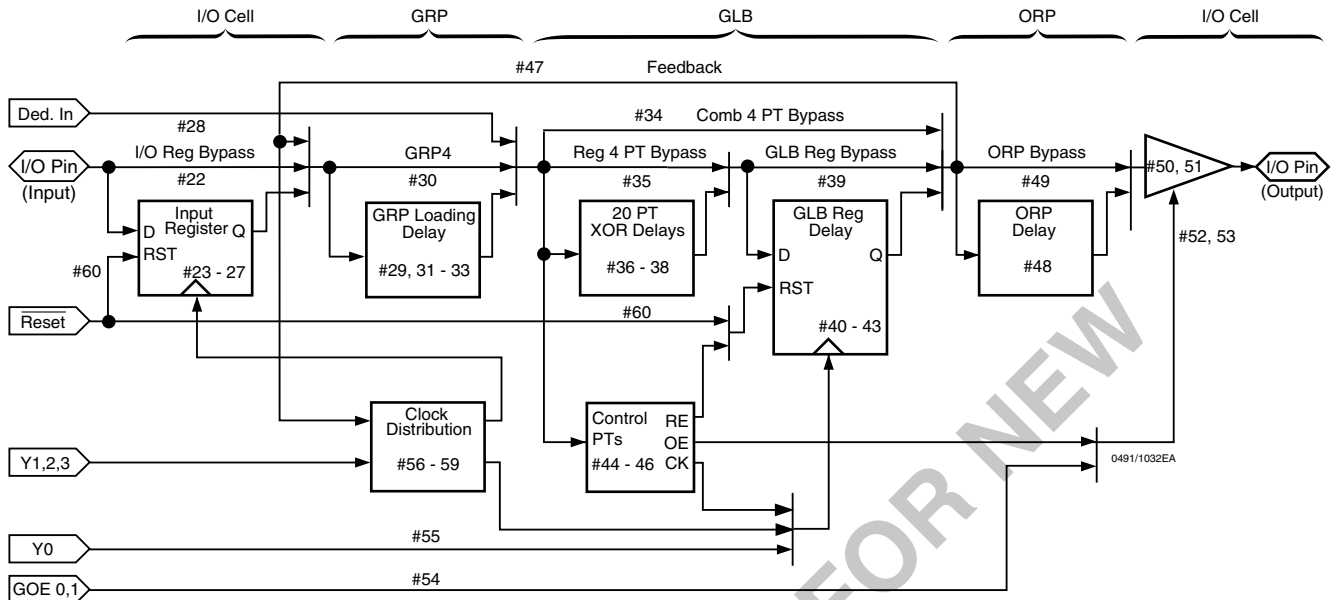
| PARAM. | # | DESCRIPTION | -200 | | -125 | | -100 | | UNITS |
|---------------------------|----|--|------|------|------|------|------|------|-------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Outputs | | | | | | | | | |
| t_{ob} | 50 | Output Buffer Delay | — | 0.9 | — | 1.7 | — | 2.0 | ns |
| t_{sl} | 51 | Output Buffer Delay, Slew Limited Adder | — | 5.0 | — | 5.0 | — | 5.0 | ns |
| t_{oen} | 52 | I/O Cell OE to Output Enabled | — | 3.1 | — | 4.0 | — | 5.1 | ns |
| t_{odis} | 53 | I/O Cell OE to Output Disabled | — | 3.1 | — | 4.0 | — | 5.1 | ns |
| t_{goe} | 54 | Global OE | — | 1.4 | — | 3.0 | — | 3.9 | ns |
| Clocks | | | | | | | | | |
| t_{gy0} | 55 | Clock Delay, Y0 to Global GLB Clock Line (Ref. clk) | 0.9 | 0.9 | 1.1 | 1.1 | 1.9 | 1.9 | ns |
| t_{gy1/2} | 56 | Clock Delay, Y1 or Y2 to Global GLB Clock Line | 0.9 | 0.9 | 0.9 | 0.9 | 1.5 | 1.5 | ns |
| t_{gcp} | 57 | Clock Delay, Clock GLB to Global GLB Clock Line | 0.8 | 1.8 | 0.8 | 1.8 | 0.8 | 1.8 | ns |
| t_{ioy2/3} | 58 | Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | ns |
| t_{iocp} | 59 | Clock Delay, Clock GLB to I/O Cell Global Clock Line | 0.8 | 2.8 | 0.8 | 2.8 | 0.8 | 2.8 | ns |
| Global Reset | | | | | | | | | |
| t_{gr} | 60 | Global Reset to GLB and I/O Registers | — | 0.0 | — | 2.1 | — | 5.1 | ns |

1. Internal Timing Parameters are not tested and are for reference only.

Table 2-0037A/1024EA
v.2.5

USE ISPMACH 4A5 FOR NEW 5V DESIGNS

ispLSI 1024EA Timing Model



Derivations of t_{su} , t_h and t_{co} from the Product Term Clock¹

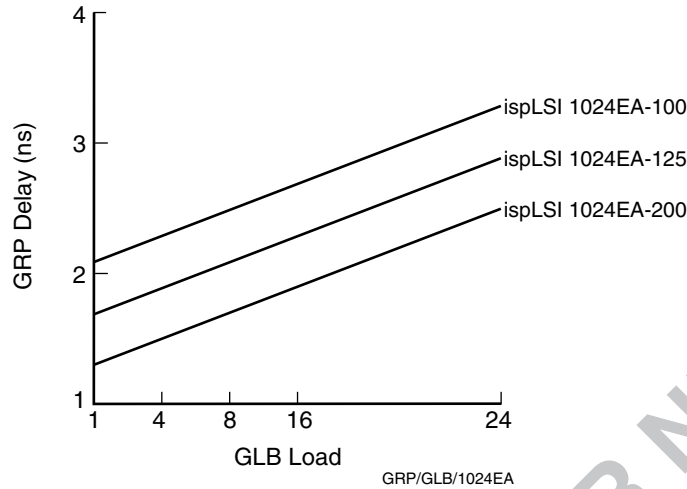
$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } s_u - \text{Clock (min)} \\
 &= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)}) \\
 &= (\#22 + \#30 + \#37) + (\#40) - (\#22 + \#30 + \#46) \\
 0.6 &= (0.3 + 1.5 + 1.9) + (0.2) - (0.3 + 1.5 + 1.5) \\
 \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
 &= (\#22 + \#30 + \#46) + (\#41) - (\#22 + \#30 + \#37) \\
 1.6 &= (0.3 + 1.5 + 2.5) + (1.0) - (0.3 + 1.5 + 1.9) \\
 \\
 t_{co} &= \text{Clock (max)} + \text{Reg } c_o + \text{Output} \\
 &= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#22 + \#30 + \#46) + (\#42) + (\#48 + \#50) \\
 7.4 &= (0.3 + 1.5 + 2.5) + (1.4) + (0.8 + 0.9)
 \end{aligned}$$

Derivations of t_{su} , t_h and t_{co} from the Clock GLB¹

$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg (setup)} - \text{Clock (min)} \\
 &= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)}) \\
 &= (\#22 + \#30 + \#37) + (\#40) - (\#55 + \#42 + \#57) \\
 0.8 &= (0.3 + 1.5 + 1.9) + (0.2) - (0.9 + 1.4 + 0.8) \\
 \\
 t_h &= \text{Clock (max)} + \text{Reg (hold)} - \text{Logic} \\
 &= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
 &= (\#55 + \#42 + \#57) + (\#41) - (\#22 + \#30 + \#37) \\
 1.4 &= (0.9 + 1.4 + 1.8) + (1.0) - (0.3 + 1.5 + 1.9) \\
 \\
 t_{co} &= \text{Clock (max)} + \text{Reg (clock-to-out)} + \text{Output} \\
 &= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#55 + \#42 + \#57) + (\#42) + (\#48 + \#50) \\
 7.2 &= (0.9 + 1.4 + 1.8) + (1.4) + (0.8 + 0.9)
 \end{aligned}$$

1. Calculations are based upon timing specifications for the ispLSI 1024EA-200.

Maximum GRP Delay vs GLB Loads

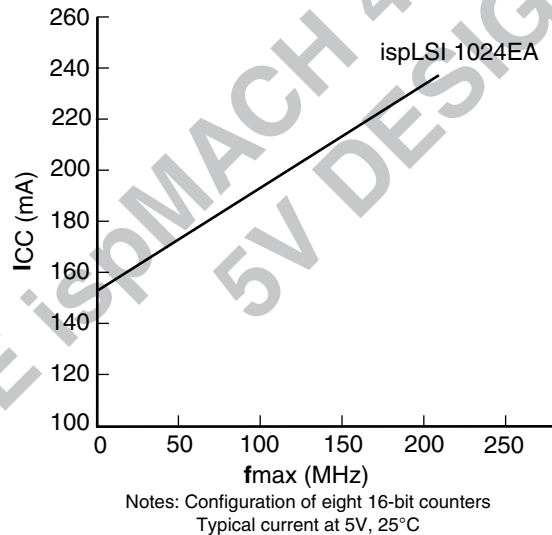


Power Consumption

Power consumption in the ispLSI 1024EA device depends on two primary factors: the speed at which the device is operating, and the number of product terms

used. Figure 4 shows the relationship between power and operating speed.

Figure 4. Typical Device Power Consumption vs fmax



Icc can be estimated for the ispLSI 1024EA using the following equation:

$$I_{cc} = 17\text{mA} + (\# \text{ of PTs} * .726) + (\# \text{ of nets} * \text{Max Freq} * .0043)$$

Where:

- # of PTs = Number of Product Terms used in design
- # of nets = Number of Signals used in device
- Max freq = Highest Clock Frequency to the device (in MHz)

The Icc estimate is based on typical conditions (Vcc = 5.0V, room temperature) and an assumption of four GLB loads on average exists. These values are for estimates only. Since the value of Icc is sensitive to operating conditions and the program in the device, the actual Icc should be verified.

Pin Description

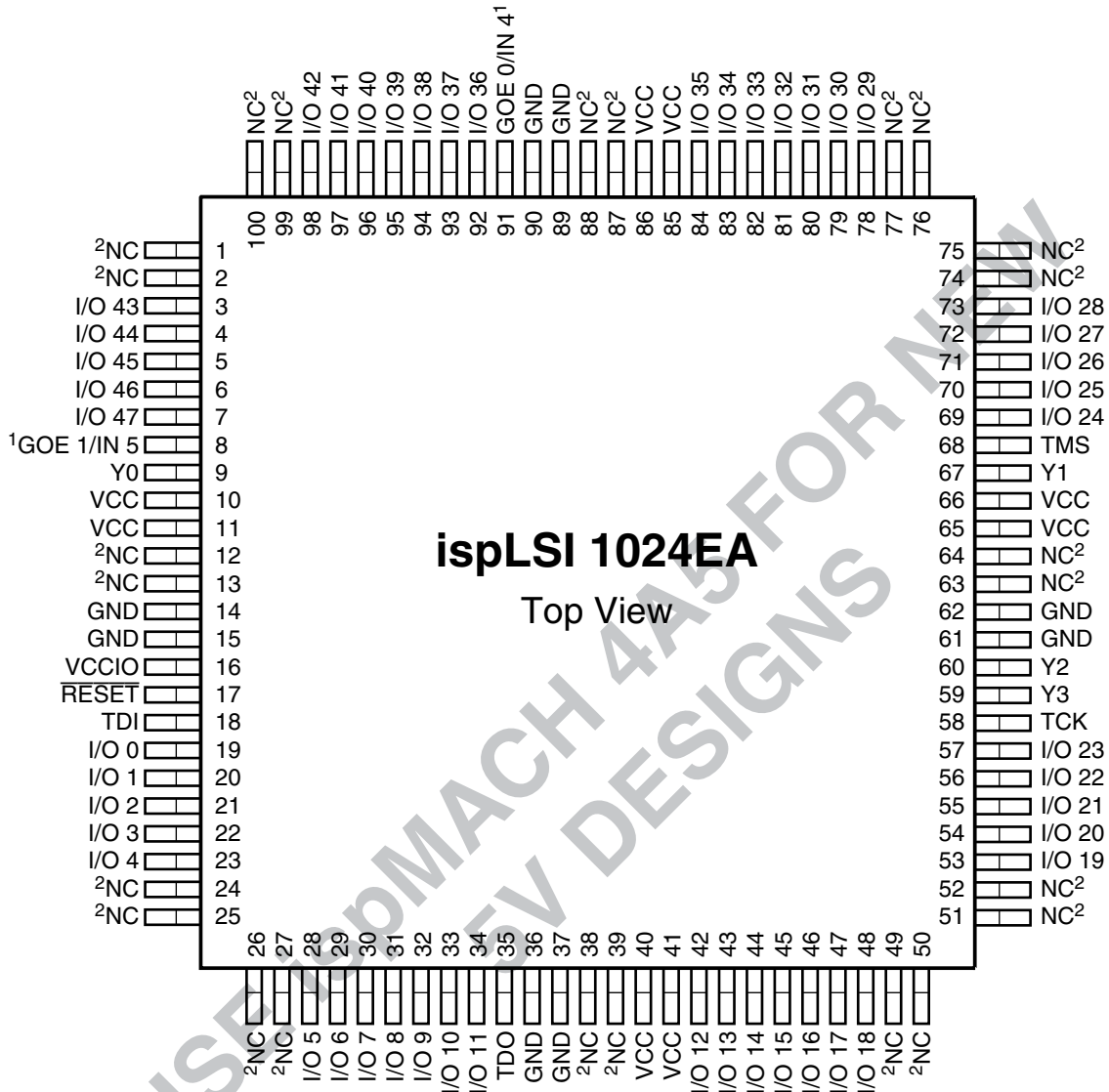
| NAME | TQFP PIN NUMBERS | DESCRIPTION |
|---|--|--|
| I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 I/O 32 - I/O 35 I/O 36 - I/O 39 I/O 40 - I/O 43 I/O 44 - I/O 47 | 19, 20, 21, 22, 23, 28, 29, 30, 31, 32, 33, 34, 42, 43, 44, 45, 46, 47, 48, 53, 54, 55, 56, 57, 69, 70, 71, 72, 73, 78, 79, 80, 81, 82, 83, 84, 92, 93, 94, 95, 96, 97, 98, 3, 4, 5, 6, 7 | Input/Output Pins - These are the general purpose I/O pins used by the logic array. |
| GOE 0/IN 4 ¹ | 91 | This is a dual function pin. It can be used either as Global Output Enable for all I/O cells or it can be used as a dedicated input pin. |
| GOE 1/IN 5 ¹ | 8 | This is a dual function pin. It can be used either as Global Output Enable for all I/O cells or it can be used as a dedicated input pin. |
| TDI | 18 | Input - Functions as an input pin to load programming data into the device and also used as one of the two control pins for the ispJTAG state machine. |
| TMS | 68 | Input - Controls the operation of the ISP state machine. |
| TDO | 35 | Output - Functions as an output pin to read serial shift register data. |
| TCK | 58 | Input - Functions as a clock pin for the Serial Shift Register. |
| RESET | 17 | Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device. |
| Y0 | 9 | Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device. |
| Y1 | 67 | Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device. |
| Y2 | 60 | Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device. |
| Y3 | 59 | Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device. |
| GND | 14, 15, 36, 37, 61, 62, 89, 90 | Ground (GND) |
| VCC | 10, 11, 40, 41, 65, 66, 85, 86 | Vcc |
| VCCIO | 16 | Supply voltage for output drivers, 5V or 3.3V. |
| NC ² | 1, 2, 12, 13, 24, 25, 26, 27, 38, 39, 49, 50, 51, 52, 63, 64, 74, 75, 76, 77, 87, 88, 99, 100 | No Connect |

1. Pins have dual function capability which is software selectable.
2. NC pins are not to be connected to any active signals, Vcc or GND.

Table 2-0002A/1024EA

Pin Configurations

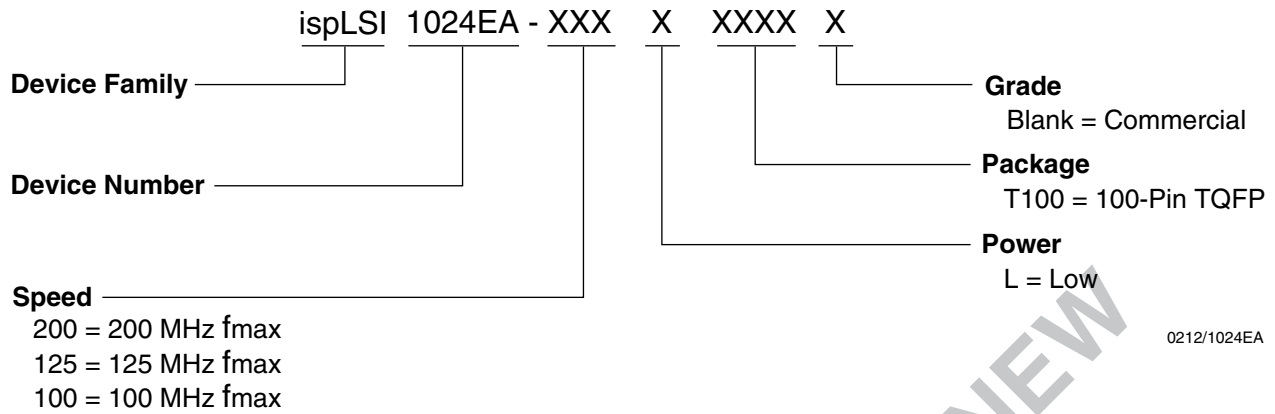
ispLSI 1024EA 100-Pin TQFP Pinout Diagram



1. Pins have dual function capability which is software selectable.
2. NC pins are not to be connected to any active signal, VCC or GND.

100-TQFP/1024EA

Part Number Description



ispLSI 1024EA Ordering Information

COMMERCIAL

| FAMILY | fmax (MHz) | tpd (ns) | ORDERING NUMBER | PACKAGE |
|--------|------------|----------|------------------------|--------------|
| ispLSI | 200 | 4.5 | ispLSI 1024EA-200LT100 | 100-Pin TQFP |
| | 125 | 7.5 | ispLSI 1024EA-125LT100 | 100-Pin TQFP |
| | 100 | 10 | ispLSI 1024EA-100LT100 | 100-Pin TQFP |

Table 2-0041A/1024EA

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for [CPLD - Complex Programmable Logic Devices](#) category:

Click to view products by [Lattice](#) manufacturer:

Other Similar products are found below :

[5962-9952001QYA](#) [5M1270ZT144I5](#) [M4A5-12864-10YNI](#) [M4A5-12864-12YNI](#) [M4A5-3232-5VNC](#) [M4A5-6432-7VNC](#) [M4A5-6432-7VNI](#)
[CY3LV002-10JC](#) [CY7C344B-15JI](#) [EPM7064LC68-10](#) [ISPLSI 1032-90LJ](#) [ISPLSI 1048-70LQ](#) [LA4064V-75TN44E](#) [LC4064ZC-5MN56C](#)
[M4A3-3232-10VC](#) [M4A5-256128-12YNI](#) [MACH435Q-20JC](#) [ISPLSI 1032-60LJ](#) [ISPLSI 1032-80LJ](#) [ISPLSI 1048-50LQ](#) [LA4032V-75TN44E](#)
[LC4032ZC-5MN56I](#) [5962-9759901QZC](#) [XC95288XL-10CS280I](#) [LC4032ZC-75MN56I](#) [LC5512MV-45F256C](#) [M4A5-6432-10VNI](#)
[ISPLSI2096A-80LT128I](#) [M4A3-256192-10FAI](#) [LA4128V-75TN128E](#) [ISPLSI5256VA-100LB208](#) [M4A3-3232-5VC48](#) [M4A3-64/32-](#)
[12VNI48](#) [CP4878DM](#) [M4A3-256/160-7YC](#) [M4A3-256/192-7FAC](#) [M4A3-32/32-10VNC48](#) [M4A3-384/192-10FANC](#) [M4A3-512/160-14YI](#)
[M4A3-512/192-7FAC](#) [M4A3-64/32-10VNC](#) [M4A5-128/64-7YI](#) [M4A5-192/96-10VC](#) [M4A5-192/96-10VI](#) [M4A5-256/128-10YNC](#) [M4A5-](#)
[256/128-7YC](#) [M4A5-32/32-10VC](#) [M4A5-64/32-10VNC](#) [M5-192/120-10YI/1](#) [M5-320/160-10YI](#)