MachXO3 Family Data Sheet

Data Sheet

FPGA-DS-02032-2.5

March 2020

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AES	Advanced Encryption Standard
BGA	Ball Grid Array
CMOS	Complementary Metal Oxide Semiconductor
EBR	Embedded Block RAM
ECDSA	Elliptic Curve Digital Signature Algorithm
ECLK	Edge Clock
ESB	Embedded Security Block
I^2C	Inter-Integrated Circuit
LUT	Look-Up Table
LVCMOS	Low-Voltage CMOS
PCLK	Primary Clock
PFU	Programmable Functional Unit
PLL	Phase Locked Loop
SHA	Secure Hash Algorithm
SPI	Serial Peripheral Interface

1. Introduction

MachXO3™ device family is an Ultra-Low Density family that supports the most advanced programmable bridging and I/O expansion. It has the breakthrough I/O density and the lowest cost per I/O. The device I/O features have the integrated support for latest industry standard I/O.

The MachXO3L/LF family of low power, instant-on, non-volatile PLDs has five devices with densities ranging from 640 to 9400 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I^2C controller and timer/counter. MachXO3LF devices also support User Flash Memory (UFM). These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO3L/LF devices are designed on a 65nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO3L/LF devices are available in two versions C and E with two speed grades: -5 and -6, with -6 being the fastest. C devices have an internal linear voltage regulator which supports external VCC supply voltages of 3.3 V or 2.5 V. E devices only accept 1.2 V as the external VCC supply voltage. With the exception of power supply voltage both C and E are functionally compatible with each other.

The MachXO3L/LF PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5 x 2.5 mm WLCSP to the 19 x 19 mm caBGA. MachXO3L/LF devices support density migration within the same package. Table 1.1 shows the LUT densities, package and I/O options, along with other key parameters.

The MachXO3L/LF devices offer enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pull-down and bus-keeper features are controllable on a “per-pin” basis. A user-programmable internal oscillator is included in MachXO3L/LF devices. The clock output from this oscillator may be divided by the timer/counter for use as clock input in functions such as LED control, keyboard scanner and similar state machines.

The MachXO3L/LF devices also provide flexible, reliable and secure configuration from on-chip NVCM/Flash. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the I^2C port. Additionally, MachXO3L/LF devices support dual-boot capability (using external Flash memory) and remote field upgrade (TransFR) capability.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO3L/LF family of devices. Popular logic synthesis tools provide synthesis library support for MachXO3L/LF. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO3L/LF device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) LatticeCORE™ modules, including a number of reference designs licensed free of charge, optimized for the MachXO3L/LF PLD family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

1.1. Features

1.1.1. Solutions

- Smallest footprint, lowest power, high data throughput bridging solutions for mobile applications
- Optimized footprint, logic density, I/O count, I/O performance devices for I/O management and logic applications
- High I/O logic, lowest cost I/O, high I/O devices for I/O expansion applications

1.1.2. Flexible Architecture

- Logic Density ranging from 64 to 9.4K LUT4
- High I/O to LUT ratio with up to 384 I/O pins

1.1.3. Advanced Packaging

- 0.4 mm pitch: 1K to 4K densities in very small footprint WLCSP (2.5 mm × 2.5 mm to 3.8 mm × 3.8 mm) with 28 to 63 I/Os
- 0.5 mm pitch: 640 to 9.4K LUT densities in 6 mm x 6 mm to 10 mm x 10 mm BGA packages with up to 281 I/Os
- 0.8 mm pitch: 1K to 9.4K densities with up to 384 I/Os in BGA packages

1.1.4. Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells
- Dedicated gearing logic
- 7:1 Gearing for Display I/Os
- Generic DDR, DDRx2, DDRx4

1.1.5. High Performance, Flexible I/O Buffer

- Programmable sysI/O™ buffer supports wide range of interfaces:
  - LVCMOS 3.3/2.5/1.8/1.5/1.2
  - LVTTL
  - LVDS, Bus-LVDS, MLVDS, LVPECL
  - MIPI D-PHY Emulated
  - Schmitt trigger inputs, up to 0.5 V hysteresis
- Ideal for I/O bridging applications
- I/Os support hot socketing
- On-chip differential termination
- Programmable pull-up or pull-down mode

1.1.6. Flexible On-Chip Clocking

- Eight primary clocks
- Up to two edge clocks for high-speed I/O interfaces (top and bottom sides only)
- Up to two analog PLLs per device with fractional-n frequency synthesis
  - Wide input frequency range (7 MHz to 400 MHz).

1.1.7. Non-volatile, Multi-time Programmable

- Instant-on
  - Powers up in microseconds
- Optional dual boot with external SPI memory
- Single-chip, secure solution
- Programmable through JTAG, SPI or I2C
- MachXO3L includes multi-time programmable
- NVCM
- MachXO3LF reconfigurable Flash includes 100,000 write/erase cycle
  - Supports background programming of non volatile memory

1.1.8. TransFR Reconfiguration

- In-field logic update while I/O holds the system state

1.1.9. Enhanced System Level Support

- On-chip hardened functions: SPI, I2C, timer/counter
- On-chip oscillator with 5.5% accuracy
- Unique TraceID for system tracking
- Single power supply with extended operating range
- IEEE Standard 1149.1 boundary scan
- IEEE 1532 compliant in-system programming

1.1.10. Applications

- Consumer Electronics
- Compute and Storage
- Wireless Communications
- Industrial Control Systems
- Automotive System

1.1.11. Low Cost Migration Path

- Migration from the Flash based MachXO3LF to the NVCM based MachXO3L
- Pin compatible and equivalent timing

Table 1.1. MachXO3L/LF Family Selection Guide

Features		MachXO3L-640/ MachXO3LF-640	MachXO3L-1300/ MachXO3LF-1300	MachXO3L-2100/ MachXO3LF-2100	MachXO3L-4300/ MachXO3LF-4300	MachXO3L-6900/ MachXO3LF-6900	MachXO3L-9400/ MachXO3LF-9400
LUTs		640	1300	2100	4300	6900[4]	9400[4]
Distributed RAM (kb)		5	10	16	34	54	73
EBR SRAM (kb)		64	64	74	92	240	432
UFM (kb, MachXO3LF only)		64	64	80	96	256	448
Device Options	C[5]	—	Yes	Yes	Yes	Yes	Yes
	E[6]	Yes	Yes	Yes	Yes	Yes	Yes
Number of PLLs		1	1	1	2	2	2
Hardened Functions	I²C	2	2	2	2	2	2
	SPI	1	1	1	1	1	1
	Timer/ Counter	1	1	1	1	1	1
	Oscillator	1	1	1	1	1	1
MIPI D-PHY Support		Yes	Yes	Yes	Yes	Yes	Yes
Multi Time Programmable NVCM		MachXO3L-640	MachXO3L-1300	MachXO3L-2100	MachXO3L-4300	MachXO3L-6900	MachXO3L-9400
Programmable Flash		MachXO3LF-640	MachXO3LF-1300	MachXO3LF-2100	MachXO3LF-4300	MachXO3LF-6900	MachXO3LF-9400

Packages	I/O					
36-ball WLCSP[1] (2.5 mm x 2.5 mm, 0.4 mm)		28				
49-ball WLCSP[1] (3.2 mm x 3.2 mm, 0.4 mm)			38			
81-ball WLCSP[1] (3.8 mm x 3.8 mm, 0.4 mm)				63		
121-ball csfBGA[1] (6 mm x 6 mm, 0.5 mm)	100	100	100	100		
256-ball csfBGA[1] (9 mm x 9 mm, 0.5 mm)		206	206	206	206	206
324-ball csfBGA[1] (10 mm x 10 mm, 0.5 mm)			268	268	281	
256-ball caBGA (14 mm x 14 mm, 0.8 mm)		206[2]	206[2]	206[2]	206[2]	206[3]
324-ball caBGA[2] (15 mm x 15 mm, 0.8 mm)			279	279	279	
400-ball caBGA (17 mm x 17 mm, 0.8 mm)				335[2]	335[2]	335[3]
484-ball caBGA (19 mm x 19 mm, 0.8 mm)						384[3]

Notes:

1. Package is only available for E=1.2 V devices.
2. Package is only available for C=2.5 V/3.3 V devices in 6900 LUT and smaller densities. (Both C and E variants are available for 9400 LUT devices).
3. Package is available for both E=1.2 V and C=2.5 V/3.3 V devices.
4. Refer to Power and Thermal Estimation and Management for MachXO3 Devices (FPGA-TN-02059) for determination of safe ambient operating conditions.
5. High Performance with regulator – VCC = 2.5 V/3.3 V.
6. High Performance without regulator – VCC = 1.2 V.

2. Architecture

2.1. Architecture Overview

The MachXO3L/LF family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). All logic density devices in this family have sysCLOCK™ PLLs and blocks of sysMEM Embedded Block RAM (EBRs). Figure 2.1 and Figure 2.2 show the block diagrams of the various family members.

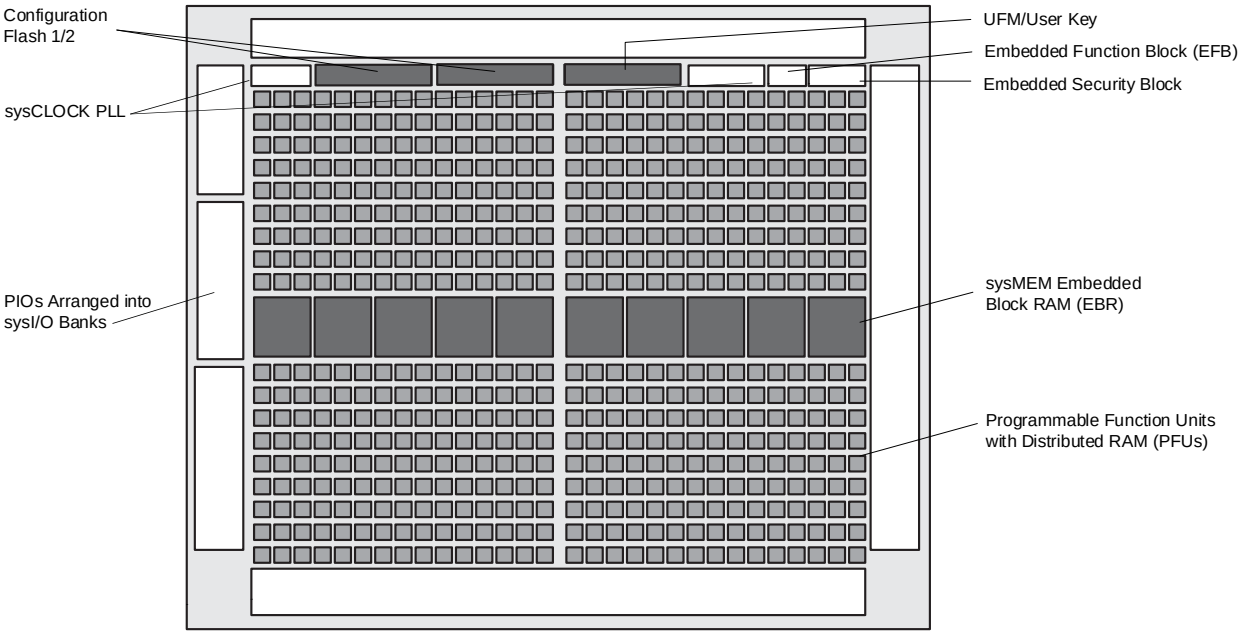
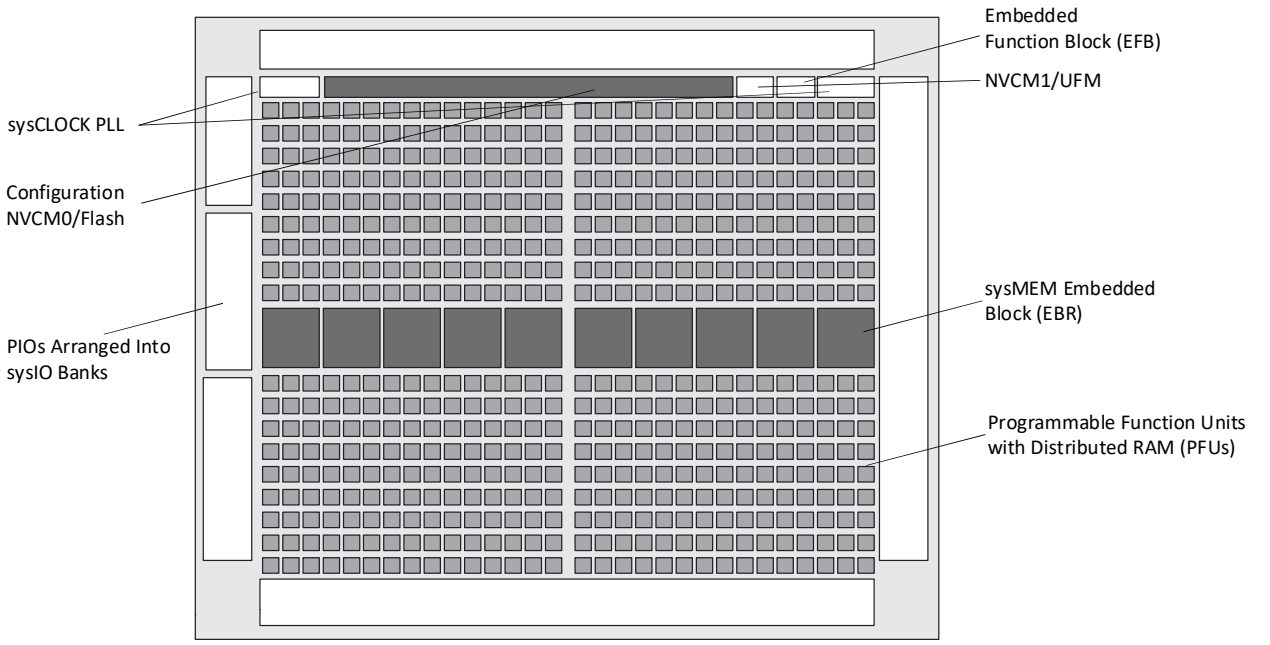


Figure 2.1. Top View of the MachXO3L/LF-1300 Device

Notes:

- MachXO3L/LF-640 is similar to MachXO3L/LF-1300. MachXO3L/LF-640 has a lower LUT count.
- MachXO3L devices have NVCM, MachXO3LF devices have Flash.



Notes:
- MachXO3L/LF-1300, MachXO3L/LF-2100, MachXO3L/LF-6900 and MachXO3L/LF-9400 are similar to MachXO3L/LF-4300. MachXO3L/LF-1300 has a lower LUT count, one PLL, and seven EBR blocks. MachXO3L/LF-2100 has a lower LUT count, one PLL, and eight EBR blocks. MachXO3L/LF-6900 has a higher LUT count, two PLLs, and 26 EBR blocks. MachXO3L/LF-9400 has a higher LUT count, two PLLs, and 48 E blocks.
- MachXO3L devices have NVCM, MachXO3LF devices have Flash.

Figure 2.2. Top View of the MachXO3L/LF-4300 Device

The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysI/O buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO3L/LF family, the number of sysI/O banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag “hard” control logic to minimize LUT usage.

The MachXO3L/LF registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration set-ting, allowing device entering to a known state for predictable system function.

The MachXO3L/LF architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks. These blocks are located at the ends of the on-chip NVCM/Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

MachXO3L/LF devices provide commonly used hardened functions such as SPI controller, I^2C controller and timer/counter.

MachXO3LF devices also provide User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, I^2C and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO3L/LF devices are available for operation from 3.3 V, 2.5 V and 1.2 V power supplies, providing easy integration into the overall system.

2.2. PFU Blocks

The core of the MachXO3L/LF device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2.3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.

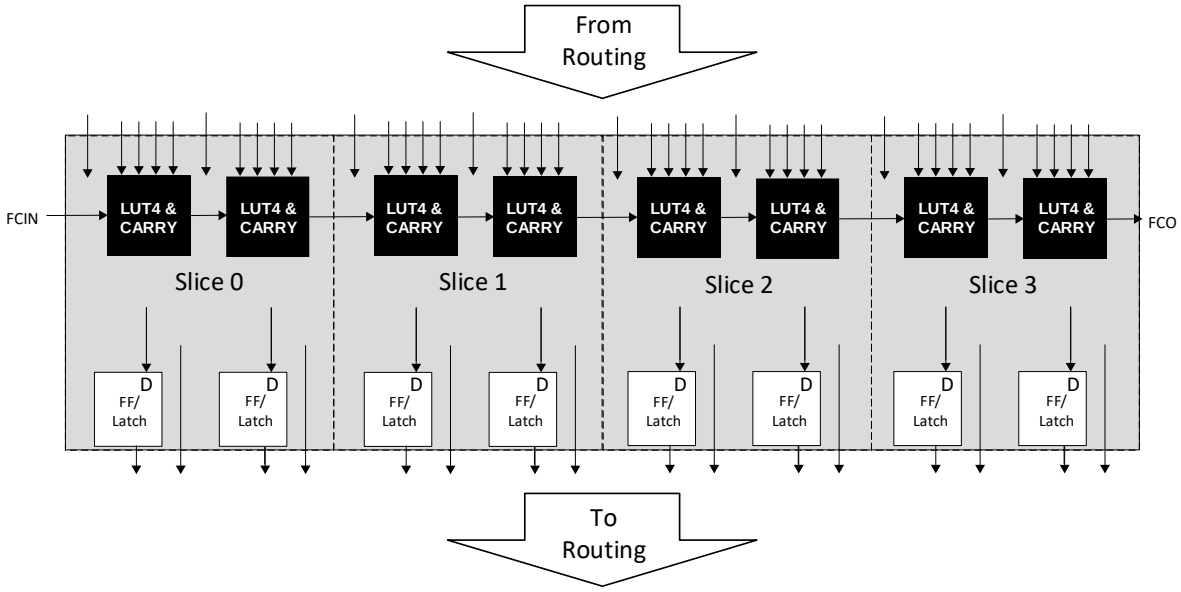


Figure 2.3. PFU Block Diagram

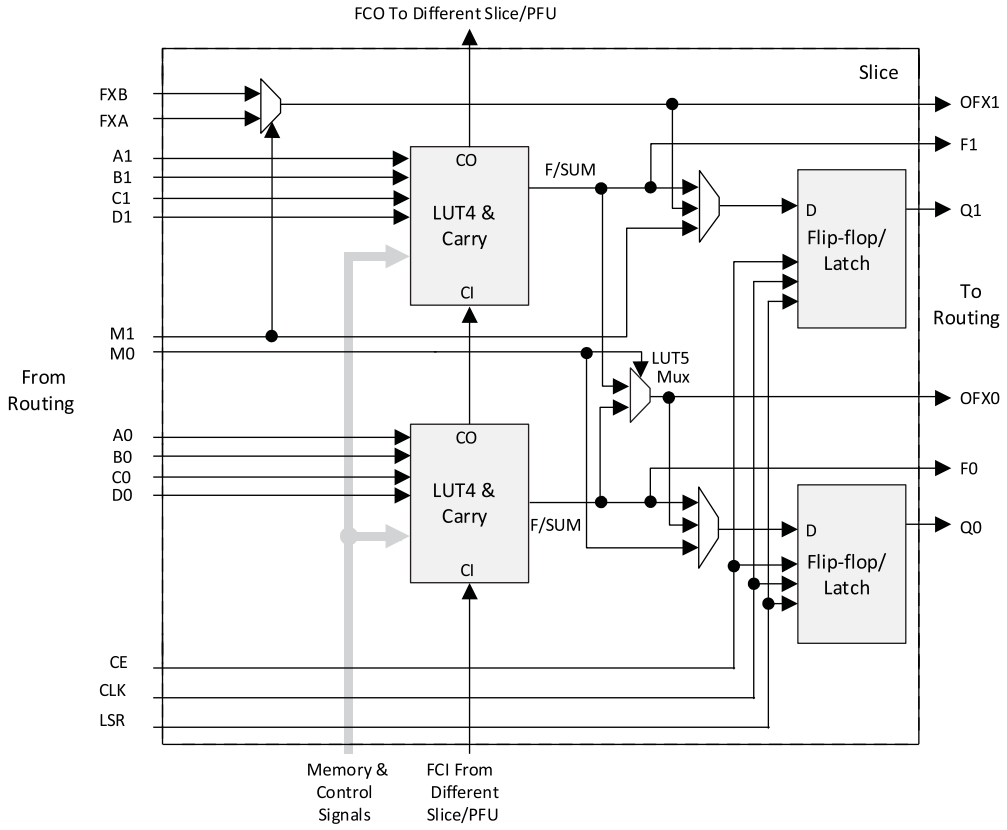
2.2.1. Slices

Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2.1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip select and wider RAM/ROM functions.

Table 2.1. Resources and Modes Available per Slice

Slice	PFU Block	
	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM

Figure 2.4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/ negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2.2 lists the signals associated with Slices 0-3.



For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:

- WCK is CLK
- WRE is from LSR
- DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
- WAD [A:D] is a 4-bit address from slice 2 LUT input

Figure 2.4. Slice Diagram

Table 2.2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0/M1	Multi-purpose input
Input	Control signal	CE	Clock enable
Input	Control signal	LSR	Local set/reset
Input	Control signal	CLK	System clock
Input	Inter-PFU signal	FCIN	Fast carry in[1]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	Fast carry out[1]

Notes:

1. See Figure 2.3 for connection details.
2. Requires two PFUs.

2.2.2. Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

2.2.2.1. Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

2.2.2.2. Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In Ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/down counter with asynchronous clear
- Up/down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
- A greater-than-or-equal-to B
- A not-equal-to B
- A less-than-or-equal-to B

Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

2.2.3. RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed by using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals.

MachXO3L/LF devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2.3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in MachXO3L/LF devices, please see Memory Usage Guide for MachXO3 Devices (TN1290).

Table 2.3. Number of Slices Required For Implementing Distributed RAM

	SPR 16 x 4	PDPR 16 x 4
Number of slices	3	3

Note: SPR = Single Pot RAM, PDPR = Pseudo Dual Port RAM

2.2.4. ROM Mode

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, please refer to Memory Usage Guide for MachXO3 Devices (FPGA-TN-02060).

2.3. Routing

There are many resources provided in the MachXO3L/LF devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

2.4. Clock/Control Distribution Network

Each MachXO3L/LF device has eight clock inputs (PCLK [T, C] [Banknum]_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

The MachXO3L/LF architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO3L/LF devices have two edge clocks each on the top and bottom edges. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO3L/LF devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO3L/LF External Switching Characteristics table.

Primary clock signals for the MachXO3L/LF-1300 and larger devices are generated from eight 27:1 muxes The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sysCLOCK PLL outputs.

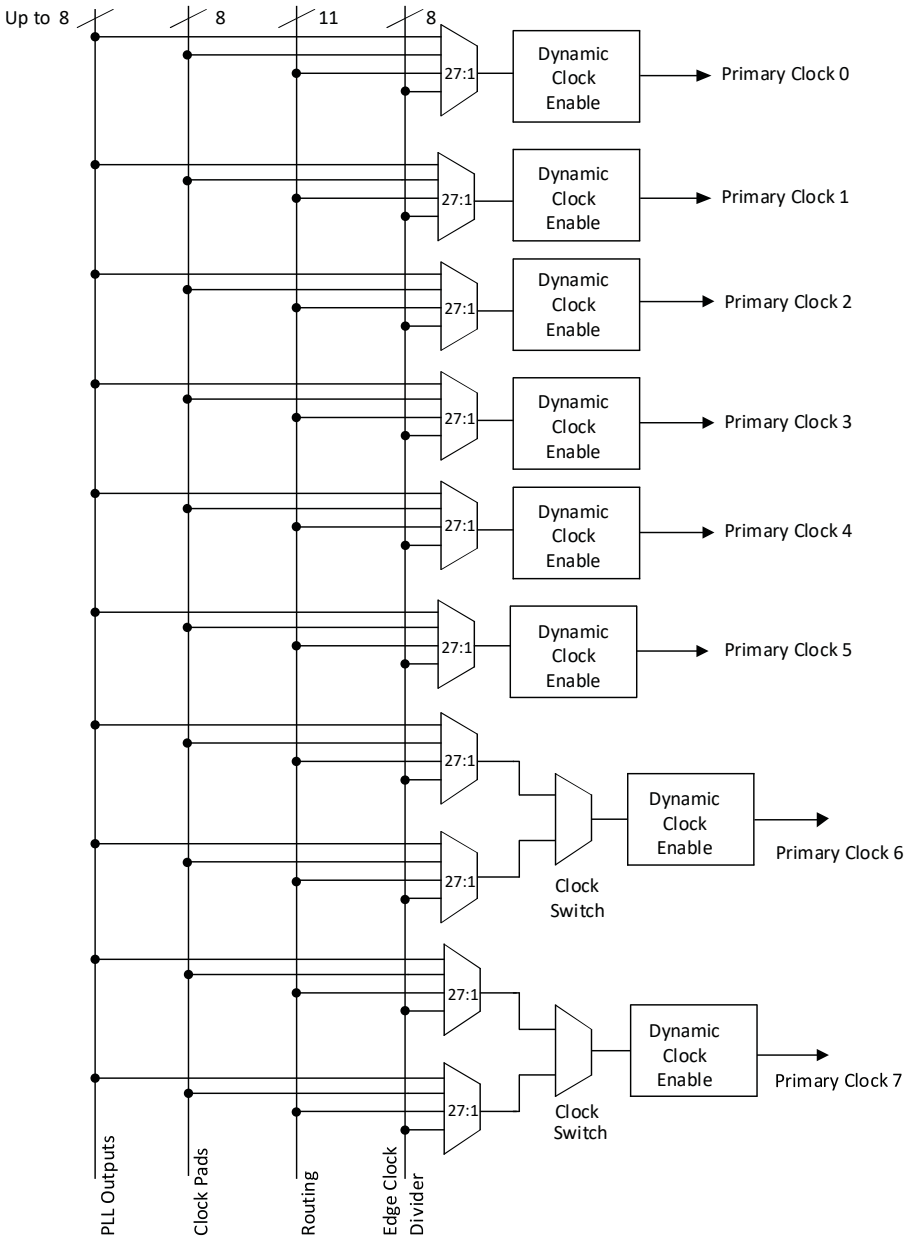


Figure 2.5. Primary Clocks for MachXO3L/F Devices

Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in Figure 2.6. One of the eight inputs to the secondary high fanout net input mux comes from dual function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in MachXO3L/LF External Switching Characteristics table.

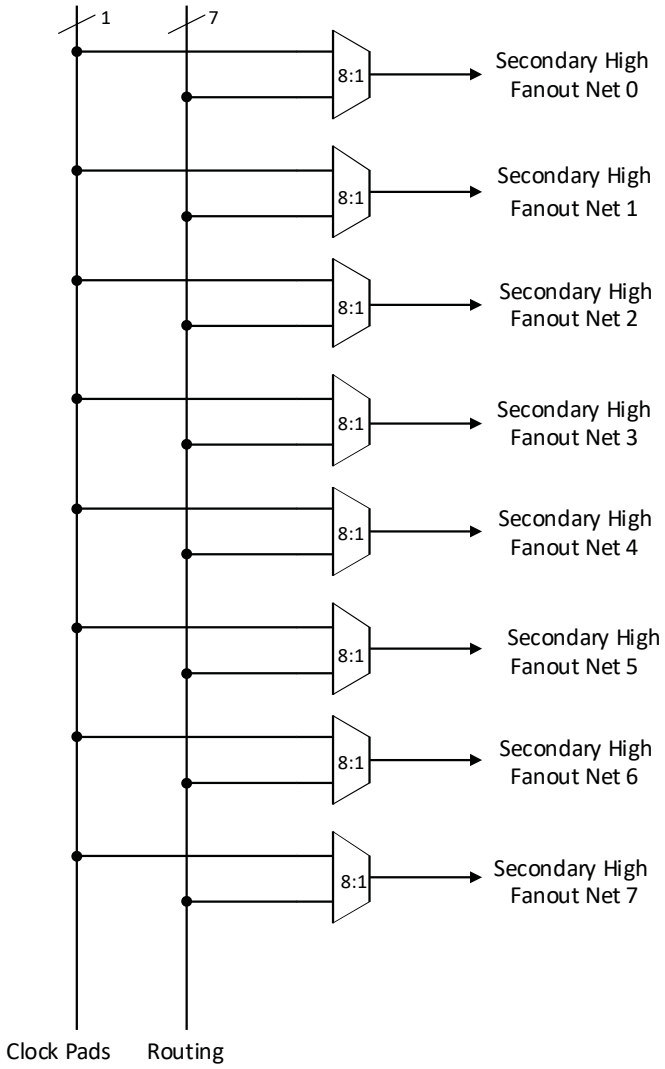


Figure 2.6. Secondary High Fanout Nets for MachXO3L/F Devices

2.4.1. sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. All MachXO3L/LF devices have one or more sysCLOCK PLL. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The MachXO3L/LF sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis. Fractional-N frequency synthesis allows the user to generate an output clock which is a non-integer multiple of the input frequency. For more information about using the PLL with Fractional-N synthesis, please see MachXO3 sysCLOCK PLL Design and Usage Guide (FPGA-TN-02058).

Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The output dividers may also be cascaded together to generate low frequency clocks. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the MachXO3L/LF clock distribution network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2.7.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock.

This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the t_{LOCK} parameter has been satisfied.

The MachXO3L/LF also has a feature that allows the user to select between two different reference clock sources dynamically. This feature is implemented using the PLLREFCS primitive. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

The MachXO3L/LF PLL contains a WISHBONE port feature that allows the PLL settings, including divider values, to be dynamically changed from the user logic. When using this feature the EFB block must also be instantiated in the design to allow access to the WISHBONE ports. Similar to the dynamic phase adjustment, when PLL settings are updated through the WISHBONE port the PLL may lose lock and not relock until the tLOCK parameter has been satisfied. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

For more details on the PLL and the WISHBONE interface, see MachXO3 sysCLOCK PLL Design and Usage Guide (FPGA-TN-02058).

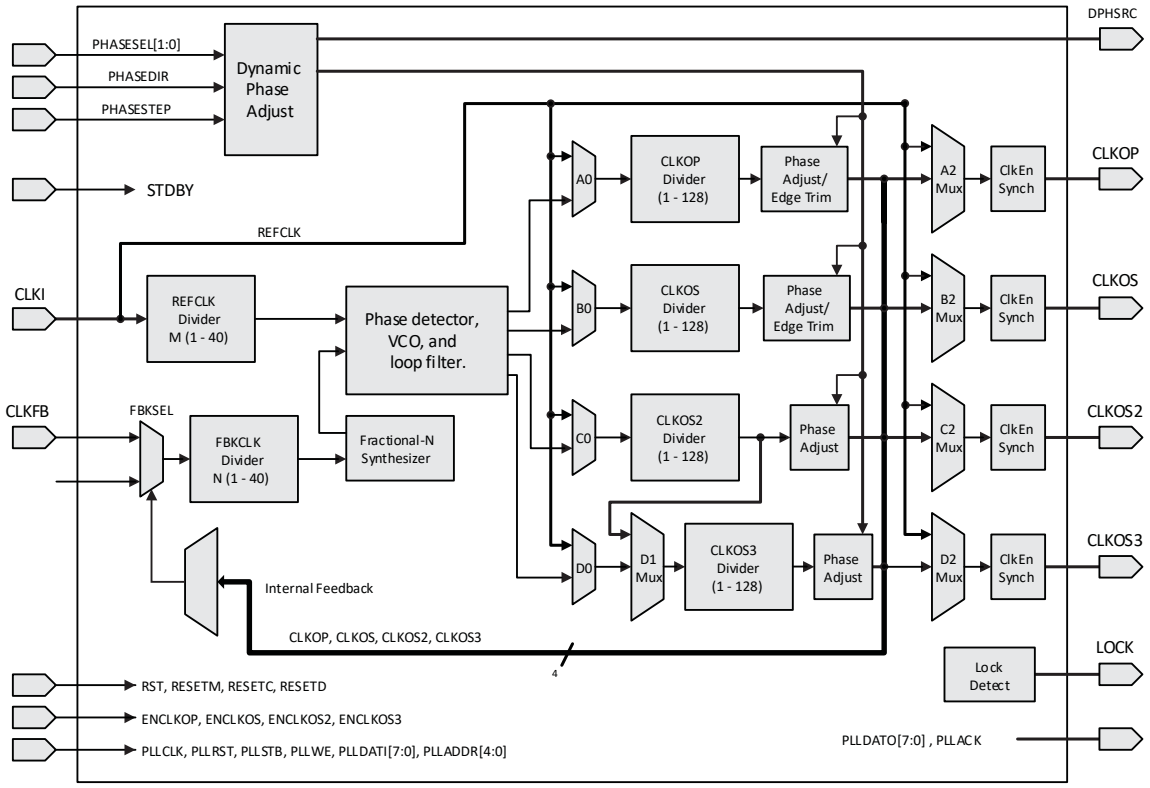


Figure 2.7. PLL Diagram

Table 2.4 provides signal descriptions of the PLL block.

Table 2.4. PLL Signal Descriptions

Port Name	I/O	Description
CLKI	I	Input clock to PLL
CLKFB	I	Feedback clock
PHASESEL[1:0]	I	Select which output is affected by Dynamic Phase adjustment ports
PHASEDIR	I	Dynamic Phase adjustment direction
PHASESTEP	I	Dynamic Phase step – toggle shifts VCO phase adjust by one step.
CLKOP	O	Primary PLL output clock (with phase shift adjustment)
CLKOS	O	Secondary PLL output clock (with phase shift adjust)
CLKOS2	O	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	O	Secondary PLL output clock3 (with phrase shift adjust)
LOCK	O	PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feedback signals.
DPHSRC	O	Dynamic Phase source – ports or WISHBONE is active
STDBY	I	Standby signal to power down the PLL
RST	I	PLL reset without resetting the M-driver. Active high reset.
RESETM	I	PLL rest – includes resetting the M-divider. Active high reset.
RESETC	I	Reset for CLKOS2 output divider only. Active high reset.
RESETD	I	Reset for CLKOS3 output divider only. Active high reset.
ENCLKOP	I	Enable PLL output CLKOP
ENCLKOS	I	Enable PLL output CLKOS when port is active
ENCLKOS2	I	Enable PLL output CLKOS2 when port is active
ENCLKOS3	I	Enable PLL output CLKOS3 when port is active
PLLCLK	I	PLL data bus clock input signal
PLLRST	I	PLL data bus reset. This resets only the data bus not any register values.
PLLSTB	I	PLL data bus strobe signal
PLLWE	I	PLL data bus write enable signal
PLLADDR [4:0]	I	PLL data bus address
PLLDATI [7:0]	I	PLL data bus data input
PLLDATO [7:0]	O	PLL data bus data output
PLLACK	O	PLL data bus acknowledge signal

2.5. sysMEM Embedded Block RAM Memory

The MachXO3L/LF devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

2.5.1. sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2.5.

Table 2.5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
FIFO	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18

2.5.2. Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

2.5.3. RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. EBR initialization data can be loaded from the NVCM or Configuration Flash.

MachXO3LF EBR initialization data can also be loaded from the UFM. To maximize the number of UFM bits, initialize the EBRs used in your design to an all-zero pattern. Initializing to an all-zero pattern does not use up UFM bits. MachXO3LF devices have been designed such that multiple EBRs share the same initialization memory space if they are initialized to the same pattern.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

2.5.4. Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

2.5.5. Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2.8 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.

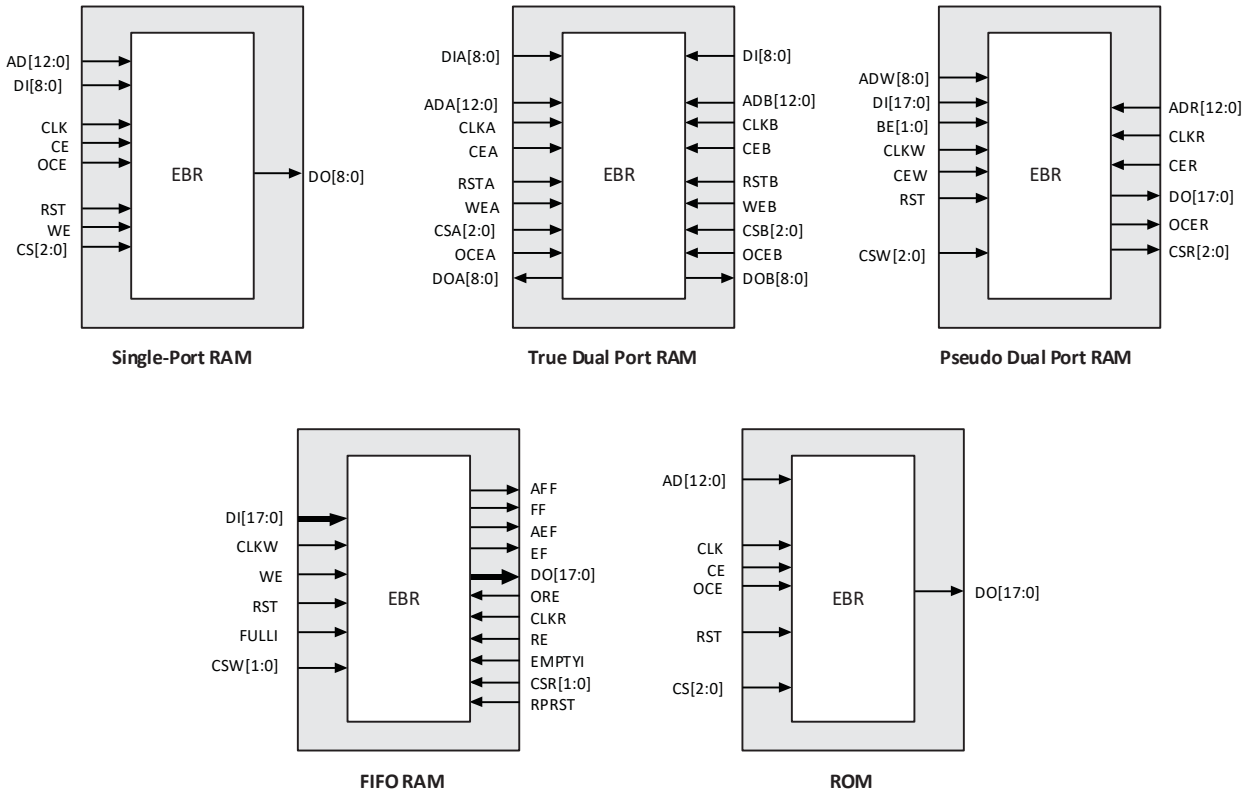


Figure 2.8. sysMEM Memory Primitives

Table 2.6. EBR Signal Descriptions

Port Name	Description	Active State
CLK	Clock	Rising Clock Edge
CE	Clock Enable	Active High
OCE[1]	Output Clock Enable	Active High
RST	Reset	Active High
BE[1]	Byte Enable	Active High
WE	Write Enable	Active High
AD	Address Bus	—
DI	Data In	—
DO	Data Out	—
CS	Chip Select	Active High
AFF	FIFO RAM Almost Full Flag	—
FF	FIFO RAM Full Flag	—
AEF	FIFO RAM Almost Empty Flag	—

Port Name	Description	Active State
EF	FIFO RAM Empty Flag	—
RPRST	FIFO RAM Read Pointer Reset	—

Notes:
1. Optional signals.
2. For dual port EBR primitives a trailing 'A' or 'B' in the signal name specifies the EBR port A or port B respectively.
3. For FIFO RAM mode primitive, a trailing 'R' or 'W' in the signal name specifies the FIFO read port or write port respectively.
4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).
5. In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port chip select, ORE is the output read enable.

The EBR memory supports three forms of write behavior for single or dual port operation:

- Normal – Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
- Write Through – A copy of the input data appears at the output of the same port. This mode is supported for all data widths.
- Read-Before-Write – When new data is being written, the old contents of the address appears at the output.

2.5.6. FIFO Configuration

The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. Table 2.7 shows the range of programming values for these flags.

Table 2.7. Programmable FIFO Flag Ranges

Flag Name	Programming Range
Full (FF)	1 to max (up to 2^N-1)
Almost Full (AF)	1 to Full-1
Almost Empty (AE)	1 to Full-1
Empty (EF)	0

N = Address bit width.

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

2.5.7. Memory Core Reset

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2.9.

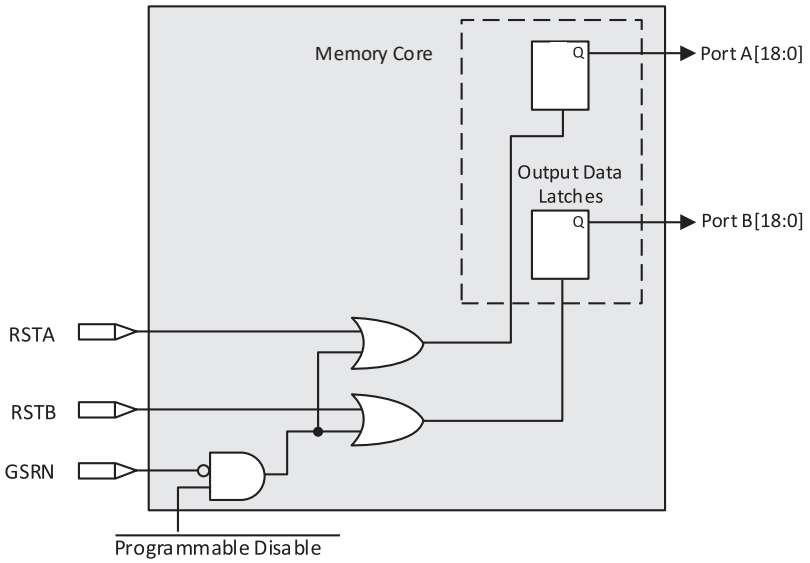


Figure 2.9. Memory Core Reset

For further information on the sysMEM EBR block, please refer to Memory Usage Guide for MachXO3 Devices (FPGA-TN-02060).

2.5.8. EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2.10. The GSR input to the EBR is always asynchronous.

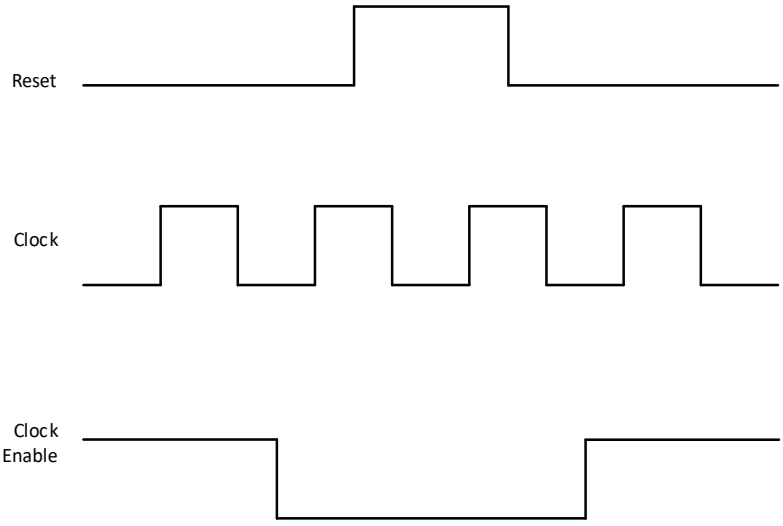


Figure 2.10. EBR Asynchronous Reset (Including GSR) Timing Diagram

If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of 1/fMAX (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device wake up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2.10. The reset timing rules apply to the RPReset input versus the RE input and the RST input versus the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs. For more details refer to Memory Usage Guide for MachXO3 Devices (FPGA-TN-02060).

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

2.6. Programmable I/O Cells (PIC)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysI/O buffers and pads. On the MachXO3L/LF devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the MachXO3L/LF devices, two adjacent PIOs can be combined to provide a complementary output driver pair.

All PIO pairs can implement differential receivers. Half of the PIO pairs on the top edge of these devices can be configured as true LVDS transmit pairs. The PIO pairs on the bottom edge of these devices have on-chip differential termination and, in the MachXO3L/LF-9400 devices, also provide PCI support.

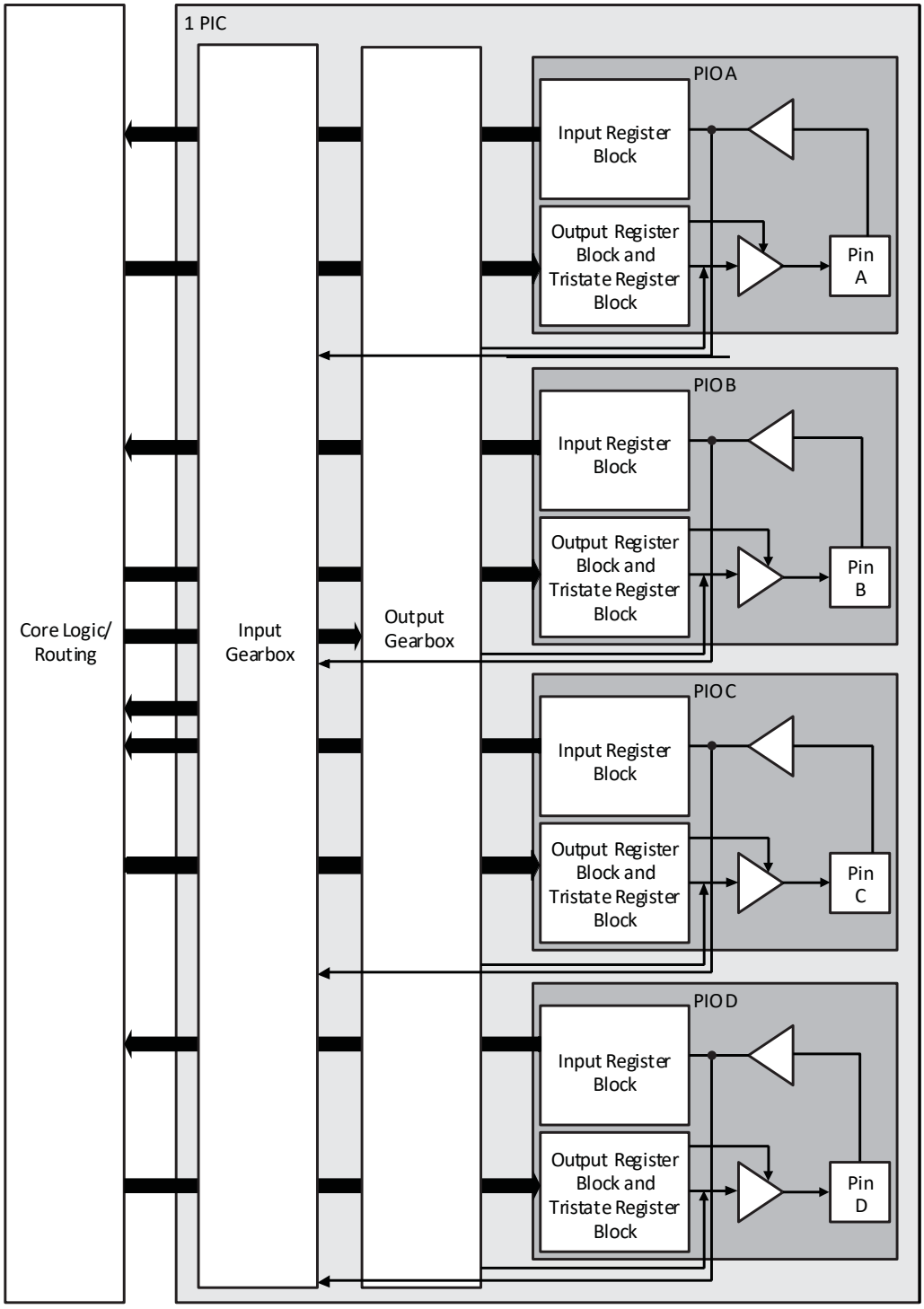


Figure 2.11. Group of Four Programmable I/O Cells

2.7. PIO

The PIO contains three blocks: an input register block, output register block and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Table 2.8. PIO Signal List

Pin Name	I/O Type	Description
CE	Input	Clock Enable
D	Input	Pin input from sysI/O buffer
INDD	Output	Register bypassed input
INCK	Output	Clock input
Q0	Output	DDR positive edge input
Q1	Output	Registered input/DDR negative edge input
D0	Input	Output signal from the core (SDR and DDR)
D1	Input	Output signal from the core (DDR)
TD	Input	Tri-state signal from the core
Q	Output	Data output signals to sysI/O Buffer
TQ	Output	Tri-state output signals to sysI/O Buffer
SCLK	Input	System clock for input and output/tri-state blocks.
RST	Input	Local set reset signal

2.7.1. Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core.

2.7.1.1. Left, Top, Bottom Edges

Input signals are fed from the sysI/O buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/Os on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.

2.7.2. Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysI/O buffers.

2.7.2.1. Left, Top, Bottom Edges

In SDR mode, D0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type register or latch.

In DDR generic mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the same clock is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2.12 shows the output register block on the left, top and bottom edges.

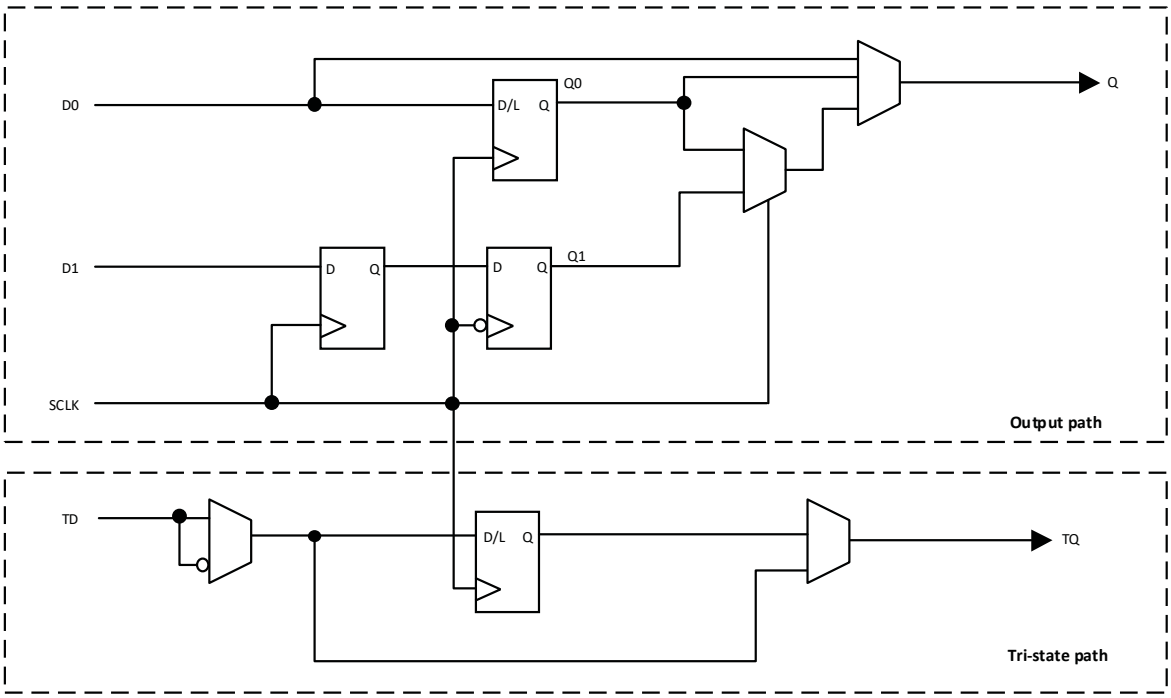


Figure 2.12. Output Register Block Diagram (PIO on the Left, Top and Bottom Edges)

2.7.3. Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.

2.8. Input Gearbox

Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2.9 shows the gearbox signals.

Table 2.9. Input Gearbox Signal List

Name	I/O Type	Description
D	Input	High-speed data input after programmable delay in PIO A input register block
ALIGNWD	Input	Data alignment signal from device core
SCLK	Input	Slow-speed system clock
ECLK[1:0]	Input	High-speed edge clock
RST	Input	Reset
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDRX4(1:8): Q[7:0] GDDRX2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDRX2(1:4)(IOL-C): Q0, Q1, Q2, Q3

Note:

These gearboxes have three stage pipeline registers. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals UPDATE and SEL0 from the control block. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. Figure 2.13 shows a block diagram of the input gearbox.

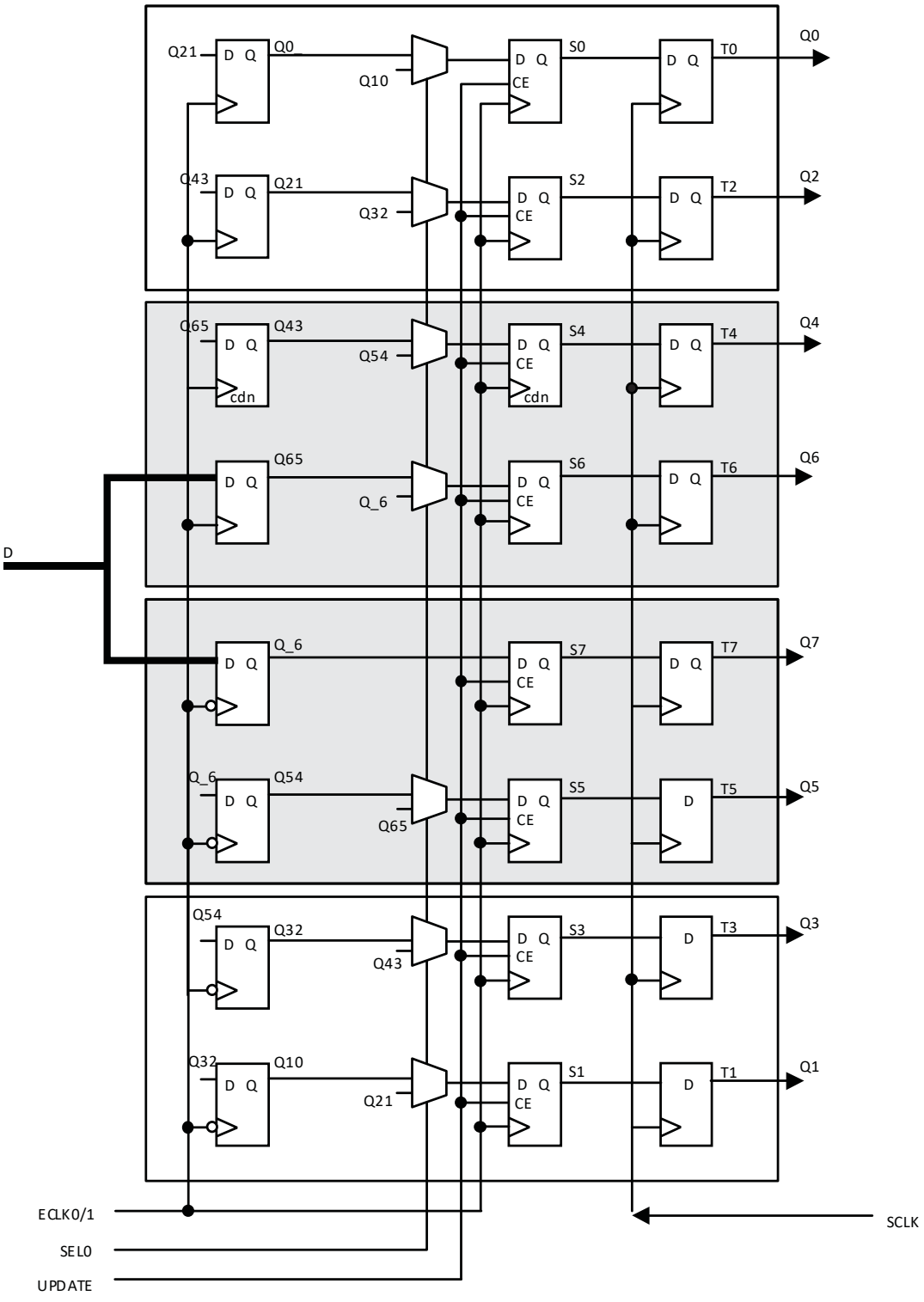


Figure 2.13. Input Gearbox

More information on the input gearbox is available in Implementing High-Speed Interfaces with MachXO3 Devices (FPGA-TN-02057).

2.9. Output Gearbox

Each PIC on the top edge has a built-in 8:1 output gearbox. Each of these output gearboxes may be programmed as a 7:1 serializer or as one ODDRX4 (8:1) gearbox or as two ODDRX2 (4:1) gearboxes. Table 2.10 shows the gearbox signals.

Table 2.10. Output Gearbox Signal List

Name	I/O Type	Description
Q	Output	High-speed data output
D[7:0]	Input	Low-speed data from device core
Video TX(7:1): D[6:0]	—	—
GDDRX4(8:1): D[7:0]	—	—
GDDRX2(4:1)(IOL-A): D[3:0]	—	—
GDDRX2(4:1)(IOL-C): D[7:4]	—	—
SCLK	Input	Slow-speed system clock
ECLK [1:0]	Input	High-speed edge clock
RST	Input	Reset

The gearboxes have three stage pipeline registers. The first stage registers sample the low-speed input data on the low-speed system clock. The second stage registers transfer data from the low-speed clock registers to the high- speed clock registers. The third stage pipeline registers controlled by high-speed edge clock shift and mux the high-speed data out to the sysI/O buffer. Figure 2.14 shows the output gearbox block diagram.

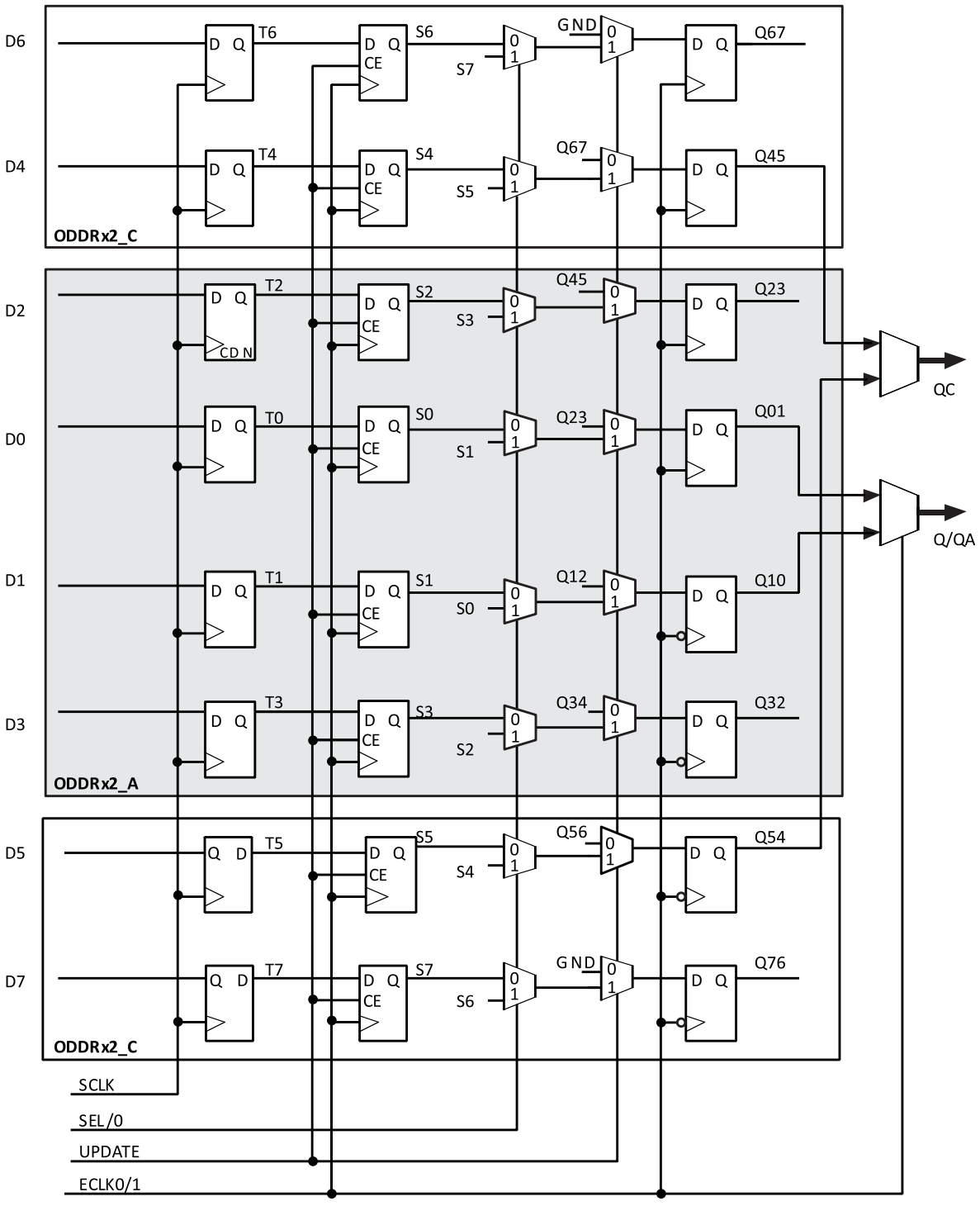


Figure 2.14. Output Gearbox

More information on the output gearbox is available in Implementing High-Speed Interfaces with MachXO3 Devices (FPGA-TN-02057).

2.10. sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS, TTL, PCI (MachXO3L/LF-9400 devices only), LVDS, BLVDS, MLVDS and LVPECL.

Each bank is capable of supporting multiple I/O standards. In the MachXO3L/LF devices, single-ended output buffers, ratioed input buffers (LVTTL, LVCMOS and PCI), differential (LVDS) input buffers are powered using I/O supply voltage (V_{CCIO}). Each sysI/O bank has its own V_{CCIO}.

MachXO3L/LF devices contain three types of sysI/O buffer pairs.

- Left and Right sysI/O Buffer Pairs

  The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the left and right of the devices also have differential input buffers.
- Bottom sysI/O Buffer Pairs

  The sysI/O buffer pairs in the bottom bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the bottom also have differential input buffers. In the MachXO3L/LF-9400 devices, only the I/Os on the bottom banks have programmable PCI clamps and differential input termination. The PCI clamp is enabled after V_{CC} and V_{CCIO} are at valid operating levels and the device has been configured.
- Top sysI/O Buffer Pairs

  The sysI/O buffer pairs in the top bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the top also have differential I/O buffers. Half of the sysI/O buffer pairs on the top edge have true differential outputs. The sysI/O buffer pair comprising of the A and B PIOs in every PIC on the top edge have a differential output driver.

2.10.1. Typical I/O Behavior during Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} and V_{CCIO0} have reached VPORUP level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pull-down to GND (some pins such as PROGRAMN and the JTAG pins have weak pull-up to V_{CCIO} as the default functionality). The I/O pins will maintain the blank configuration until V_{CC} and V_{CCIO} (for I/O banks containing configuration I/Os) have reached VPORUP levels at which time the I/Os will take on the user-configured settings only after a proper download/configuration.

2.10.2. Supported Standards

The MachXO3L/LF sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL, and PCI. The buffer supports the LVTTL, PCI, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS, MLVDS and LVPECL output emulation is supported on all devices. The MachXO3L/LF devices support on-chip LVDS output buffers on approximately 50% of the I/Os on the top bank. Differential receivers for LVDS, BLVDS, MLVDS and LVPECL are supported on all banks of MachXO3L/LF devices. PCI compatibility is supported in the bottom bank of the MachXO3L/LF-9400 devices only. PCI support is provided by:

- Selecting the LVTTL33 buffer standard
- Enabling the clamp feature
- Setting 16 mA drive strength (PCI output only).

Table 2.11 shows the I/O standards (together with their supply and reference voltages) supported by the MachXO3L/LF devices. For further information on utilizing the sysI/O buffer to support a variety of standards please see MachXO3 sysI/O Usage Guide (FPGA-TN-02047).

Table 2.11. Supported Input Standards

	V_{CCIO} (Typ.)				
Input Standard	**3.3 V**	**2.5 V**	**1.8 V**	**1.5 V**	**1.2 V**
Single-Ended Interfaces					
LVTTL	Yes	Yes[2]	Yes[2]	Yes[2]	—
LVCMOS33	Yes	Yes[2]	Yes[2]	Yes[2]	—
LVCMOS25	Yes[2]	Yes	Yes[2]	Yes[2]	—
LVCMOS18	Yes[2]	Yes[2]	Yes	Yes[2]	—
LVCMOS15	Yes[2]	Yes[2]	Yes[2]	Yes	Yes[2]
LVCMOS12	Yes[2]	Yes[2]	Yes[2]	Yes[2]	Yes
PCI[3]	Yes	—	—	—	—
Differential Interfaces					
LVDS	Yes	Yes	—	—	—
BLVDS, MLVDS, LVPECL, RSDS	Yes	Yes	—	—	—
MIPI[1]	Yes	Yes	—	—	—
LVTTLD	Yes	—	—	—	—
LVCMOS33D	Yes	—	—	—	—
LVCMOS25D	—	Yes	—	—	—
LVCMOS18D	—	—	Yes	—	—

Notes:

1. These interfaces can be emulated with external resistors in all devices.
2. Reduced functionality. Refer to MachXO3 sysI/O Usage Guide (FPGA-TN-02047) for more details.
3. PCI input is supported for MachXO3L/LF-9400 devices, bottom bank 2 only. See the Supported Standards section.

Table 2.12. Supported Output Standards

Output Standard	V_{CCIO} (Typ.)
Single-Ended Interfaces	
LVTTL	3.3
LVCMOS33	3.3
LVCMOS25	2.5
LVCMOS18	1.8
LVCMOS15	1.5
LVCMOS12	1.2
LVCMOS33, Open Drain	—
LVCMOS25, Open Drain	—
LVCMOS18, Open Drain	—
LVCMOS15, Open Drain	—
LVCMOS12, Open Drain	—
PCI33[2]	3.3
Differential Interfaces	
LVDS[1]	2.5, 3.3
BLVDS, MLVDS, RSDS[1]	2.5
LVPECL[1]	3.3
MIPI[1]	2.5
LVTTLD	3.3
LVCMOS33D	3.3
LVCMOS25D	2.5
LVCMOS18D	1.8

Notes:

1. These interfaces can be emulated with external resistors in all devices.
2. PCI input is supported for MachXO3L/LF-9400 devices, bottom bank 2 only. See the Supported Standards section.

2.10.3. sysI/O Buffer Banks

The numbers of banks vary between the devices of this family. MachXO3L/LF-1300 in the 256 Ball packages and the MachXO3L/LF-2100 and higher density devices have six I/O banks (one bank on the top, right and bottom side and three banks on the left side). The MachXO3L/LF-1300 and lower density devices have four banks (one bank per side). Figure 2.15 and Figure 2.16 show the sysI/O banks and their associated supplies for all devices.

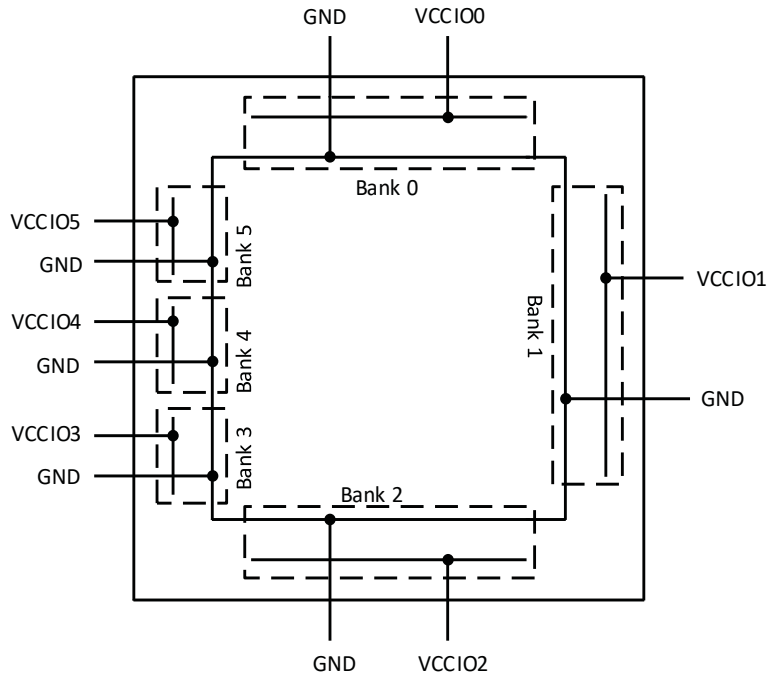


Figure 2.15. MachXO3L/LF-1300 in 256 Ball Packages, MachXO3L/LF-2100, MachXO3L/LF-4300, MachXO3L/LF-6900 and MachXO3L/LF-9400 Banks I/O Banks

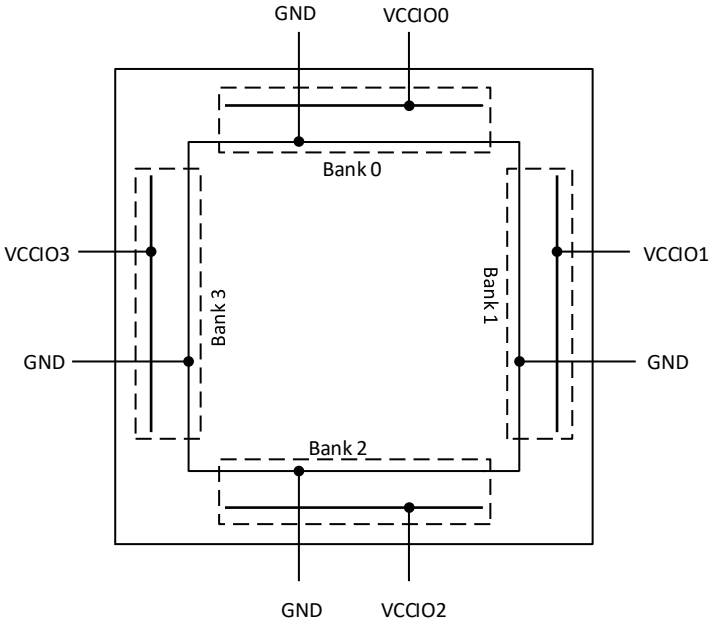


Figure 2.16. MachXO3L/LF-640 and MachXO3L/LF-1300 Banks

2.11. Hot Socketing

The MachXO3L/LF devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO3L/LF ideal for many multiple power supply and hot-swap applications.

2.12. On-chip Oscillator

Every MachXO3L/LF device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal MCLK frequency of 2.08 MHz.
2. During configuration, users select a different master clock frequency.
3. The MCLK frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2.13 lists all the available MCLK frequencies.

Table 2.13. Available MCLK Frequencies

MCLK (MHz, Nominal)	MCLK (MHz, Nominal)	MCLK (MHz, Nominal)
2.08 (default)	9.17	33.25
2.46	10.23	38
3.17	13.3	44.33
4.29	14.78	53.2
5.54	20.46	66.5
7	26.6	88.67
8.31	29.56	133

2.13. Embedded Hardened IP Functions

All MachXO3L/LF devices provide embedded hardened functions such as SPI, I^2C and Timer/Counter. MachXO3LF devices also provide User Flash Memory (UFM). These embedded blocks interface through the WISHBONE interface with routing as shown in Figure 2.17.

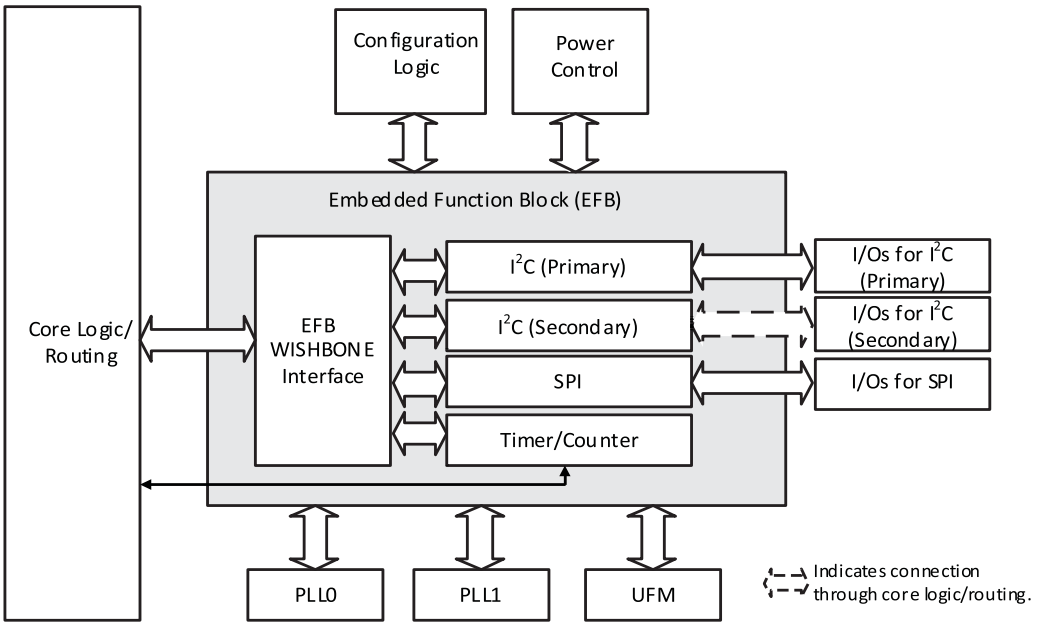


Figure 2.17. Embedded Function Block Interface

2.13.1. Hardened I²C IP Core

Every MachXO3L/LF device contains two I²C IP cores. These are the primary and secondary I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master it will be able to control other devices on the I²C bus through the interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed
- General call support
- Interface to custom logic through 8-bit WISHBONE interface

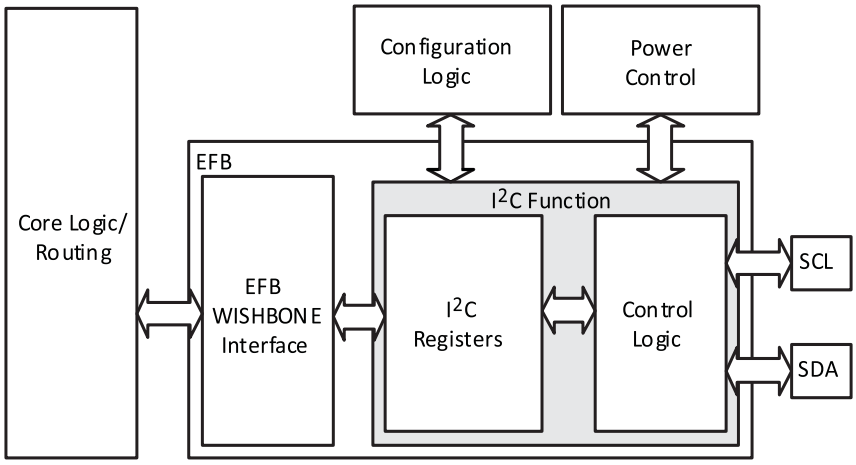


Figure 2.18. I²C Core Block Diagram

Table 2.14 describes the signals interfacing with the I²C cores.

Table 2.14. I²C Core Signal Description

Signal Name	I/O	Description
i2c_scl	Bi-directional	Bi-directional clock line of the I²C core. The signal is an output if the I²C core is in master mode. The signal is an input if the I²C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I²C ports in each MachXO3L/LF device.
i2c_sda	Bi-directional	Bi-directional data line of the I²C core. The signal is an output when data is transmitted from the I²C core. The signal is an input when data is received into the I²C core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I²C ports in each MachXO3L/LF device.
i2c_irqo	Output	Interrupt request output signal of the I²C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I²C register definitions.
cfg_wake	Output	Wake-up signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I²C Tab.
cfg_stdby	Output	Stand-by signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I²C Tab.

2.13.2. Hardened SPI IP Core

Every MachXO3L/LF device has a hard SPI IP core that can be configured as a SPI master or slave. When the IP core is configured as a master it will be able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device will be able to interface to an external SPI master. The SPI IP core on MachXO3L/LF devices supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer
- Interface to custom logic through 8-bit WISHBONE interface

There are some limitations on the use of the hardened user SPI. These are defined in the following technical notes:

- Minimizing System Interruption During Configuration Using TransFR Technology (FPGA-TN-02025) (Appendix B)
- Using Hardened Control Functions in MachXO3 Devices (FPGA-TN-02063)

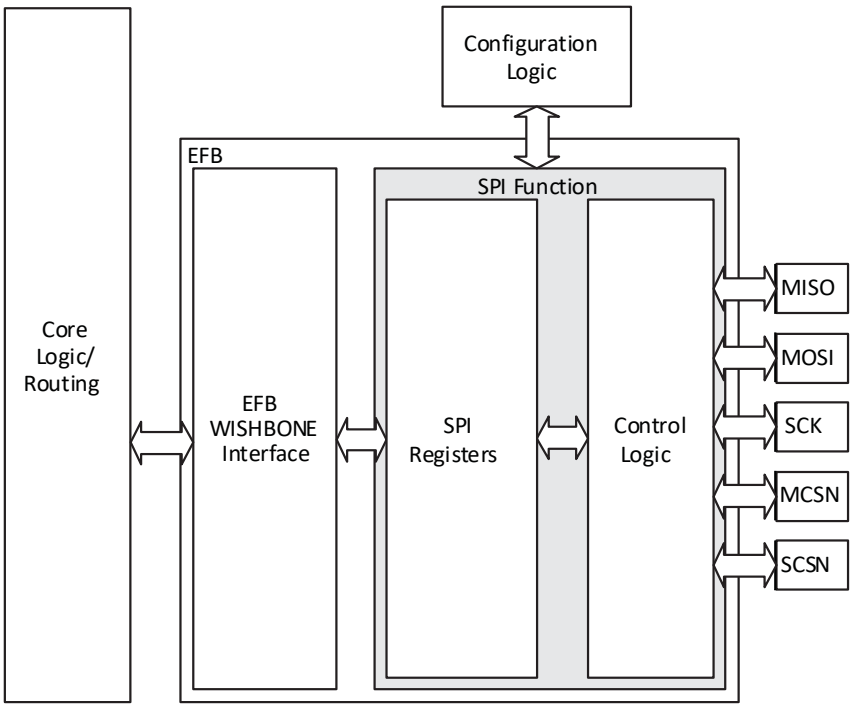


Figure 2.19. SPI Core Block Diagram

Table 2.15 describes the signals interfacing with the SPI cores.

Table 2.15. SPI Core Signal Description

Signal Name	I/O	Master/Slave	Description
spi_csn[0]	O	Master	SPI master chip-select output
spi_csn[1..7]	O	Master	Additional SPI chip-select outputs (total up to eight slaves)
spi_scsn	I	Slave	SPI slave chip-select input
spi_irq	O	Master/Slave	Interrupt request
spi_clk	I/O	Master/Slave	SPI clock. Output in master mode. Input in slave mode.
spi_miso	I/O	Master/Slave	SPI data. Input in master mode. Output in slave mode.

Signal Name	I/O	Master/Slave	Description
spi_mosi	I/O	Master/Slave	SPI data. Output in master mode. Input in slave mode.
sn	I	Slave	Configuration Slave Chip Select (active low), dedicated for selecting the Configuration Logic.
cfg_stdby	O	Master/Slave	Stand-by signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, SPI Tab.
cfg_wake	O	Master/Slave	Wake-up signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, SPI Tab.

2.13.3. Hardened Timer/Counter

MachXO3L/LF devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bidirectional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
- Watchdog timer
- Clear timer on compare match
- Fast PWM
- Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- Stand-alone mode with preloaded control registers and direct reset input

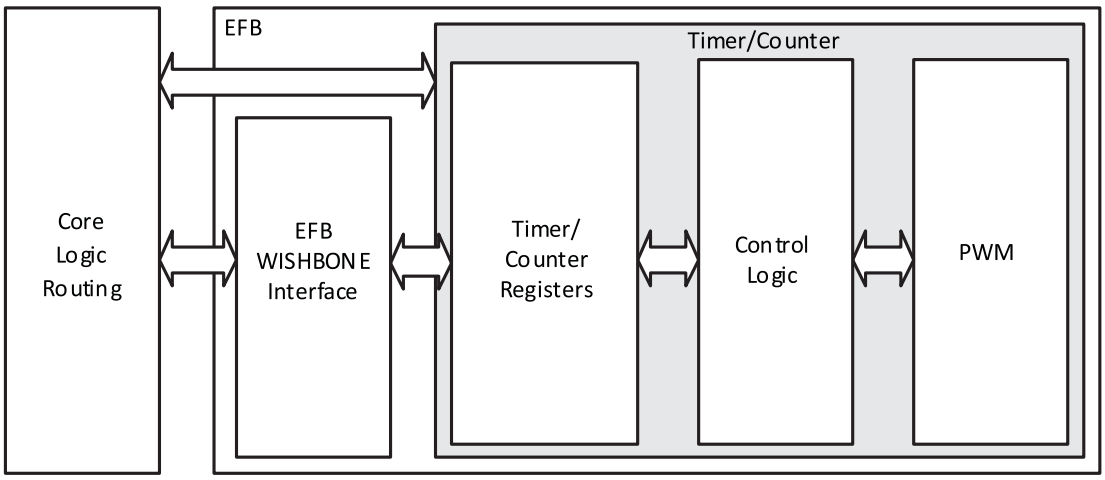


Figure 2.20. Timer/Counter Block Diagram

Table 2.16. Timer/Counter Signal Description

Port	I/O	Description
tc_clki	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	O	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	O	Timer counter output signal

For more details on these embedded functions, please refer to Using Hardened Control Functions in MachXO3 Devices (FPGA-TN-02063).

2.14. User Flash Memory (UFM)

MachXO3LF devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, I^2C and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 448 kbits
- 100K write/erase cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to Using Hardened Control Functions in MachXO3 Devices (FPGA-TN-02063).

2.15. Standby Mode and Power Saving Options

MachXO3L/LF devices are available in two options, the C and E devices. The C devices have a built-in voltage regulator to allow for 2.5 V VCC and 3.3 V VCC while the E devices operate at 1.2 V VCC.

MachXO3L/LF devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO3L/LF devices support a low power Stand-by mode.

In the stand-by mode the MachXO3L/LF devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I^2C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc. can be configured such that they are automatically turned “off” or go into a low power consumption state to save power when the device enters this state. Note that the MachXO3L/LF devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.

Table 2.17. MachXO3L/LF Power Saving Features Description

Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors VCC levels. In the event of unsafe VCC drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Differential I/O buffers (used to implement standards such as LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

For more details on the standby mode refer to Power and Thermal Estimation and Management for MachXO3 Devices (FPGA-TN-02059).

2.16. Power On Reset

MachXO3L/LF devices have power-on reset circuitry to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up and operation. At power-up, the POR circuitry monitors V_{CCINT} and V_{CCIO0} (controls configuration) voltage levels. It then triggers download from the on-chip configuration NVCM/Flash memory after reaching the VPORUP level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For “E” devices without voltage regulators, V_{CCINT} is the same as the V_{CC} supply voltage. For “C” devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as NVCM/Flash Download Time ($t_{REFRESH}$) in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration. Note that for “C” devices, a separate POR circuit monitors external V_{CC} voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor V_{CCINT} levels. If V_{CCINT} drops below $V_{PORDNBG}$ level (with the bandgap circuitry switched on) or below $V_{PORDNSRAM}$ level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the V_{CCINT} and V_{CCIO} voltage levels. $V_{PORDNBG}$ and $V_{PORDNSRAM}$ are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once an “E” device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a minimal, low power POR circuit is still operational (this corresponds to the $V_{PORDNSRAM}$ reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the V_{CC} supply dropping below V_{CC} (min) they should not shut down the bandgap or POR circuit.

2.17. Configuration and Testing

This section describes the configuration and testing features of the MachXO3L/LF family.

2.17.1. IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO3L/LF devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with V_{CCIO} Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see Boundary Scan Testability with Lattice sysI/O Capability (AN8066) and Minimizing System Interruption During Configuration Using TransFR Technology (FPGA-TN-02025).

2.17.2. Device Configuration

All MachXO3L/LF devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I^2C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO3L/LF device:

- Internal Flash Download
- JTAG
- Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
- System microprocessor to drive a serial slave SPI port (SSPI mode)
- Standard I2C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the de- vice can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See MachXO3 Programming and Configuration Usage Guide (FPGA-TN-02055) for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO3L/ LF devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip NVCM/Flash, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip NVCM/Flash. For more details, refer to MachXO3 Programming and Configuration Usage Guide (FPGA-TN-02055).

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to MachXO3 Programming and Configuration Usage Guide (FPGA-TN-02055).

2.17.2.1. TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting sys- tem operation using a simple push-button solution. For more details, refer to Minimizing System Interruption During Configuration Using TransFR Technology (FPGA-TN-02025) for details.

2.17.2.2. Security and One-Time Programmable Mode (OTP)

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO3L/LF devices contain security bits that, when set, prevent the readback of the SRAM configuration and NVCM/Flash spaces. The device can be in one of two modes:

- Unlocked – Readback of the SRAM configuration and NVCM/Flash spaces is allowed.
- Permanently Locked – The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the NVCM/Flash and SRAM OTP portions of the device. For more details, refer to MachXO3 Programming and Configuration Usage Guide (FPGA-TN-02055).

2.17.2.3. Password

The MachXO3LF supports a password-based security access feature also known as Flash Protect Key. Optionally, the MachXO3L device can be ordered with a custom specification (c-spec) to support this feature. The Flash Protect Key feature provides a method of controlling access to the Configuration and Programming modes of the device. When enabled, the Configuration and Programming edit mode operations (including Write, Verify and Erase operations) are allowed only when coupled with a Flash Protect Key which matches that expected by the device. Without a valid Flash Protect Key, the user can perform only rudimentary non-configuration operations such as Read Device ID. For more details, refer to Using Password Security with MachXO3 Devices (FPGA-TN-02072).

2.17.2.4. Dual Boot

MachXO3L/LF devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the external SPI Flash. The golden image MUST reside in an on-chip NVCM/Flash. For more details, refer to MachXO3 Programming and Configuration Usage Guide (FPGA-TN-02055).

2.17.2.5. Soft Error Detection

The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to MachXO3 Soft Error Detection Usage Guide (FPGA-TN-02062).

2.17.2.6. Soft Error Correction

The MachXO3LF device supports Soft Error Correction (SEC). Optionally, the MachXO3L device can be ordered with a custom specification (c-spec) to support this feature. When BACKGROUND_RECONFIG is enabled using the Lattice Diamond Software in a design, asserting the PROGRAMN pin or issuing the REFRESH sysConfig command refreshes the SRAM array from configuration memory. Only the detected error bit is corrected. No other SRAM cells are changed, allowing the user design to function uninterrupted.

During the project design phase, if the overall system cannot guarantee containment of the error or its subsequent effects on downstream data or control paths, Lattice recommends using SED only. The MachXO3 can be then be soft-reset by asserting PROGRAMN or issuing the Refresh command over a sysConfig port in response to SED. Soft-reset additionally erases the SRAM array prior to the SRAM refresh, and asserts internal Reset circuitry to guarantee a known state. For more details, refer to MachXO3 Soft Error Detection (SED)/Correction (SEC) Usage Guide (FPGA-TN-02062).

2.18. TraceID

Each MachXO3L/LF device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I^2C, or JTAG interfaces.

2.19. Density Shifting

The MachXO3L/LF family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the MachXO3 migration files.

2.20. MachXO3LF to MachXO3L Low Cost Migration Path

To support the MachXO3LF to MachXO3L low cost migration path, the MachXO3L Migration options (JEDEC and Bitstream) are added to the Process List in Diamond. This migration path is a time saving feature as it allows you to validate functionality and timing on one project without having to recompile your design for the MachXO3L device. MachXO3L device does not support UFM, SEC, and Password Protect features. For example if a MachXO3LF design is using UFM, an error message is produced if converting this design to MachXO3L.

3. DC and Switching Characteristics

3.1. Absolute Maximum Rating

Table 3.1. Absolute Maximum Rating[1, 2, 3]

	MachXO3L/LF E (1.2 V)	MachXO3L/LF C (2.5 V/3.3 V)6
Supply Voltage V_{CC}	–0.5 V to 1.32 V	–0.5 V to 3.75 V
Output Supply Voltage V_{CCIO}	–0.5 V to 3.75 V	–0.5 V to 3.75 V
I/O Tri-state Voltage Applied[4, 5]	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Dedicated Input Voltage Applied[4]	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Storage Temperature (Ambient)	–55 °C to 125 °C	–55 °C to 125 °C
Junction Temperature (T_J)	–40 °C to 125 °C	–40 °C to 125 °C

Notes:

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of –2 V to (VIHMAX + 2) volts is permitted for a duration of <20 ns.
5. The dual function I^2C pins SCL and SDA are limited to –0.25 V to 3.75 V or to –0.3 V with a duration of <20 ns.
6. Refer to Power and Thermal Estimation and Management for MachXO3 Devices (FPGA-TN-02059) for determination of safe ambient operating conditions.

3.2. Recommended Operating Conditions

Table 3.2. Recommended Operating Conditions[1]

Symbol	Parameter	Min.	Max.	Units
V_{CC}[1]	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
	Core Supply Voltage for 2.5 V/3.3 V Devices	2.375	3.465	V
V_{CCIO}[1, 2, 3]	I/O Driver Supply Voltage	1.14	3.465	V
t_{JCOM}	Junction Temperature Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature Industrial Operation	–40	100	°C

Notes:

1. Like power supplies must be tied together. For example, if V_{CCIO} and V_{CC} are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.

3.3. Power Supply Ramp Rates

Table 3.3. Power Supply Ramp Rates

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	0.01	—	100	V/ms

Note: Assumes monotonic ramp rates.

3.4. Power-On-Reset Voltage Levels

Table 3.4. Power-On Reset Voltage Levels

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{PORUP}	Power-On-Reset ramp up trip point (band gap based circuit monitoring V_{CCINT} and V_{CCIO0})	0.9	—	1.06	V
$V_{PORUPEXT}$	Power-On-Reset ramp up trip point (band gap based circuit monitoring external V_{CC} power supply)	1.5	—	2.1	V
$V_{PORDNBG}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CCINT})	0.75	—	0.93	V
$V_{PORDNBGEXT}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CC})	0.98	—	1.33	V
$V_{PORDNSRAM}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CCINT})	—	0.6	—	V
$V_{PORDNSRAMEXT}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CC})	—	0.96	—	V

Notes:

- These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
- For devices without voltage regulators VCCINT is the same as the VCC supply voltage. For devices with voltage regulators, VCCINT is regulated from the VCC supply voltage.
- Note that VPORUP (min.) and VPORDNBG (max.) are in different process corners. For any given process corner VPORDNBG (max.) is always 12.0 mV below VPORUP (min.).
- VPORUPEXT is for C devices only. In these devices, a separate POR circuit monitors the external VCC power supply.
- VCCIO0 does not have a Power-On-Reset ramp down trip point. VCCIO0 must remain within the Recommended Operating Conditions to ensure proper operation.

3.5. Hot Socketing Specifications

Table 3.5. Hot Socketing Specifications

Symbol	Parameter	Condition	Max.	Units
I_{DK}	Input or I/O leakage Current	$0 < V_{IN} < V_{IH}$ (MAX)	± 1000	µA

Notes:

- Insensitive to sequence of V_{CC} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCIO}.
- $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCIO} < V_{CCIO}$ (MAX).
- I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.

3.6. Programming/Erase Specifications

Table 3.6. Programming/Erase Specifications

Symbol	Parameter	Min.	Max.[1]	Units
$N_{PROGCYC}$	NVCM CFG, UFM, and Feature Row Programming cycles per $t_{RETENTION}$	—	9	Cycles
	Flash Programming cycles per $t_{RETENTION}$	—	10,000	
	Flash Write/Erase cycles[2]	—	100,000	
$t_{RETENTION}$	Data retention at 100 °C junction temperature	10	—	Years
	Data retention at 85 °C junction temperature	20	—	

Notes:

1. All times are averages, in (ms). SRAM erase times are < 0.1 ms.
2. tErase (max) is recommended for algorithm based time-outs.

3.7. ESD Performance

Refer to the MachXO3/MachXO3LF Product Family Qualification Summary for complete qualification data, including ESD performance.

3.8. DC Electrical Characteristics

Over recommended operating conditions.

Table 3.7. DC Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 4]	Input or I/O Leakage	Clamp OFF and $V_{CCIO} < V_{IN} < V_{IH}$ (MAX)	—	—	+175	µA
		Clamp OFF and $V_{IN} = V_{CCIO}$	–10	—	10	µA
		Clamp OFF and V_{CCIO} - 0.97 V < V_{IN} < V_{CCIO}	–175	—	—	µA
		Clamp OFF and 0 V < V_{IN} < V_{CCIO} – 0.97 V	—	—	10	µA
		Clamp OFF and V_{IN} = GND	—	—	10	µA
		Clamp ON and 0 V < V_{IN} < V_{CCIO}	—	—	10	µA
I_{PU}	I/O Active Pull-up Current	0 < V_{IN} < 0.7 V_{CCIO}	–30	—	–309	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) < V_{IN} < V_{CCIO}	30	—	305	µA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	–30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive current	0 ≤ V_{IN} ≤ V_{CCIO}	—	—	305	µA
I_{BHHO}	Bus Hold High Overdrive current	0 ≤ V_{IN} ≤ V_{CCIO}	—	—	–309	µA
V_{BHT}[3]	Bus Hold Trip Points	—	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	3	5	9	pf
V_{HYST}	Hysteresis for Schmitt Trigger Inputs[5]	V_{CCIO} = 3.3 V, Hysteresis = Large	—	450	—	mV
		V_{CCIO} = 2.5 V, Hysteresis = Large	—	250	—	mV
		V_{CCIO} = 1.8 V, Hysteresis = Large	—	125	—	mV
		V_{CCIO} = 1.5 V, Hysteresis = Large	—	100	—	mV
		V_{CCIO} = 3.3 V, Hysteresis = Small	—	250	—	mV
		V_{CCIO} = 2.5 V, Hysteresis = Small	—	150	—	mV
		V_{CCIO} = 1.8 V, Hysteresis = Small	—	60	—	mV
		V_{CCIO} = 1.5 V, Hysteresis = Small	—	40	—	mV

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25 °C, f = 1.0 MHz.
3. Refer to V_{IL} and V_{IH} in the sysI/O Single-Ended DC Electrical Characteristics table of this document.
4. When V_{IH} is higher than V_{CCIO}, a transient current typically of 30 ns in duration or less with a peak current of 6 mA can occur on the high-to-low transition. For true LVDS output pins in MachXO3L/LF devices, V_{IH} must be less than or equal to V_{CCIO}.
5. With bus keeper circuit turned on. For more details, refer to MachXO3 sysI/O Usage Guide (FPGA-TN-02047).

3.9. Static Supply Current – C/E Devices

Table 3.8. Static Supply Current – C/E Devices[1, 2, 3, 6]

Symbol	Parameter	Device	Typ.[4]	Units
I_{CC}	Core Power Supply	LCMXO3/L/LF-1300C 256 Ball Package	4.8	mA
		LCMXO3L/LF-2100C	4.8	mA
		LCMXO3L/LF-2100C 324 Ball Package	8.45	mA
		LCMXO3L/LF-4300C	8.45	mA
		LCMXO3L/LF-4300C 400 Ball Package	12.87	mA
		LCMXO3L/LF-6900C	12.87	mA
		LCMXO3L/LF-9400C	17.86	mA
		LCMXO3L/LF-640E	1.00	mA
		LCMXO3L/LF-1300E	1.00	mA
		LCMXO3L/LF-1300E 256 Ball Package	1.39	mA
		LCMXO3L/LF-2100E	1.39	mA
		LCMXO3L/LF-2100E 324 Ball Package	2.55	mA
		LCMXO3L/LF-4300E	2.55	mA
		LCMXO3L/LF-6900E	4.06	mA
		LCMXO3L/LF-9400E	5.66	mA
I_{CCIO}	Bank Power Supply[5] V_{CCIO} = 2.5 V	All devices	0	mA

Notes:

1. For further information on supply current, refer to Power and Thermal Estimation and Management for MachXO3 Devices (FPGA-TN-02059).
2. Assumes a test pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off.
3. Frequency = 0 MHz.
4. TJ = 25 °C, power supplies at nominal voltage.
5. Does not include pull-up/pull-down.
6. To determine the MachXO3L/LF peak start-up current data, use the Power Calculator tool.

3.10. Programming and Erase Supply Current – C/E Devices

Table 3.9. Programming and Erase Supply Current – C/E Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ.[4]	Units
I_{CC}	Core Power Supply	LCMXO3L/LF-1300C 256 Ball Package	22.1	mA
		LCMXO3L/LF-2100C	22.1	mA
		LCMXO3L/LF-2100C 324 Ball Package	26.8	mA
		LCMXO3L/LF-4300C	26.8	mA
		LCMXO3L/LF-4300C 400 Ball Package	33.2	mA
		LCMXO3L/LF-6900C	33.2	mA
		LCMXO3L/LF-9400C	39.6	mA
		LCMXO3L/LF-640E	17.7	mA
		LCMXO3L/LF-1300E	17.7	mA
		LCMXO3L/LF-1300E 256 Ball Package	18.3	mA
		LCMXO3L/LF-2100E	18.3	mA
		LCMXO3L/LF-2100E 324 Ball Package	20.4	mA
		LCMXO3L/LF-4300E	20.4	mA
		LCMXO3L/LF-6900E	23.9	mA
		LCMXO3L/LF-9400E	28.5	mA
I_{CCIO}	Bank Power Supply[5] V_{CCIO} = 2.5 V	All devices	0	mA

Notes:

1. For further information on supply current, refer to Power and Thermal Estimation and Management for MachXO3 Devices (FPGA-TN-02059).
2. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
3. Typical user pattern.
4. JTAG programming is at 25 MHz.
5. T_J = 25 °C, power supplies at nominal voltage.
6. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up/pull-down.

3.11. sysI/O Recommended Operating Conditions

Table 3.10. sysI/O Recommended Operating Conditions

Standard	V_{CCIO} (V)			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.135	3.3	3.465	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
LVDS25[1, 2]	2.375	2.5	2.625	—	—	—
LVDS33[1, 2]	3.135	3.3	3.465	—	—	—
LVPECL[1]	3.135	3.3	3.465	—	—	—
BLVDS[1]	2.375	2.5	2.625	—	—	—
MIPI[3]	2.375	2.5	2.625	—	—	—
MIPI_LP[3]	1.14	1.2	1.26	—	—	—
LVCMOS25R33	3.135	3.3	3.6	1.1	1.25	1.4
LVCMOS18R33	3.135	3.3	3.6	0.75	0.9	1.05
LVCMOS18R25	2.375	2.5	2.625	0.75	0.9	1.05
LVCMOS15R33	3.135	3.3	3.6	0.6	0.75	0.9
LVCMOS15R25	2.375	2.5	2.625	0.6	0.75	0.9
LVCMOS12R33[4]	3.135	3.3	3.6	0.45	0.6	0.75
LVCMOS12R25[4]	2.375	2.5	2.625	0.45	0.6	0.75
LVCMOS10R33[4]	3.135	3.3	3.6	0.35	0.5	0.65
LVCMOS10R25[4]	2.375	2.5	2.625	0.35	0.5	0.65

Notes:

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.
2. For the dedicated LVDS buffers.
3. Requires the addition of external resistors.
4. Supported only for inputs and BIDIs for –6 speed grade devices.

3.12. sysI/O Single-Ended DC Electrical Characteristics

Table 3.11. sysI/O Single-Ended DC Electrical Charateristics[1, 2, 4]

Standard	VIL		VIH		VOL Max. (V)	VOH Min. (V)	IOL Max.[5] (mA)	IOH Max.[5] (mA)
	Min. (V)[3]	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3 LVTTL	–0.3	0.8	2.0	3.6	0.4	VCCIO – 0.4	4	–4
							8	–8
							12	–12
							16	–16
					0.2	VCCIO – 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	3.6	0.4	VCCIO – 0.4	4	–4
							8	–8
							12	–12
							16	–16
					0.2	VCCIO – 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	0.35 VCCIO	0.65 VCCIO	3.6	0.4	VCCIO – 0.4	4	–4
							8	–8
							12	–12
					0.2	VCCIO – 0.2	0.1	–0.1
LVCMOS 1.5	–0.3	0.35 VCCIO	0.65 VCCIO	3.6	0.4	VCCIO – 0.4	4	–4
							8	–8
					0.2	VCCIO – 0.2	0.1	–0.1
LVCMOS 1.2	–0.3	0.35 VCCIO	0.65 VCCIO	3.6	0.4	VCCIO – 0.4	4	–2
							8	–6
					0.2	VCCIO – 0.2	0.1	–0.1
LVCMOS25R33	–0.3	VREF – 0.1	VREF+0.1	3.6	NA	NA	NA	NA
LVCMOS18R33	–0.3	VREF – 0.1	VREF+0.1	3.6	NA	NA	NA	NA
LVCMOS18R25	–0.3	VREF – 0.1	VREF+0.1	3.6	NA	NA	NA	NA
LVCMOS15R33	–0.3	VREF – 0.1	VREF+0.1	3.6	NA	NA	NA	NA
LVCMOS15R25	–0.3	VREF – 0.1	VREF+0.1	3.6	NA	NA	NA	NA
LVCMOS12R33	–0.3	VREF – 0.1	VREF+0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain
LVCMOS12R25	–0.3	VREF – 0.1	VREF+0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain
LVCMOS10R33	–0.3	VREF – 0.1	VREF+0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain
LVCMOS10R25	-0.3	VREF – 0.1	VREF+0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain

Notes:

1. MachXO3L/LF devices allow LVCMOS inputs to be placed in I/O banks where V_{CCIO} is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases this operation follows or exceeds the applicable JEDEC specification. The cases where MachXO3L/LF devices do not meet the relevant JEDEC specification are documented in the table below.
2. MachXO3L/LF devices allow for LVCMOS referenced I/Os which follow applicable JEDEC specifications. For more details about mixed mode operation please refer to please refer to MachXO3 sysI/O Usage Guide (FPGA-TN-02047).
3. The dual function I^2C pins SCL and SDA are limited to a VIL min of –0.25 V or to –0.3 V with a duration of <10 ns.
4. V_{CCIO} represents the typical value as listed in the following tables for the respective I/O standard.
5. For electromigration, the average DC current sourced or sinked by I/O pads between two consecutive V_{CCIO} or GND pad connections, or between the last V_{CCIO} or GND in an I/O bank and the end of an I/O bank, shall not exceed a maximum of n * 8 mA. “n” is the number of I/O pads between the two consecutive bank V_{CCIO} or GND connections or between the last V_{CCIO} and GND in a bank and the end of a bank. I/O Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.

3.13. sysI/O Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of the MachXO3L/LF PLD family.

3.13.1. LVDS

Over recommended operating conditions.

Table 3.12. LVDS

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage	V_{CCIO} = 3.3 V	0	—	2.605	V
		V_{CCIO} = 2.5 V	0	—	2.05	V
V_{THD}	Differential Input Threshold	—	±100	—	—	mV
V_{CM}	Input Common Mode Voltage	V_{CCIO} = 3.3 V	0.05	—	2.6	V
		V_{CCIO} = 2.5 V	0.05	—	2.0	V
I_{IN}	Input current	Power on	—	—	±10	µA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	R_T = 100 Ω	—	1.375	—	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	R_T = 100 Ω	0.90	1.025	—	V
V_{OD}	Output voltage differential	(V_{OP} - V_{OM}), R_T = 100 Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low	—	—	—	50	mV
V_{OS}	Output voltage offset	(V_{OP} - V_{OM})/2, R_T = 100 Ω	1.125	1.20	1.395	V
ΔV_{OS}	Change in V_{OS} between H and L	—	—	—	50	mV
I_{OSD}	Output short circuit current	V_{OD} = 0 V driver outputs shorted	—	—	24	mA

3.13.2. LVDS Emulation

MachXO3L/LF devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3.1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3.1 are industry standard values for 1% resistors.

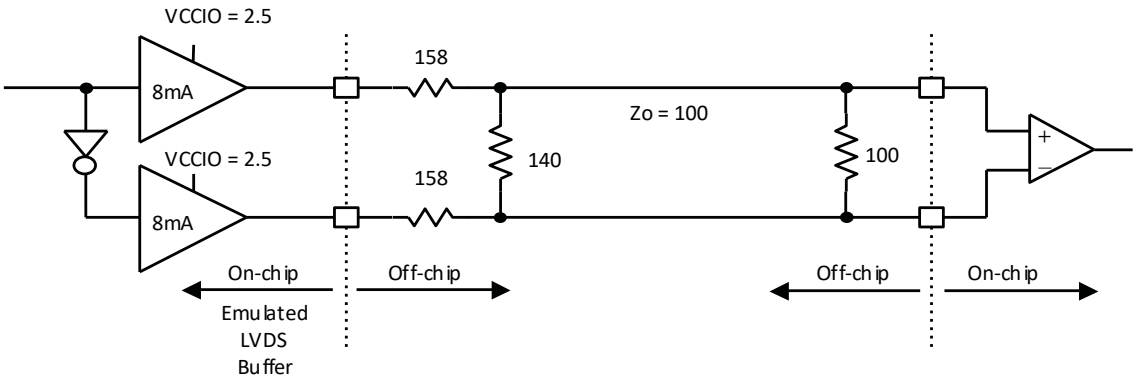


Figure 3.1. LVDS Using External Resistors (LVDS25E)

Over recommended operating conditions.

Table 3.13. LVDS25E DC Conditions

Parameter	Description	Typ.	Units
Z_{OUT}	Output impedance	20	Ω
R_S	Driver series resistor	158	Ω
R_P	Driver parallel resistor	140	Ω
R_T	Receiver termination	100	Ω
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100.5	Ω
I_{DC}	DC output current	6.03	mA

3.13.3. BLVDS

The MachXO3L/LF family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3.2 is one possible solution for bi-directional multi-point differential signals.

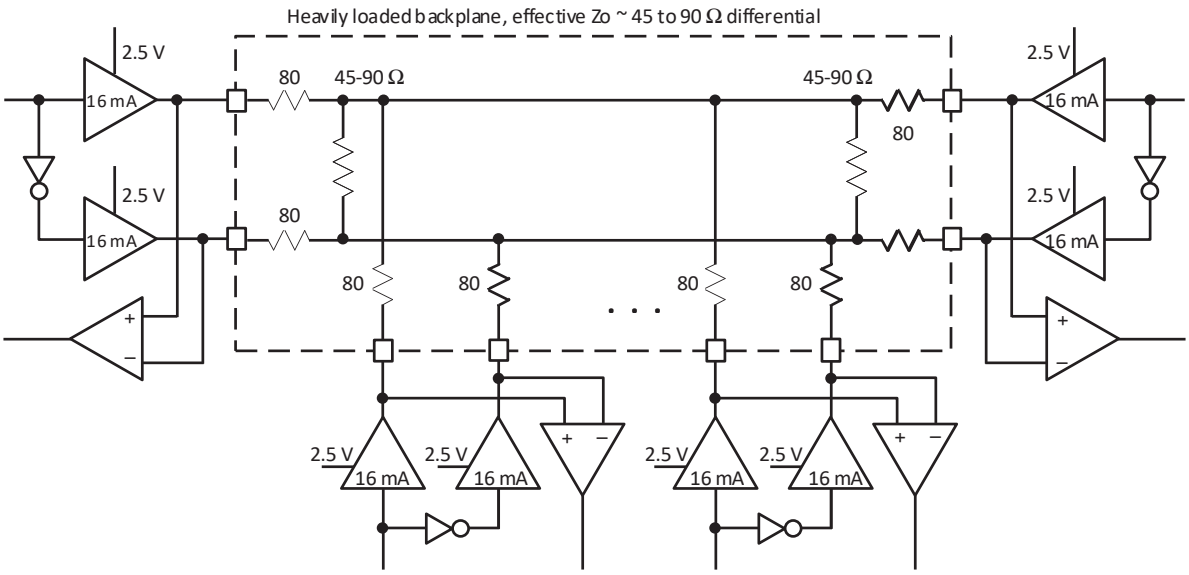


Figure 3.2. BLVDS Multi-point-Output Example

Over recommended operating conditions.

Table 3.14. BLVDS DC Condition

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	20	20	Ω
R_S	Driver series resistance	80	80	Ω
R_{TLEFT}	Left end termination	45	90	Ω
R_{TRIGHT}	Right end termination	45	90	Ω
V_{OH}	Output high voltage	1.376	1.480	V
V_{OL}	Output low voltage	1.124	1.020	V
V_{OD}	Output differential voltage	0.253	0.459	V
V_{CM}	Output common mode voltage	1.250	1.250	V
I_{DC}	DC output current	11.236	10.204	mA

Note: For input buffer, see LVDS table.

3.13.4. LVPECL

The MachXO3L/LF family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Differential LVPECL is one possible solution for point-to-point signals.

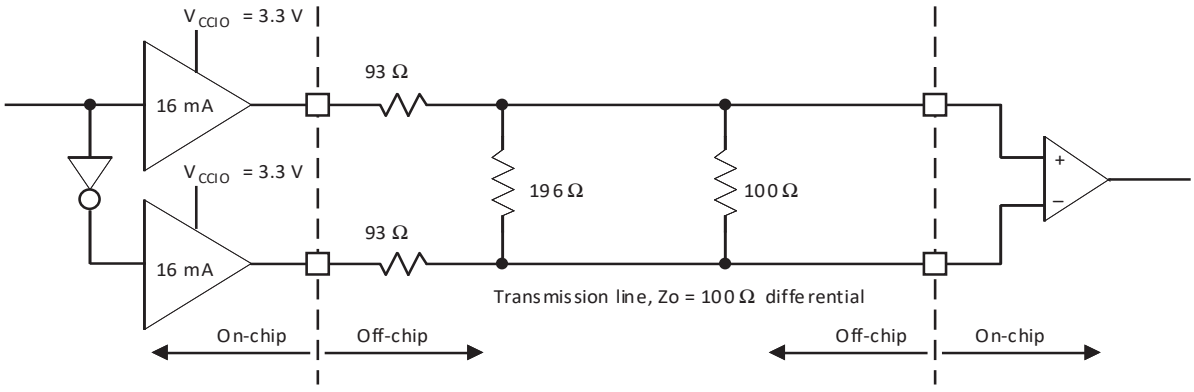


Figure 3.3. Differential LVPECL

Over recommended operating conditions.

Table 3.15. LVPECL DC Conditions

Symbol	Description	Nominal	Units
Z_{OUT}	Output impedance	20	Ω
R_S	Driver series resistor	93	Ω
R_P	Driver parallel resistor	196	Ω
R_T	Receiver termination	100	Ω
V_{OH}	Output high voltage	2.05	V
V_{OL}	Output low voltage	1.25	V
V_{OD}	Output differential voltage	0.80	V
V_{CM}	Output common mode voltage	1.65	V
Z_{BACK}	Back impedance	100.5	Ω
I_{DC}	DC output current	12.11	mA

Note: For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces, see details of additional technical documentation at the end of the data sheet.

3.13.5. MIPI D-PHY Emulation

MachXO3L/LF devices can support MIPI D-PHY unidirectional HS (High Speed) and bidirectional LP (Low Power) inputs and outputs via emulation. In conjunction with external resistors High Speed I/Os use the LVDS25E buffer and Low Power I/Os use the LVCMOS buffers. The scheme shown in Figure 3.4 is one possible solution for MIPI D-PHY Receiver implementation. The scheme shown in Figure 3.5 is one possible solution for MIPI D-PHY Transmitter implementation.

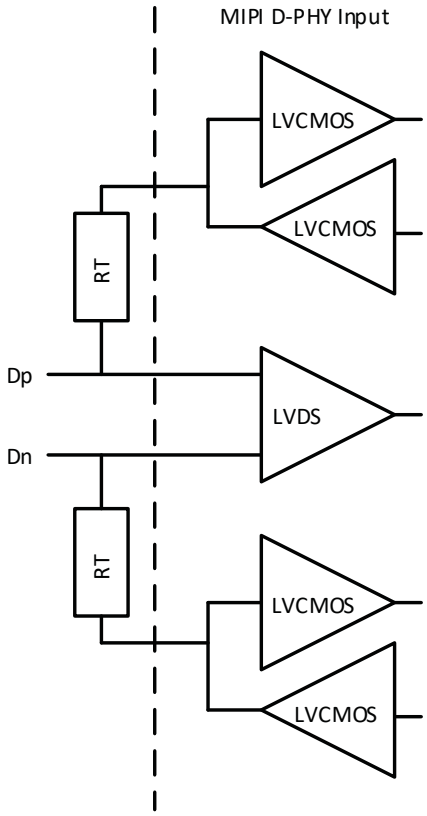


Figure 3.4. MIPI D-PHY Input Using External Resistors

Over recommended operating conditions.

Table 3.16. MIPI DC Conditions

	Description	Min.	Typ.	Max.	Units
Receiver					
External Termination					
RT	1% external resistor with V_{CCIO}=2.5 V	—	50	—	Ω
	1% external resistor with V_{CCIO}=3.3 V	—	50	—	Ω
High Speed					
V_{CCIO}	V_{CCIO} of the Bank with LVDS Emulated input buffer	—	2.5	—	V
	V_{CCIO} of the Bank with LVDS Emulated input buffer	—	3.3	—	V
V_{CMRX}	Common-mode voltage HS receive mode	150	200	250	mV
V_{IDTH}	Differential input high threshold	—	—	100	mV
V_{IDTL}	Differential input low threshold	–100	—	—	mV
V_{IHHS}	Single-ended input high voltage	—	—	300	mV
V_{ILHS}	Single-ended input low voltage	100	—	—	mV
ZID	Differential input impedance	80	100	120	Ω
Low Power					
V_{CCIO}	V_{CCIO} of the Bank with LVCMOS12D 6 mA drive bidirectional I/O buffer	—	1.2	—	V
V_{IH}	Logic 1 input voltage	—	—	0.88	V
V_{IL}	Logic 0 input voltage, not in ULP State	0.55	—	—	V
V_{HYST}	Input hysteresis	25	—	—	mV

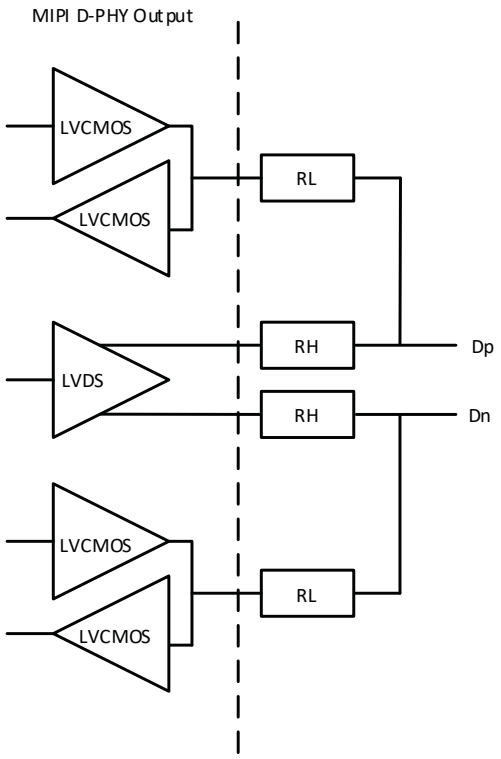


Figure 3.5. MIPI D-PHY Output Using External Resistors

Over recommended operating conditions.

Table 3.17. MIPI D-PHY Output DC Conditions

	Description	Min.	Typ.	Max.	Units
Transmitter					
External Termination					
R_L	1% external resistor with V_{CCIO} = 2.5 V	—	50	—	Ω
	1% external resistor with V_{CCIO} = 3.3 V	—	50	—	
R_H	1% external resistor with performance up to 800 Mbps or with performance up 900 Mbps when V_{CCIO} = 2.5 V	—	330	—	Ω
	1% external resistor with performance between 800 Mbps to 900 Mbps when V_{CCIO} = 3.3 V	—	464	—	Ω
High Speed					
V_{CCIO}	V_{CCIO} of the Bank with LVDS Emulated output buffer	—	2.5	—	V
	V_{CCIO} of the Bank with LVDS Emulated output buffer	—	3.3	—	V
V_{CMTX}	HS transmit static common mode voltage	150	200	250	mV
V_{OD}	HS transmit differential voltage	140	200	270	mV
V_{OHHS}	HS output high voltage	—	—	360	V
ZOS	Single ended output impedance	—	50	—	Ω
ΔZOS	Single ended output impedance mismatch	—	—	10	%
Low Power					
V_{CCIO}	V_{CCIO} of the Bank with LVCMOS12D 6 mA drive bidirectional I/O buffer	—	1.2	—	V
V_{OH}	Output high level	1.1	1.2	1.3	V
V_{OL}	Output low level	–50	0	50	mV
ZOLP	Output impedance of LP transmitter	110	—	—	Ω

3.14.Typical Building Block Function Performance – C/E Devices

3.14.1. Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Table 3.18. Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–6 Timing	Units
Basic Functions		
16-bit decoder	8.9	ns
4:1 MUX	7.5	ns
16:1 MUX	8.3	ns

3.14.2. Register-to-Register Performance

Table 3.19. Register-to-Register Performance

Function	–6 Timing	Units
Basic Functions		
16:1 MUX	412	MHz
16-bit adder	297	MHz
16-bit counter	324	MHz
64-bit counter	161	MHz
Embedded Memory Functions		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	183	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	500	MHz

Note: The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

3.15. Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

3.16. Maximum sysI/O Buffer Performance

Table 3.20. Maximum sysI/O Buffer Performance

I/O Standard	Max. Speed	Units
MIPI	450	MHz
LVDS25	400	MHz
LVDS25E	150	MHz
BLVDS25	150	MHz
BLVDS25E	150	MHz
MLVDS25	150	MHz
MLVDS25E	150	MHz
LVPECL33	150	MHz
LVPECL33E	150	MHz
LVTTL33	150	MHz
LVTTL33D	150	MHz
LVCMOS33	150	MHz
LVCMOS33D	150	MHz
LVCMOS25	150	MHz
LVCMOS25D	150	MHz
LVCMOS18	150	MHz
LVCMOS18D	150	MHz
LVCMOS15	150	MHz
LVCMOS15D	150	MHz
LVCMOS12	91	MHz
LVCMOS12D	91	MHz

3.17. MachXO3L/LF External Switching Characteristics – C/E Devices

Over recommended operating conditions.

Table 3.21. MachXO3L/LF External Switching Characteristics – C/E Devices[1, 2, 3, 4, 5, 6, 10]

Parameter	Description	Device	–6		–5		Units
			Min.	Max.	Min.	Max.	
Clocks							
Primary Clocks							
f_{MAX_PRI}[7]	Frequency for Primary Clock Tree	All MachXO3L/LF devices	—	388	—	323	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO3L/LF devices	0.5	—	0.6	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	MachXO3L/LF-1300	—	867	—	897	ps
		MachXO3L/LF-2100	—	867	—	897	ps
		MachXO3L/LF-4300	—	865	—	892	ps
		MachXO3L/LF-6900	—	902	—	942	ps
		MachXO3L/LF-9400	—	908	—	950	ps
Edge Clock							
f_{MAX_EDGE}[7]	Frequency for Edge Clock	MachXO3L/LF	—	400	—	333	MHz
Pin-LUT-Pin Propagation Delay							
t_{PD}	Best case propagation delay through one LUT-4	All MachXO3L/LF devices	—	6.72	—	6.96	ns
General I/O Pin Parameters (Using Primary Clock without PLL)							
t_{CO}	Clock to Output – PIO Output Register	MachXO3L/LF-1300	—	7.46	—	7.66	ns
		MachXO3L/LF-2100	—	7.46	—	7.66	ns
		MachXO3L/LF-4300	—	7.51	—	7.71	ns
		MachXO3L/LF-6900	—	7.54	—	7.75	ns
		MachXO3L/LF-9400	—	7.53	—	7.83	ns
t_{SU}	Clock to Data Setup – PIO Input Register	MachXO3L/LF-1300	–0.20	—	–0.20	—	ns
		MachXO3L/LF-2100	–0.20	—	–0.20	—	ns
		MachXO3L/LF-4300	–0.23	—	–0.23	—	ns
		MachXO3L/LF-6900	–0.23	—	–0.23	—	ns
		MachXO3L/LF-9400	–0.24	—	–0.24	—	ns
t_{H}	Clock to Data Hold – PIO Input Register	MachXO3L/LF-1300	1.89	—	2.13	—	ns
		MachXO3L/LF-2100	1.89	—	2.13	—	ns
		MachXO3L/LF-4300	1.94	—	2.18	—	ns
		MachXO3L/LF-6900	1.98	—	2.23	—	ns
		MachXO3L/LF-9400	1.99	—	2.24	—	ns
t_{SU_DEL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO3L/LF-1300	1.61	—	1.76	—	ns
		MachXO3L/LF-2100	1.61	—	1.76	—	ns
		MachXO3L/LF-4300	1.66	—	1.81	—	ns
		MachXO3L/LF-6900	1.53	—	1.67	—	ns
		MachXO3L/LF-9400	1.65	—	1.80	—	ns
t_{H_DEL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO3L/LF-1300	–0.23	—	–0.23	—	ns
		MachXO3L/LF-2100	–0.23	—	–0.23	—	ns
		MachXO3L/LF-4300	–0.25	—	–0.25	—	ns
		MachXO3L/LF-6900	–0.21	—	–0.21	—	ns
		MachXO3L/LF-9400	–0.24	—	–0.24	—	ns
$f_{MAX\_I/O}$	Clock Frequency of I/O and PFU Register	All MachXO3L/LF devices	—	388	—	323	MHz

Parameter	Description	Device	–6		–5		Units
			Min.	Max.	Min.	Max.	
General I/O Pin Parameters (Using Edge Clock without PLL)							
t_{COE}	Clock to Output – PIO Output Register	MachXO3L/LF-1300	—	7.53	—	7.76	ns
		MachXO3L/LF-2100	—	7.53	—	7.76	ns
		MachXO3L/LF-4300	—	7.45	—	7.68	ns
		MachXO3L/LF-6900	—	7.53	—	7.76	ns
		MachXO3L/LF-9400	—	8.93	—	9.35	ns
t_{SUE}	Clock to Data Setup – PIO Input Register	MachXO3L/LF-1300	–0.19	—	–0.19	—	ns
		MachXO3L/LF-2100	–0.19	—	–0.19	—	ns
		MachXO3L/LF-4300	–0.16	—	–0.16	—	ns
		MachXO3L/LF-6900	–0.19	—	–0.19	—	ns
		MachXO3L/LF-9400	–0.20	—	–0.20	—	ns
t_{HE}	Clock to Data Hold – PIO Input Register	MachXO3L/LF-1300	1.97	—	2.24	—	ns
		MachXO3L/LF-2100	1.97	—	2.24	—	ns
		MachXO3L/LF-4300	1.89	—	2.16	—	ns
		MachXO3L/LF-6900	1.97	—	2.24	—	ns
		MachXO3L/LF-9400	1.98	—	2.25	—	ns
t_{SU_DELE}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO3L/LF-1300	1.56	—	1.69	—	ns
		MachXO3L/LF-2100	1.56	—	1.69	—	ns
		MachXO3L/LF-4300	1.74	—	1.88	—	ns
		MachXO3L/LF-6900	1.66	—	1.81	—	ns
		MachXO3L/LF-9400	1.71	—	1.85	—	ns
t_{H_DELE}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO3L/LF-1300	–0.23	—	–0.23	—	ns
		MachXO3L/LF-2100	–0.23	—	–0.23	—	ns
		MachXO3L/LF-4300	–0.34	—	–0.34	—	ns
		MachXO3L/LF-6900	–0.29	—	–0.29	—	ns
		MachXO3L/LF-9400	–0.30	—	–0.30	—	ns
General I/O Pin Parameters (Using Primary Clock with PLL)							
t_{COPLL}	Clock to Output – PIO Output Register	MachXO3L/LF-1300	—	5.98	—	6.01	ns
		MachXO3L/LF-2100	—	5.98	—	6.01	ns
		MachXO3L/LF-4300	—	5.99	—	6.02	ns
		MachXO3L/LF-6900	—	6.02	—	6.06	ns
		MachXO3L/LF-9400	—	5.55	—	6.13	ns
t_{SUPLL}	Clock to Data Setup – PIO Input Register	MachXO3L/LF-1300	0.36	—	0.36	—	ns
		MachXO3L/LF-2100	0.36	—	0.36	—	ns
		MachXO3L/LF-4300	0.35	—	0.35	—	ns
		MachXO3L/LF-6900	0.34	—	0.34	—	ns
		MachXO3L/LF-9400	0.33	—	0.33	—	ns
t_{HPLL}	Clock to Data Hold – PIO Input Register	MachXO3L/LF-1300	0.42	—	0.49	—	ns
		MachXO3L/LF-2100	0.42	—	0.49	—	ns
		MachXO3L/LF-4300	0.43	—	0.50	—	ns
		MachXO3L/LF-6900	0.46	—	0.54	—	ns
		MachXO3L/LF-9400	0.47	—	0.55	—	ns

Parameter	Description	Device	–6		–5		Units
			Min.	Max.	Min.	Max.	
t_{SU_DELPLL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO3L/LF-1300	2.87	—	3.18	—	ns
		MachXO3L/LF-2100	2.87	—	3.18	—	ns
		MachXO3L/LF-4300	2.96	—	3.28	—	ns
		MachXO3L/LF-6900	3.05	—	3.35	—	ns
		MachXO3L/LF-9400	3.06	—	3.37	—	ns
t_{H_DELPLL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO3L/LF-1300	–0.83	—	–0.83	—	ns
		MachXO3L/LF-2100	–0.83	—	–0.83	—	ns
		MachXO3L/LF-4300	–0.87	—	–0.87	—	ns
		MachXO3L/LF-6900	–0.91	—	–0.91	—	ns
		MachXO3L/LF-9400	–0.93	—	–0.93	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[8, 9]							
t_{DVA}	Input Data Valid After CLK	All MachXO3L/LF devices, all sides	—	0.317	—	0.344	UI
t_{DVE}	Input Data Hold After CLK		0.742	—	0.702	—	UI
f_{DATA}	DDRX1 Input Data Speed		—	300	—	250	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[8, 9]							
t_{SU}	Input Data Setup Before CLK	All MachXO3L/LF devices, all sides	0.566	—	0.560	—	ns
t_{HO}	Input Data Hold After CLK		0.778	—	0.879	—	ns
f_{DATA}	DDRX1 Input Data Speed		—	300	—	—	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[8, 9]							
t_{DVA}	Input Data Valid After CLK	MachXO3L/LF devices, bottom side only	—	0.316	—	0.342	UI
t_{DVE}	Input Data Hold After CLK		0.710	—	0.675	—	UI
f_{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[8, 9]							
t_{SU}	Input Data Setup Before CLK	MachXO3L/LF devices, bottom side only	0.233	—	0.219	—	ns
t_{HO}	Input Data Hold After CLK		0.287	—	0.287	—	ns
f_{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	MHz
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Aligned[8]							
t_{DVA}	Input Data Valid After ECLK	MachXO3L/LF devices, bottom side only	—	0.307	—	0.320	UI
t_{DVE}	Input Data Hold After ECLK		0.782	—	0.699	—	UI
f_{DATA}	DDRX4 Serial Input Data Speed		—	800	—	630	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	400	—	315	MHz
f_{SCLK}	SCLK Frequency		—	100	—	79	MHz
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Centered[8]							
t_{SU}	Input Data Setup Before ECLK	MachXO3L/LF devices, bottom side only	0.233	—	0.219	—	ns
t_{HO}	Input Data Hold After ECLK		0.287	—	0.287	—	ns
f_{DATA}	DDRX4 Serial Input Data Speed		—	800	—	630	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	400	—	315	MHz
f_{SCLK}	SCLK Frequency		—	100	—	79	MHz

Parameter	Description	Device	–6		–5		Units
			Min.	Max.	Min.	Max.	
7:1 LVDS Inputs (GDDR71_RX.ECLK.7:1)[9]							
t_{DVA}	Input Data Valid After ECLK	MaxhXO3L/LF devices, bottom side only	—	0.290	—	0.320	UI
t_{DVE}	Input Data Hold After ECLK		0.739	—	0.699	—	UI
f_{DATA}	DDR71 Serial Input Data Speed		—	756	—	630	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	378	—	315	MHz
f_{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	MHz
MIPI D-PHY Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - GDDRX4_RX.ECLK.Centered[10, 11, 12]							
t_{SU}[15]	Input Data Setup Before ECLK	All MachXO3L/LF devices, bottom side only	0.200	—	0.200	—	UI
t_{HO}[15]	Input Data Hold After ECLK		0.200	—	0.200	—	UI
f_{DATA}[14]	MIPI D-PHY Input Data Speed		—	900	—	900	Mbps
f_{DDRX4}[14]	MIPI D-PHY ECLK Frequency		—	450	—	450	MHz
f_{SCLK}[14]	SCLK Frequency		—	112.5	—	112.5	MHz
Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Aligned[8]							
t_{DIA}	Output Data Invalid After CLK Output	All MachXO3L/LF devices, all sides	—	0.520	—	0.550	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.520	—	0.550	ns
f_{DATA}	DDRX1 Output Data Speed		—	300	—	250	Mbps
f_{DDRX1}	DDRX1 SCLK frequency		—	150	—	125	MHz
Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Centered[8]							
t_{DVB}	Output Data Valid Before CLK Output	All MachXO3L/LF devices, all sides	1.210	—	1.510	—	ns
t_{DVA}	Output Data Valid After CLK Output		1.210	—	1.510	—	ns
f_{DATA}	DDRX1 Output Data Speed		—	300	—	250	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency (minimum limited by PLL)		—	150	—	125	MHz
Generic DDRX2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Aligned[8]							
t_{DIA}	Output Data Invalid After CLK Output	MachXO3L/LF devices, top side only	—	0.200	—	0.215	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	664	—	554	Mbps
f_{DDRX2}	DDRX2 ECLK frequency		—	332	—	277	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	MHz
Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered[8, 9]							
t_{DVB}	Output Data Valid Before CLK Output	MachXO3L/LF devices, top side only	0.535	—	0.670	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.535	—	0.670	—	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	664	—	554	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)		—	332	—	277	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	MHz

Parameter	Description	Device	–6		–5		Units
			Min.	Max.	Min.	Max.	
Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned[8, 9]							
t_{DIA}	Output Data Invalid After CLK Output	MachXO3L/LF devices, top side only	—	0.200	—	0.215	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	800	—	630	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	400	—	315	MHz
f_{SCLK}	SCLK Frequency		—	100	—	79	MHz
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[8, 9]							
t_{DVB}	Output Data Valid Before CLK Output	MachXO3L/LF devices, top side only	0.455	—	0.570	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.455	—	0.570	—	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	800	—	630	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)		—	400	—	315	MHz
f_{SCLK}	SCLK Frequency		—	100	—	79	MHz
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1[8, 9]							
t_{DIB}	Output Data Invalid Before CLK Output	MachXO3L/LF devices, top side only	—	0.160	—	0.180	ns
t_{DIA}	Output Data Invalid After CLK Output		—	0.160	—	0.180	ns
f_{DATA}	DDR71 Serial Output Data Speed		—	756	—	630	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	378	—	315	MHz
f_{CLKOUT}	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	MHz
MIPI D-PHY Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[10, 11, 12]							
t_{DVB}	Output Data Valid Before CLK Output	All MachXO3L/LF devices, top side only	0.200	—	0.200	—	UI
t_{DVA}	Output Data Valid After CLK Output		0.200	—	0.200	—	UI
f_{DATA}	MIPI D-PHY Output Data Speed		—	900	—	900	Mbps
F_{DDRX4}	MIPI D-PHY ECLK Frequency (minimum limited by PLL)		—	450	—	450	MHz
f_{SCLK}	SCLK Frequency		—	112.5	—	112.5	MHz

Notes:

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
5. For Generic DDRX1 mode tSU = tHO = (tDVE - tDVA - 0.03 ns)/2.
6. The tSU_DEL and tH_DEL values use the SCLK_ZERHOLD default step size. Each step is 105 ps (–6), 113 ps (–5), 120 ps (–4).
7. This number for general purpose usage. Duty cycle tolerance is +/–10%.
8. Duty cycle is +/– 5% for system usage.
9. Performance is calculated with 0.225 UI.
10. Performance is calculated with 0.20 UI.

11. Performance for Industrial devices are only supported with VCC between 1.16 V to 1.24 V.
12. Performance for Industrial devices and –5 devices are not modeled in the Diamond design tool.
13. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
14. Above 800 Mbps is only supported with WLCSP and csfBGA packages.
15. Between 800 Mbps to 900 Mbps:
    - VIDTH exceeds the MIPI D-PHY Input DC Conditions (Table 3.16) and can be calculated with the equation tSU or tH = -0.0005*VIDTH + 0.3284
      Example calculations:
      - t_{SU} and t_{HO} = 0.28 with VIDTH = 100 mV
      - t_{SU} and t_{HO} = 0.25 with VIDTH = 170 mV
      - t_{SU} and t_{HO} = 0.20 with VIDTH = 270 mV

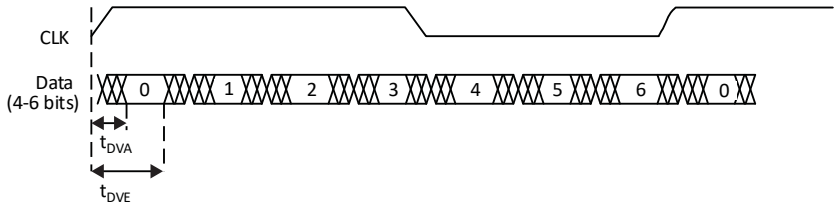


Figure 3.6.Receiver GDDR71_RX. Waveforms

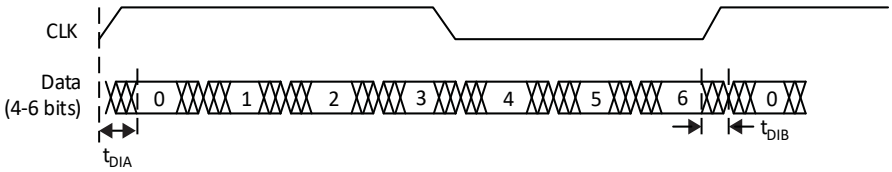


Figure 3.7. Transmitter GDDR71_TX. Waveforms

3.18. sysCLOCK PLL Timing

Over recommended operating conditions.

Table 3.22. sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	—	7	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS, CLKOS2)	—	1.5625	400	MHz
f_{OUT2}	Output Frequency (CLKOS3 cascaded from CLKOS2)	—	0.0122	400	MHz
f_{VCO}	PLL VCO Frequency	—	200	800	MHz
f_{PFD}	Phase Detector Input Frequency	—	7	400	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	Without duty trim selected3	45	55	%
t_{DT_TRIM}[7]	Edge Duty Trim Accuracy	—	–75	75	%
t_{PH}[4]	Output Phase Accuracy	—	–6	6	%
t_{OPJIT}[1, 8]	Output Clock Period Jitter	fOUT > 100 MHz	—	150	ps p-p
		fOUT < 100 MHz	—	0.007	UIPP
	Output Clock Cycle-to-cycle Jitter	fOUT > 100 MHz	—	180	ps p-p
		fOUT < 100 MHz	—	0.009	UIPP
	Output Clock Phase Jitter	fPFD > 100 MHz	—	160	ps p-p
		fPFD < 100 MHz	—	0.011	UIPP
	Output Clock Period Jitter (Fractional-N)	fOUT > 100 MHz	—	230	ps p-p
		fOUT < 100 MHz	—	0.12	UIPP
	Output Clock Cycle-to-cycle Jitter (Fractional-N)	fOUT > 100 MHz	—	230	ps p-p
		fOUT < 100 MHz	—	0.12	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	–120	120	ps
t_{W}	Output Clock Pulse Width	At 90% or 10%3	0.9	—	ns
t_{LOCK}[2, 5]	PLL Lock-in Time	—	—	15	ms
t_{UNLOCK}	PLL Unlock Time	—	—	50	ns
t_{IPJIT}[6]	Input Clock Period Jitter	fPFD ??20 MHz	—	1,000	ps p-p
		fPFD < 20 MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{STABLE}[5]	STANDBY High to PLL Stable	—	—	15	ms
t_{RST}	RST/RESETM Pulse Width	—	1	—	ns
t_{RSTREC}	RST Recovery Time	—	1	—	ns
t_{RST_DIV}	RESETC/D Pulse Width	—	10	—	ns
t_{RSTREC_DIV}	RESETC/D Recovery Time	—	1	—	ns
$t_{ROTATE-SETUP}$	PHASESTEP Setup Time	—	10	—	ns
t_{ROTATE_WD}	PHASESTEP Pulse Width	—	4	—	VCO Cycles

Notes:

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after tLOCK for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See MachXO3 sysCLOCK PLL Design and Usage Guide (FPGA-TN-02058) for more details.
5. At minimum fPFD. As the fPFD increases the time will decrease to approximately 60% the value listed.

6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.
7. Edge Duty Trim Accuracy is a percentage of the setting value. Settings available are 70 ps, 140 ps, and 280 ps in addition to the default value of none.
8. Jitter values measured with the internal oscillator operating. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

3.19. NVCM/Flash Download Time

Table 3.23. NVCM/Flash Download Time

Symbol	Parameter	Device	Typ.	Units
$t_{REFRESH}$	POR to Device I/O Active	LCMXO3L/LF-640	1.9	ms
		LCMXO3L/LF-1300	1.9	ms
		LCMXO3L/LF-1300 256-Ball Package	1.4	ms
		LCMXO3L/LF-2100	1.4	ms
		LCMXO3L/LF-2100 324-Ball Package	2.4	ms
		LCMXO3L/LF-4300	2.4	ms
		LCMXO3L/LF-4300 400-Ball Package	3.8	ms
		LCMXO3L/LF-6900	3.8	ms
		LCMXO3L/LF-9400C	5.2	ms

Notes:

- Assumes sysMEM EBR initialized to an all zero pattern if they are used.
- The NVCM/Flash download time is measured starting from the maximum voltage of POR trip point.
- The worst case can be up to 1.75 times the Typ value.

3.20. JTAG Port Timing Specifications

Table 3.24. JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	20	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

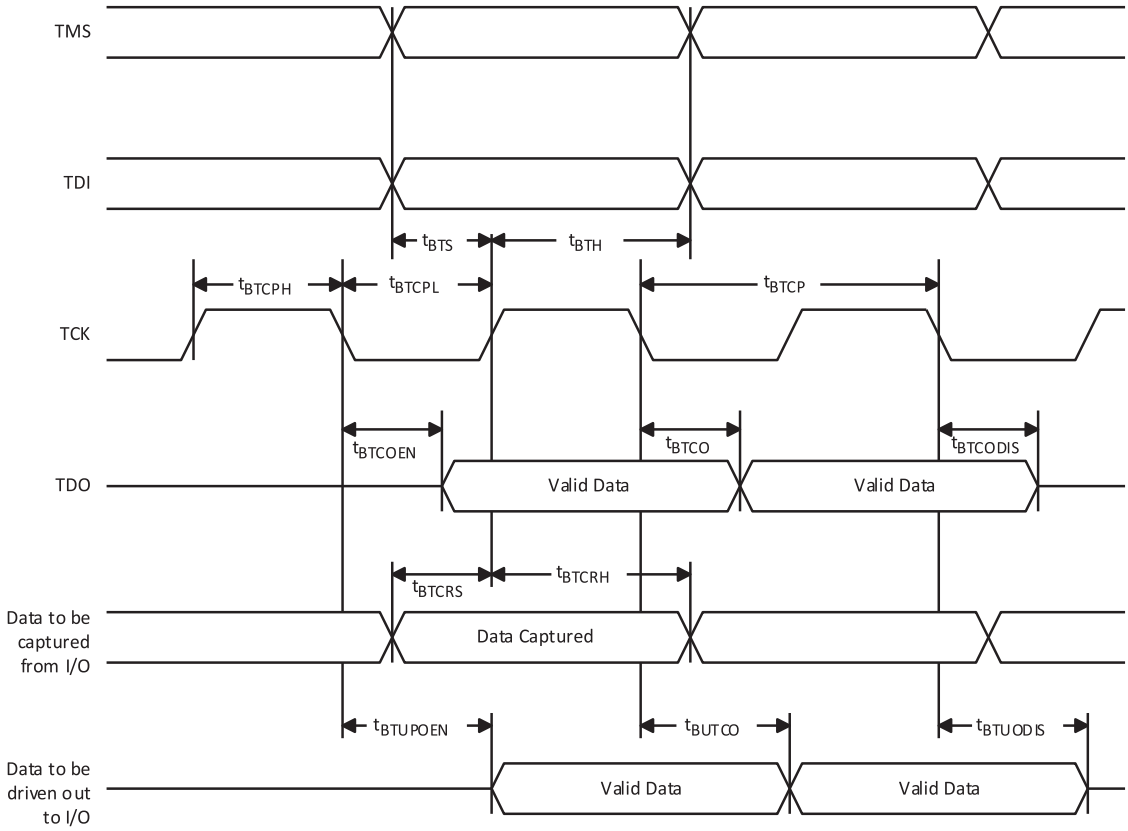


Figure 3.8. JTAG Port Timing Waveforms

3.21. sysCONFIG Port Timing Specifications

Table 3.25. sysCONFIG Port Timing Specifications

Symbol	Parameter		Min.	Max.	Units
All Configuration Modes					
t_{PRGM}	PROGRAMN low pulse accept		55	—	ns
t_{PRGMJ}	PROGRAMN low pulse rejection		—	25	ns
t_{INITL}	INITN low time	LCMXO3L/LF-640/ LCMXO3L/LF-1300	—	55	us
		LCMXO3L/LF-1300 256-Ball Package/ LCMXO3L/LF-2100	—	70	us
		LCMXO3L/LF-2100 324-Ball Package/ LCMXO3-4300	—	105	us
		LCMXO3L/LF-4300 400-Ball Package/ LCMXO3-6900	—	130	us
		LCMXO3L/LF-9400C	—	175	us
$t_{DPPINIT}$	PROGRAMN low to INITN low		—	150	ns
$t_{DPPDONE}$	PROGRAMN low to DONE low		—	150	ns
t_{IODISS}	PROGRAMN low to I/O disable		—	120	ns
Slave SPI					
f_{MAX}	CCLK clock frequency		—	66	MHz
t_{CCLKH}	CCLK clock pulse width high		7.5	—	ns
t_{CCLKL}	CCLK clock pulse width low		7.5	—	ns
t_{STSU}	CCLK setup time		2	—	ns
t_{STH}	CCLK hold time		0	—	ns
t_{STCO}	CCLK falling edge to valid output		—	10	ns
t_{STOZ}	CCLK falling edge to valid disable		—	10	ns
t_{STOV}	CCLK falling edge to valid enable		—	10	ns
t_{SCS}	Chip select high time		25	—	ns
t_{SCSS}	Chip select setup time		3	—	ns
t_{SCSH}	Chip select hold time		3	—	ns
Master SPI					
f_{MAX}	MCLK clock frequency		—	133	MHz
t_{MCLKH}	MCLK clock pulse width high		3.75	—	ns
t_{MCLKL}	MCLK clock pulse width low		3.75	—	ns
t_{STSU}	MCLK setup time		5	—	ns
t_{STH}	MCLK hold time		1	—	ns
t_{CSSPI}	INITN high to chip select low		100	200	ns
t_{MCLK}	INITN high to first MCLK edge		0.75	1	us

3.22. I²C Port Timing Specifications

Table 3.26. I²C Port Timing Specification

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	Maximum SCL clock frequency	—	400	kHz

Notes:

- MachXO3L/LF supports the following modes:
  - Standard-mode (Sm), with a bit rate up to 100 kb/s (user and configuration mode)
  - Fast-mode (Fm), with a bit rate up to 400 kb/s (user and configuration mode)
- Refer to the I²C specification for timing requirements.

3.23. SPI Port Timing Specifications

Table 3.27. SPI Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	Maximum SCK clock frequency	—	45	MHz

Note: Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

3.24. Switching Test Conditions

Figure 3.9 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3.28.

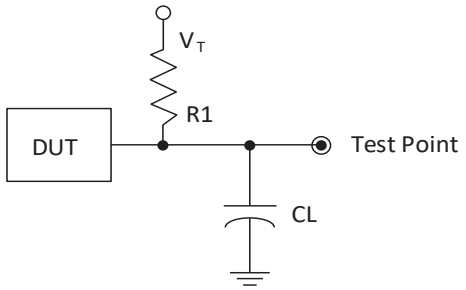


Figure 3.9. Output Test Load, LVTTL and LVCMOS Standards

Table 3.28. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R1	CL	Timing Ref.	VT
LVTTL and LVCMOS settings (L -> H, H -> L)	∞	0 pF	LVTTL, LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = VCCIO/2	—
			LVCMOS 1.8 = VCCIO/2	—
			LVCMOS 1.5 = VCCIO/2	—
			LVCMOS 1.2 = VCCIO/2	—
LVTTL and LVCMOS 3.3 (Z -> H)	188	0 pF	1.5	V_{OL}
LVTTL and LVCMOS 3.3 (Z -> L)			1.5	V_{OH}
Other LVCMOS (Z -> H)			VCCIO/2	V_{OL}
Other LVCMOS (Z -> L)			VCCIO/2	V_{OH}
LVTTL + LVCMOS (H -> Z)			VOH – 0.15	V_{OL}
LVTTL + LVCMOS (L -> Z)			VOL – 0.15	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

4. Signal Descriptions

Table 4.1. Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
P[Edge] [Row/Column Number]_[A/B/C/D]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B/C/D] indicates the PIO within the group to which the pad is connected. Some of these user-programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/Os for user logic. During configuration of the user-programmable I/Os, the user has an option to tri-state the I/Os and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/Os to be tri-stated with an internal pull-down resistor enabled. When the device is erased, I/Os will be tri-stated with an internal pull-down resistor enabled. Some pins, such as PROGRAMN and JTAG pins, default to tri-stated I/Os with pull-up resistors enabled when the device is erased.
NC	—	No connect.
GND	—	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together.
V_{CC}	—	V_{CC} – The power supply pins for core logic. Dedicated pins. It is recommended that all V_{CC}s are tied to the same supply.
V_{CCIO}x	—	V_{CCIO} – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all V_{CCIO}s located in the same bank are tied to the same supply.
PLL and Clock Functions (Used as user-programmable I/O pins when not used for PLL or clock pins)		
[LOC]_GPLL[T, C]_IN	—	Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
[LOC]_GPLL[T, C]_FB	—	Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
PCLK [n]_[2:0]	—	Primary Clock pads. One to three clock pads per side.
Test and Programming (Dual function pins used for test access port and during sysCONFIG™)		
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.
TDO	O	Output pin – Test Data output pin used to shift data out of the device using 1149.1.
JTAGENB	I	Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then: If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O. If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins. For more details, refer to MachXO3 Programming and Configuration Usage Guide (FPGA-TN-02055).
Configuration (Dual function pins used during sysCONFIG)		
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress.
MCLK/CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes.
SN	I	Slave SPI active low chip select input.
CSSPIN	I/O	Master SPI active low chip select output.
SI/SPISI	I/O	Slave SPI serial data input and master SPI serial data output.

Signal Name	I/O	Descriptions
SO/SPISO	I/O	Slave SPI serial data output and master SPI serial data input.
SCL	I/O	Slave I^2C clock input and master I^2C clock output.
SDA	I/O	Slave I^2C data input and master I^2C data output.

4.1. Pin Information Summary

Table 4.2. MachXO3L/LF-640 and MachXO3L/LF-1300 Pin Summary

	MachXO3L/ LF-640	MachXO3L/LF-1300			
	CSFBGA121	WLCSP36	CSFBGA121	CSFBGA256	CABGA256
General Purpose I/O per Bank					
Bank 0	25	16	25	51	51
Bank 1	26	0	26	52	52
Bank 2	26	9	26	52	52
Bank 3	24	4	24	16	16
Bank 4	0	0	0	16	16
Bank 5	0	0	0	20	20
Total General Purpose Single Ended I/O	101	29	101	207	207
Minimum Reserved for Configuration*	1	1	1	1	1
Maximum Programmable Single Ended I/O	100	28	100	206	206
Differential I/O per Bank					
Bank 0	12	8	12	25	25
Bank 1	13	0	13	26	26
Bank 2	13	4	13	26	26
Bank 3	11	2	11	8	8
Bank 4	0	0	0	8	8
Bank 5	0	0	0	10	10
Total General Purpose Differential I/O	49	14	49	103	103
Dual Function I/O	33	25	33	33	33
Number 7:1 or 8:1 Gearboxes					
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	7	3	7	14	14
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	7	2	7	14	14
High-speed Differential Outputs					
Bank 0	7	3	7	14	14
VCCIO Pins					
Bank 0	1	1	1	4	4
Bank 1	1	0	1	3	4
Bank 2	1	1	1	4	4
Bank 3	3	1	3	2	1
Bank 4	0	0	0	2	2
Bank 5	0	0	0	2	1
VCC	4	2	4	8	8
GND	10	2	10	24	24
NC	0	0	0	0	1
Total Count of Bonded Pins	**121**	**36**	**121**	**256**	**256**

***Note:** One pin for JTAGENB or four pins for JTAG.

Table 4.3. MachXO3L/LF-2100 Pin Summary

	MachXO3L/LF-2100					
	WLCSP49	**CSFBGA121**	**CSFBGA256**	**CSFBGA324**	**CABGA256**	**CABGA324**
General Purpose I/O per Bank						
Bank 0	20	25	51	72	51	72
Bank 1	0	26	52	62	52	68
Bank 2	13	26	52	72	52	72
Bank 3	0	7	16	22	16	24
Bank 4	0	7	16	14	16	16
Bank 5	6	10	20	27	20	28
Total General Purpose Single Ended I/O	39	101	207	269	207	280
Minimum Reserved for Configuration*	1	1	1	1	1	1
Maximum Programmable Single Ended I/O	38	100	206	268	206	279
Differential I/O per Bank						
Bank 0	10	12	25	36	25	36
Bank 1	0	13	26	30	26	34
Bank 2	6	13	26	36	26	36
Bank 3	0	3	8	10	8	12
Bank 4	0	3	8	6	8	8
Bank 5	3	5	10	13	10	14
Total General Purpose Differential I/O	19	49	103	131	103	140
Dual Function I/O	25	33	33	37	33	37
Number 7:1 or 8:1 Gearboxes						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	7	14	18	14	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	13	14	18	14	18
High-speed Differential Outputs						
Bank 0	5	7	14	18	14	18
VCCIO Pins						
Bank 0	2	1	4	4	4	4
Bank 1	0	1	3	4	4	4
Bank 2	1	1	4	4	4	4
Bank 3	0	1	2	2	1	2
Bank 4	0	1	2	2	2	2
Bank 5	1	1	2	2	1	2
VCC	2	4	8	8	8	10
GND	4	10	24	16	24	16
NC	0	0	0	13	1	0
Total Count of Bonded Pins	**49**	**121**	**256**	**324**	**256**	**324**

***Note:** One pin for JTAGENB or four pins for JTAG.

Table 4.4. MachXO3L/LF-4300 Pin Summary

	MachXO3L/LF-4300						
	WLCSP81	**CSFBGA121**	**CSFBGA256**	**CSFBGA324**	**CABGA256**	**CABGA324**	**CABGA400**
General Purpose I/O per Bank							
Bank 0	30	25	51	72	51	72	84
Bank 1	0	26	52	62	52	68	84
Bank 2	20	26	52	72	52	72	84
Bank 3	7	7	16	22	16	24	28
Bank 4	0	7	16	14	16	16	24
Bank 5	7	10	20	27	20	28	32
Total General Purpose Single Ended I/O	64	101	207	269	207	280	336
Minimum Reserved for Configuration*	1	1	1	1	1	1	1
Maximum Programmable Single Ended I/O	63	100	206	268	206	279	335
Differential I/O per Bank							
Bank 0	15	12	25	36	25	36	42
Bank 1	0	13	26	30	26	34	42
Bank 2	10	13	26	36	26	36	42
Bank 3	3	3	8	10	8	12	14
Bank 4	0	3	8	6	8	8	12
Bank 5	3	5	10	13	10	14	16
Total General Purpose Differential I/O	31	49	103	131	103	140	168
Dual Function I/O	25	37	37	37	37	37	37
Number 7:1 or 8:1 Gearboxes							
Number of 7:1 or 8:1 Output Gearboxes Available (Bank 0)	10	7	18	18	18	18	21
Number of 7:1 or 8:1 Input Gearboxes Available (Bank 2)	10	13	18	18	18	18	21
High-speed Differential Outputs							
Bank 0	10	7	18	18	18	18	21
VCCIO Pins							
Bank 0	3	1	4	4	4	4	5
Bank 1	0	1	3	4	4	4	5
Bank 2	2	1	4	4	4	4	5
Bank 3	1	1	2	2	1	2	2
Bank 4	0	1	2	2	2	2	2
Bank 5	1	1	2	2	1	2	2
VCC	4	4	8	8	8	10	10
GND	6	10	24	16	24	16	33
NC	0	0	0	13	1	0	0
Total Count of Bonded Pins	**81**	**121**	**256**	**324**	**256**	**324**	**400**

***Note:** One pin for JTAGENB or four pins for JTAG.

Table 4.5. MachXO3L/LF-6900 Pin Summary

	MachXO3L/LF-6900				
	CSFBGA256	**CSFBGA324**	**CABGA256**	**CABGA324**	**CABGA400**
General Purpose I/O per Bank					
Bank 0	51	74	51	72	84
Bank 1	52	68	52	68	84
Bank 2	52	72	52	72	84
Bank 3	16	24	16	24	28
Bank 4	16	16	16	16	24
Bank 5	20	28	20	28	32
Total General Purpose Single Ended I/O	207	282	207	280	336
Minimum Reserved for Configuration*	1	1	1	1	1
Maximum Programmable Single Ended I/O	206	281	206	279	335
Differential I/O per Bank					
Bank 0	25	36	25	36	42
Bank 1	26	34	26	34	42
Bank 2	26	36	26	36	42
Bank 3	8	12	8	12	14
Bank 4	8	8	8	8	12
Bank 5	10	14	10	14	16
Total General Purpose Differential I/O	103	140	103	140	168
Dual Function I/O	37	37	37	37	37
Number 7:1 or 8:1 Gearboxes					
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	20	21	20	21	21
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	20	21	20	21	21
High-speed Differential Outputs					
Bank 0	20	21	20	21	21
VCCIO Pins					
Bank 0	4	4	4	4	5
Bank 1	3	4	4	4	5
Bank 2	4	4	4	4	5
Bank 3	2	2	1	2	2
Bank 4	2	2	2	2	2
Bank 5	2	2	1	2	2
VCC	8	8	8	10	10
GND	24	16	24	16	33
NC	0	0	1	0	0
Total Count of Bonded Pins	**256**	**324**	**256**	**324**	**400**

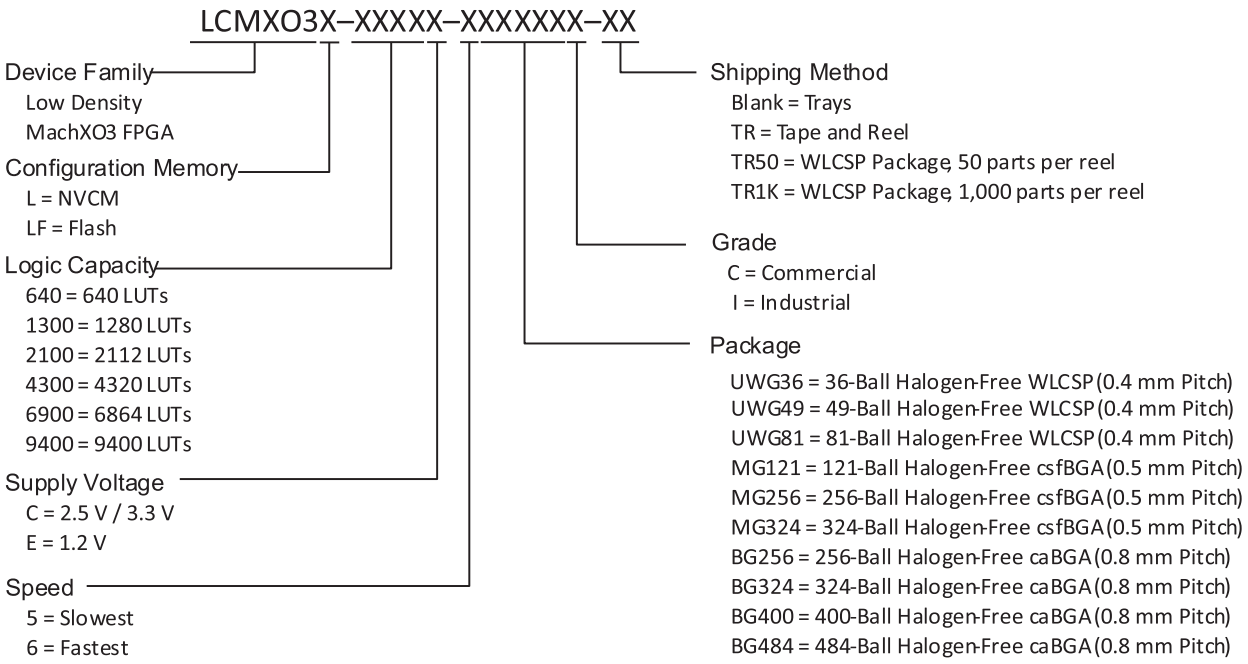
***Note:** One pin for JTAGENB or four pins for JTAG.

Table 4.6. MachXO3L/LF-9400C Pin Summary

	MachXO3L/LF-9400C			
	CSFBGA256	**CABGA256**	**CABGA400**	**CABGA484**
General Purpose I/O per Bank				
Bank 0	51	51	84	96
Bank 1	52	52	84	96
Bank 2	52	52	84	96
Bank 3	16	16	28	36
Bank 4	16	16	24	24
Bank 5	20	20	32	36
Total General Purpose Single Ended I/O	207	207	336	384
Minimum Reserved for Configuration*	1	1	1	1
Maximum Programmable Single Ended I/O	206	206	335	383
Differential I/O per Bank				
Bank 0	25	25	42	48
Bank 1	26	26	42	48
Bank 2	26	26	42	48
Bank 3	8	8	14	18
Bank 4	8	8	12	12
Bank 5	10	10	16	18
Total General Purpose Differential I/O	103	103	168	192
Dual Function I/O	37	37	37	45
Number 7:1 or 8:1 Gearboxes				
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	20	20	22	24
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	20	20	22	24
High-speed Differential Outputs				
Bank 0	20	20	21	24
VCCIO Pins				
Bank 0	4	4	5	9
Bank 1	3	4	5	9
Bank 2	4	4	5	9
Bank 3	2	1	2	3
Bank 4	2	2	2	3
Bank 5	2	1	2	3
VCC	8	8	10	12
GND	24	24	33	52
NC	0	1	0	0
Total Count of Bonded Pins	**256**	**256**	**400**	**484**

***Note:** One pin for JTAGENB or four pins for JTAG.

5. MachXO3 Part Number Description



6. Ordering Information

MachXO3L/LF devices have top-side markings as shown in the examples below, on the 256-Ball caBGA package with MachXO3-6900 device in Commercial Temperature in Speed Grade 5. Notice that for the MachXO3LF device, *LMXO3LF* is used instead of *LCMXO3LF* as in the Part Number.

Note: LCMXO3LF is marked with LMXO3LF

Note: Markings are abbreviated for small packages. MachXO3L WLSC packages (UWG) are dual speed grade marked *5C-5I*.

6.1. MachXO3L Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-640E-5MG121C	640	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3L-640E-6MG121C	640	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3L-640E-5MG121I	640	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3L-640E-6MG121I	640	1.2 V	6	Halogen-Free csfBGA	121	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-1300E-5UWG36CTR	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3L-1300E-5UWG36CTR50	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3L-1300E-5UWG36CTR1K	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3L-1300E-5UWG36ITR	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3L-1300E-5UWG36ITR50	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3L-1300E-5UWG36ITR1K	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3L-1300E-5MG121C	1300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3L-1300E-6MG121C	1300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3L-1300E-5MG121I	1300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3L-1300E-6MG121I	1300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3L-1300E-5MG256C	1300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-1300E-6MG256C	1300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-1300E-5MG256I	1300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-1300E-6MG256I	1300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-1300C-5BG256C	1300	2.5 V/3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-1300C-6BG256C	1300	2.5 V/3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-1300C-5BG256I	1300	2.5 V/3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-1300C-6BG256I	1300	2.5 V/3.3 V	6	Halogen-Free caBGA	256	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-2100E-5UWG49CTR	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3L-2100E-5UWG49CTR50	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3L-2100E-5UWG49CTR1K	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3L-2100E-5UWG49ITR	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3L-2100E-5UWG49ITR50	2100	1.2 V	5	Halogen-Free WLCSP	49	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-2100E-5UWG49ITR1K	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3L-2100E-5MG121C	2100	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3L-2100E-6MG121C	2100	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3L-2100E-5MG121I	2100	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3L-2100E-6MG121I	2100	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3L-2100E-5MG256C	2100	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-2100E-6MG256C	2100	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-2100E-5MG256I	2100	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-2100E-6MG256I	2100	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-2100E-5MG324C	2100	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3L-2100E-6MG324C	2100	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3L-2100E-5MG324I	2100	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3L-2100E-6MG324I	2100	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-2100C-5BG256C	2100	2.5 V/3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-2100C-6BG256C	2100	2.5 V/3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-2100C-5BG256I	2100	2.5 V/3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-2100C-6BG256I	2100	2.5 V/3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-2100C-5BG324C	2100	2.5 V/3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-2100C-6BG324C	2100	2.5 V/3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-2100C-5BG324I	2100	2.5 V/3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3L-2100C-6BG324I	2100	2.5 V/3.3 V	6	Halogen-Free caBGA	324	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-4300E-5UWG81CTR	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81CTR50	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81CTR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81ITR	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5UWG81ITR50	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5UWG81ITR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5MG121C	4300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3L-4300E-6MG121C	4300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3L-4300E-5MG121I	4300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3L-4300E-6MG121I	4300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3L-4300E-5MG256C	4300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-4300E-6MG256C	4300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-4300E-5MG256I	4300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-4300E-6MG256I	4300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-4300E-5MG324C	4300	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3L-4300E-6MG324C	4300	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3L-4300E-5MG324I	4300	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3L-4300E-6MG324I	4300	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-4300C-5BG256C	4300	2.5 V/3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-4300C-6BG256C	4300	2.5 V/3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-4300C-5BG256I	4300	2.5 V/3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-4300C-6BG256I	4300	2.5 V/3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-4300C-5BG324C	4300	2.5 V/3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-4300C-6BG324C	4300	2.5 V/3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-4300C-5BG324I	4300	2.5 V/3.3 V	5	Halogen-Free caBGA	324	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-4300C-6BG324I	4300	2.5 V/3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3L-4300C-5BG400C	4300	2.5 V/3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-4300C-6BG400C	4300	2.5 V/3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-4300C-5BG400I	4300	2.5 V/3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-4300C-6BG400I	4300	2.5 V/3.3 V	6	Halogen-Free caBGA	400	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-6900E-5MG256C	6900	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-6900E-6MG256C	6900	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-6900E-5MG256I	6900	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-6900E-6MG256I	6900	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-6900E-5MG324C	6900	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3L-6900E-6MG324C	6900	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3L-6900E-5MG324I	6900	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3L-6900E-6MG324I	6900	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-6900C-5BG256C	6900	2.5 V/3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-6900C-6BG256C	6900	2.5 V/3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-6900C-5BG256I	6900	2.5 V/3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-6900C-6BG256I	6900	2.5 V/3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-6900C-5BG324C	6900	2.5 V/3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-6900C-6BG324C	6900	2.5 V/3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-6900C-5BG324I	6900	2.5 V/3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3L-6900C-6BG324I	6900	2.5 V/3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3L-6900C-5BG400C	6900	2.5 V/3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-6900C-6BG400C	6900	2.5 V/3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-6900C-5BG400I	6900	2.5 V/3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-6900C-6BG400I	6900	2.5 V/3.3 V	6	Halogen-Free caBGA	400	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-9400E-5MG256C	9400	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-9400E-6MG256C	9400	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-9400E-5MG256I	9400	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-9400E-6MG256I	9400	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-9400E-5BG256C	9400	1.2 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-9400E-6BG256C	9400	1.2 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-9400E-5BG256I	9400	1.2 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-9400E-6BG256I	9400	1.2 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-9400E-5BG400C	9400	1.2 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-9400E-6BG400C	9400	1.2 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-9400E-5BG400I	9400	1.2 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-9400E-6BG400I	9400	1.2 V	6	Halogen-Free caBGA	400	IND
LCMXO3L-9400E-5BG484C	9400	1.2 V	5	Halogen-Free caBGA	484	COM
LCMXO3L-9400E-6BG484C	9400	1.2 V	6	Halogen-Free caBGA	484	COM
LCMXO3L-9400E-5BG484I	9400	1.2 V	5	Halogen-Free caBGA	484	IND
LCMXO3L-9400E-6BG484I	9400	1.2 V	6	Halogen-Free caBGA	484	IND
LCMXO3L-9400C-5BG256C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-9400C-6BG256C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-9400C-5BG256I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-9400C-6BG256I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-9400C-5BG400C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-9400C-6BG400C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-9400C-5BG400I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-9400C-6BG400I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	IND
LCMXO3L-9400C-5BG484C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	COM
LCMXO3L-9400C-6BG484C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	484	COM
LCMXO3L-9400C-5BG484I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	IND
LCMXO3L-9400C-6BG484I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	484	IND

6.2. MachXO3LF Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-640E-5MG121C	640	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3LF-640E-6MG121C	640	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3LF-640E-5MG121I	640	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3LF-640E-6MG121I	640	1.2 V	6	Halogen-Free csfBGA	121	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-1300E-5UWG36CTR	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3LF-1300E-5UWG36CTR50	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3LF-1300E-5UWG36CTR1K	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3LF-1300E-5UWG36ITR	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3LF-1300E-5UWG36ITR50	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3LF-1300E-5UWG36ITR1K	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3LF-1300E-5MG121C	1300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3LF-1300E-6MG121C	1300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3LF-1300E-5MG121I	1300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3LF-1300E-6MG121I	1300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3LF-1300E-5MG256C	1300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-1300E-6MG256C	1300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-1300E-5MG256I	1300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-1300E-6MG256I	1300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-1300C-5BG256C	1300	2.5 V/3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-1300C-6BG256C	1300	2.5 V/3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-1300C-5BG256I	1300	2.5 V/3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-1300C-6BG256I	1300	2.5 V/3.3 V	6	Halogen-Free caBGA	256	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-2100E-5UWG49CTR	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3LF-2100E-5UWG49CTR50	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3LF-2100E-5UWG49CTR1K	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3LF-2100E-5UWG49ITR	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3LF-2100E-5UWG49ITR50	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3LF-2100E-5UWG49ITR1K	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3LF-2100E-5MG121C	2100	1.2 V	5	Halogen-Free csfBGA	121	COM

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-2100E-6MG121C	2100	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3LF-2100E-5MG121I	2100	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3LF-2100E-6MG121I	2100	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3LF-2100E-5MG256C	2100	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-2100E-6MG256C	2100	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-2100E-5MG256I	2100	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-2100E-6MG256I	2100	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-2100E-5MG324C	2100	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3LF-2100E-6MG324C	2100	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3LF-2100E-5MG324I	2100	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3LF-2100E-6MG324I	2100	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3LF-2100C-5BG256C	2100	2.5 V/3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-2100C-6BG256C	2100	2.5 V/3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-2100C-5BG256I	2100	2.5 V/3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-2100C-6BG256I	2100	2.5 V/3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-2100C-5BG324C	2100	2.5 V/3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3LF-2100C-6BG324C	2100	2.5 V/3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3LF-2100C-5BG324I	2100	2.5 V/3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3LF-2100C-6BG324I	2100	2.5 V/3.3 V	6	Halogen-Free caBGA	324	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-4300E-5UWG81CTR	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3LF-4300E-5UWG81CTR50	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3LF-4300E-5UWG81CTR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3LF-4300E-5UWG81ITR	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3LF-4300E-5UWG81ITR50	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3LF-4300E-5UWG81ITR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3LF-4300E-5MG121C	4300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3LF-4300E-6MG121C	4300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3LF-4300E-5MG121I	4300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3LF-4300E-6MG121I	4300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3LF-4300E-5MG256C	4300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-4300E-6MG256C	4300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-4300E-5MG256I	4300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-4300E-6MG256I	4300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-4300E-5MG324C	4300	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3LF-4300E-6MG324C	4300	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3LF-4300E-5MG324I	4300	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3LF-4300E-6MG324I	4300	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3LF-4300C-5BG256C	4300	2.5 V/3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-4300C-6BG256C	4300	2.5 V/3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-4300C-5BG256I	4300	2.5 V/3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-4300C-6BG256I	4300	2.5 V/3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-4300C-5BG324C	4300	2.5 V/3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3LF-4300C-6BG324C	4300	2.5 V/3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3LF-4300C-5BG324I	4300	2.5 V/3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3LF-4300C-6BG324I	4300	2.5 V/3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3LF-4300C-5BG400C	4300	2.5 V/3.3 V	5	Halogen-Free caBGA	400	COM

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-4300C-6BG400C	4300	2.5 V/3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3LF-4300C-5BG400I	4300	2.5 V/3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3LF-4300C-6BG400I	4300	2.5 V/3.3 V	6	Halogen-Free caBGA	400	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-6900E-5MG256C	6900	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-6900E-6MG256C	6900	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-6900E-5MG256I	6900	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-6900E-6MG256I	6900	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-6900E-5MG324C	6900	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3LF-6900E-6MG324C	6900	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3LF-6900E-5MG324I	6900	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3LF-6900E-6MG324I	6900	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3LF-6900C-5BG256C	6900	2.5 V/3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-6900C-6BG256C	6900	2.5 V/3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-6900C-5BG256I	6900	2.5 V/3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-6900C-6BG256I	6900	2.5 V/3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-6900C-5BG324C	6900	2.5 V/3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3LF-6900C-6BG324C	6900	2.5 V/3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3LF-6900C-5BG324I	6900	2.5 V/3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3LF-6900C-6BG324I	6900	2.5 V/3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3LF-6900C-5BG400C	6900	2.5 V/3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3LF-6900C-6BG400C	6900	2.5 V/3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3LF-6900C-5BG400I	6900	2.5 V/3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3LF-6900C-6BG400I	6900	2.5 V/3.3 V	6	Halogen-Free caBGA	400	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-9400E-5MG256C	9400	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-9400E-6MG256C	9400	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-9400E-5MG256I	9400	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-9400E-6MG256I	9400	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-9400E-5BG256C	9400	1.2 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-9400E-6BG256C	9400	1.2 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-9400E-5BG256I	9400	1.2 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-9400E-6BG256I	9400	1.2 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-9400E-5BG400C	9400	1.2 V	5	Halogen-Free caBGA	400	COM
LCMXO3LF-9400E-6BG400C	9400	1.2 V	6	Halogen-Free caBGA	400	COM
LCMXO3LF-9400E-5BG400I	9400	1.2 V	5	Halogen-Free caBGA	400	IND
LCMXO3LF-9400E-6BG400I	9400	1.2 V	6	Halogen-Free caBGA	400	IND
LCMXO3LF-9400E-5BG484C	9400	1.2 V	5	Halogen-Free caBGA	484	COM
LCMXO3LF-9400E-6BG484C	9400	1.2 V	6	Halogen-Free caBGA	484	COM
LCMXO3LF-9400E-5BG484I	9400	1.2 V	5	Halogen-Free caBGA	484	IND
LCMXO3LF-9400E-6BG484I	9400	1.2 V	6	Halogen-Free caBGA	484	IND
LCMXO3LF-9400C-5BG256C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-9400C-6BG256C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-9400C-5BG256I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-9400C-6BG256I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-9400C-5BG400C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	COM

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-9400C-6BG400C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3LF-9400C-5BG400I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3LF-9400C-6BG400I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	IND
LCMXO3LF-9400C-5BG484C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	COM
LCMXO3LF-9400C-6BG484C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	484	COM
LCMXO3LF-9400C-5BG484I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	IND
LCMXO3LF-9400C-6BG484I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	484	IND

References

A variety of technical notes for the MachXO3 family are available on the Lattice web site.

- MachXO3 sysCLOCK PLL Design and Usage Guide (FPGA-TN-02058)
- Implementing High-Speed Interfaces with MachXO3 Devices (FPGA-TN-02057)
- MachXO3 sysI/O Usage Guide (FPGA-TN-02047)
- MachXO3 Programming and Configuration Usage Guide (FPGA-TN-02055)
- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- Minimizing System Interruption During Configuration Using TransFR Technology (FPGA-TN-02025)
- Boundary Scan Testability with Lattice sysI/O Capability (AN8066)
- MachXO3 Device Pinout File
- Thermal Management (FPGA-TN-02044)
- Lattice Design Tools

Revision History

Revision 2.5, March 2020

Section	Change Summary
Disclaimers	Added this section.
Architecture	• Added the MachXO3LF to MachXO3L Low Cost Migration Path section. • Removed last paragraph from the Typical I/O Behavior during Power-up section.
DC and Switching Characteristics	• Added NVCM Programming cycles and Flash Feature Row Programming Cycles to Table 3.6. • Added clarification to "Blank Pattern" in footnote to Table 3.9. • Added footnote to clarify VCCIO in Table 3.12.
Signal Descriptions	• Added rows and footnote to clarify configuration usage in Table 4.1 thru Table 4.6. • Added "Pin Summary" to table captions for clarity.

Revision 2.4, February 2019

Section	Change Summary
Architecture	Updated Figure 2.12. Output Register Block Diagram (PIO on the Left, Top and Bottom Edges) caption.

Revision 2.3, November 2018

Section	Change Summary
Architecture	Clarified PCI support in the following sections and tables: • Programmable I/O Cells (PIC)Programmable I/O Cells (PIC) • sysI/O Buffer • Table 2.11. Supported Input Standards • Table 2.12. Supported Output Standards
References	Updated PCB Layout Recommendations for BGA Packages document number to FPGA-TN-02024.

Revision 2.2, October 2018

Section	Change Summary
Introduction	• Added Device Options to Table 1.1. MachXO3L/LF Family Selection Guide. • Updated footnotes.
Architecture	General update to Table 2.11. Supported Input Standards
Ordering Information	• Corrected BG256 packages for 1300 LUT parts. • Added information on dual marking for MachXO3L WLCS packages.
All	Minor formatting changes.

Revision 2.1, March 2018

Section	Change Summary
DC and Switching Characteristics	Removed extraneous T_{JAUTO} specification from Table 3.2 Recommended Operating Conditions.
Ordering Information	Restored MachXO3LF Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section back to the Ordering Information section.
Revision History	Restored Revision History contents for Revision 1.6 and prior back to this Revision History section.

Revision 2.0, January 2018

Section	Change Summary
All	• Applied new company template. • Changed document number fron DS1047 to FPGA-DS-02032. • Fixed various reference links.
DC and Switching Characteristics	• Added Programming/Erase Specifications section. Clarified Write/Erase cycle. • Removed unnecessary C2 Dedicated Input Capacitance specification from the DC Electrical Characteristics section. • Added note to the NVCM/Flash Download Time section to clarify maximum $t_{REFRESH}$ time.

Revision 1.9, October 2017

Section	Change Summary
Introduction	• Updated Features section. Changed Advanced Packaging feature to “0.5 mm pitch: 640 to 9.4K LUT densities....” • Updated Table 1.1, MachXO3L Family Selection Guide. • Added footnotes to MachXO3L-6900/MachXO3LF-6900 and MachXO3L-9400/MachXO3LF-9400 LUTs. • Added UFM (kbits, MachXO3LF only) feature. • Moved footnotes from packages to corresponding I/O values in 256- ball caBGA, 400-ball caBGA and 484-ball caBGA. • Updated footnote 2. • Added footnotes 3 and 4.
Architecture	• Updated User Flash Memory (UFM) section. Changed feature to “Non-volatile storage up to 448 kbits”. • Updated Standby Mode and Power Saving Options section. Updated the title of TN1289 reference.
DC and Switching Characteristics	• Updated Absolute Maximum Ratings section. Added footnote 6. • Updated Static Supply Current – C/E Devices section. • Updated the title of TN1289 reference in footnote 1. • Removed footnote 7. Updated Programming and Erase Supply Current – C/E Devices section. Updated the title of TN1289 reference in footnote 1
Ordering Information	• Updated the MachXO3L Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added MachXO3L-9600E part numbers. • Updated the MachXO3LF Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added MachXO3LF-9600E part numbers.

Revision 1.8, February 2017

Section	Change Summary
Architecture	• Updated Supported Standards section. • Corrected “MDVS” to “MLDVS” in Table 2.11, Supported Input Standards.
DC and Switching Characteristics	• Updated ESD Performance section. Added reference to the MachXO2 Product Family Qualification Summary document. • Updated Static Supply Current – C/E Devices section. Added footnote 7. • Updated MachXO3L/LF External Switching Characteristics – C/E Devices section. • Populated values for MachXO3L/LF-9400. • Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, corrected “tDVB” to “tDIB” and “tDVA” to “tDIA” and revised their descriptions. • Added Figure 3-6, Receiver GDDR71_RX Waveforms and Figure 3-7, Transmitter GDDR71_TX Waveforms.
Pinout Information	• Updated the Pin Information Summary section. Added MachXO3L/LF- 9600C packages.

Revision 1.7, May 2016

Section	Change Summary
DC and Switching Characteristics	• Updated Absolute Maximum Ratings section. Modified I/O Tri-state Voltage Applied and Dedicated Input Voltage Applied footnotes. • Updated sysI/O Recommended Operating Conditions section. • Added standards. • Added VREF (V) • Added footnote 4. • Updated sysI/O Single-Ended DC Electrical Characteristics section. • Added I/O standards.
Ordering Information	• Updated MachXO3L Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L- 9400C part numbers. • Updated MachXO3LF Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L- 9400C part numbers.

Revision 1.6, April 2016

Section	Change Summary
Introduction	• Updated Features section. • Revised logic density range and I/O to LUT ratio under Flexible Architecture. • Revised 0.8 mm pitch information under Advanced Packaging. • Added MachXO3L-9400/MachXO3LF-9400 information to Table 1-1, MachXO3L/LF Family Selection Guide. • Updated Introduction section. • Changed density from 6900 to 9400 LUTs. • Changed caBGA packaging to 19 x 19 mm.
Architecture	• Updated Architecture Overview section. • Changed statement to “All logic density devices in this family...” • Updated Figure 2-2 heading and notes. • Updated sysCLOCK Phase Locked Loops (PLLs) section. • Changed statement to “All MachXO3L/LF devices have one or more sysCLOCK PLL.” • Updated Programmable I/O Cells (PIC) section. • Changed statement to “All PIO pairs can implement differential receivers.” • Updated sysI/O Buffer Banks section. Updated Figure 2-5 heading. • Updated Device Configuration section. Added Password and Soft Error Correction.
DC and Switching Characteristics	• Updated Static Supply Current – C/E Devices section. Added LCMXO3L/LF-9400C and LCMXO3L/LF-9400E devices. • Updated Programming and Erase Supply Current – C/E Devices section. • Added LCMXO3L/LF-9400C and LCMXO3L/LF-9400E devices. • Changed LCMXO3L/LF-640E and LCMXO3L/LF-1300E Typ. values. • Updated MachXO3L/LF External Switching Characteristics – C/E Devices section. Added MachXO3L/LF-9400 devices. • Updated NVCM/Flash Download Time section. Added LCMXO3L/LF-9400C device. • Updated sysCONFIG Port Timing Specifications section. • Added LCMXO3L/LF-9400C device. • Changed tINITL units to from ns to us. • Changed tDPPINIT and tDPPDONE Max. values are per PCN#03A-16.
Pinout Information	Updated Pin Information Summary section. Added LCMXO3L/LF-9400C device.

Section	Change Summary
Ordering Information	• Updated MachXO3 Part Number Description section. • Added 9400 = 9400 LUTs. • Added BG484 package. • Updated MachXO3L Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers. • Updated MachXO3LF Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.

Revision 1.5, September 2015

Section	Change Summary
DC and Switching Characteristics	• Updated the MIPI D-PHY Emulation section. Revised Table 3-5, MIPI DPHY Output DC Conditions. • Revised RL Typ. value. • Revised RH description and values. • Updated the Maximum sysI/O Buffer Performance section. Revised MIPI Max. Speed value. • Updated the MachXO3L/LF External Switching Characteristics – C/E Devices section. Added footnotes 14 and 15.

Revision 1.4, August 2015

Section	Change Summary
Architecture	Updated the Device Configuration section. Added JTAGENB to TAP dual purpose pins.
Ordering Information	Updated the top side markings section to indicate the use of LMXO3LF for the LCMXO3LF device.

Revision 1.3, March 2015

Section	Change Summary
All	General update. Added MachXO3LF devices.

Revision 1.2, August 2015

Section	Change Summary
Introduction	Updated Table 1-1, MachXO3L Family Selection Guide. Revised XO3L-2100 and XO3L-4300 I/O for 324-ball csfBGA package.
Architecture	Updated the Dual Boot section. Corrected information on where the primary bitstream and the golden image must reside.
DC and Switching Characteristics	• Updated the BLVDS section. Changed output impedance nominal values in Table 3-2, BLVDS DC Condition. • Updated the LVPECL section. Changed output impedance nominal value in Table 3-3, LVPECL DC Condition. • Updated the sysCONFIG Port Timing Specifications section. Updated INITN low time values.
Pinout Information	• Changed General Purpose I/O Bank 5 values for MachXO3L-2100 and MachXO3L-4300 CSFBGA 324 package. • Changed Number 7:1 or 8:1 Gearboxes for MachXO3L-640 and MachXO3L-1300. • Removed DQS Groups (Bank 1) section. • Changed VCCIO Pins Bank 1 values for MachXO3L-1300, MachXO3L-2100, MachXO3L-4300 and MachXO3L-6900 CSFBGA 256 package. • Changed GND values for MachXO3L-1300, MachXO3L-2100, MachXO3L-4300 and MachXO3L-6900 CSFBGA 256 package. • Changed NC values for MachXO3L-2100 and MachXO3L-4300 CSFBGA 324 package.

Revision 1.1, July 2014

Section	Change Summary
DC and Switching Characteristics	• Updated the Static Supply Current – C/E Devices section. Added devices. • Updated the Programming and Erase Supply Current – C/E Device section. Added devices. • Updated the sysI/O Single-Ended DC Electrical Characteristics section. Revised footnote 4. • Added the NVCM Download Time section. • Updated the Typical Building Block Function Performance – C/E Devices section. Added information to footnote.
Pinout Information	Updated the Pin Information Summary section.
Ordering Information	• Updated the MachXO3L Part Number Description section. Added packages. • Updated the Ordering Information section. General update.

Revision 1.0, June 2014

Section	Change Summary
Introduction	• Updated Features section. • Updated Table 1-1, MachXO3L Family Selection Guide. Changed fcCSP packages to csfBGA. Adjusted 121-ball csfBGA arrow. • Introduction section general update.
Architecture	General update.
DC and Switching Characteristics	• Updated sysI/O Recommended Operating Conditions section. Removed VREF (V) column. Added standards. • Updated Maximum sysI/O Buffer Performance section. Added MIPI I/O standard. • Updated MIPI D-PHY Emulation section. Changed Low Speed to Low Power. Updated Table 3-4, MIPI DC Conditions. • Updated Table 3-5, MIPI D-PHY Output DC Conditions. • Updated Maximum sysI/O Buffer Performance section. • Updated MachXO3L External Switching Characteristics – C/E Device section.

Revision 00.3, May 2014

Section	Change Summary
Introduction	• Updated Features section. • Updated Table 1-1, MachXO3L Family Selection Guide. Moved 121-ball fcCSP arrow. • General update of Introduction section.
Architecture	General update.
Pinout Information	Updated Pin Information Summary section. Updated or added data on WLCSP49, WLCSP81, CABGA324, and CABGA400 for specific devices.
Ordering Information	• Updated MachXO3L Part Number Description section. Updated or added data on WLCSP49, WLCSP81, CABGA324, and CABGA400 for specific devices. • Updated Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added part numbers. • Revision 00.2, February 2014 • DC and Switching Characteristics section: • Updated MachXO3L External Switching Characteristics – C/E Devices table. Removed LPDDR and DDR2 parameters.

Revision 00.2, February 2014

Section	Change Summary
DC and Switching Characteristics	Updated MachXO3L External Switching Characteristics – C/E Devices table. Removed LPDDR and DDR2 parameters.

Revision 00.1, February 2014

Section	Change Summary
All	Initial release.

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