Lattice USB3 Video Bridge Development Kit

User's Guide

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EB88_1.0

Introduction

The Lattice USB3 Video Bridge board allows designers to investigate and experiment with the features of the LatticeECP3™ Field-Programmable Gate Array device in applications of transporting video and audio data through the Universal Serial Bus (USB) 3.0 link. The Lattice USB3 Video Bridge board is the hardware platform of the Lattice USB3 Video Bridge Development Kit. Combined with the control and configuration application software and drivers, the features of the Lattice USB3 Video Bridge board can assist design engineers with rapid prototype and validation of their specific USB3 Video Bridge designs. This guide is intended to be referenced in conjunction with the RD1203, Lattice USB3 Video Bridge Reference Design User's Guide to demonstrate the capability and performance of LatticeECP3 FPGA.

Features

Key features of the Lattice USB 3.0 Video Bridge Development Kit include:

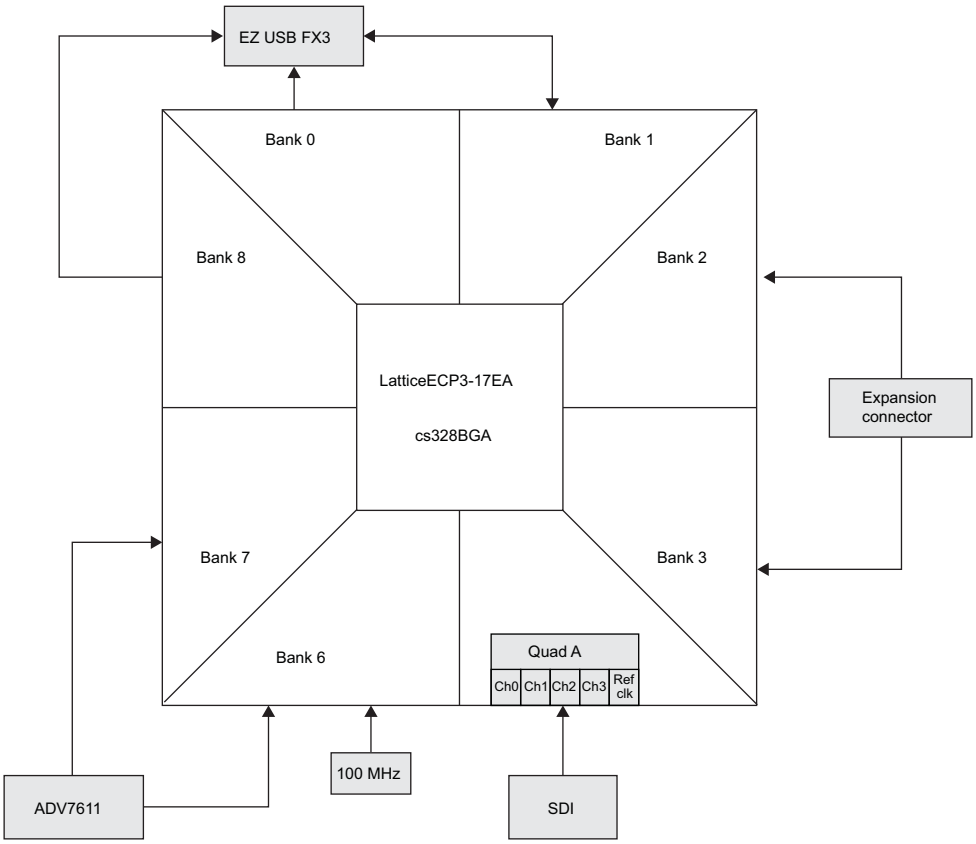
- SuperSpeed USB 3.0 Interface over Cypress EZ-USB FX3 (CYUSB3014) IC
- HDMI interface over Analog Devices ADV7611 IC
- Embedded SDI Receiver interface with TI LMH0394 Cable Equalizer
- Si5338 programmable clock generator
- LatticeECP3-17 FPGA programmed with USB3 Video and Audio bridge function
- Expansion connector for Image sensors using SubLVDS or MIPI CSI-2
- Selectable expansion VCCIO
- Selectable power supply (USB or Auxiliary 5V)
- Fly-wire ispDownload cable connection for JTAG fast program and Reveal Analyzer
- SPI serial flash controlled by the FX3 USB controller
- FPGA configuration at startup by the FX3 via the ispCONFIG SPI interface
- I2C and SPI bus for onboard device controls from the FX3
- FX3 JTAG Connector
- 2-pin GPIO debug connector (LVTTL) useful for I2C or UART

General Description

The Lattice USB3 Video Bridge Development Kit is built around the LatticeECP3-17EA 328-ball csBGA FPGA device. The board with the FPGA, peripheral devices and connectors provide a seamless USB3 bridge function for video streaming and capturing applications utilizing the USB 3.0 USB Video Class (UVC) standard. It also supports multi-channel I2S PCM audio streaming through the same USB3 link. The parallel video and audio interface from the ADV7611 HDMI Receiver, the embedded CML SERDES Receiver interface, and differential I/Os on the sensor expansion header are useful for evaluating various Lattice IP cores for video interfacing, as well as the USB 3.0 UVC bridge design. A number of test points are provided to validate various power and configuration status. Figure 1 shows the conceptual connections between LatticeECP3 FPGA device and other peripheral components of the USB3 Bridge board.

The contents of this user's guide include top-level functional descriptions of the various portions of the board, descriptions of the on-board connectors, diodes and switches and a complete set of schematics.

Figure 1. Lattice USB3 Video Bridge Board Block Diagram



Initial Setup and Handling

The following is recommended reading prior to removing the evaluation board from the static shielding bag and may or may not apply to your particular use of the board.

CAUTION: The devices on the board can be damaged by improper handling.

The devices on the evaluation board contain fairly robust ESD (Electro Static Discharge) protection structures within them, able to withstand typical static discharges (see the “Human Body Model” specification for an example of ESD characterization requirements). Even so, the devices are static sensitive to conditions that exceed their designed in protection. For example: higher static voltages, as well as lower voltages with lower series resistance or larger capacitance than the respective ESD specifications can potentially damage or degrade the devices on the evaluation board.

As such, it is recommended that you wear an approved and functioning grounded wrist strap at all times while handling the evaluation board when it is removed from the static shielding bag. If you will not be using the board for a while, it is best to put it back in the static shielding bag. Please save the static shielding bag and packing box for future storage of the board when it is not in use.

When reaching for the board, it is recommended that you first touch the outside shield portion of the SDI connector. This will neutralize any static voltage difference between your body and the board prior to any contact with signal I/O.

CAUTION: To minimize the possibility of ESD damage, the first and last electrical connections to the board should always be from test equipment chassis ground to the pin 1 of the J3 header.

Before connecting signals or power to the board, attach a cable from chassis ground on grounded test equipment to the to the pin 1 of the J3 header. Connecting the board ground to test equipment chassis ground will decrease the risk of ESD damage to the I/O on the board as the initial connections to the board are made. Likewise, when unplugging cables from the evaluation board, the last connection unplugged, should be the chassis GND connection to the evaluation board GND. If you have a signal source that is floating with respect to chassis GND, attempt to neutralize any static charge on that signal source prior to attaching it to the evaluation board.

If you are holding or carrying the board when it is not in a static shielding bag, please keep one finger on the outside shield portion of the SDI connector. This will keep the board at the same voltage potential as your body until you can pick up the Dstatic shielding bag and put the board back in it.

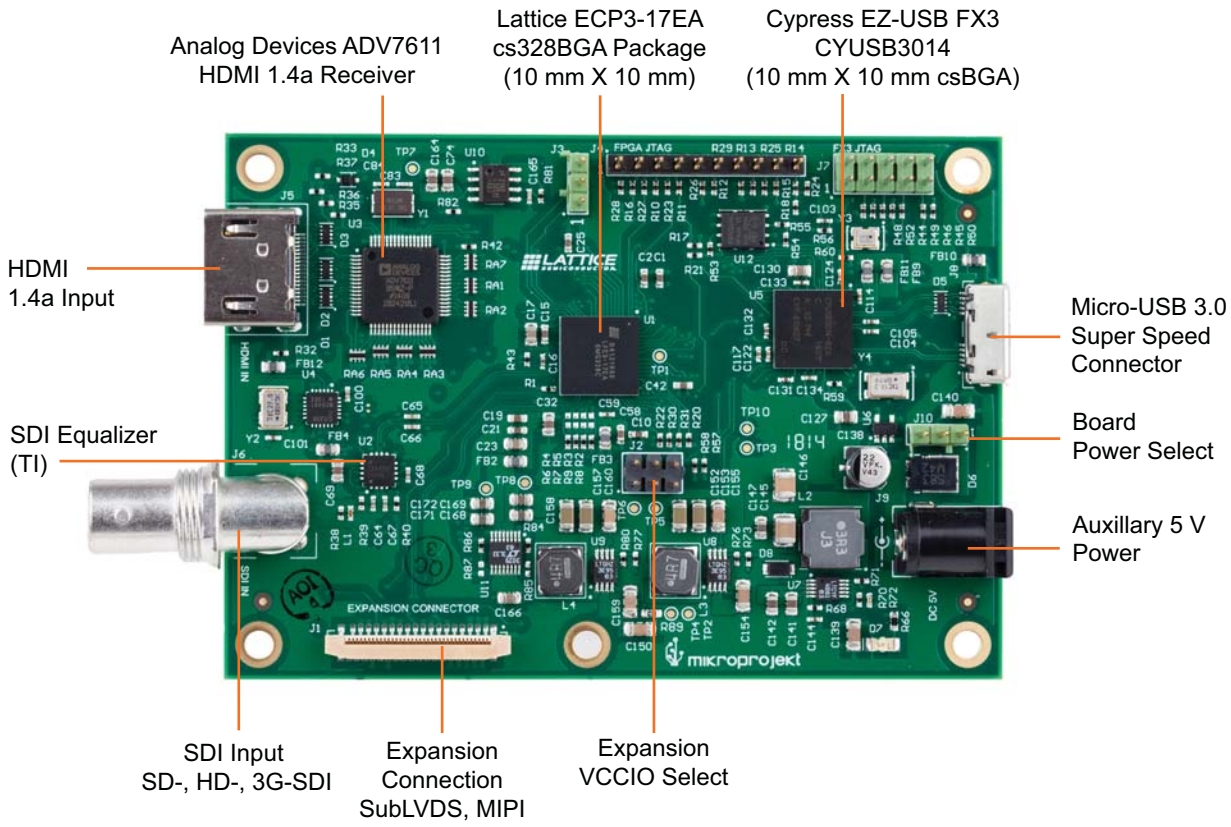
Electrical, Mechanical and Environmental Specifications

The nominal board dimensions are 99 mm x 69 mm. On the physical board itself, connectors include pin 1 indicators as a dot, or a number “1” beside the pin 1 on the outer layer silk screen. The environmental specifications are as follows:

- Operating temperature: 0 °C to 55 °C
- Storage temperature: -40 °C to 75 °C
- Humidity: <95% without condensation
- 5 V DC

Functional Description

Figure 2. Lattice USB3 Video Bridge Board, Top View



LatticeECP3 Device

This board features a LatticeECP3-17 FPGA with a 1.2 V DC core in a 328-ball csBGA 10 mm x10 mm package. A complete description of this device can be found on the Lattice web site at www.latticesemi.com/products/fpga/ecp3.

USB3 Connector (J8)

The board is powered and communicates with the USB 3.0 Host through an USB 3.0 Micro b connector/receptacle. It is connected to the host with the provided USB 3.0 A-to-Micro b cable.

Auxiliary Power Connector (J9)

The board can be alternately supplied by a single 5 V DC power supply at J9. On-board step-down switching regulators then provide the necessary supply voltages: 3.3 V, 2.5 V, 1.8 V, 1.2 V. For proper operation, the 5 V DC power applied at J9 should be within the range of +4,75 V min. to +5,25 V max. The requirements for the J10 power jack itself are listed in Table 1.

Table 1. Auxiliary Power Jack J9 Specifications

Polarity	**Positive Center**
Inside diameter	0.1" (2.5 mm)
Outside diameter	0.218" (5.5 mm)
Current Capacity	Up to 2.5 A

Power Supplies

The on-board switching and linear regulator output voltages can be measured at test points located around the board as shown in Table 2.

Table 2. Test Points for On-Board Regulator Voltages

Supply	Regulator	Test Point	Resistor Ratio	Comment
5.0 V	-	TP2	NA	Input voltage
3.3 V	U8	TP5	R73/R76	
2.5 V	U9	TP6	R77/R80	
1.8 V	U10	TP7	R82/R83	
1.2 V	U7	TP3	R70/R72	
1.2 V (SERDES)	U11	TP8	NA	

Each of the step-down switching regulators, U7, U8 and U9, incorporate typical resistor divider voltage feedback to divide down the regulator output voltage and compare it against an internal reference voltage. The regulator then adjusts the output voltage higher or lower such that the resistor divided voltage matches the internal reference. By doing this, the regulator output voltage remains at a constant voltage value independent of the load driven. Each regulator output voltage follows this equation:

Vout= (1 + resistor ratio) x (regulator internal reference voltage)

See the LT3685 and LTC3621 device data sheets for additional details about these devices.

The 1.8 V regulator (U10) is a low dropout linear type regulator with an adjustable output voltage which is set using the external resistive divider. The output voltage is given by the formula:

Vout= (1 + resistor ratio) x (Vadj)

where Vadj is feedback voltage.

See the LP38511 device data sheet for additional details about this device.

The SERDES 1.2 V regulators (U11) are low dropout linear types that deliver a constant 1.2 V output voltage when powered by the 2.5 V input voltage. In contrast to the switching regulators discussed above, the U11 linear regulators do not generate switching noise, so they are a good choice for powering the LatticeECP3 SERDES to give the lowest jitter generation. Also, U11 does not use resistor divider networks to set the output voltage, instead it is set up to directly copy its own internal 1.215 V reference voltage to its outputs. The U11 regulator outputs are available for testing at test points TP8 and TP9. See the LT3029 device data sheets for additional details about this device.

When using the various I/O test points located around the board, be sure to not exceed the LatticeECP3 Family Data Sheet specified absolute maximum rating for Output Supply Voltage VCCIO range of -0.5 V to +3.75 V, or damage to the device may occur. Also, for I/O input capability of the various I/O standards supported by the LatticeECP3 sysIO structures, see the LatticeECP3 sysIO Usage Guide.

Cypress EZ-USB FX3 (U5)

Cypress's EZ-USB FX3 is the next-generation USB 3.0 peripheral controller, providing integrated and flexible features.

FX3 integrates a fully configurable, parallel, general programmable interface called GPIF II, which can connect to any processor, ASIC, or FPGA. It provides simple connectivity to popular interfaces, such as asynchronous SRAM, asynchronous and synchronous address data multiplexed interfaces, and parallel ATA.

FX3 has integrated the USB 3.0 and USB 2.0 physical layers (PHYs) along with a 32-bit ARM926EJ-S microprocessor for powerful data processing and for building custom applications. It implements an architecture that enables 375-MBps data transfer from GPIF II to the USB interface.

For more information on the EZ-USB FX3, please refer to the EZ-USB FX3 Datasheet http://www.cypress.com/?docID=44322.

GPIF II Interface

The GPIF II interface implements the Slave FIFO signaling to receive the UVC and UAC packeted streaming data from the LatticeECP3. For more information about the Slave FIFO interface, please consult the EZ-USB FX3 Datasheet technical reference manual http://www.cypress.com/?docID=44322. The signal connections between the EZ-USB FX3 and the Lattice ECP3 Device are shown in Table 3.

Table 3. LatticeECP3(U1) connections to EZ-USB FX3 (U5) GPIF II interface

Signal	sysIO Bank	LatticeECP3 BGA Ball	EZ-USB FX3 Interface Signal
sf_data[0]	8	D18	dq[0]
sf_data[1]	1	A12	dq[1]
sf_data[2]	0	B10	dq[2]
sf_data[3]	8	L17	dq[3]
sf_data[4]	8	A16	dq[4]
sf_data[5]	1	A11	dq[5]
sf_data[6]	8	H18	dq[6]
sf_data[7]	8	D17	dq[7]
sf_data[8]	8	J18	dq[8]
sf_data[9]	8	F17	dq[9]
sf_data[10]	8	J17	dq[10]
sf_data[11]	8	F19	dq[11]
sf_data[12]	8	J19	dq[12]

Signal	sysIO Bank	LatticeECP3 BGA Ball	EZ-USB FX3 Interface Signal
sf_data[13]	1	B13	dq[13]
sf_data[14]	8	G18	dq[14]
sf_data[15]	1	A14	dq[15]
sf_data[16]	0	C7	dq[16]
sf_data[17]	0	B8	dq[17]
sf_data[18]	0	C6	dq[18]
sf_data[19]	0	B4	dq[19]
sf_data[20]	0	B7	dq[20]
sf_data[21]	0	A7	dq[21]
sf_data[22]	0	A6	dq[22]
sf_data[23]	0	B5	dq[23]
sf_data[24]	0	A9	dq[24]
sf_data[25]	0	B3	dq[25]
sf_data[26]	0	A5	dq[26]
sf_data[27]	0	A4	dq[27]
sf_data[28]	0	C10	dq[28]
sf_data[29]	0	A3	dq[29]
sf_data[30]	0	B6	dq[30]
sf_data[31]	0	A8	dq[31]
sf_addr[0]	1	B11	ctl[12]
sf_addr[1]	0	C9	ctl[11]
sf_csn	1	C12	ctl[0]
sf_wen	1	A13	ctl[1]
sf_oen	1	B12	ctl[2]
sf_rdn	8	A15	ctl[3]
sf_pktend	8	B16	ctl[7]
sf_clko	0	B9	pclk
sf_flaga	1	C11	ctl[4]
sf_flagb	1	C13	ctl[5]

SPI Serial Flash (U12)

The U12 SPI Flash device used on this board is a 16-pin, 16-Mbit device, operated by the EZ-USB FX3. It is sufficient to store both the EZ-USB FX3 Firmware and the LatticeECP3 Bitstream. The EZ-USB FX3 will boot from the SPI flash, then read out and download the LatticeECP3 Bitstream over the Slave SPI sysCONFIG interface. The SPI Flash device is an STMicro SPI-M25P16 in an 8-pin package.

LatticeECP3 IO Bank Voltages

Most of the bank voltages on the LatticeECP3-17 device (U1) have been hard-wired to specific power supply values, except for the bank 2 which can be set to different voltage levels to support various sensor and camera interfaces through the expansion connector J1. The voltage assignment is shown in Table 4.

Table 4. LatticeECP3 (U1) Bank Voltage Settings

LatticeECP3 Bank VCCIO	Voltage	Comment
0 and 1	2.5 V	EZ-USB FX3
2	Adjustable	Expansion connector SubLVDS, MIPI 3.3 V: Jumper on J2 pins 1-2 2.5 V: Jumper on J2 pins 3-4 1.2 V: Jumper on J2 pins 5-6
3	3.3 V	Expansion connector SubLVDS, MIPI
6	3.3 V	ADV7611, I2C and UART bus
7	3.3 V	ADV7611
8	2.5 V	LatticeECP3 programming, EZ-USB FX3
Quad A	1.2 V	SERDES

Clock Sources

There are two crystals, two oscillators, and a programmable clock generator on the Lattice USB 3.0 Video Bridge Development Kit. The two crystals are used as clocks for the ADV7611 and the EZ-USB FX3. One oscillator is used to provide the 32.768 kHz RTC clock to the EZ-USB FX3, While the 27 MHz oscillator is used as the reference clock for the Si5338 clock generator, which is used to drive the (by default 100 MHz) system and GPIF interface frequency to the LatticeECP3 (U1), as well as the reference differential clock to the LatticeECP3 SERDES used for the SDI interface. Table 5 shows the oscillator usage. Locations Y2 and Y3 are the oscillators.

Table 5. LatticeECP3 (U1)

Source	Frequency	Comment	LatticeECP3 Input and IO Setting
Y1	28.63636 MHz	ADV7611 pins 58 and 59	-
Y2	27 MHz	SI5338 pin 3	-
Y3	32.768 kHz	CYUSB3014 pin D6	-
Y4	19.2 MHz	CYUSB3014 pins C6 and C7	-
Si5338 CLK0 (A/B)	Adjustable	QuadA pins U10 and T10	
Si5338 CLK2 (A)	Adjustable (100 MHz Typ.)	LatticeECP3 pin R2	

HDMI Video Input

The HDMI Video input is connected to the Analog Devices ADV7611 (U3).

The ADV7611 is an HDMI receiver that supports all mandatory 2D and 3D video formats defined in HDMI 1.4a. It supports HDMI audio extraction and has an audio output port for the audio data extracted from the HDMI stream. Accessible audio formats are: a stream from the I2S serializer (two audio channels), a stream from the S/PDIF serializer (two uncompressed channels or N compressed channels, for example, AC3) and DST stream.

The LatticeECP3 interfaces to the ADV7611 as shown in Table 6.

Table 6. LatticeECP3(U1) connections to ADV7611 (U3)

Signal	sysIO Bank	LatticeECP3 BGA Ball	ADV7611 Signal
vp[2]	7	F3	p[0]
vp[3]	7	F1	p[1]
vp[4]	7	G1	p[2]
vp[5]	7	H1	p[3]
vp[6]	7	J1	p[4]

Signal	sysIO Bank	LatticeECP3 BGA Ball	ADV7611 Signal
vp[7]	7	H3	p[5]
vp[8]	7	G2	p[6]
vp[9]	7	L1	p[7]
vp[12]	7	G3	p[8]
vp[13]	7	J2	p[9]
vp[14]	7	K2	p[10]
vp[15]	7	J3	p[11]
vp[16]	7	H2	p[12]
vp[17]	7	L2	p[13]
vp[18]	7	N2	p[14]
vp[19]	7	N3	p[15]
vp[22]	7	M2	p[16]
vp[23]	6	R3	p[17]
vp[24]	7	N1	p[18]
vp[25]	6	T2	p[19]
vp[26]	6	V1	p[20]
vp[27]	6	T3	p[21]
vp[28]	7	L3	p[22]
vp[29]	7	M1	p[23]
hs	7	E3	hs
vs	7	D2	vs/field/alsb
de	7	E2	de
pclk	7	M3	llc
lrclk_a	7	D3	lrclk
sclk_a	7	D1	sclk/int2
i2s0_a	7	E1	ap
adv_t_rst_n	6	V2	resetn

SDI Video Input

The SDI Video input is connected to the Texas Instruments LMH0394 (U2) SDI cable equalizer. The equalizer operates over a wide range of data rates, from 125 Mbps to 2.97 Gbps and supports SMPTE 424M, SMPTE 292M, SMPTE 344M, and SMPTE 259M standards.

The signal connections between the LatticeECP3 device and the LMH0394 are shown in Table 7.

Table 7. LatticeECP3(U1) connections to LMH0384 (U2)

Signal	sysIO Bank	Polarity	LatticeECP3 BGA Ball	LMH0394 signal
sdi_inp_ch0	Quad A	P	W14	SDO
sdi_inn_ch0	Quad A	N	W15	SDOn

Expansion Connector (J1)

Expansion connector Molex 52559-3652 is provided to connect the LatticeECP3 to a camera or a sensor. Various camera or sensor module interfaces are supported: parallel, SubLVDS or MIPI-CSI-2. Adapter boards are available for various camera/sensor options: HDR-60 NanoVesta connector with SubLVDS lines (MN34041), Sony FCB-MA130 Block camera with MIPI CSI-2 interface.

The signal connections between the LatticeECP3 device and the Molex expansion connector are shown in Table 8.

Table 8. LatticeECP3(U1) Connections to Molex Expansion Connector (J1)

Signal	sysIO Bank	Polarity	LatticeECP3 BGA Ball	Molex pin number
mipi_dck_p	3	P	P17	11
mipi_dck_n	3	N	P19	12
mipi_d0_p	3	P	R18	13
mipi_d0_n	3	N	R17	14
mipi_d1_p	3	P	T17	15
mipi_d1_n	3	N	T18	16
mipi_d2_p	3	P	R19	17
mipi_d2_n	3	N	T19	18
mipi_d3_p	3	P	U18	19
mipi_d3_n	3	N	U19	20
mipi_gpio0	2	-	L18	31
mipi_gpio1	2	-	K18	32
mipi_gpio2	3	-	V18	33
mipi_gpio3	3	-	V19	34
mipi_lp0_0	2	-	M18	24
mipi_lp0_1	2	-	M19	23
mipi_lpclk_0	2	-	L19	28
mipi_lpclk_1	2	-	N17	27

Configuration/Programming Header (J4)

The J4 JTAG 1x10 header is provided on the board for accessing the LatticeECP3 JTAG port. It can be used for downloading the LatticeECP3 FPGA bitstream and reveal troubleshooting. It cannot be used for SPI Flash programming.

Pin #	Description	LatticeECP3 BGA Ball
Pin 1	VCC	-
Pin 2	TDO	B1
Pin 3	TDI	C1
Pin 4	PROGRAMN	C19
Pin 5	NC	-
Pin 6	TMS	A2
Pin 7	GND	-
Pin 8	TCK	B2
Pin 9	DONE	E19
Pin 10	INITN	C18

Debug Header (J3)

For general testing and debugging purposes I/Os on the LatticeECP3 are brought to dedicated connector header J3. The signal connections between the LatticeECP3 device and the J3 header are shown in Table 9.

Table 9. LatticeECP3(U1) connections to debug header (J3)

Signal	sysIO Bank	LatticeECP3 BGA Ball	J3 header pin number
dbg_0	6	T1	1
dbg_1	6	U1	2

Default Jumper Settings

Figure 3. Default Jumper Settings - J10

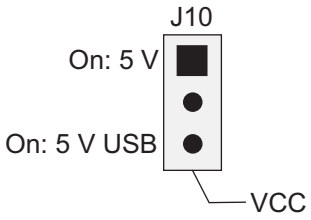
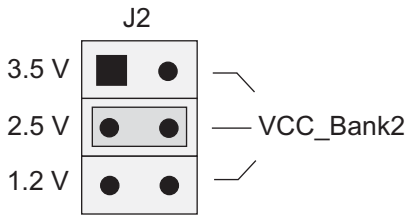


Figure 3 shows the Lattice USB3 Video Bridge Board default jumper settings of J10 header. J10 selects the power supply source for the board. By installing a jumper between pins 1-2 of the J10 header, the board is supplied by a single 5 V DC power supply at J9. The board is powered through an USB 3.0 Micro b connector/receptacle.

Figure 4. Default Jumper Settings - J2



J2 selects the IO bank power supply for the LatticeECP3 bank 2. Placing a jumper on J2 pins 1-2 selects 3.3 V, jumper on J2 pins 3-4 selects 2.5 V and jumper on J2 pins 5-6 selects 1.2 V.

LEDs

There is one LED (D7) on the Lattice USB3 Video Bridge Board which indicates the power-on status of the board.

Board Programming/Configuration

After initial board setup, use the following procedure to program the board. There is an onboard SPI flash memory (U12) which stores the image file of both FX3 firmware and FPGA bitstream. The SPI flash memory can be programmed through the USB3 link by the USB3 Configurator application installed on the Windows PC. The image file then will be automatically loaded to program and configure the FX3 and FPGA devices during power-up.

The USB3 Bridge is equipped with two separated JTAG connectors which allow the user to configure the SRAM of the FPGA and FX3 devices respectively. The J4 connector is connected to the JTAG port of ECP3-17 device and is useful for on-chip debug using Reveal Analyzer tool; the J7 connector is connected to the JTAG port of FX3 device for SRAM configuration and debugging using Cypress USB Suite Control Center tool.

For more details of Lattice ECP3 FPGA configuration, please refer to TN1169, LatticeECP3 sysCONFIG Usage Guide.

Install the Configurator and Drivers

Lattice USB3 Video Bridge Development Kit provides a versatile USB3 Configurator tool to allow the user to program and configure the FX3 and FPGA devices within a unified Windows GUI. The configurator application is also used to control the video input and format for the USB Video Bridge demonstration. Follow the procedure below to install the USB3 Video Bridge Configurator application.

1. Go to Lattice USB3 Video Bridge Development Kit website (www.latticesemi.com/usb3) to download the development kit. DK-ECP3-USB3-xxx.zip. [xxx] represents the revision of the development kit
2. Unzip the kit and copy all the files to the default \Lattice_DevKits directory or any user-specified directory
3. Go to the sub-directory <install_dir>\DK-ECP3-USB3-xxx\Software and run the setup.exe installer.
4. Accept the license agreement and continue to install the Configurator application to the *\Program Files\Lattice USB 3.0 Video Bridge Configurator* folder.

The Cypress USB Bootloader and Lattice USB3 Video Converter driver will be installed as part of the USB3 Video Bridge Configurator installation.

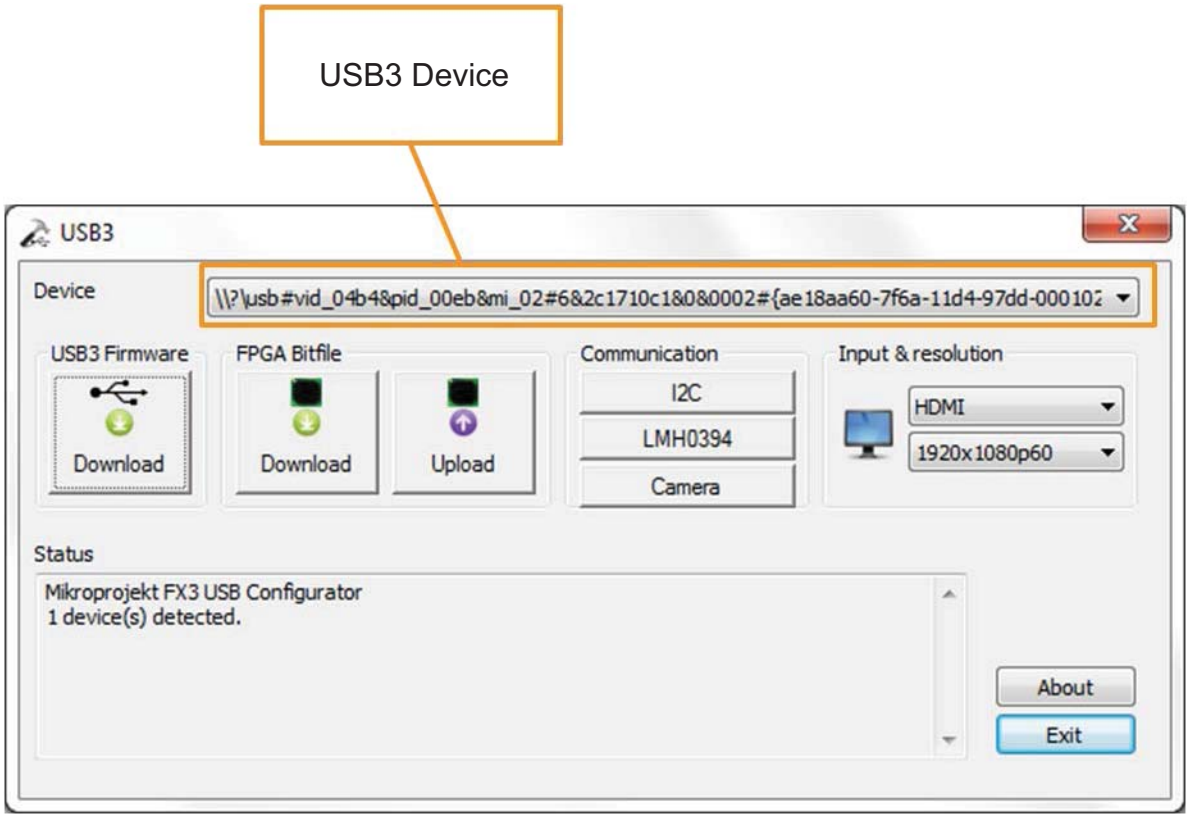
Download USB3 Firmware

1. Connect the Lattice USB3 Video Bridge board to the PC's USB 3.0 port colored in blue, or marked with the USB SuperSpeed logo. It is also suggested to use the USB 3.0 ports which can provide extra power (additionally marked with a lightning icon).
2. The board will enumerate after approximately 15 seconds and appear in the Devices and Printers folder as a Lattice USB3 Video Bridge device. You can also check the same device name under the *Imaging devices* and *Sound, video and game controller* categories of the Device Manager.

   Note: The on-board SPI flash memory is pre-loaded with the firmware and bitstream for the USB3 Video Bridge demo. If the board is not pre-loaded with the USB3 Video Bridge firmware, the default driver invoked is Cypress USB Bootloader.

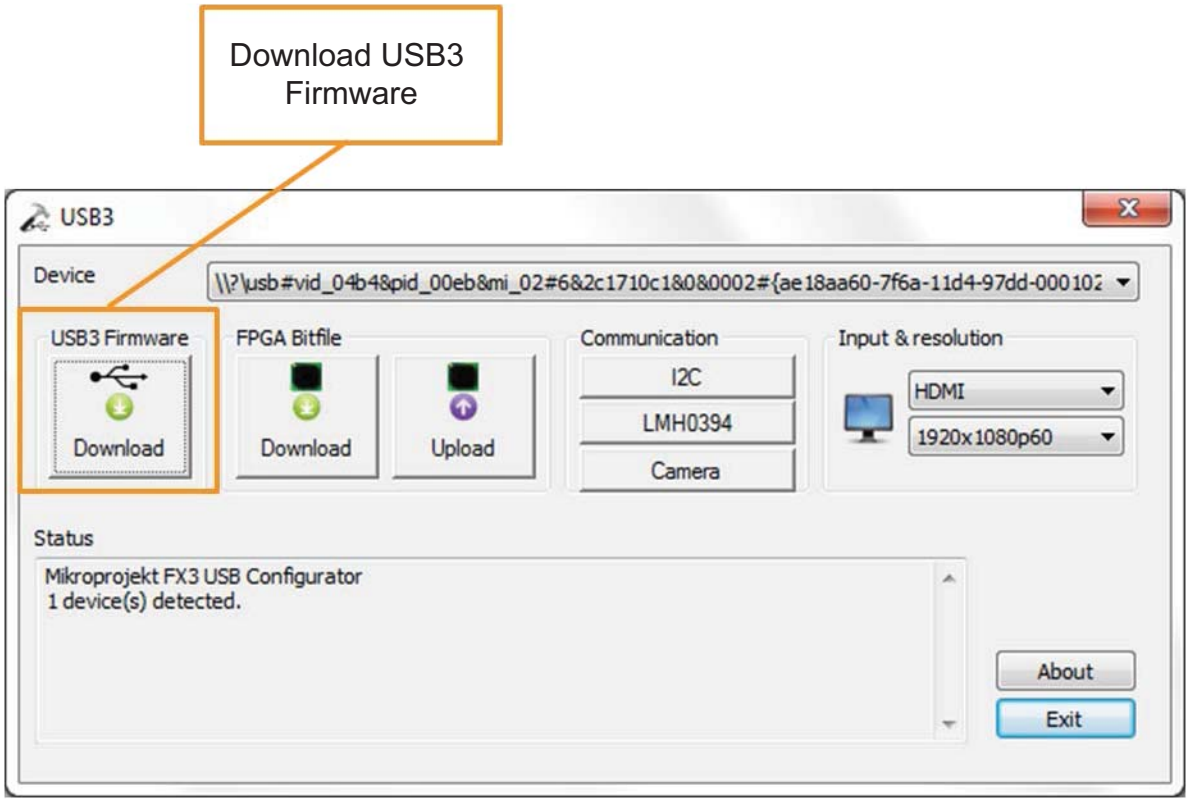
3. After opening the USB3 Video Bridge Configurator application, the USB3 device should appear in the Device dialog box.

Figure 5. Device Dialog Box



4. Click the **USB3 Firmware Download** button and choose the appropriate USB3 firmware file (Disc image file) from <install_dir>\DK-ECP3-USB3-xxx\Demonstration\FX3_firmware folder in the pop-up window.
5. Restart the board by recycling the board power supply if pins 1-2 of J10 are shunted; or unplug and re-plug in the USB 3.0 cable if pin 2 and pin 3 of J10 are shunted.

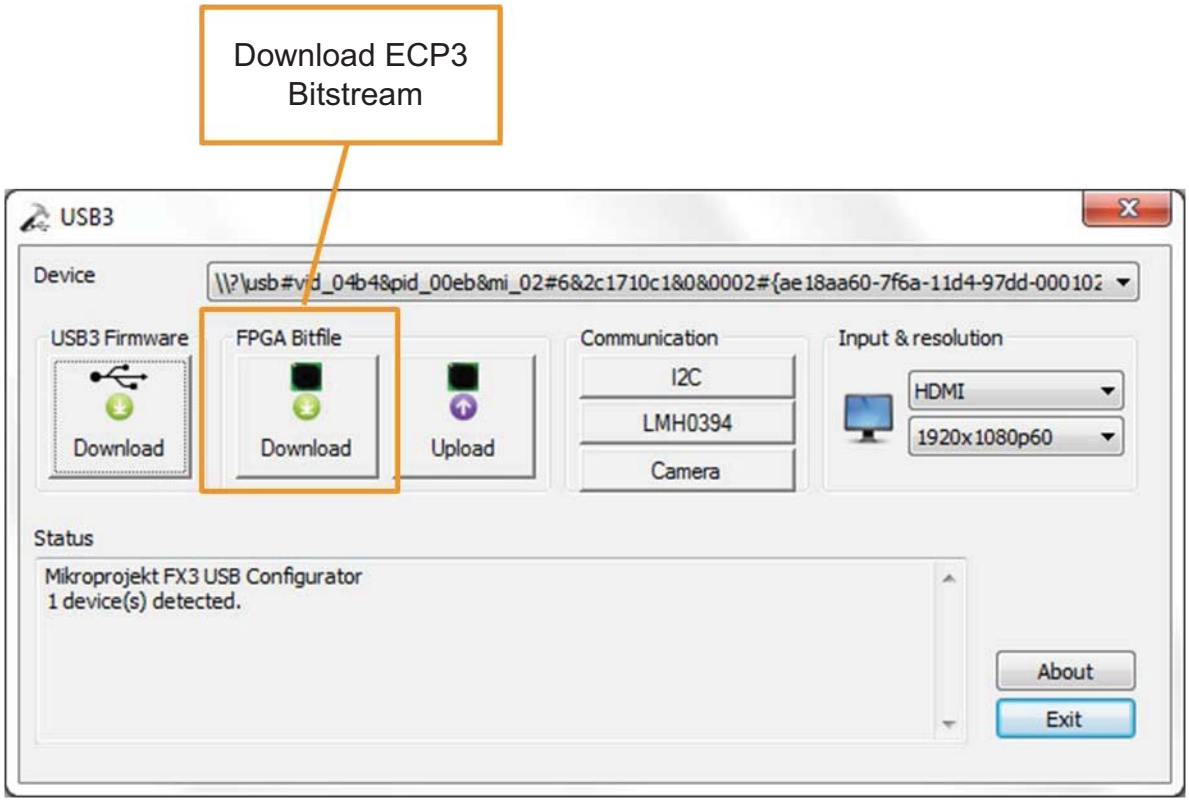
Figure 6. USB3 Firmware Download Button



Download FPGA Bitstream

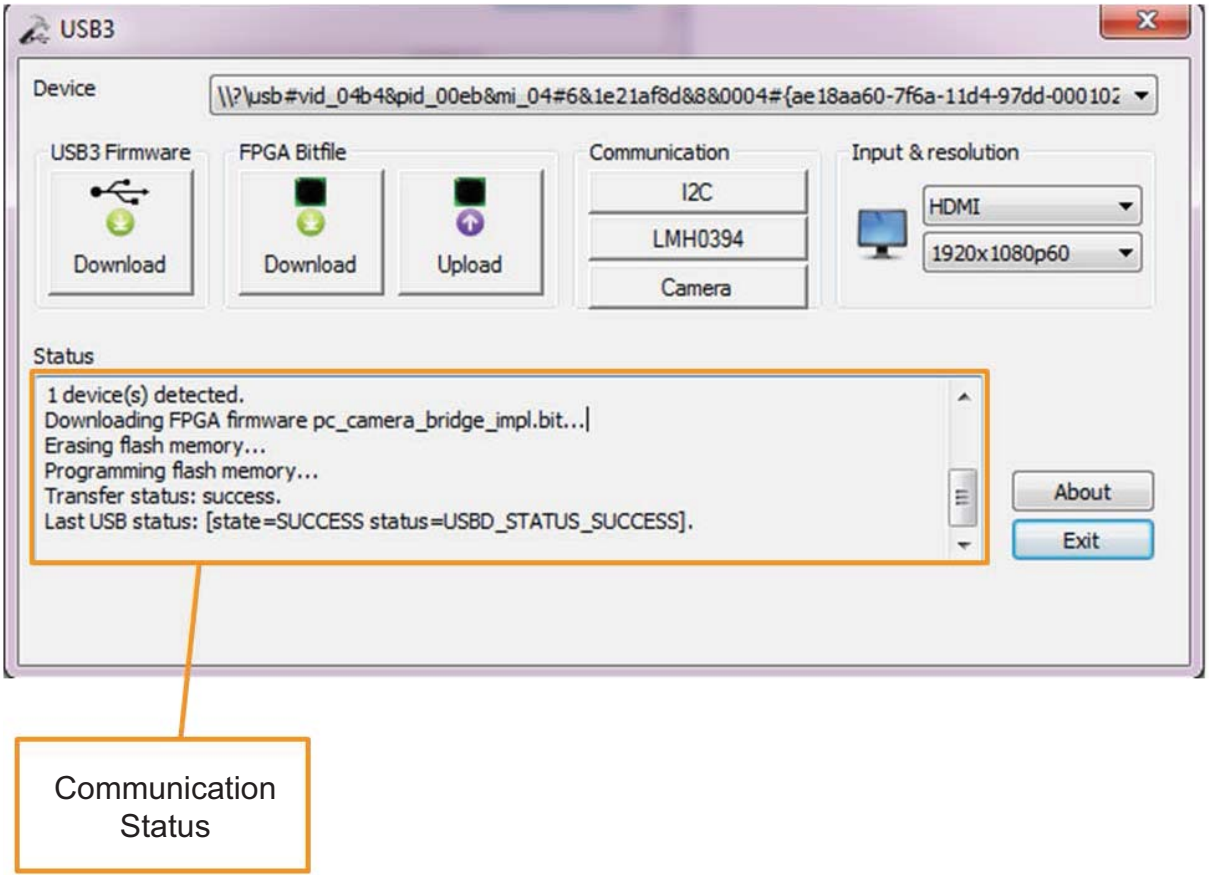
Repeat steps 1 and 2 in the Download USB3 Firmware section above if the board is not powered on and plugged into the USB 3.0 port of the PC. Download the FPGA bitstream by clicking the **FPGA Bitfile Download** button in the USB3 Video Bridge Configurator application and choosing the bitstream from the <install_dir>\DK-ECP3-USB3-xxx\Demonstration\ECP3_bitstream folder in the pop-up window.

Figure 7. FPGA Bitfile Download Button



After the download has completed, the following message should appear in the communication status box.

Figure 8. Communication Status Box



Configure Audio Device

The Lattice USB3 Video Bridge can transfer audio data through a USB isochronous mode endpoint. The demo design supports two-channel 16-bit PCM audio data of 48 KHz sampling rate. It preserves the resources to support more audio channels of different sampling rate and audio data width (e.g. eight-channel 24-bit 96 KHz sampling rate) for future development.

After the success of the board enumeration, the Lattice USB 3.0 Video Bridge device should appear in the Device Manager under both the *Imaging devices* and the *Sound, video and game controllers device* categories. Depending on the Windows operating system, the Lattice USB 3.0 Video Bridge may not be chosen as the default audio device. Follow the procedure described below to configure and enable the audio device in Windows Control Panel.

1. Go to **Control Panel > Hardware and Sound** folder and open the Sound link. This opens a new Sound configuration window.
2. Select the **Recording** tab, click on **Lattice USB 3.0 Video Bridge** and set it as the default Microphone device. See Figure 9.
3. Click the **Properties** button to open the Microphone Properties window.
4. Select the **Listen** tab, select the **Listen to this device** check box and click the **Apply** button to accept the change. See Figure 10.

After enabling Lattice USB 3.0 Video Bridge as the default Microphone device, the Lattice USB3 Video Bridge board is ready to stream both video and audio to the Windows PC equipped with the USB 3.0 port.

Figure 9. Sound-Recording Tab Configuration

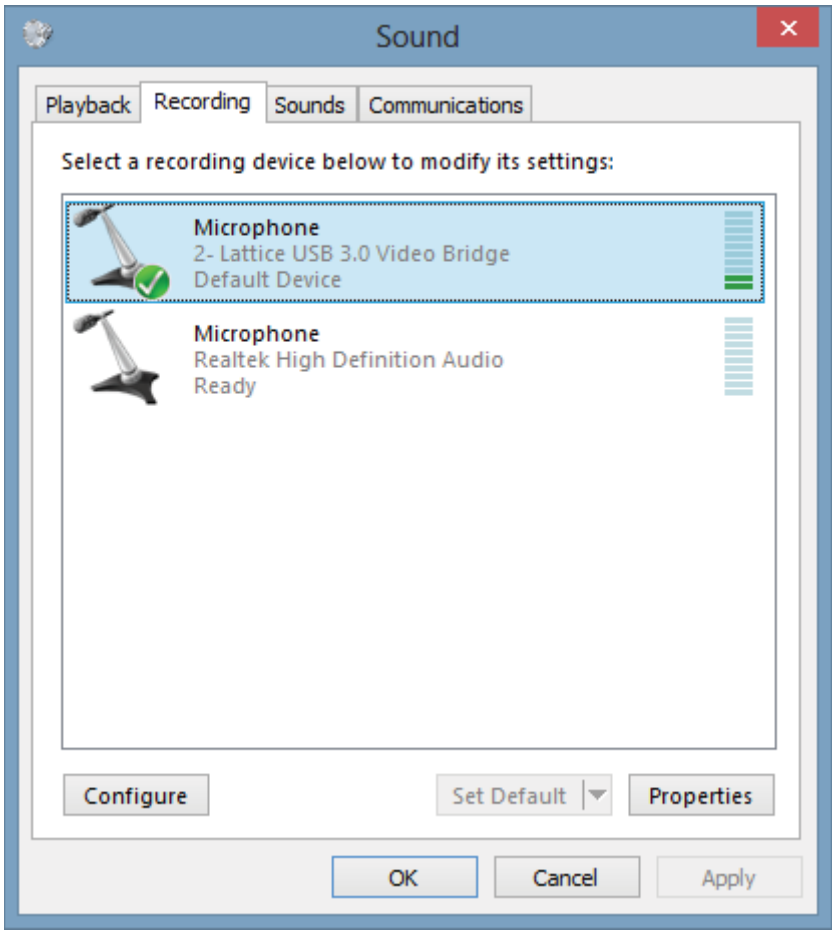
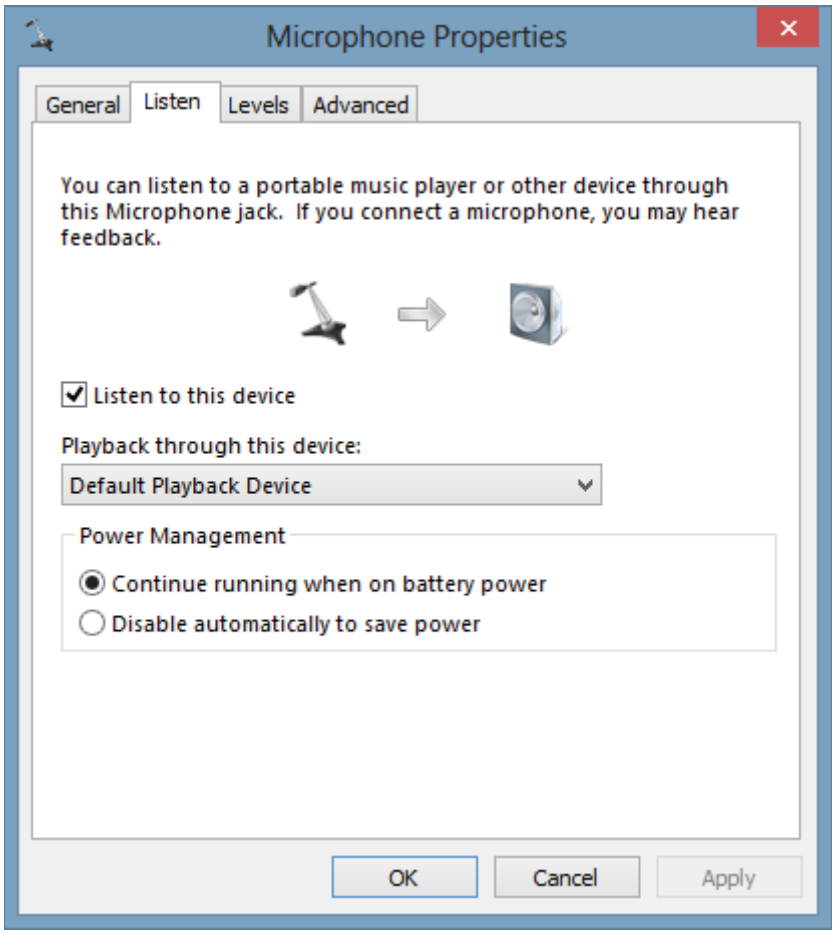


Figure 10. Microphone Properties – Listen Tab Configuration



Ordering Information

Description	Ordering Part Number	China RoHS Environmental Friendly Use Period (EFUP)
Lattice USB3 Video Bridge Development Kit	LFE3-17EA-USB3-EVN	

Technical Support Assistance

e-mail: techsupport@latticesemi.com

Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
August 2014	1.0	Initial release.

Appendix A. Schematics

Figure 11. Sheet 1 of 17

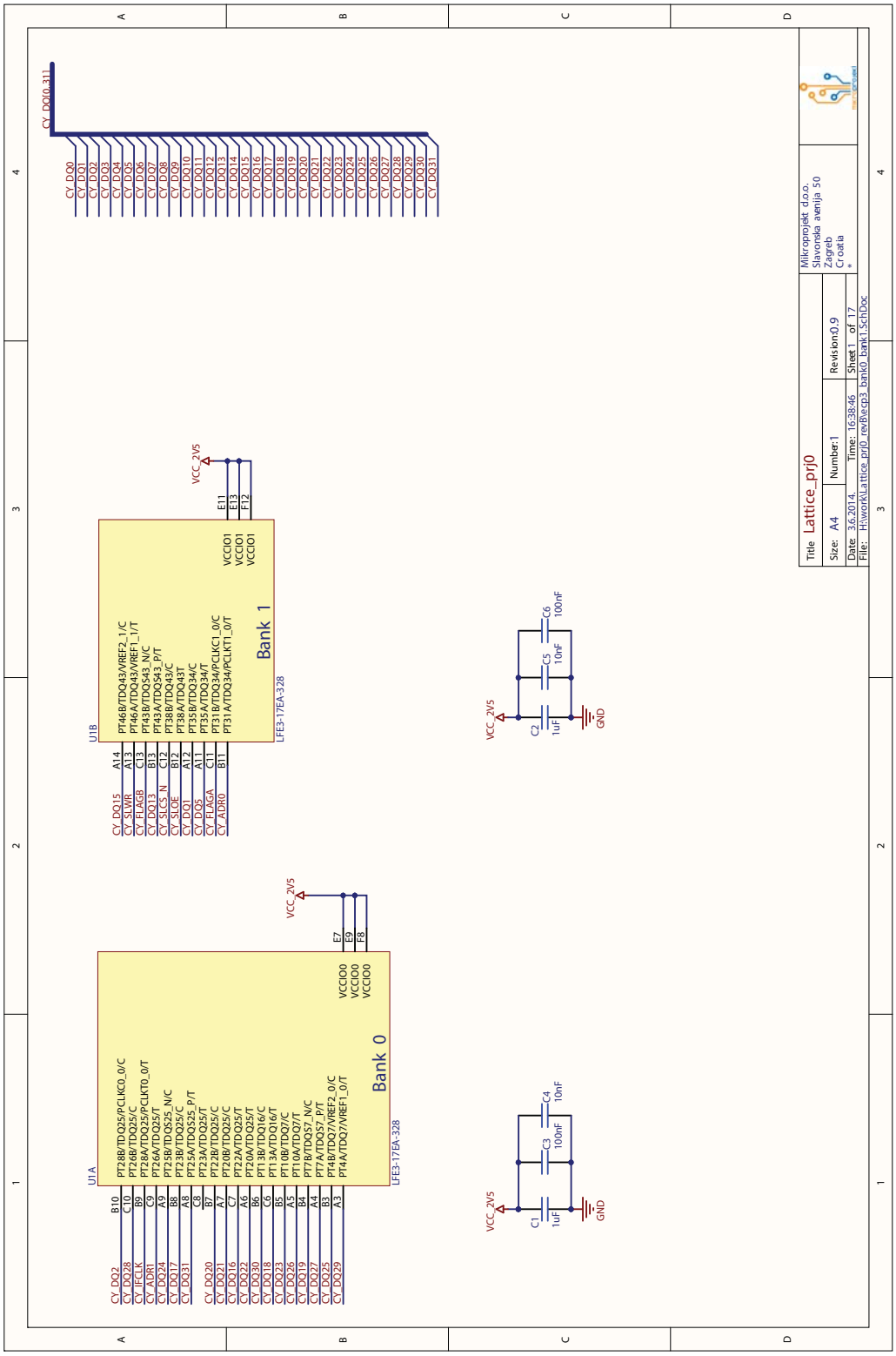


Figure 12. Sheet 2 of 17

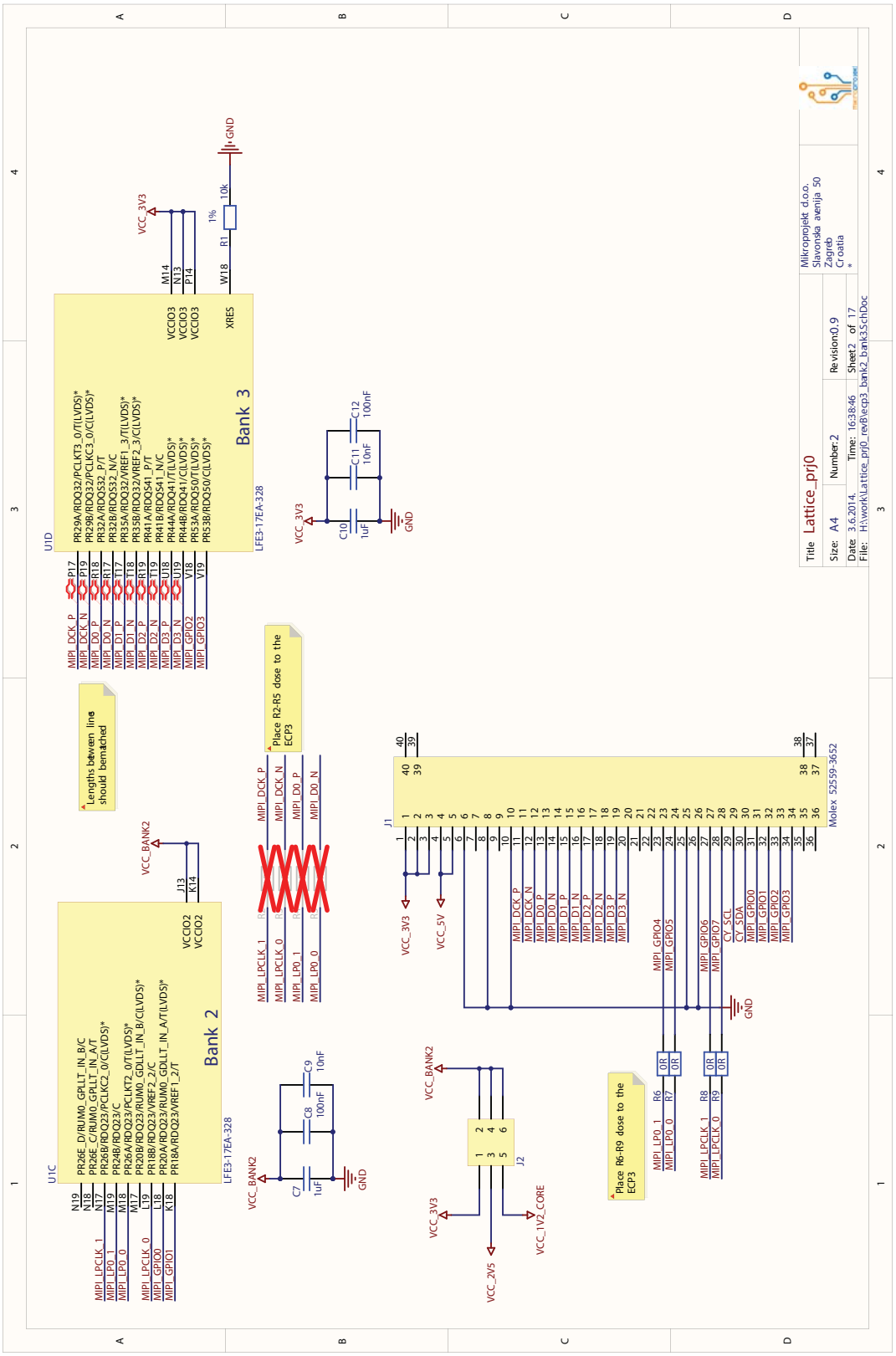


Figure 13. Sheet 3 of 17

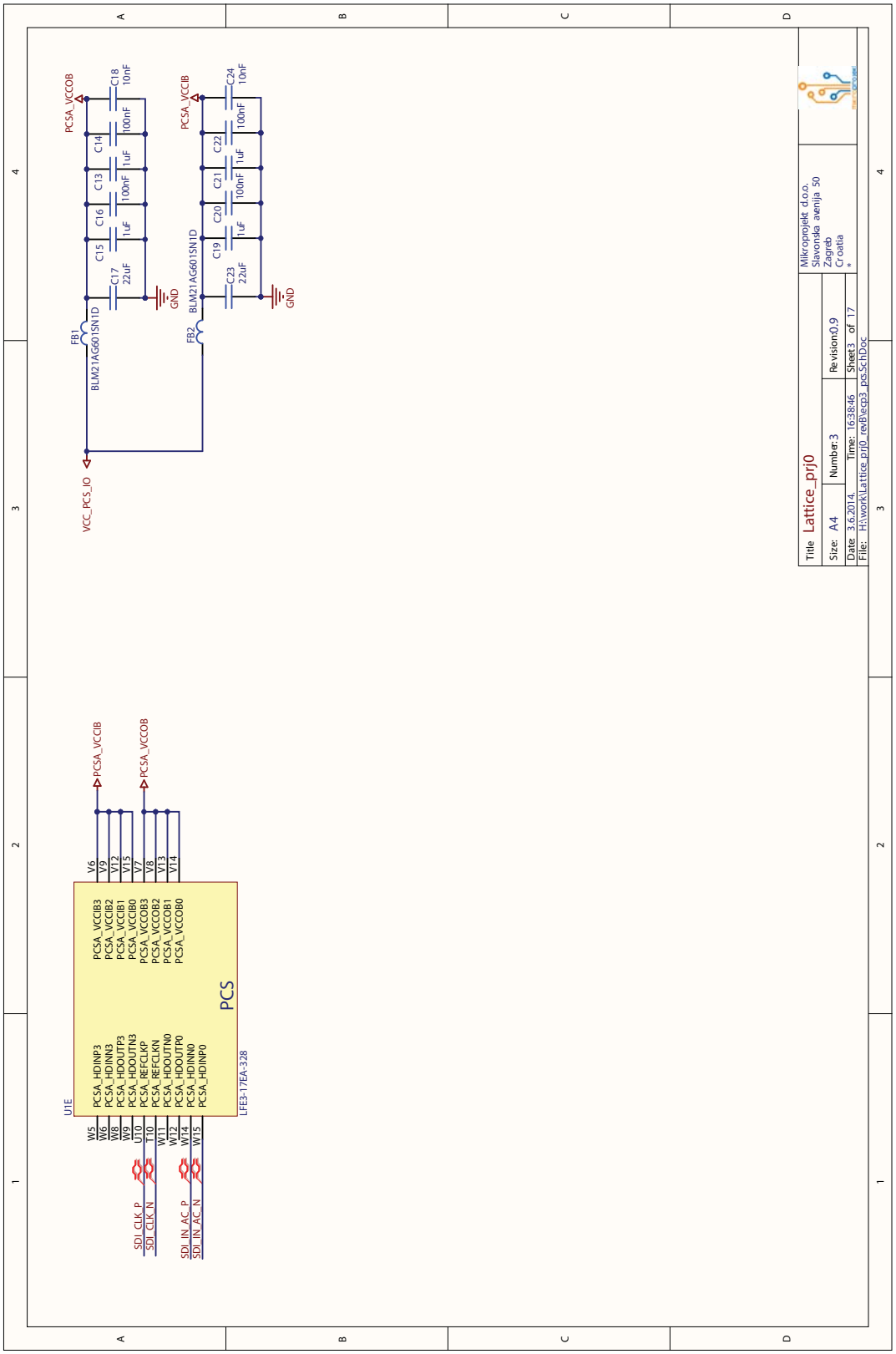


Figure 14. Sheet 4 of 17

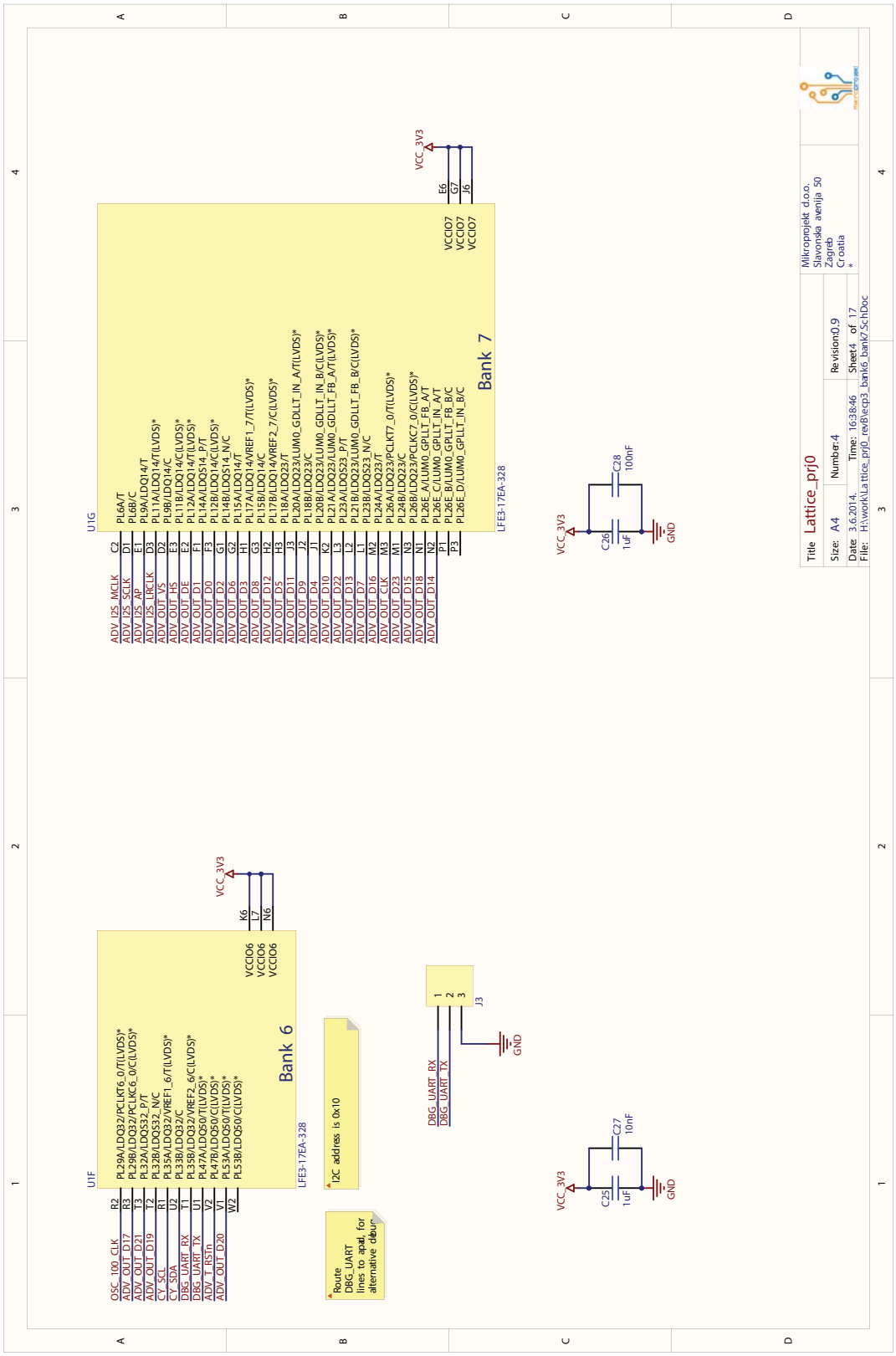


Figure 15. Sheet 5 of 17

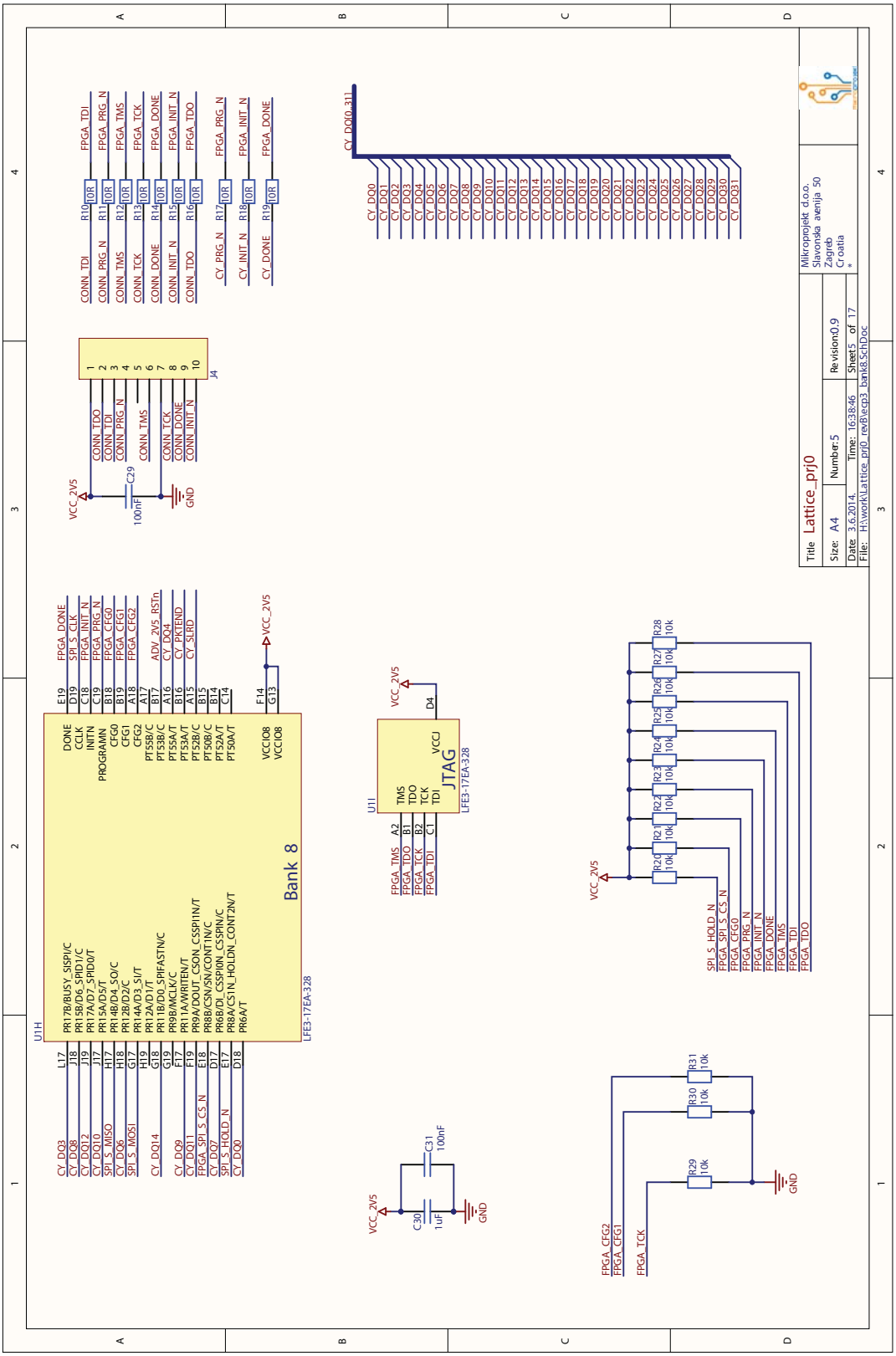


Figure 16. Sheet 6 of 17

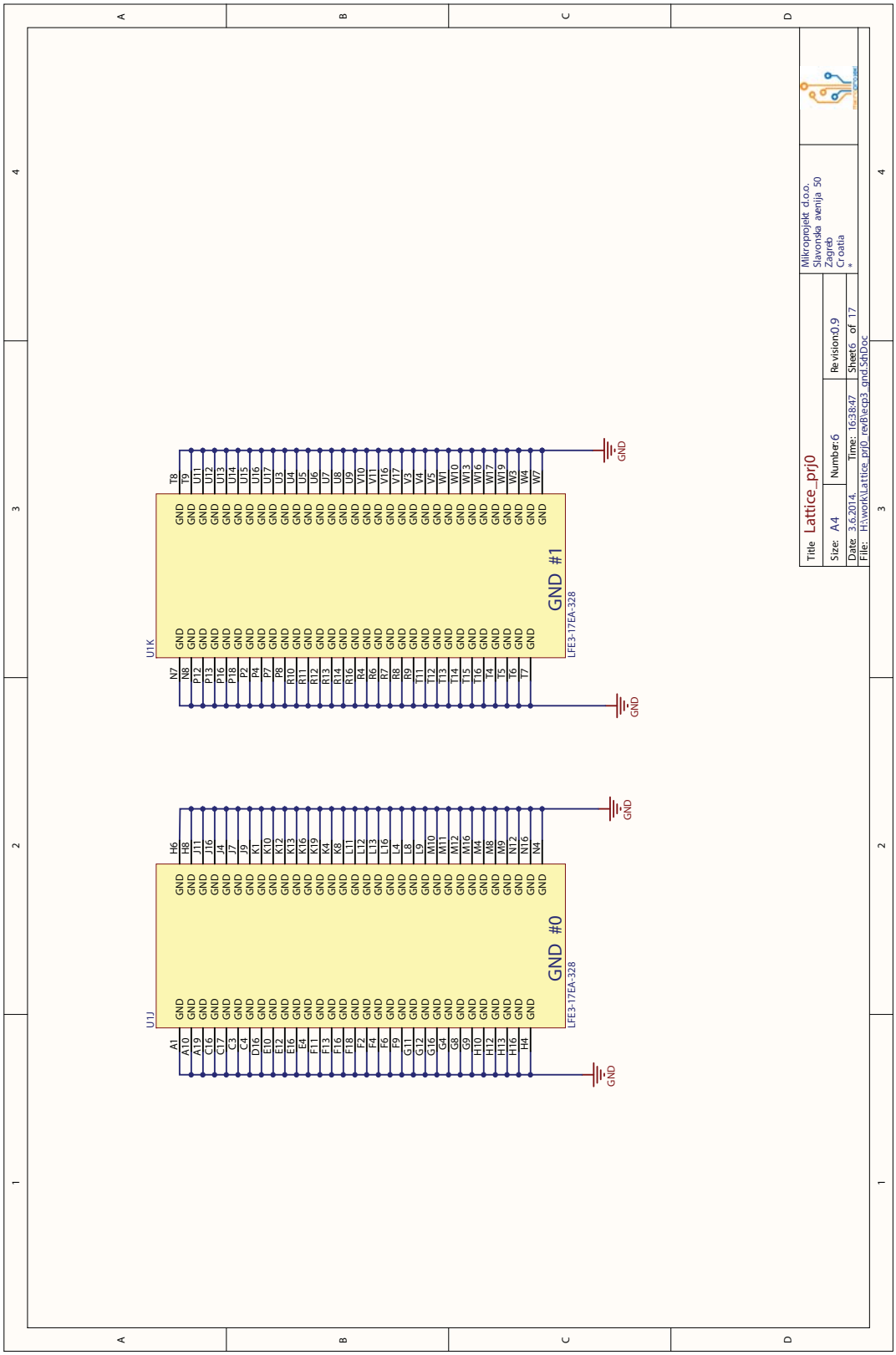


Figure 17. Sheet 7 of 17

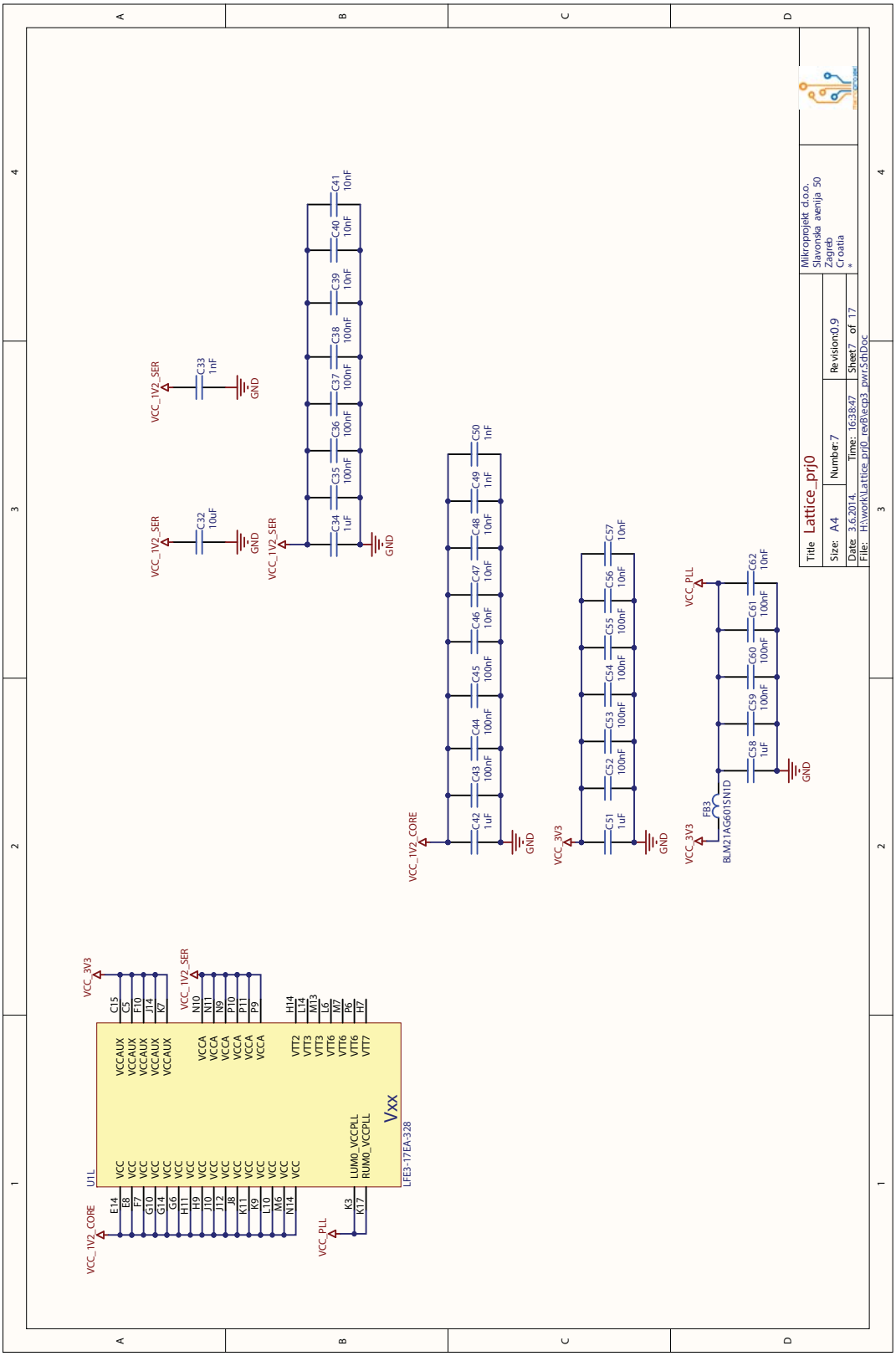


Figure 18. Sheet 8 of 17

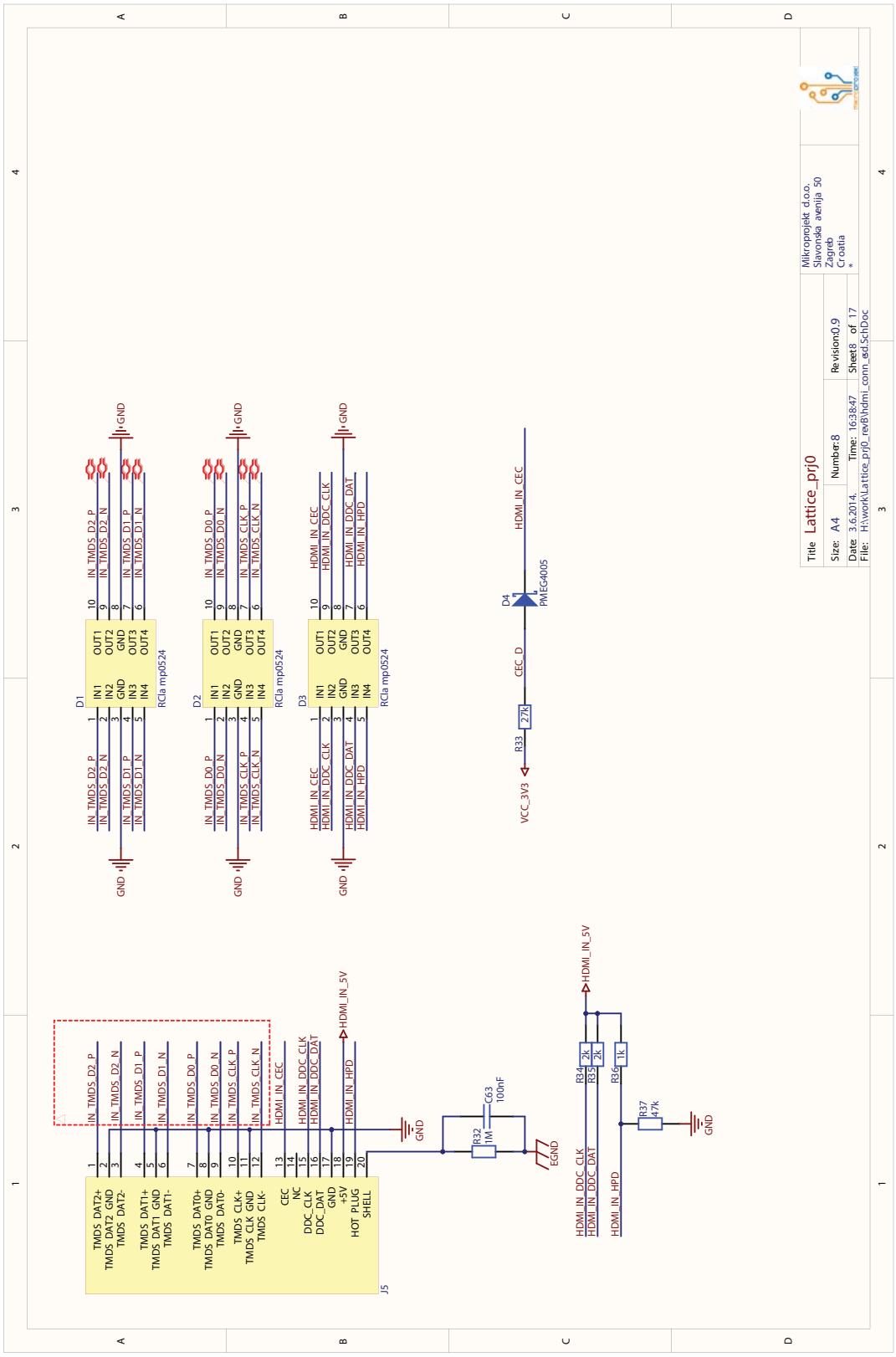


Figure 19. Sheet 9 of 17

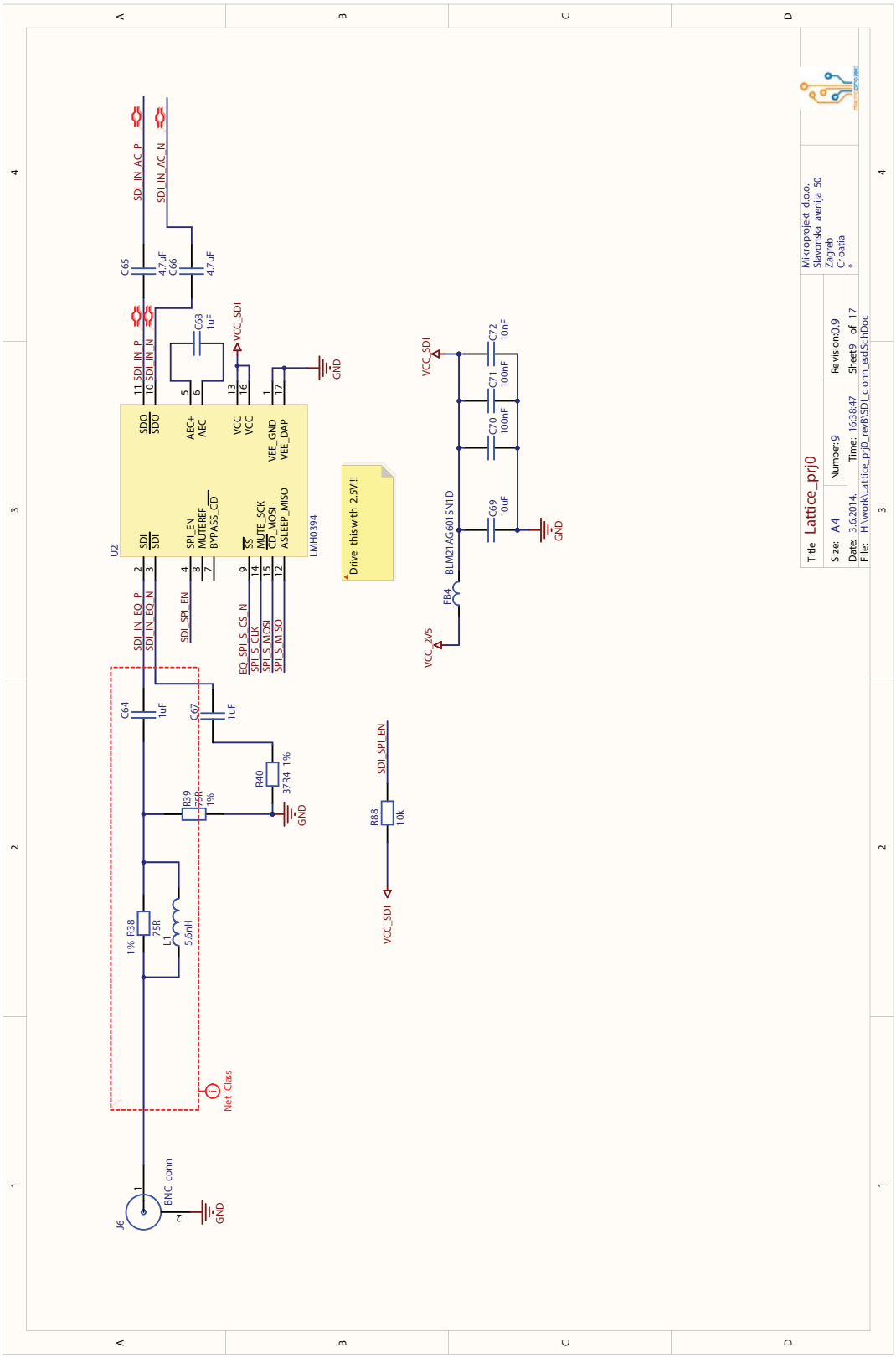


Figure 20. Sheet 10 of 17

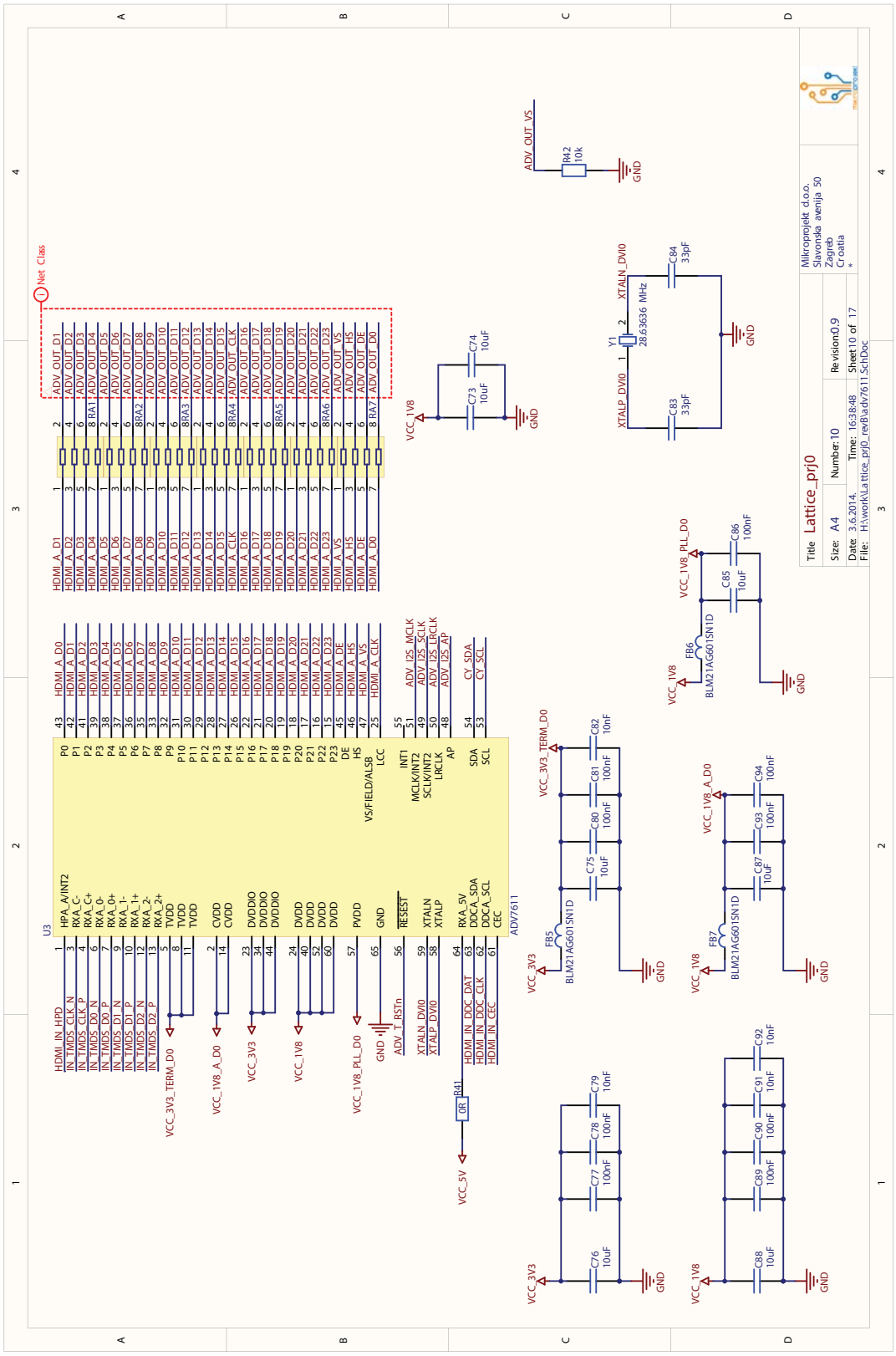


Figure 21. Sheet 11 of 17

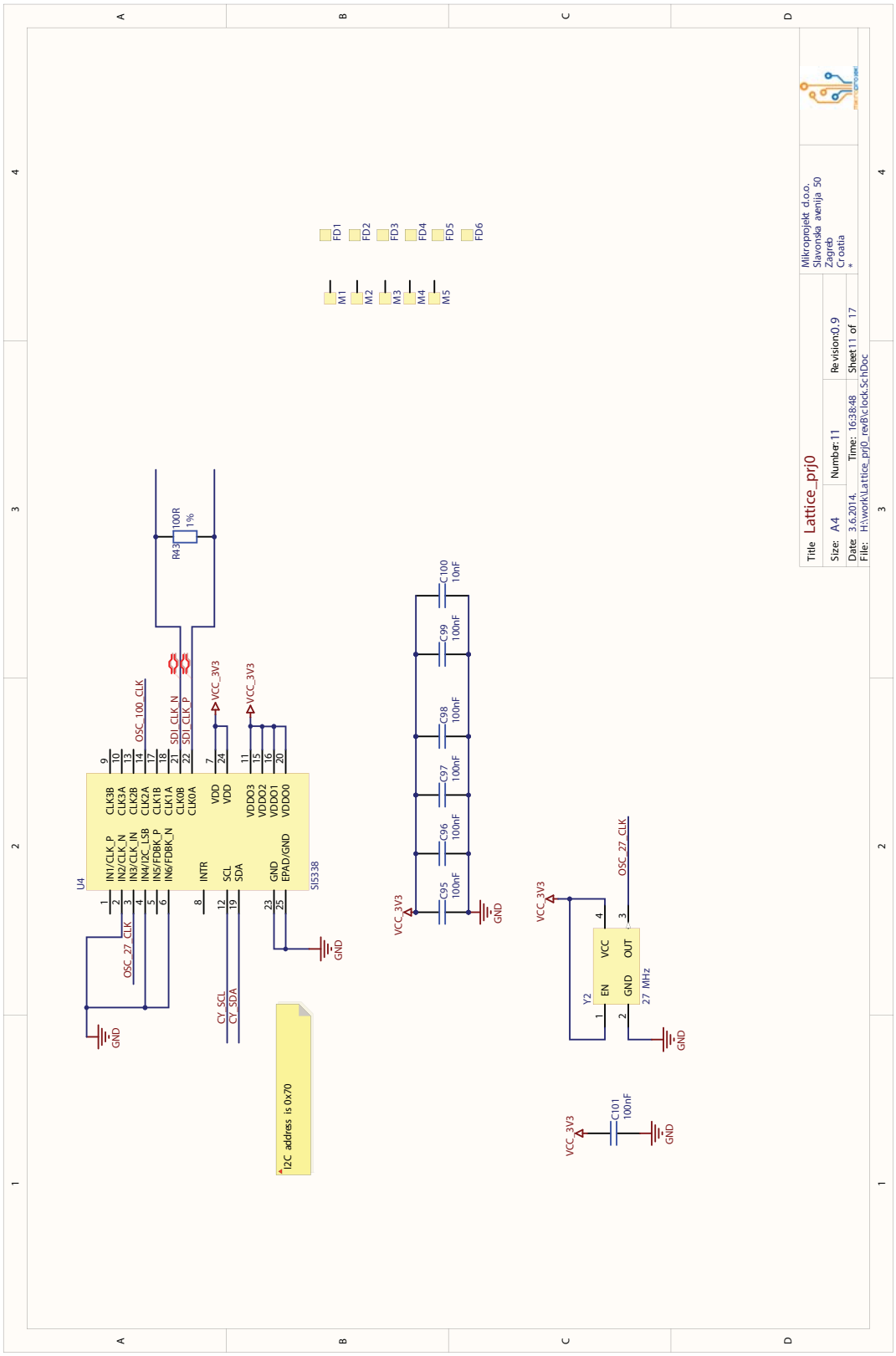


Figure 22. Sheet 12 of 17

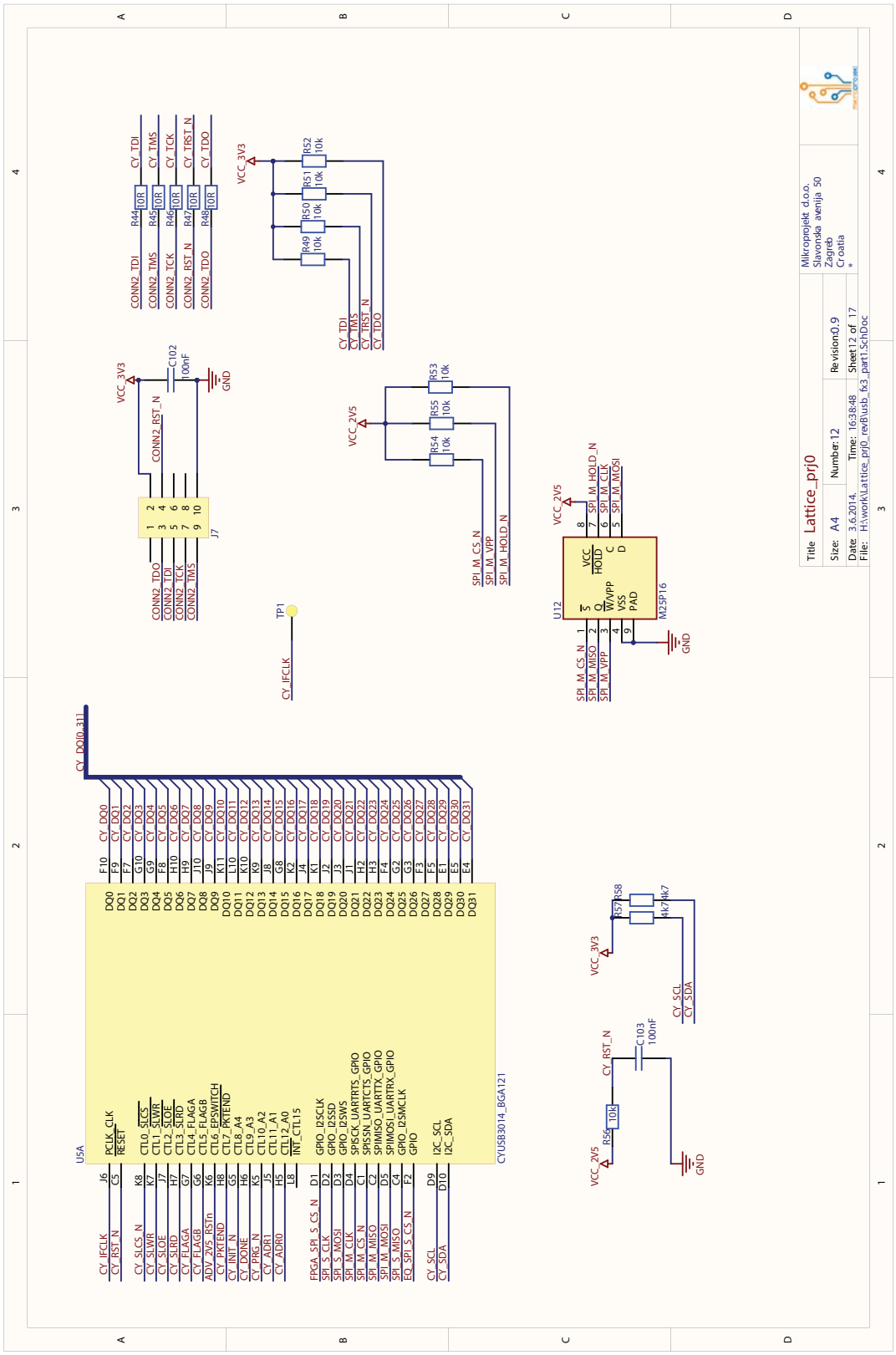


Figure 23. Sheet 13 of 17

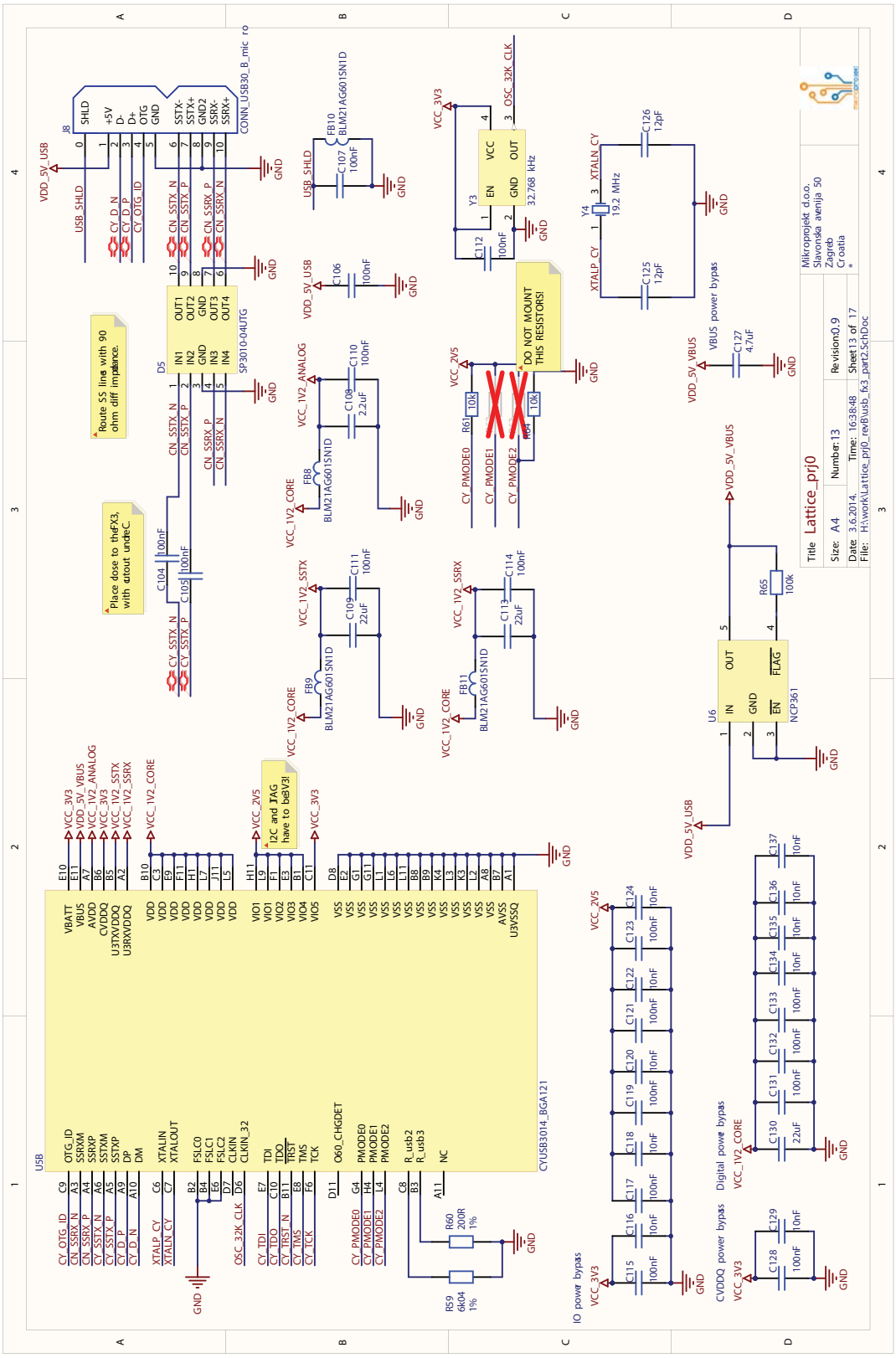


Figure 24. Sheet 14 of 17

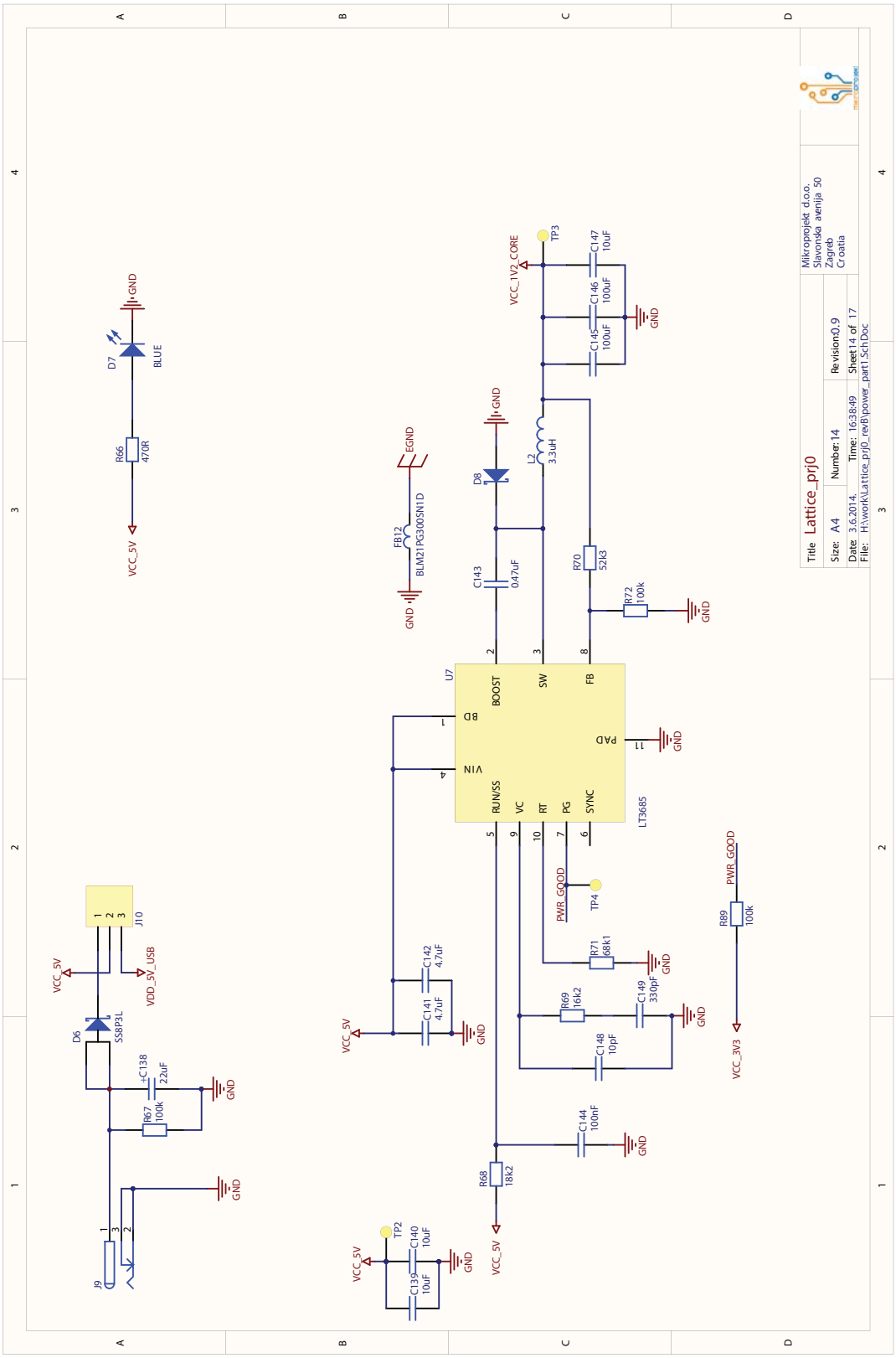


Figure 25. Sheet 15 of 17

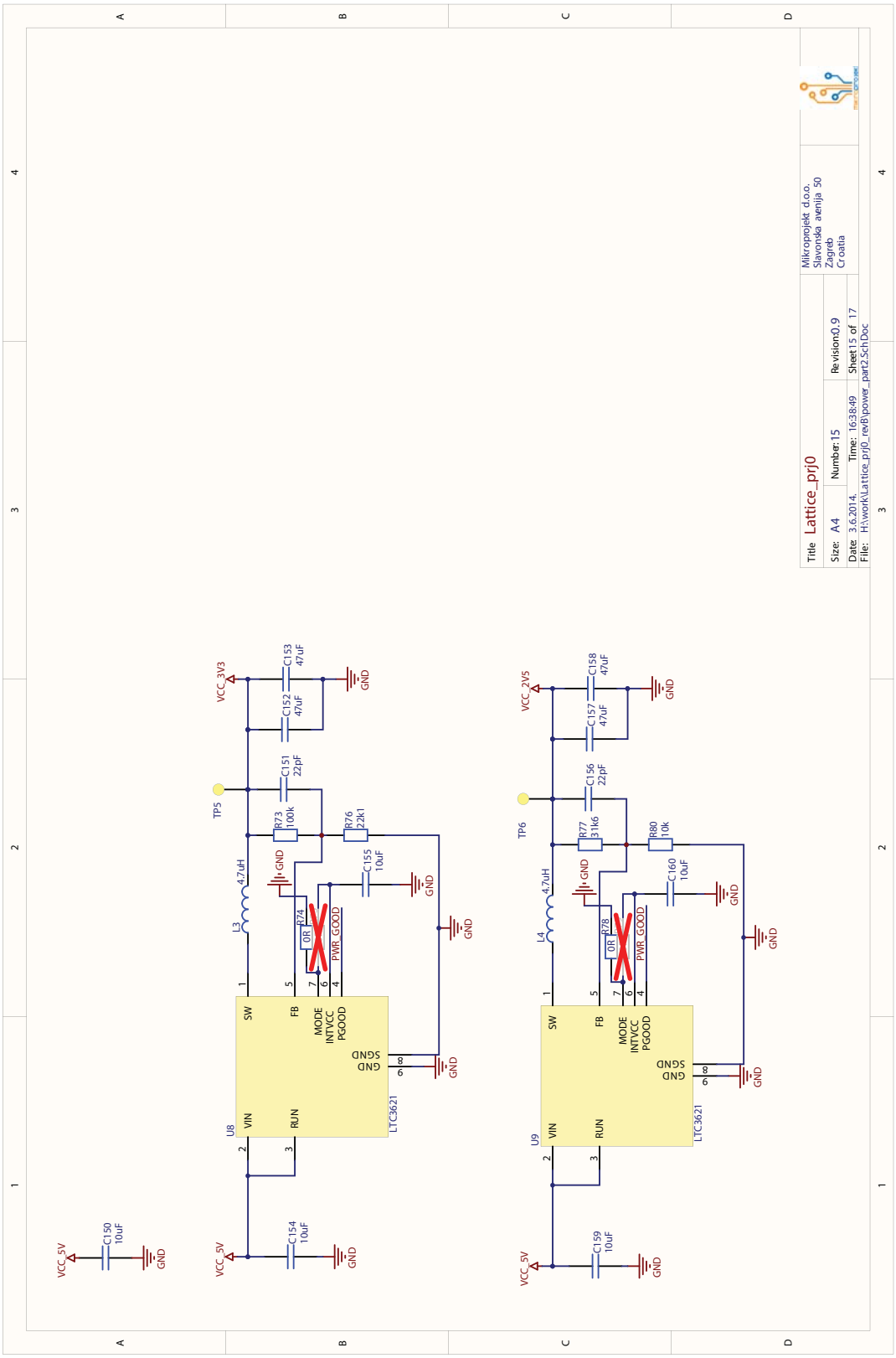


Figure 26. Sheet 16 of 17

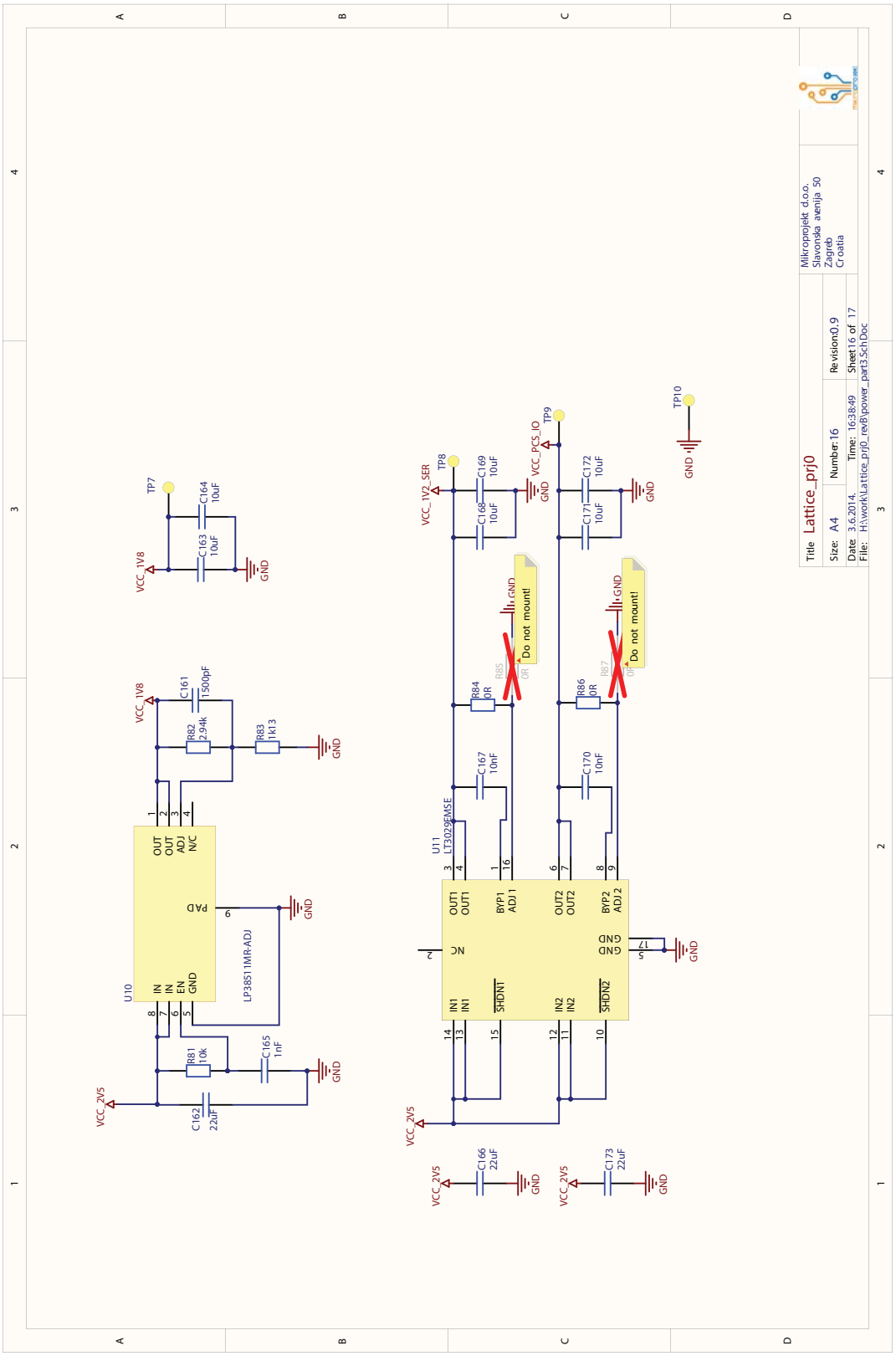


Figure 27. Sheet 17 of 17

Appendix B. Bill of Materials

Table 10. Bill of Materials

Reference	Quantity	Part Number	Manufacturer	Description	Value
U3	1	DV7611BSWZ-P	Analog	Low Power 165 MHz HDMI Receiver	
J6	1	0731713356	Molex	BNC connector	
C1, C2, C7, C10, C13, C15, C19, C21, C25, C26, C30, C34, C42, C51, C58	15	LMK107B7105KA-T	Taiyo Yuden	Capacitor	1uF
C108	1	LMK212BJ225KD-T	Taiyo Yuden	Capacitor	2.2uF
C125, C126	2	CC0402JRNPO9BN120	Yageo	Capacitor	12pF
C127, C141, C142	3	LMK212BJ475KD-T	Taiyo Yuden	Capacitor	4.7uF
C139, C140, C150, C154, C155, C159, C160	7	TMK316B7106KL-TD	Taiyo Yuden	Capacitor	10uF
C143	1	UMK107B7474KA-TR	Taiyo Yuden	Capacitor	0.47uF
C145, C146	2	JMK325BJ107MM-T	Taiyo Yuden	Capacitor	100uF
C148	1	CC0402JRNPO9BN100	Yageo	Capacitor	10pF
C149	1	C1005X7R1H331K	TDK Corporation	Capacitor	330pF
C151, C156	2	CC0402JRNPO9BN220	Yageo	Capacitor	22pF
C152, C153, C157, C158	4	LMK316BJ476ML-T	Taiyo Yuden	Capacitor	47uF
C161	1	CC0402KRX7R9BB152	Yageo	Capacitor	1500pF
C167, C170	2	GRM155R71C103KA01D	Murata Electronics	Capacitor	10nF
C17, C23, C109, C113, C130, C162, C166, C173	8	C2012X5R1A226M/1.25	TDK Corporation	Capacitor	22uF
C3, C6, C8, C12, C14, C16, C20, C22, C28, C29, C31, C35, C36, C37, C38, C43, C44, C45, C52, C53, C54, C55, C59, C60, C61, C63, C70, C71, C77, C78, C80, C81, C86, C89, C90, C93, C94, C95, C96, C97, C98, C99, C101, C102, C103, C104, C105, C106, C107, C110, C111, C112, C114, C115, C117, C119, C121, C123, C128, C131, C132, C133, C144	63	GRM155R71C104KA88D	Murata Electronics	Capacitor	100nF

Reference	Quantity	Part Number	Manufacturer	Description	Value
C32, C69, C73, C74, C75, C76, C85, C87, C88, C147, C163, C164, C168, C169, C171, C172	16	LMK212BJ106KG-T	Taiyo Yuden	Capacitor	10uF
C33, C49, C50, C165	4	0402YC102KAT2A	AVX Corporation	Capacitor	1nF
C4, C5, C9, C11, C18, C24, C27, C39, C40, C41, C46, C47, C48, C56, C57, C62, C72, C79, C82, C91, C92, C100, C116, C118, C120, C122, C124, C129, C134, C135, C136, C137	32	GRM155R71C103KA01D	Murata Electronics	Capacitor	10nF
C64, C67, C68	3	04026D105KAT2A	Avex	Capacitor	1uF
C65, C66	2	C1005X5R0J475M050BC	TDK	Capacitor	4.7uF
C83, C84	2	CC0402JRNPO9BN330	Yageo	Capacitor	33pF
C138	1	EEEFK1V220R	Panasonic Electronic Components	Capacitor Polarized	22uF
J9	1	PJ-002A	CUI Inc	Barrel Connector - Low Voltage Power Supply Connector	
J3, J10	2	825433-3	TE Connectivity		
J2	1	67996-206HLF	FCI		
J4	1	1-87224-0	TE Connectivity		
J7	1	826925-5	TE Connectivity	Header 2x5 WAYs	
J8	1	USB3110-30-A	Global Connector Technology	USB 3.0, B micro	
U5	1	CYUSB3014-BZXC	Cypress	Cypress USB 3.0 Device, 121-ball BGA	
D8	1	DFLS240L-7	Diodes Inc	Schottky Rectifier	
FB1, FB2, FB3, FB4, FB5, FB6, FB7, FB8, FB9, FB10, FB11	11	BLM21AG601SN1D	Murata Electronics		
FB12	1	BLM21PG300SN1D	Murata Electronics		
J5	1	0471511001	Molex	HDMI Connector	
L1	1	LQP15MN5N6B02D	Murata	Inductor	5.6nH
L2	1	NRS8030T3R3MJGJ	Taiyo Yuden	Inductor	3.3uH
L3, L4	2	NRS6028T4R7MMGK	Taiyo Yuden	Inductor	4.7uH
D7	1	KP-3216PBC	Kingbright	LED	
U1	1	LFE3-17EA-6MG328C	Lattice	LFE3-17EA-328	
U2	1	LMH0394SQ	Texas Instruments	SDI equalizer	

Reference	Quantity	Part Number	Manufacturer	Description	Value
U10	1	LP38511MR-ADJ	National Semiconductor	LP38511MR-ADJ 3A Fast-Transient Response Adjustable Low-Dropout Linear	
U11	1	LT3029EMSE#PBF	Linear Technology	Dual 500 mA/500 mA Low Dropout, Low Noise, Micropower Linear Regulator	
U7	1	LT3685EMSE#PBF	Linear Technology	36V, 2A 2.4 MHz Step-Down Switching Regulator	
U8, U9	2	LTC3621EMS8E-2#PBF	Linear Technology	17V, 1A Synchronous Step-Down Regulator	
U12	1	M25PX16-VMP6TG	Micron Technology Inc	Numonyx SPI FLASH, 16 MBit	
J1	1	52559-3652	Molex	FFC/FPC Connector, Vertical, SMT, ZIF, 36 Circuits	
U6	1	NCP361SNT1G	ON Semi	USB Positive Overvoltage Protection Controller with Internal PMOS FET and Overcurrent Protection	
Y2	1	7C-27.000BB-T	TXC Corporation	Oscillator	
Y3	1	7XZ-32.768KBE-T	TXC	Oscillator	
D4	1	PMEG4005EJ,115	NXP Semiconductors	Schottky Rectifier	
D1, D2, D3	3	RCLAMP0524PATCT	Semtech	Ultra Low Capacitance TVS Arrays	
R1, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R42, R49, R50, R51, R52, R53, R54, R55, R56, R61, R64, R80, R81, R88	27	CRCW040210K0FKED	Vishay Dale	RESISTOR	10k
R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R44, R45, R46, R47, R48	15	RC0402JR-0710RL	Yageo	RESISTOR	10R
R32	1	ERJ-2GEJ105X	Panasonic Electronic Components	RESISTOR	1M
R33	1	CRCW040227K0FKED	Vishay Dale	RESISTOR	27k
R34, R35	2	CRCW04022K00JNED	Vishay Dale	RESISTOR	2k
R36	1	CRCW04021K00FKED	Vishay Dale	RESISTOR	1k
R37	1	CRCW040247K0FKED	Vishay Dale	RESISTOR	47k
R38, R39	2	CRCW040275R0FKED	Vishay	RESISTOR	75R
R40	1	CRCW040237R4FKED	Vishay	RESISTOR	37R4
R43	1	ERJ-2RKF1000X	Panasonic Electronic Components	RESISTOR	100R

Reference	Quantity	Part Number	Manufacturer	Description	Value
R57, R58	2	CRCW04024K70FKEAHP		RESISTOR	4k7
R59	1	CRCW04026K04FKED	Vishay	RESISTOR	6k04
R6, R7, R8, R9, R41, R74, R78, R84, R86	9	CRCW04020000Z0ED	Vishay Dale	RESISTOR	0R
R60	1	CRCW0402200RFKED	Vishay	RESISTOR	200R
R65, R72	2	ERA-2AED104X	Panasonic Electronic Components	RESISTOR	100k
R66	1	CRCW0603470RFKEA	Vishay	RESISTOR	470R
R67, R89	2	ERJ-3GEYJ104V	Panasonic Electronic Components	RESISTOR	100k
R68	1	ERJ-2RKF1822X	Panasonic Electronic Components	RESISTOR	18k2
R69	1	ERJ-2RKF1622X	Panasonic Electronic Components	RESISTOR	16k2
R70	1	ERJ-2RKF5232X	Panasonic Electronic Components	RESISTOR	52k3
R71	1	ERJ-2RKF6812X	Panasonic Electronic Components	RESISTOR	68k1
R73	1	CRCW0402100KFKED	Vishay Dale	RESISTOR	100k
R76	1	CRCW040222K1FKED	Vishay Dale	RESISTOR	22k1
R77	1	CRCW040231K6FKED	Vishay Dale	RESISTOR	31k6
R82	1	ERJ-2RKF2941X	Panasonic Electronic Components	RESISTOR	2.94k
R83	1	ERJ-2RKF1131X	Panasonic Electronic Components	RESISTOR	1k13
RA1, RA2, RA3, RA4, RA5, RA6, RA7	7	EXBN8V220JX	Panasonic Electronic Components	Resistor array (4 resistors)	
U4	1	SI5338C-A-GM	Silicon Laboratories Inc	SI5338A/B/C clock synthesizer	
D5	1	SP3010-04UTG	Littelfuse	Low Capacitance TVS Arrays	
D6	1	SS8P3L-M3/86A	Vishay General Semiconductor	High Current Density Schottky Rectifier	
Y1	1	7A-28.63636MAAJ-T	TXC Corporation	Crystal	
Y4	1	7B-19.200MAAJ-T		Crystal	

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