CrossLink LIF-MD6000 Master Link Board - Revision B

Evaluation Board User Guide

FPGA-EB-02010 Version 1.5

June 2018

Contents

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
CMOS	Complementary Metal-Oxide Semiconductor
CSI-2	Camera Serial Interface
DSI	Display Serial Interface
FTDI	Future Technology Devices International
I^2C	Inter-Integrated Circuit
IO	Input/Output
LVDS	Low-Voltage Differential Signaling
MIPI	Mobile Industry Processor Interface
SPI	Serial Peripheral Interface

1. Introduction

This document describes the Lattice Semiconductor CrossLink™ LIF-MD6000 Master Link Board – Revision B that supports a variety of demos, encompassing different signaling logic standards bridging with MIPI® CSI-2/DSI interface. The board's key component is the CrossLink Family device that features built in MIPI D-PHY hard blocks to support different bridging solutions.

For the latest information about this board, including optional Tx/Rx Link boards, demo files, further documentation and more, see the Lattice website at: www.latticesemi.com/masterlink

For details about the CrossLink device, refer to CrossLink Family Data Sheet (FPGA-DS-02007)

The content of this user guide includes descriptions of on-board jumper settings, programming circuit, a complete set of schematics, and bill of materials for LIF-MD6000 Master Link Rev B board.

Refer to Appendix A, B, C, D, E, F for the schematics and BOM of the CrossLink LIF-MD6000 Master Link Rev B board and the schematics and BOMs of the Breakout IO Link and SMA IO Link boards that are included in the demo kit.

Circuits on the development kit board:

- Programming Circuit
  - Mini USB Type-B connector to FTDI
  - FTDI to CrossLink using SPI
  - FTDI to XO3LF device using JTAG
- CrossLink
  - MIPI CSI-2/DSI hard block
  - Bridging of multiple signaling standards
  - SPI flash configuration
  - General Purpose Input/Output
  - LED display
- LCMXO3LF-1300E
  - I^2C muxing

Figure 1.1 shows the top view of the LIF-MD6000 Master Link Rev B board and its key components. Figure 1.2 shows the bottom view of the board.

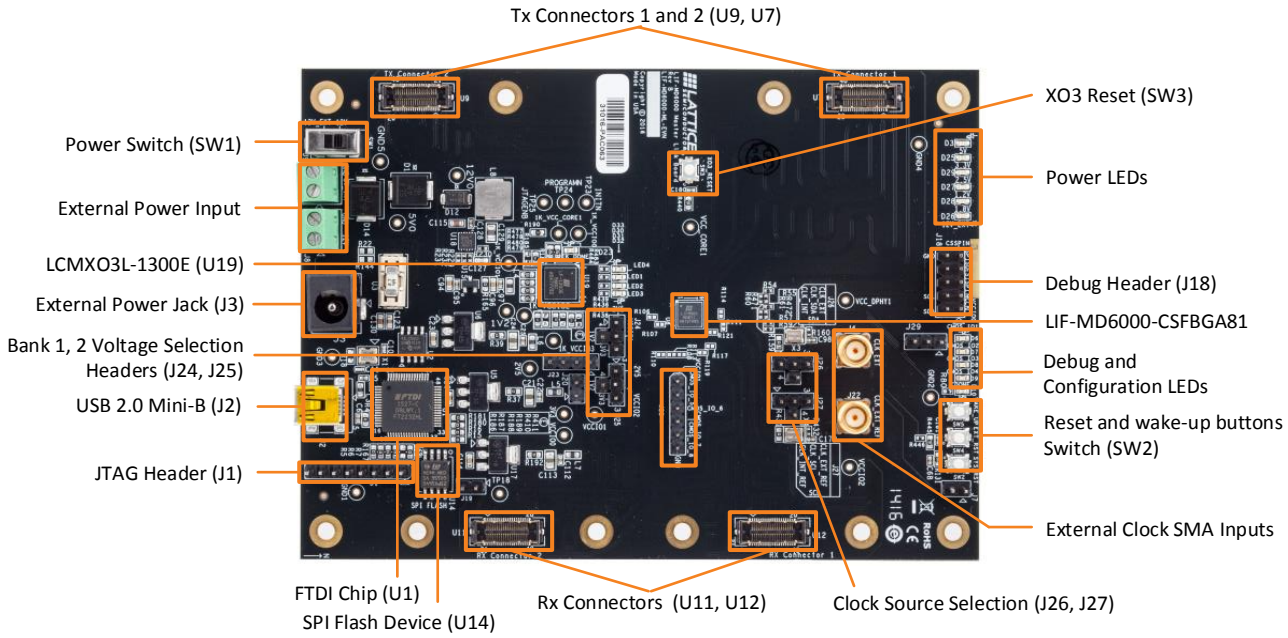


Figure 1.1. Top View of Master Link Rev B Board and its Key Components

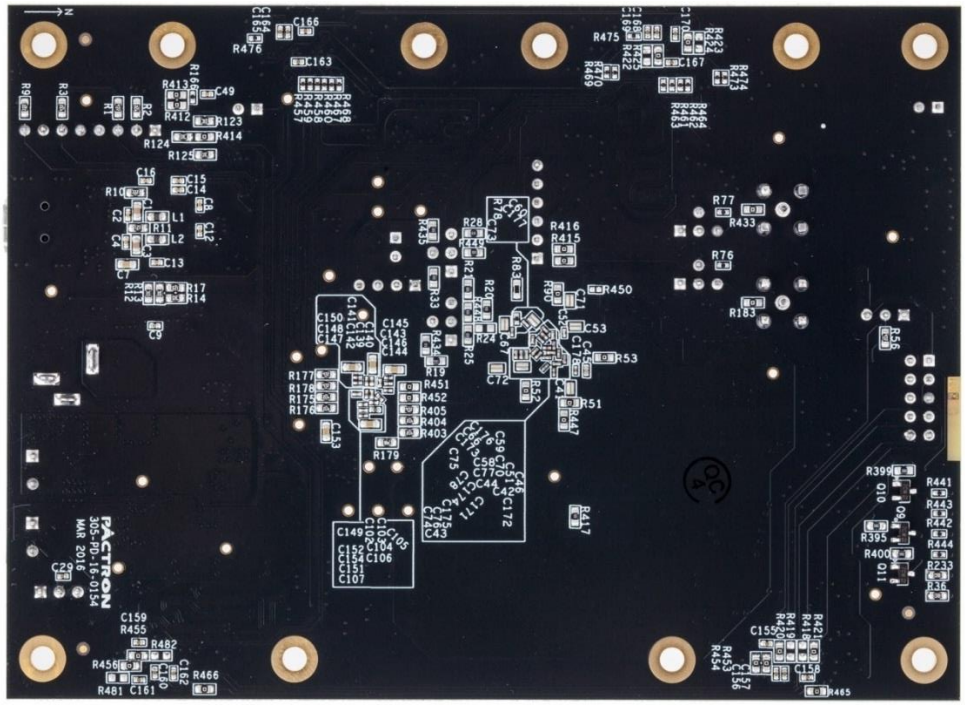


Figure 1.2. Bottom View of Master Link Rev B Board

2. Headers and Test Connections

Figure 1.1 shows the top view of the Master Link Rev B board. The headers and test connections on the board provide access to LIF-MD6000 Master Link demo board circuits. Table 2.1 lists the headers and test connectors.

Table 2.1. Headers and Test Connectors

Part	Description	Setting
J1	External JTAG interface - For LCMX03 only	—
J2	mini-B USB connector	—
J3	External power jack	—
J4	External clock input for MIPI D-PHY reference clock	—
J7	SW2 selector	OPEN-NOP, SHORT-CONFIGURATION RESET
J8	External 12 V terminal block	Open
J9	External 5 V terminal block	Open
J18	External SP/I²C access	—
J19	SPI Flash chip select	OPEN-OFF, SHORT-ON
J20	LIF-MD6000 chip select	OPEN-OFF, SHORT-ON
J22	External reference clock input for MIPI D-PHY reference clock	—
J23	Debug Header for LCMXO3L device	—
J24	VCCIO1 Bank voltage selector	1-2 (2.5 V), 2-3 (3.3 V), 2-4 (1.2 V)
J25	VCCIO2 Bank voltage selector	1-2 (2.5 V), 2-3 (3.3 V), 2-4 (1.2 V)
J26	Internal/External clock and I2C SDA Mux	1-2 (CLK_INT), 2-3 (CLK_EXT), 2-4 (SDA)
J27	Internal/External reference clock and I2C SCL Mux	1-2 (CLK_INT_REF), 2-3 (CLK_EXT_REF), 2-4 (SCL)
J28	Reveal analyzer signal connector	—
J29	Reset signal voltage selector	1-2 (VCCIO2), 2-3 (VCCIO0)
SW1	External adaptor power ON/OFF	—
SW2	Configuration reset for LIF-MD6000	—
SW3	External reset for LCMXO3L device	—
SW4*	External reset for LIF-MD6000 device	—
SW5	PMU WAKEUP Switch	—
U7	Tx Connectors for external interface	—
U9	Tx Connectors for external interface	—
U11	Rx Connectors for external interface	—
U12	Rx Connectors for external interface	—

***Note**: Some CrossLink demos utilize this reset signal to ball G9 of Bank 2 while it is configured as a 1.2 V Bank. However, LVCMOS12 inputs are no longer supported across all 3 Banks. Lattice Diamond® Software 3.9 and later will not allow this signal to be placed on a 1.2 V Bank. If it is necessary to recompile one of these demo projects, the necessary modifications should be made to the project and the board to move this reset signal to a non-1.2 V Bank on CrossLink.

3. Programming Circuit

The Mini-B USB connector is used for programming the board by using Lattice Diamond Programmer software. Figure 3.1 shows the programming block of LIF-MD6000 Master Link Rev B board.

The Mini-B USB connector interfaces to the FTDI FT2232H IC. The FTDI IC works with Diamond programmer software to provide interfaces for:

- JTAG – to program MachXO3 LCMXO3LF-1300E
- SPI – to program both CrossLink, and SPI Flash Memory

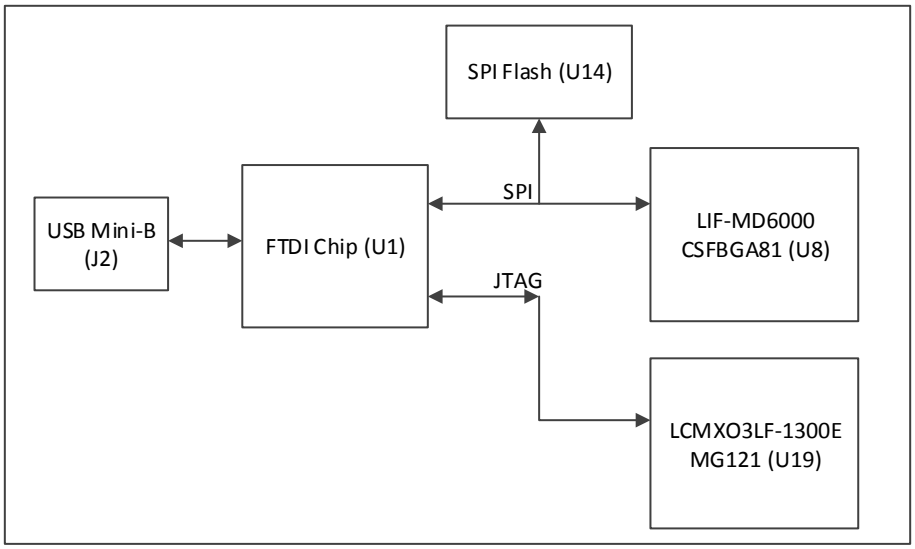


Figure 3.1. Programming Block

3.1. Bridging Circuit

Figure 3.2 shows the block diagram of bridging of different standard interfaces. The CrossLink device is used as a bridging device that supports a variety of I/O standards. This demo board supports development of the following interface bridges:

- 1:1 MIPI DSI Display Interface Bridge
- 1:2 MIPI DSI Display Interface Bridge
- 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge
- CMOS to MIPI CSI-2 Image Sensor Interface Bridge
- MIPI CSI-2 to CMOS Image Sensor Interface Bridge
- MIPI DSI to CMOS Display Interface Bridge
- OpenLDI LVDS to MIPI DSI Display Interface Bridge
- CMOS to MIPI DSI Display Interface Bridge

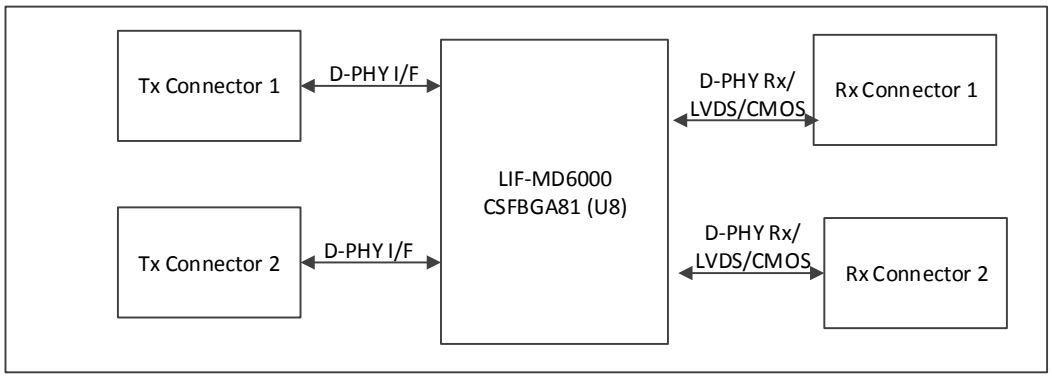


Figure 3.2. Bridging Block

3.2. I²C Expander

Figure 3.3 shows the block diagram of the I²C expander. The LCMXO3LF-1200E device is used as an I²C expander and it supports a single master and multiple slave devices connected to the board. The master I²C interface is connected to the Tx header and the slave device I²C interface is connected to the Rx connectors supporting any slave device access from the master based on the slave address.

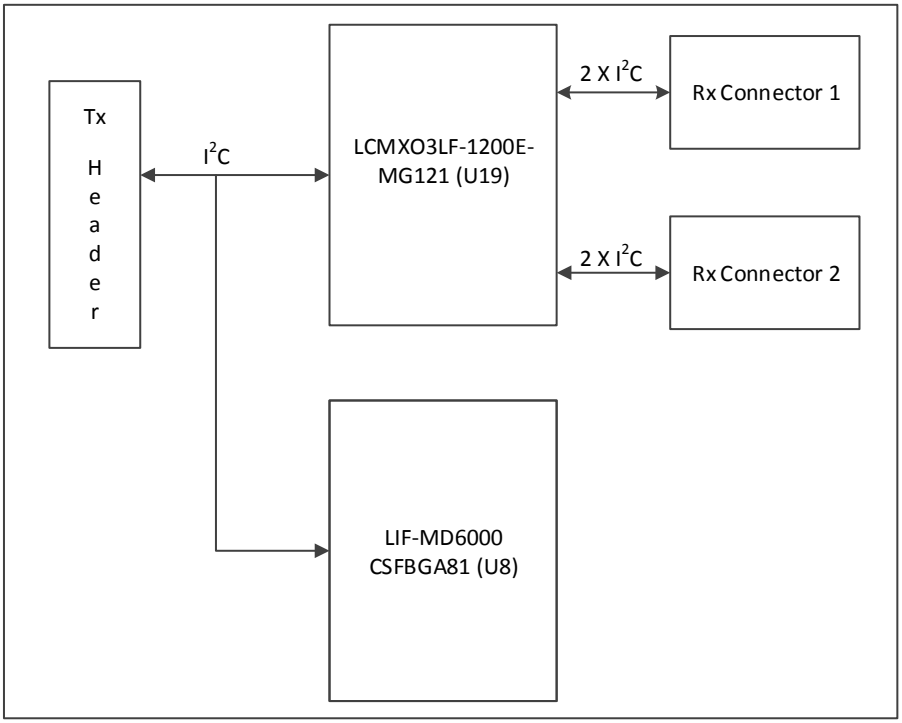


Figure 3.3. I²C Expander Block

4. Power Supply

The power supply to the development kit is provided by the Mini-B USB connector or from an external adaptor.

Figure 4.1 shows the power supply block of the CrossLink LIF-MD6000 Master Link Rev B board. The external adaptor provides 12 V power source through voltage regulators on the board to CrossLink and LCMXO3LF-1300E, as well as to the external boards connected to Tx and Rx Headers. The Mini-B USB connector provides 5 V to the various voltage regulators and is also used for device programming. Each I/O and core voltage rail on the board is accessible by a test point on the board. The current flowing to each rail can be measured using a 1 Ω resistor placed in the path of each voltage rail.

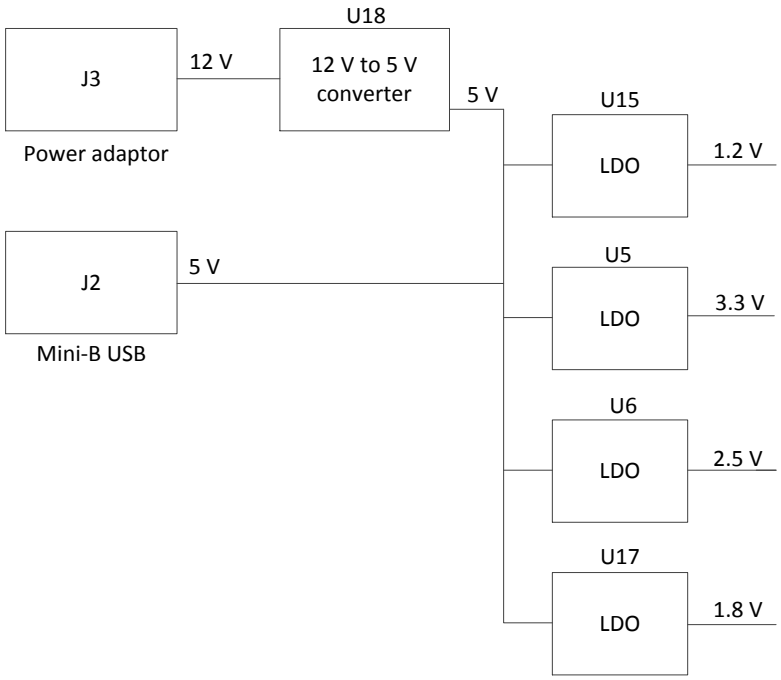


Figure 4.1. Power Supply Block

Table 4.1 lists the device power rails. There are five voltage regulators on the board used to supply the 5 V, 3.3 V, 2.5V 1.8 V, and 1.2 V rails. The input to these regulators is either from the Mini-B USB connector (J2), an external 12 V adaptor (J3), or an external power supply to the terminal blocks of J8 or J9. Switch SW1 is used to connect or disconnect the external 12 V adaptor power to the board.

Table 4.1. Power LEDs

Voltage Rail	LEDs	Color
12	D26	Green
5	D3	Green
3.3	D25	Green
2.5	D29	Green
1.8	D28	Green
1.2	D27	Green

Table 4.2 lists the board voltage rails, including the rail source voltage, test point number, and current sense resistor number.

Table 4.2. Device Power Rail Summary and Test Points

Voltage Rail	Source Rail	Current Sense Resistor	Test Points
12 V	—	—	12V0
5 V	12 V	—	5V0
+3.3 V	5 V	—	3V3
+2.5 V	5 V	—	2V5
+1.8 V	5 V	—	—
+1.2 V	5 V	—	1V2
VCCCORE	+1.2 V	R19	VCC_CORE1
VCCIO0	+2.5 V/+3.3 V	R20/R24	VCCIO0
VCCIO1	+1.2 V/+2.5 V/+3.3 V	R21/R25/R434/R448	VCCIO1
VCCIO2	+1.2 V/+2.5 V/+3.3 V	R28/R33/R435/R449	VCCIO2
VCC_DPHY	+1.2 V	R417	VCC_DPHY
1K_VCC_CORE	1.2 V	R190	1K_VCC_CORE1
1K_VCCIO0	+2.5 V/+3.3 V	R410/R411	1K_VCCIO0
1K_VCCIO1	+2.5 V/+3.3 V	R184/R185	1K_VCCIO1
1K_VCCIO2	+2.5 V/+3.3 V	R186/R187	1K_VCCIO2
1K_VCCIO3	+2.5 V/+3.3 V	R188/R189	1K_VCCIO3

5. Status Indicators

The LED status indicators on the board show power, configuration, and application status. Table 5.1 lists the status LED I/O map.

Table 5.1. Status LED I/O Map

Device	LED	Net Name	Color
CrossLink	D6	CMOS_IO_1	Blue
CrossLink	D7	CMOS_IO_2	Blue
CrossLink	D8	CMOS_IO_3	Blue
CrossLink	D9	CMOS_IO_4	Blue
CrossLink	D10	CDONE	Green
LCMX03LF-1300E	D23	DONE	Red

6. SMA IO Link Board

The SMA IO Link board connects to the CrossLink LIF-MD6000 Master Link Rev B board's Tx or Rx connectors (U7, U9, U11 or U12) and transfers signals to the respective SMA connectors.

Table 6.1. Headers and Test Connectors

Part	Description	Mapping to U1
J1	SMA connector for DCK_TX_P	Pin 1
J2	SMA connector for DCK_TX_N	Pin 2
J3	SMA connector for DATA0_TX_P	Pin 4
J4	SMA connector for DATA0_TX_N	Pin 5
J5	SMA connector for DATA1_TX_P	Pin 7
J6	SMA connector for DATA1_TX_N	Pin 8
J7	SMA connector for DATA2_TX_P	Pin 13
J8	SMA connector for DATA2_TX_N	Pin 14
J9	SMA connector for DATA3_TX_P	Pin 16
J10	SMA connector for DATA3_TX_N	Pin 17
J11	SMA connector for DATA4_TX_P	Pin 24
J12	SMA connector for DATA4_TX_N	Pin 25
J13	SMA connector for DATA5_TX_P	Pin 27
J14	SMA connector for DATA5_TX_N	Pin 28
U1	Connector to interface to CrossLink Master Link Rev B board	N/A

Table 6.2. U1 Connector Description

Pin	Name
1	CH4_DCK_P
2	CH4_DCK_N
3	GND
4	CH4_DATA0_P
5	CH4_DATA0_N
6	GND
7	CH4_DATA1_P
8	CH4_DATA1_N
9	GND
10	SN
11	SCLK
12	GND
13	CH4_DATA2_P
14	CH4_DATA2_N
15	GND
16	CH4_DATA3_P
17	CH4_DATA3_N
18	GND
19	12V
20	12V

Pin	Name
21	TBD
22	RESETN
23	PWR_5-0V
24	GND
25	GND
26	PWR_3-3V
27	GND
28	GND
29	PWR_1-8V
30	MOSI
31	MISO
32	PWR_1-8V
33	GND
34	GND
35	PWR_3-3V
36	GND
37	GND
38	PWR_5-0V
39	SDA
40	SCL

Note: U1 connector pin names may be different than the actual signal depending on which CrossLink LIF-MD6000 Master Link Rev B board connector this daughter board is connected to.

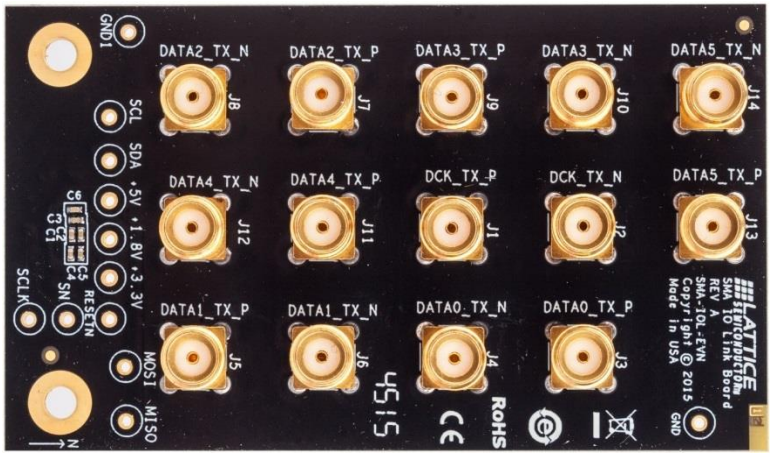


Figure 6.1. Top View of SMA IO Link Board

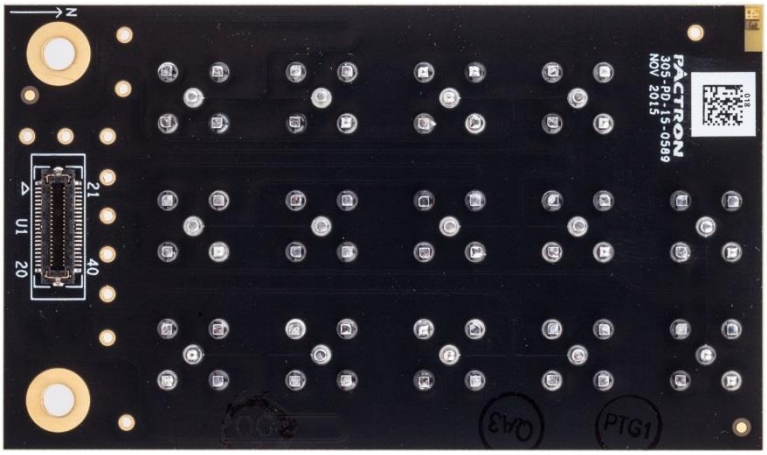


Figure 6.2. Bottom View of SMA IO Link Board

7. Breakout IO Link Board

The Breakout IO Link board connects to the CrossLink LIF-MD6000 Master Link Rev B board's Tx or Rx connectors (U7, U9, U11 or U12) and transfers signals to the 26-pin header (J2).

Table 7.1. Headers and Test Connectors

Part	Description	Setting
J2	13x2 Header	—
U1	Connector to interface to CrossLink Master Link Rev B board	—

Table 7.2. U1 Connector Description

Pin	Name
1	CH4_DCK_P
2	CH4_DCK_N
3	GND
4	CH4_DATA0_P
5	CH4_DATA0_N
6	GND
7	CH4_DATA1_P
8	CH4_DATA1_N
9	GND
10	SN
11	SCLK
12	GND
13	CH4_DATA2_P
14	CH4_DATA2_N
15	GND
16	CH4_DATA3_P
17	CH4_DATA3_N
18	GND
19	12V
20	12V

Pin	Name
21	TBD
22	RESETN
23	PWR_5-0V
24	GND
25	GND
26	PWR_3-3V
27	GND
28	GND
29	PWR_1-8V
30	MOSI
31	MISO
32	PWR_1-8V
33	GND
34	GND
35	PWR_3-3V
36	GND
37	GND
38	PWR_5-0V
39	SDA
40	SCL

Note: U1 connector pin names may be different than the actual signal depending on which CrossLink LIF-MD6000 Master Link Rev B board connector this daughter board is connected to.

Table 7.3. J2 Header Description

Pin	Name	Mapping to U1
1	+3.3V	N/A
2	+1.8V	N/A
3	RESETN	Pin 22
4	CH4_DCK_TX_P	Pin 1
5	SDA	Pin 39
6	CH4_DCK_TX_N	Pin 2
7	SCL	Pin 40
8	GND	N/A
9	GND	N/A
10	CH4_DATA0_TX_P	Pin 4
11	CH4_DATA3_TX_P	Pin 16
12	CH4_DATA0_TX_N	Pin 5
13	CH4_DATA3_TX_N	Pin 17
14	GND	N/A
15	GND	N/A
16	CH4_DATA1_TX_P	Pin 7
17	CH4_DATA4_TX_P	Pin 24
18	CH4_DATA1_TX_N	Pin 8
19	CH4_DATA4_TX_N	Pin 25
20	GND	N/A
21	GND	N/A
22	CH4_DATA2_TX_P	Pin 13
23	CH4_DATA5_TX_P	Pin 27
24	CH4_DATA2_TX_N	Pin 14
25	CH4_DATA5_TX_N	Pin 28
26	GND	N/A

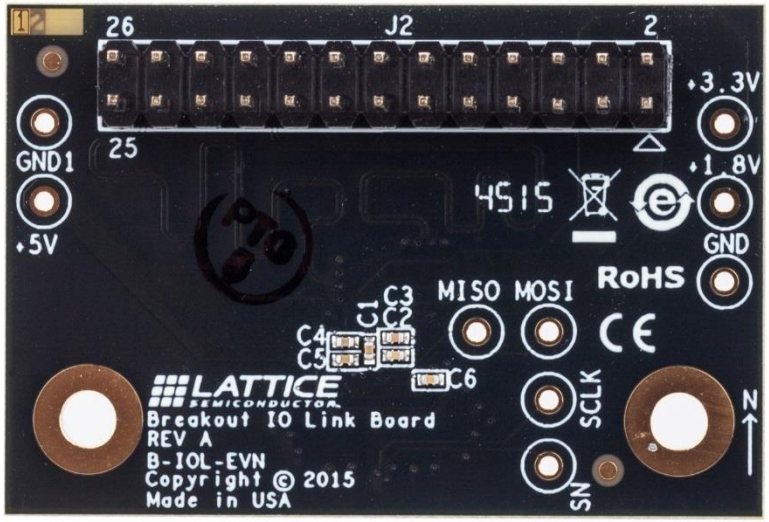


Figure 7.1. Top View of Breakout IO Link Board

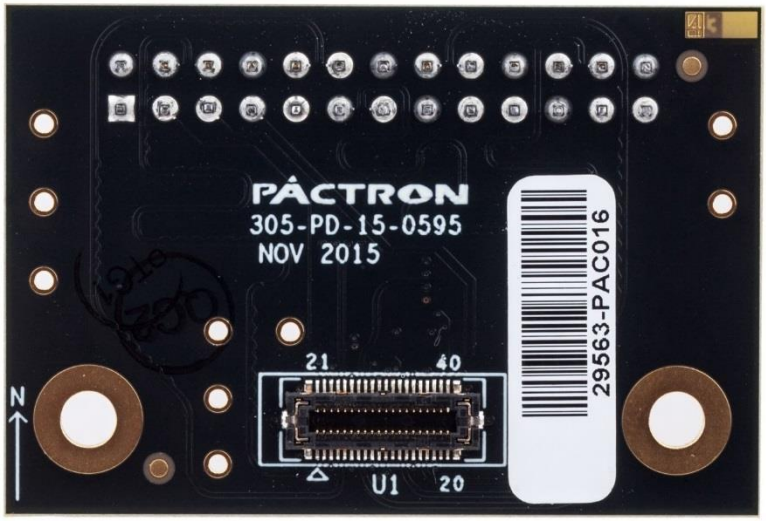


Figure 7.2. Bottom View of Breakout IO Link Board

8. Ordering Information

Table 8.1. Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
CrossLink: LIF-MD6000 Master Link Rev B board (Includes 1 SMA IO Link Board and 1 Breakout IO Link Board)	LIF-MD6000-ML-EVN	
CrossLink: LIF-MD6000 IO Link Boards (Includes 1 SMA IO Link Board and 1 Breakout IO Link Board)	LIFMD-IOL-EVN	

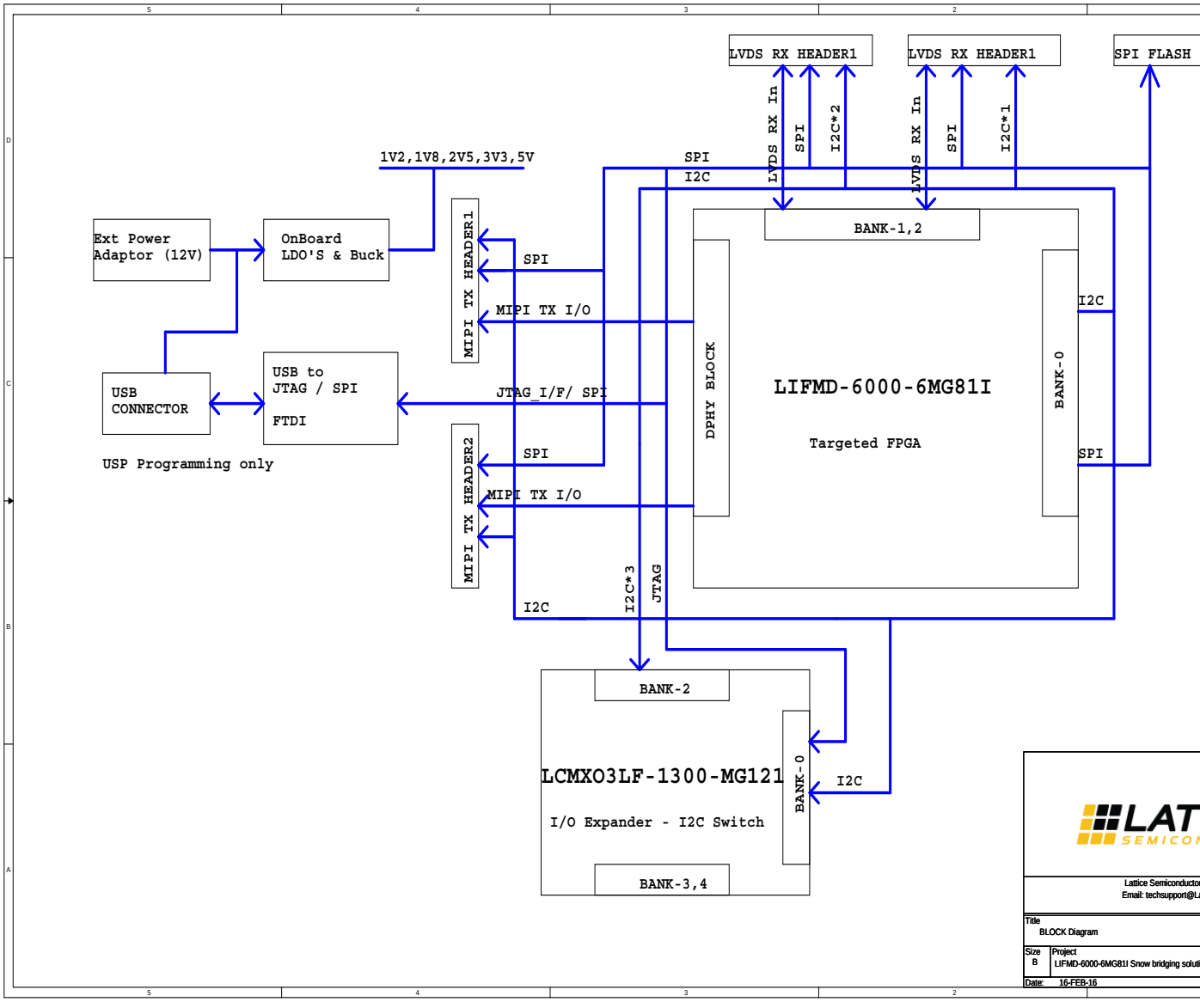
References

For more information, refer to FPGA-DS-02007 (previously DS1055), CrossLink Family Data Sheet

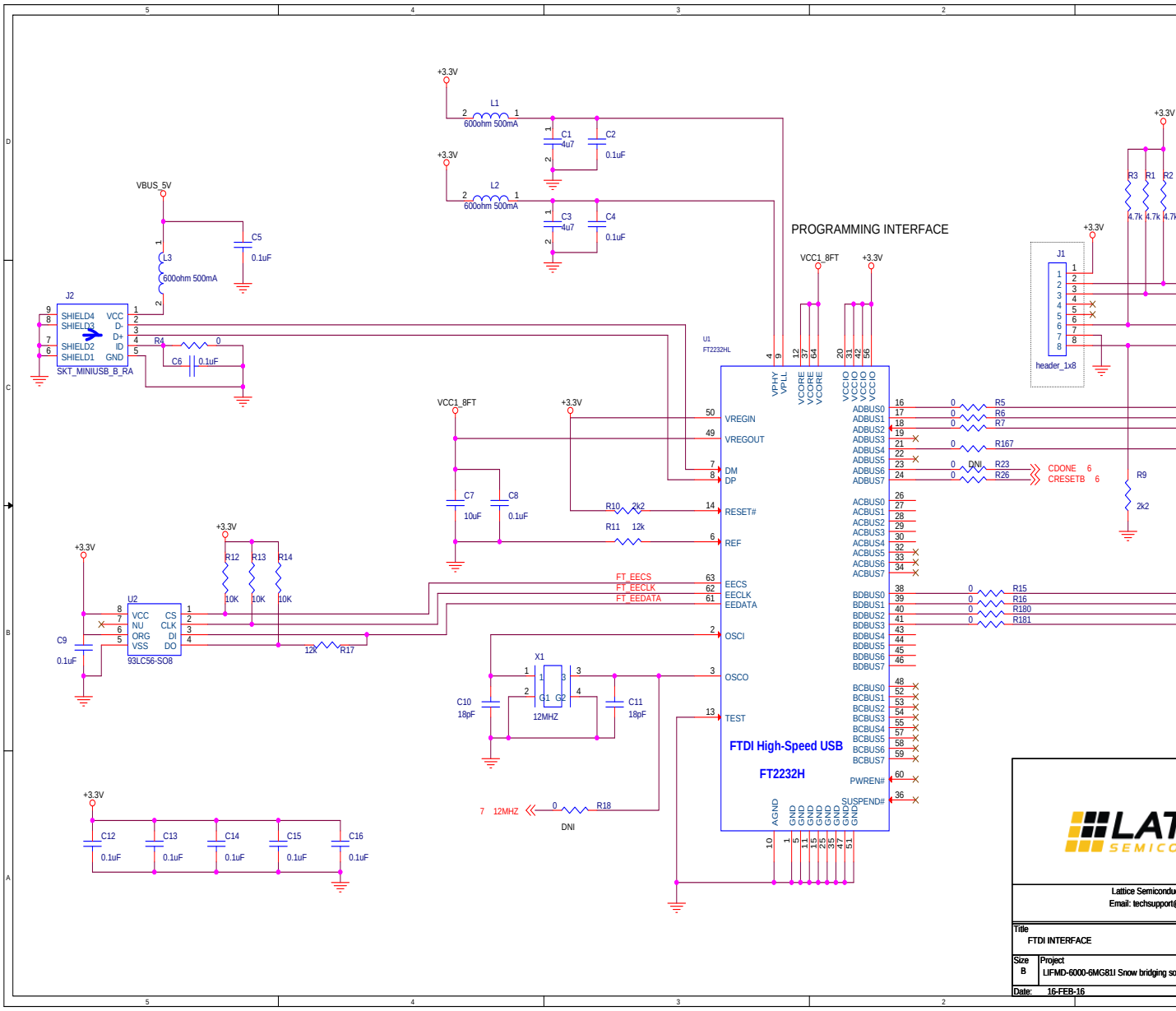
Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

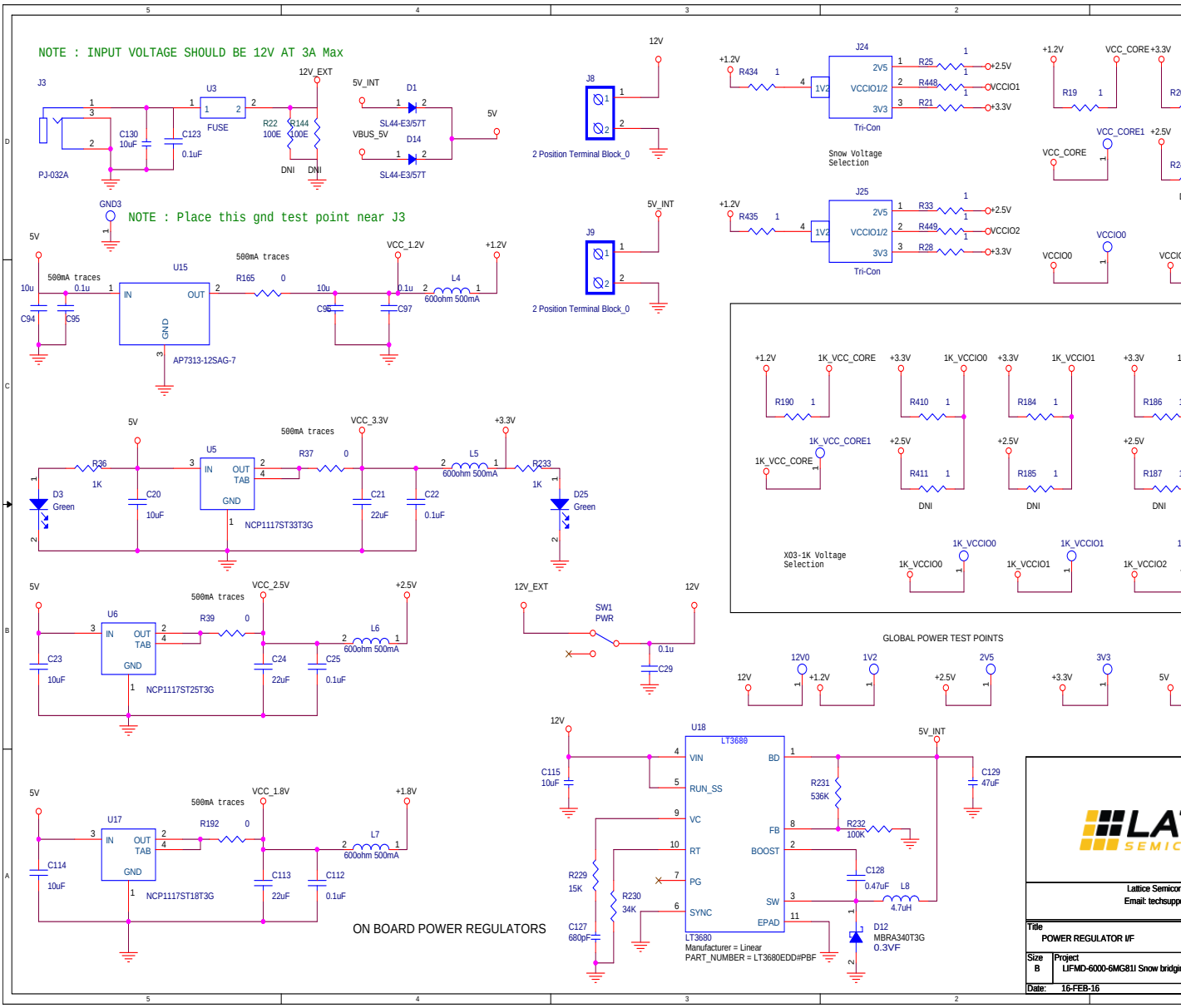
Appendix A. LIF-MD6000-ML-EVN-BRD Schematics



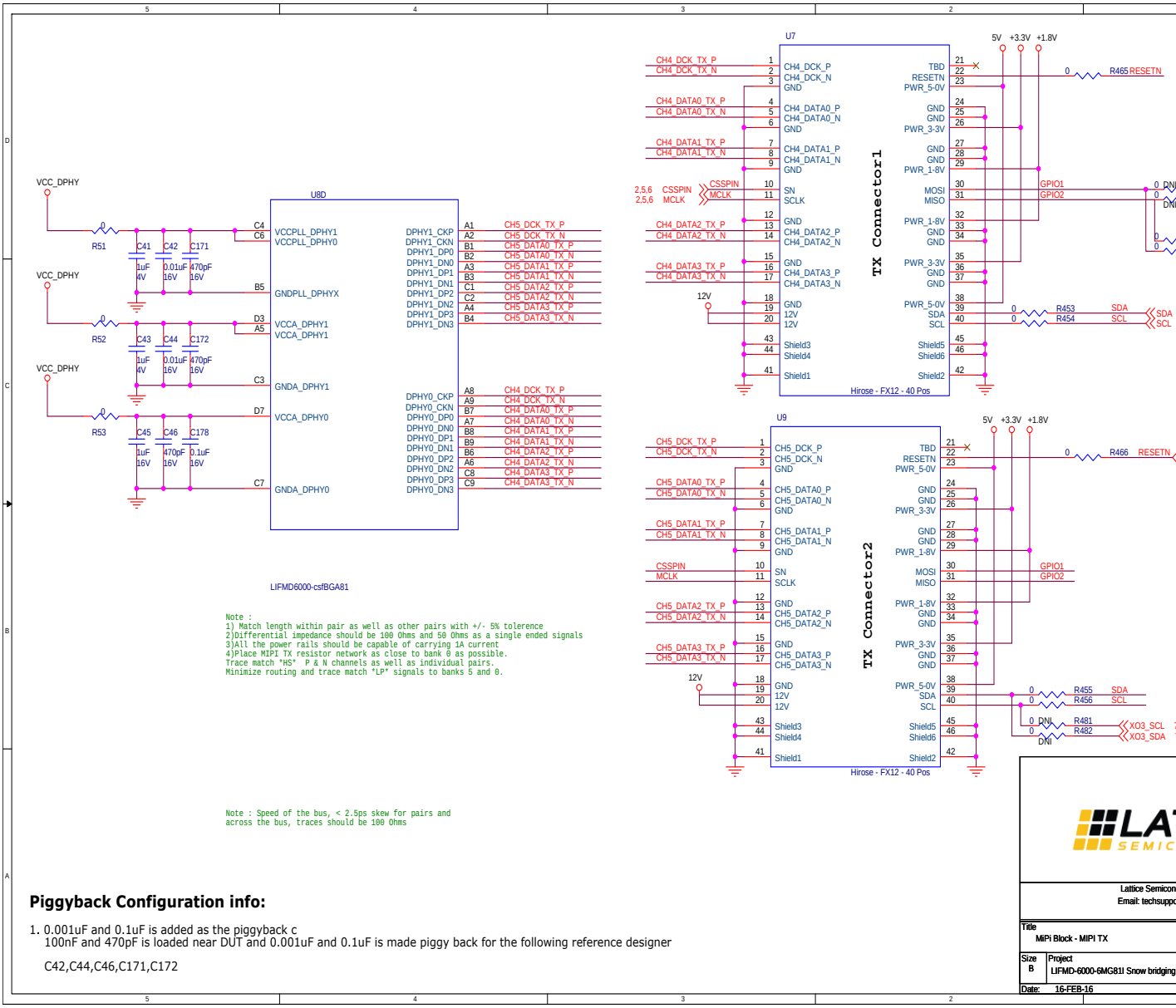
LIF-MD6000 Master Link Board Block Diagram



FTDI Interface



Power Regulator Interface

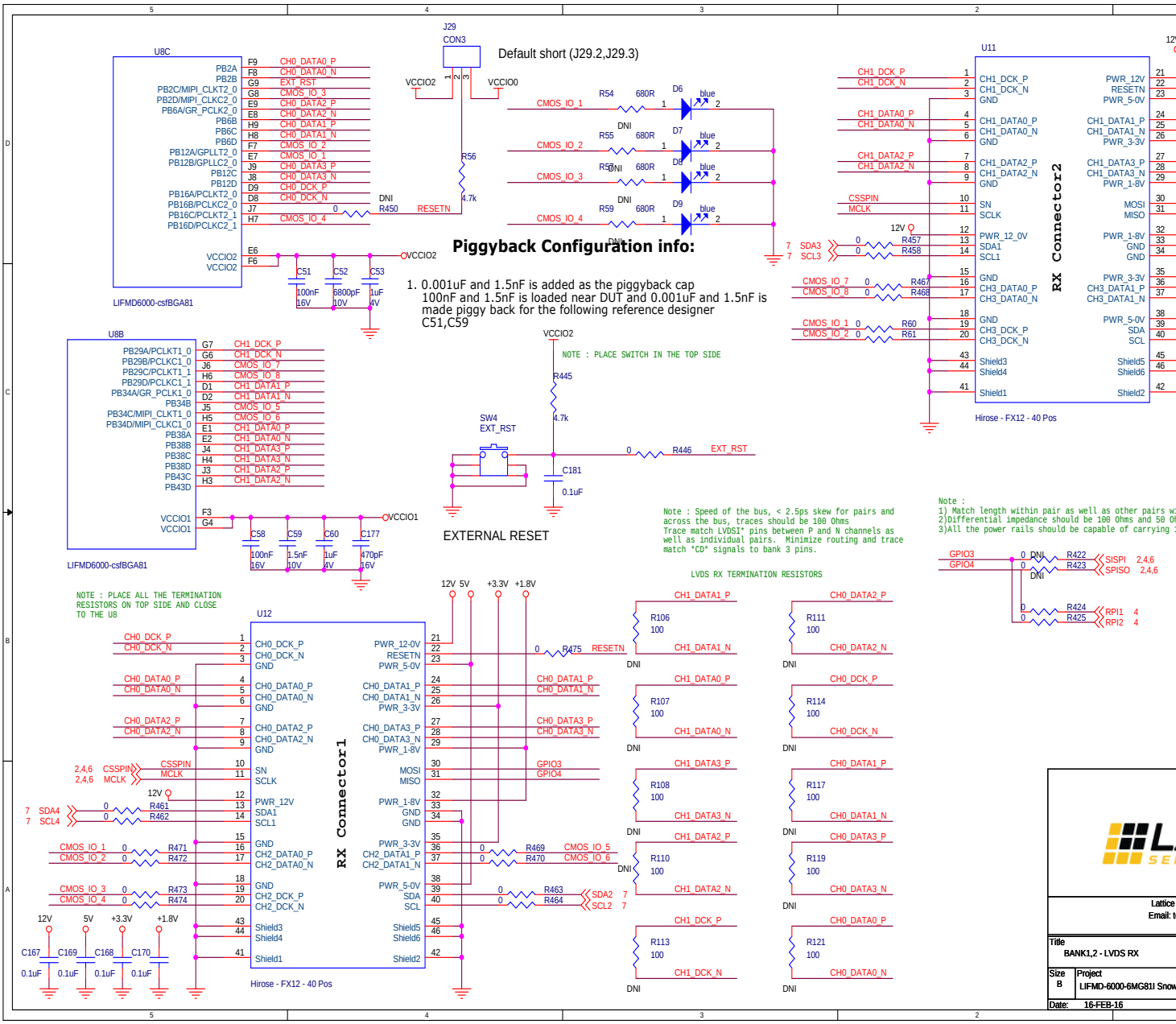


Piggyback Configuration info:

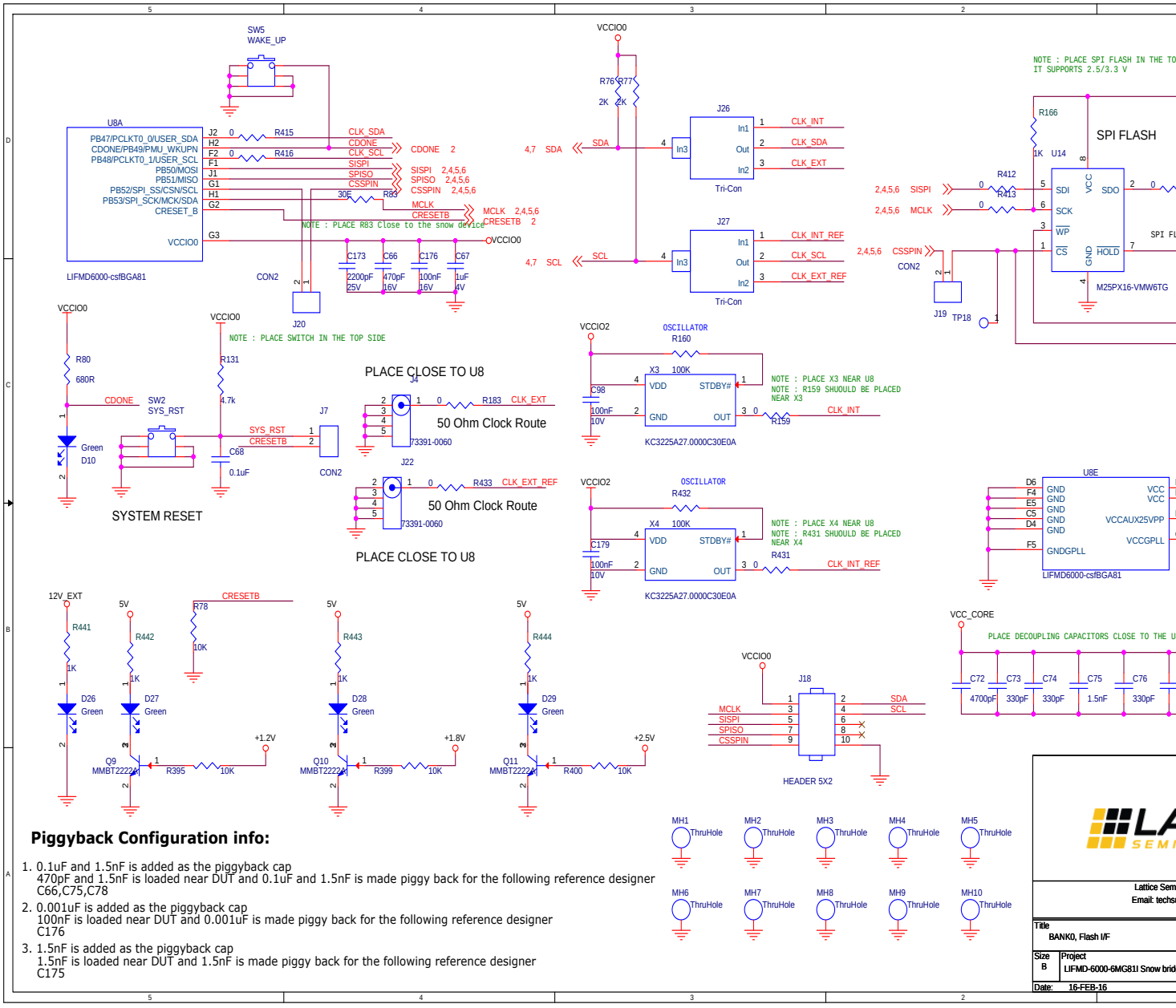
1. 0.001uF and 0.1uF is added as the piggyback c
   100nF and 470pF is loaded near DUT and 0.001uF and 0.1uF is made piggy back for the following reference designer

   C42,C44,C46,C171,C172

MIPI Block – MIPI Tx



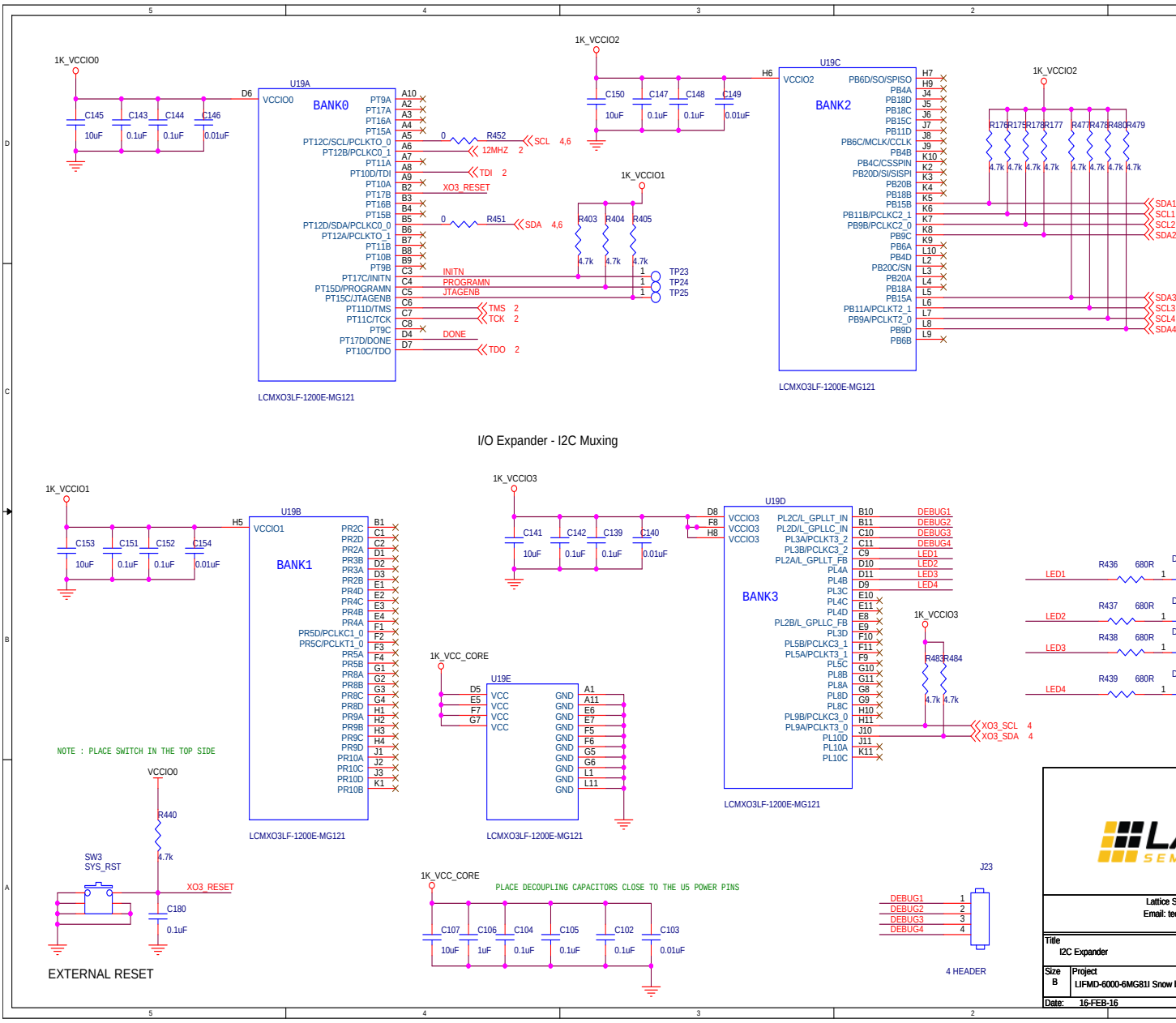
Bank 1, 2 - LVDS Rx



Piggyback Configuration info:

1. 0.1uF and 1.5nF is added as the piggyback cap
   470pF and 1.5nF is loaded near DUT and 0.1uF and 1.5nF is made piggy back for the following reference designer
   C66,C75,C78
2. 0.001uF is added as the piggyback cap
   100nF is loaded near DUT and 0.001uF is made piggy back for the following reference designer
   C176
3. 1.5nF is added as the piggyback cap
   1.5nF is loaded near DUT and 1.5nF is made piggy back for the following reference designer
   C175

Bank0, Flash Interface



Routing guidlines for MIPI & LVDS
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1)All differential routes are required to have the same length between the positive (true) and the negative (complimentary) r
Spacing between the positive (true) and the negative (complimentary) shall be 2 times trace width.

2)Target differential impedance shall be 100 Ohms

3)Trace length matching to be within 1.0 mm (40 mil) across the entire bus.

4)Use small humps for skew corrections

5)Place signal vias close together and remove copper in between vias.
Traces to be fully shielded with GND stitching terminating at both trace end points

6)Board trace impedance results must be within ±10 percent of target and
Power plane impedance to be within +/- 10 percent of target at operating frequency

MIPI &LVDS Simulation Requirement
---

1)MIPI Differential Mode insertion Loss shall be > -1.6dB at 750 MHz

2)MIPI Differential Mode Return Loss shall be < -15dB at 750 MHz

3)MIPI Common Mode Return Loss shall be < -15dB at 750 MHz

4)LVDS differential mode return loss shall be < -16.5db at 600 MHz

5)LVDS common mode return loss shall be < -16.5db at 600 MHz

6)LVDS insertion loss shall be > -1.7db at 600 MHz

7)LVDS Cross coupling shall be < -22 dB for victim IO at 600MHz

8)Power plane impedance to be within +/- 10 percent of target at operating frequency

Lattice Sem
Email: techs

Title
Layout Guidelines

Size B | Project LIFMD-6000-6MG81I Snow bric

Date: 16-FEB-16

Layout Guidelines

Appendix B. LIF-MD6000-ML-EVN-BRD Bill of Materials

LIF-MD6000 Master Link Rev B Board Bill of Materials

Item	Reference	Quantity	Part	PCB Footprint	Comments	PART_NUMBER	Manufacturer	De
1	C1, C3	2	4u7	C0603	—	ECJ-1VB0J475K	Panasonic	Ca 4.7 6.3
2	C2, C4, C5, C6, C8, C9, C12, C13, C14, C15, C16, C22, C25, C68, C112, C180, C181	17	0.1 µF	C0402	—	C0402C104K4RACTU	Kemet	CA 0.1 16
3	C7, C20, C23, C107, C114, C141, C145, C150, C153	9	10 µF	C0603	—	LMK107BJ106MALTD	Taiyo Yuden	CA 10
4	C10, C11	2	18 pF	C0402	—	C0402C180K3GACTU	Kemet	CA 04
5	C21, C24, C113	3	22 µF	C0805	—	LMK212BJ226MG-T	Taiyo Yuden	CA 22
6	C29, C95, C97	3	0.1 µF	C0402	—	CL05A104MP5NNNC	Samsung	Ca 10 85
7	C41, C43, C53, C60, C67, C71	6	1 µF	C0306	—	LLR185C70G105ME05L	Murata	CA
8	C42, C44	2	0.01 µF	C0201	—	GRM033R61C103KA12D	Murata	CA 02
9	C42, C44, C51, C176	4	0.001 µF	C0201	Piggyback Configuration	GRM033R71C102KA01D	Murata	CA 02
10	C45	1	1 µF	C0402	—	GRM155R61C105KA12D	Murata	CA 1 µ
11	C46, C66, C171, C172, C177	5	470 pF	C0201	—	GRM033R71C471KA01D	Murata	CA 47
12	C46, C66, C171, C172	4	0.1 µF	C0201	Piggyback Configuration	GRM033R61C104KE84D	Murata	CA 16

Item	Reference	Quantity	Part	PCB Footprint	Comments	PART_NUMBER	Manufacturer	De
13	C49, C98, C179	3	100 nF	C0402	—	GRM155R61A104KA01D	Murata	CA 10
14	C51, C58, C70, C176	4	100 nF	C0201	—	C0603X5R1C104K030BC	TDK	CA 0.1
15	C52	1	6800 pF	C0201	—	GRM033R71A682KA01D	Murata	CA 02
16	C59, C75, C78, C175	4	1.5 nF	C0201	—	GRM033R71A152KA01D	Murata	CA 02
17	C75, C78, C59, C175	4	1.5 nF	C0201	Piggyback Configuration	GRM033R71A152KA01D	Murata	CA 02
18	C72	1	4700 pF	C0306	—	LLL185R71H472MA01L	Murata	CA 03
19	C73, C74, C76	3	330 pF	C0201	—	GRM033R71H331KA12D	Murata	CA 33
20	C77	1	5600 pF	C0201	—	GRM033R71A562KA01D	Murata	CA 02
21	C94, C96	2	10 µF	C0603	—	CL10X106MP8NRNC	Samsung	CA 10
22	C102, C104, C105, C139, C142, C143, C144, C147, C148, C151, C152	11	0.1 µF	C0201	-—	C0603X5R1C104K030BC	TDK	CA 0.1
23	C103, C140, C146, C149, C154	5	0.01 µF	C0201	—	CC0201KRX7R7BB103	Yageo	CA 16
24	C106	1	1 µF	C0402	—	C0402C105K9PACTU	Kemet	CA 1 µ
25	C115, C130	2	10 µF	C0603	—	CL10A106MA8NRNC	Samsung	CA 10
26	C123	1	0.1 µF	C0603	—	GRM188R71E104KA01D	Murata	CA 0.1
27	C127	1	680 pF	C0603	—	C0603C681J3GACTU	Kemet	CA 68

Item	Reference	Quantity	Part	PCB Footprint	Comments	PART_NUMBER	Manufacturer	De
28	C128	1	0.47 µF	C0402	—	CL05A474KA5NNNC	Samsung	CA X5
29	C129	1	47 µF	C0805	—	C2012X5R1A476M125AC	TDK	CA 47
30	C155, C156, C157, C158, C159, C160, C161, C162, C163, C164, C165, C166, C167, C168, C169, C170	16	0.1 µF	C0402	—	04023C104KAT2A	AVX	CA 0.1
31	C173	1	2200 pF	C0201	—	GRM033R71E222KA12D	Murata	CA 02
32	C174	1	1000 pF	C0201	—	GRM033R61E102KA01D	Murata	CA 02
33	C178	1	0.1 µF	C0201	—	GRM033R61C104KE84D	Murata	CA 0.1
34	D1, D14	2	SL44-E3/ 57T	SL44E357T	—	SL44-E3/57T	Vishay semiconductor	Sc Re
35	D3, D25, D26, D27, D28, D29	6	Green	led_0603	—	LTST-C190KGKT	LITE-On INC	LE 06
36	D6, D7, D8, D9, D30, D31, D32, D33	8	blue	led_0603	—	LTST-C193TBKT-5A	LITE-On INC	Sta 47
37	D10	1	Green	led_0603	—	LG L29K-G2J1-24-Z	OSRAM	LE 06
38	D12	1	0.3 VF	MBRA340T3G	—	MBRA340T3G	ON Semi	DI SM
39	D23	1	Red	led_0603	—	LTST-C193KRKT-5A	LITE-On INC	Sta 63
40	VCC_DPHY1, VCC_CORE1, VCCIO1, GND1, VCCIO2, GND2, GND3, GND4, GND5, 1K_VCCIO0, 1K_VCC_CORE1, 1K_VCCIO1, 1V2, 1K_VCCIO2, 1K_VCCIO3,	24	TP_S_40_63	tp_s_40_63	DNI	—	—	Sq in 63

Item	Reference	Quantity	Part	PCB Footprint	Comments	PART_NUMBER	Manufacturer	De
	TP18, TP23, TP24, TP25, 2V5, 3V3, 5V0, 12V0, VCCIO0							
41	J1	1	header_ 1x8	hdr_amp_87 220_8_1x8_ 100	—	22-28-4081	Molex	CO VE
42	J2	1	SKT_MINIUS B_B_RA	skt_miniusb_ b_ra	—	5075BMR-05-SM-CR	Neltron	CO TY
43	J3	1	PJ-032A	PJ-032A	—	PJ-032A	CUI Inc.	CO 2.0
44	J4, J22	2	73391-0060	73391-0060	—	73391-0060	Molex	CO OH
45	J7, J19, J20	3	CON2	CON2	REGULAR 100 MIL HEADER	—	—	Ge 2 P
46	J8, J9	2	2 Position Terminal Block_0	TERM_BLOC K_2POS_10A	—	1727010	Phoenix Contact	TE mn
47	J18	1	HEADER 5X2	HEADER 2X5	REGULAR 100 MIL HEADER	—	—	Ge 2*
48	J23	1	4 HEADER	CON4	REGULAR 100 MIL HEADER	—	—	Ge 4 P
49	J24, J25, J26, J27	4	Tri-Con	TriCon	REGULAR 100 MIL HEADER	—	—	Ge
50	J28	1	CON6	HDR1X6	REGULAR 100 MIL HEADER	—	—	—
51	J29	1	CON3	HDR1X3	REGULAR 100 MIL HEADER	—	—	—
52	L1, L2, L3, L4, L5, L6, L7	7	600 Ω 500 mA	FB0603	—	BLM18AG601SN1 D	Murata	Fe MI
53	L8	1	4.7 uH	MPLC0730L4 R7	—	MPLC0730L4R7	Kemet	IN 4.7

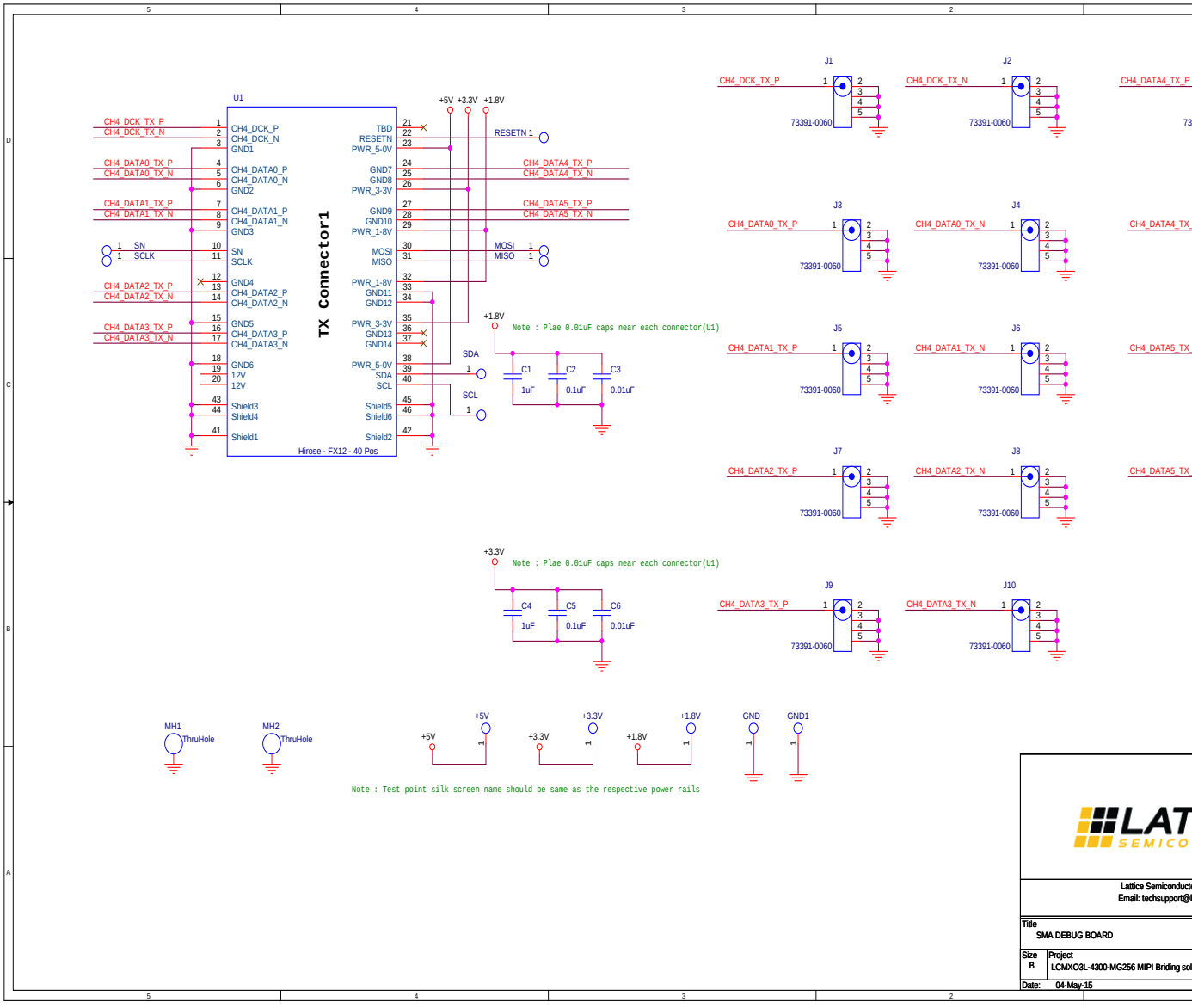
Item	Reference	Quantity	Part	PCB Footprint	Comments	PART_NUMBER	Manufacturer	De
54	MH1, MH2, MH3, MH4, MH5, MH6, MH7, MH8, MH9, MH10	10	Thru Hole	MTG125	DNL	—	—	—
55	Q9, Q10, Q11	3	MMBT2222A	SM_ SOT23-3	—	MMBT2222A,215	NXP Semiconductor	TR SO
56	R1, R2, R3, R56, R131, R175, R176, R177, R178, R403, R404, R405, R440, R445, R477, R478, R479, R480, R483, R484	20	4.7K	R0603	—	CRCW06034K70FKEA	Vishay	RE 4.7
57	R4, R5, R6, R7, R15, R16, R26, R37, R39, R51, R52, R53, R90, R159, R165, R167, R180, R181, R183, R192, R431, R433, R447	23	0	R0603	—	RC0603JR-070RL	Yageo	Re
58	R9, R10	2	2K2	R0603	—	CRCW06032K20FKEA	Vishay	RE 2.2
59	R11, R17	2	12K	R0603	—	RC0603FR-0712KL	Yageo	RE 12
60	R12, R13, R14, R123, R124, R125	6	10K	R0603	—	RMCF0603JT10K0	Stackpole Electronics Inc	RE 10 1/
61	R18, R418, R419, R422, R423	5	0	R0603	DNI	RC0603JR-070RL	Yageo	Re
62	R19, R20, R21, R25, R28, R33, R184, R186, R188, R190, R410, R417, R434, R435, R448, R449	16	1	R0603	—	CRCW06031R00JNEAHP	Vishay/Dale	RE 1 Ω
63	R22, R144	2	100E	R0603	DNI	CRCW0603100RFKEAHP	Vishay / Dale	RE 06
64	R23	1	0	R0603	DNI	RC0603JR-070RL	Yageo	Re
65	R24, R185, R187, R189, R411	5	1	R0603	DNI	CRCW06031R00JNEAHP	Vishay/Dale	RE

Item	Reference	Quantity	Part	PCB Footprint	Comments	PART_NUMBER	Manufacturer	De
								1 Ω
66	R36, R233	2	1K	R0603	—	RC0603FR-071KL	Yageo	RE 1 k
67	R54, R55, R57, R59	4	680R	R0402	DNI	RMCF0402JT680R	Stackpole Electronics Inc	RE
68	R60, R61, R446, R457, R458, R459, R460, R461, R462, R463, R464, R467, R468, R469, R470, R471, R472, R473, R474, R475, R476	21	0	R0402	—	RC0402JR-070RL	Yageo	RE 1/
69	R76, R77	2	2K	R0402	—	ERJ-2RKF2001X	Panasonic	RE 2 k
70	R78	1	10K	R0402	—	RMCF0402JT10K0	Stackpole Electronics Inc	RE
71	R80, R436, R437, R438, R439	5	680R	R0402	—	RMCF0402JT680R	Stackpole Electronics Inc	RE
72	R83	1	30E	R0603	—	RC0603FR-0730RL	Yageo	RE 30
73	R106, R107, R108, R110, R111, R113, R114, R117, R119, R121	10	100	R0402	DNI	RC0402FR-07100RL	Yageo	RE 1%
74	R160, R432	2	100K	R0402	—	RMCF0402JT100K	Stackpole Electronics Inc	RE 04
75	R166, R441, R442, R443, R444	5	1K	R0402	—	RMCF0402JT1K00	Stackpole Electronics Inc	RE
76	R179	1	650	R0603	—	RC0603FR-07649RL	Yageo	RE 06
77	R229	1	15K	R0402	—	ERJ-2RKF1502X	Panasonic	RE SM
78	R230	1	34K	R0402	—	ERJ-2RKF3402X	Panasonic	RE SM

Item	Reference	Quantity	Part	PCB Footprint	Comments	PART_NUMBER	Manufacturer	De
79	R231	1	536K	R0402	—	ERJ-2RKF5363X	Panasonic Electronic Components	RE 04
80	R232	1	100K	R0402	—	ERJ-2RKF1003X	Panasonic Electronic Components	RE 04
81	R395, R399, R400	3	10K	R0603	—	ERJ-3EKF1002V	Panasonic	RE 10
82	R412, R413, R414, R415, R416, R420, R421, R424, R425, R451, R452, R453, R454, R455, R456, R465, R466	17	0	R0603	—	RC0603JR-070RL	Yageo	Re
83	R450	1	0	R0402	DNI	RC0402JR-070RL	Yageo	RE 1/
84	R481, R482	2	0	R0603	DNL	RC0603JR-070RL	Yageo	Re
85	SW1	1	PWR	TS01CQE_switch	—	TS01CQE	C&K Components	SW 3 A
86	SW2, SW3, SW4	3	SYS_RST	2psmd_eswitch	—	TL1015AF160QG	E-Switch	SW 0.0
87	SW5	1	WAKE_UP	2psmd_eswitch	—	TL1015AF160QG	E-Switch	SW 0.0
88	U1	1	FT2232HL	tqfp64_0p5_12p2x12p2_h1p6	—	FT2232HL	FTDI	US
89	U2	1	93LC56-SO8	so8_50_244	—	93LC56C-I/SN	Microchip	IC
90	U3	1	FUSE	0154004DRT	—	0154004.DRT	Littlefuse	Su Fu ON
91	U5	1	NCP1117ST33T3G	sot223_4p	—	NCP1117ST33T3G	On Semi	IC

Item	Reference	Quantity	Part	PCB Footprint	Comments	PART_NUMBER	Manufacturer	De
92	U6	1	NCP1117ST25T3G	sot223_4p	—	NCP1117ST25T3G	On Semi	IC
93	U7, U9, U11, U12	4	Hirose - FX12 - 40 Pos	Hirose-FX12	—	FX12B-40P-0.4SV	Hirose Electric Co Ltd	Co PC 0.4
94	U8	1	LIF-MD6000-csfBGA81	LIF-MD6000-csfBGA81	Customer supplied	LIF-MD6000-csfBGA81	Lattice Semiconductor	La Cr
95	U14	1	M25PX16-VMW6TG	SOIC8	—	M25PX16-VMW6TG	Micron Technology Inc	IC 16 75
96	U15	1	AP7313-12SAG-7	SOT23	—	AP7313-12SAG-7	Diodes Inc	LD LD 1.2
97	U17	1	NCP1117ST18T3G	sot223_4p	—	NCP1117ST18T3G	On Semi	IC
98	U18	1	LT3680	LT3680_10QFN	—	LT3680EDD#PBF	Linear	5 V
99	U19	1	LCMXO3LF-1200E-MG121	LCMXO3LF-1200E-MG121	Customer supplied	LCMXO3LF-1200E-MG121	Lattice Semiconductor	CP 12 0.5
100	X1	1	12MHZ	crystal_4p_3p2x2p5	—	7M-12.000MAAJ-T	TXC	12
101	X3, X4	2	KC3225A27.0000C30E0A	27MHZ_OSC	—	KC3225A27.0000C30E0A	AVX Corporation	Sta 27
102	LIF-MD6000 MASTER LINK REV B BOARD PCB	1	—	—	—	305-PD-16-0154	PACTRON	—

Appendix C. SMA-IOL-EVN-BRD Schematics



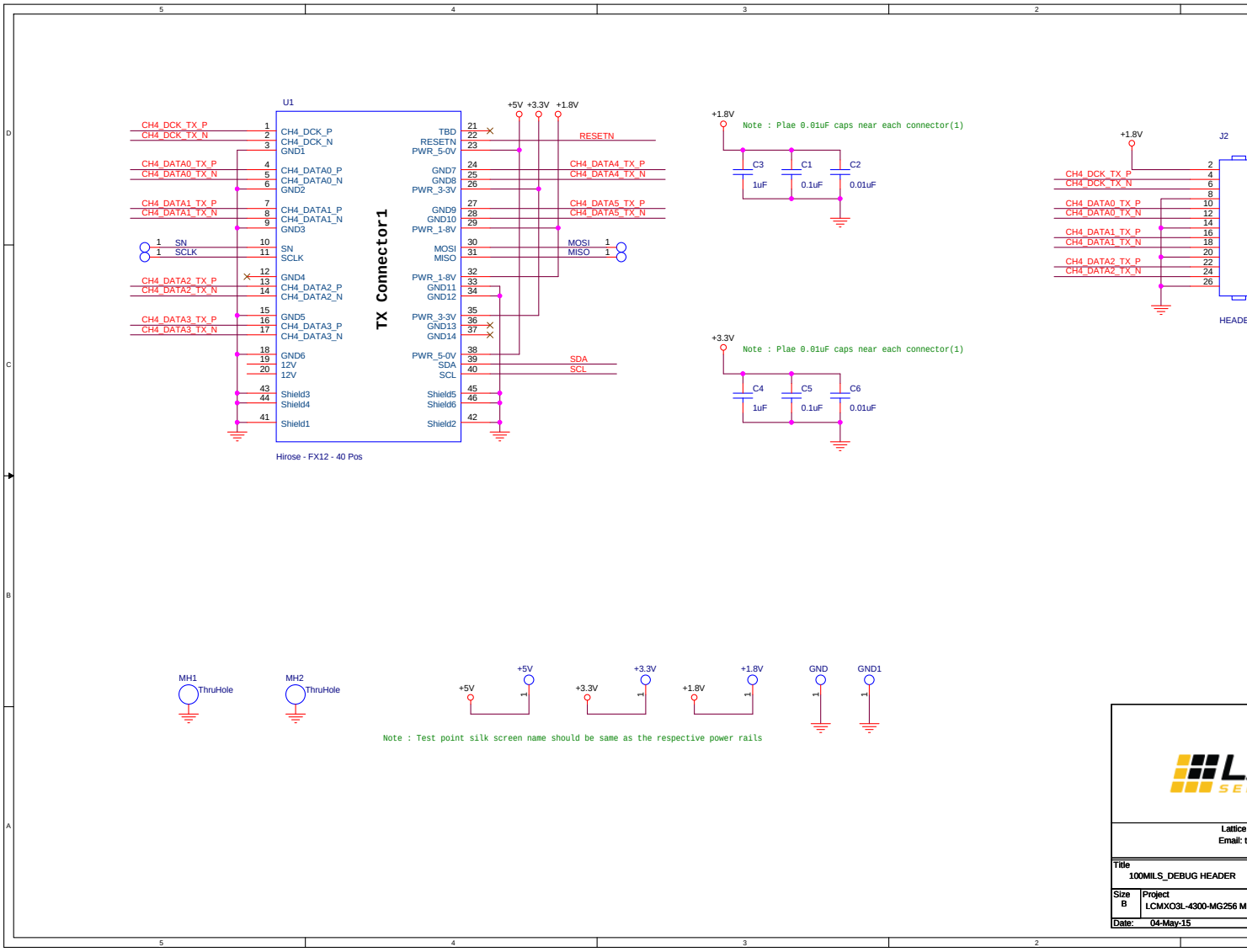
SMA Debug Board

Appendix D. SMA-IOL-EVN-BRD Bill of Materials

SMA IO Link Board Bill of Materials

Item	Reference	Qty	Part	PCB Footprint	Comments	PART_NUMBER	Manufacturer
1	GND1, +5 V, +1.8 V, +3.3 V, SN, SDA, SCLK, SCL, RESETN, MOSI, MISO, GND	12	TP_S_40_63	tp_s_40_63	DNI	—	—
2	C1, C4	2	1 µF	C0402	—	C0402C105K9PACTU	Kemet
3	C2, C5	2	0.1 µF	C0402	—	C0402C104K4RACTU	Kemet
4	C3, C6	2	0.01 µF	C0402	—	C0402C103J4RACTU	Kemet
5	J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14	14	73391-0060	73391-0060	—	73391-0060	Molex
6	MH1, MH2	2	Thru Hole	MTG125	—	—	—
7	U1	1	Hirose - FX12 - 40 Pos	Hirose-FX12S	—	FX12B-40S-0.4SV	Hirose Electric Co Ltd
8	SMA IOLINK BOARD PCB	1	—	—	—	305-PD-15-0589	PACTRON

Appendix E. B-IOL-EVN-BRD Schematics



100MILS_DEBUG Header

Appendix F. B-IOL-EVN-BRD Bill of Materials

Breakout IO Link Board Bill of Materials

Item	Reference	Qty	Part	PCB Footprint	Comments	PART_NUMBER	Manufacturer
1	GND1, +5 V, +1.8 V, +3.3 V, SN, SCLK, MOSI, MISO, GND	9	TP_S_40_63	tp_s_40_63	DNL	—	—
2	C1, C5	2	0.1 µF	C0402	—	C0402C104K4RACTU	Kemet
3	C2, C6	2	0.01 µF	C0402	—	C0402C103J4RACTU	Kemet
4	C3, C4	2	1 µF	C0402	—	C0402C105K9PACTU	Kemet
5	J2	1	HEADER 13X2	13X2_HDR	REGULAR 100 MIL HEADER	—	—
6	MH1, MH2	2	ThruHole	MTG125	DNL	—	—
7	U1	1	Hirose - FX12 - 40 Pos	Hirose-FX12S	—	FX12B-40S-0.4SV	Hirose Electric Co Ltd
8	BREAKOUT IOLINK BOARD PCB	1	—	—	—	305-PD-15-0595	PACTRON

Revision History

Date	Version	Change Summary
June 2018	1.5	• Changed document name to CrossLink LIF-MD6000 Master Link Board - Revision B Evaluation Board User Guide. • Specified Rev B in all references to the board. • Corrected device name to MachXO3 LCMXO3LF-1300E in Programming Circuit. • Updated Table 2.1. Headers and Test Connectors. • Updated Power Supply section.
April 2018	1.4	Made schematics searchable.
March 2018	1.3	Added footnote to Table 2.1.
September 2017	1.2	• Changed document number from EB105 to FPGA-EB-02010. • Changed J25 from VCCIO1 to VCCIO2 in Table 2.1. Headers and Test Connectors. • Updated 100MILS_DEBUG Header in Appendix E. B-IOL-EVN-BRD Schematics.
April 2017	1.1	New sections: • SMA IO Link Board • Breakout IO Link Board • Ordering Information Updated Appendix A. LIF-MD6000-ML-EVN-BRD Schematics: • Changed “SW4 SYS_RST” to “SW4 EXT_RST” in the Bank 1, 2 – LVDS Rx diagram. • Changed “EXTERNAL RESET” to “SYSTEM RESET” in the Bank0, Flash Interface diagram.
May 2016	1.0	Initial release.

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