SiI9187B HDMI Port Processor

Data Sheet

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Further Information

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Revision History

Revision	Date	Comment
A	9/2009	First Production release.
A01	8/2010	Inserted Export Control statement, minor editing throughout.
A02	9/2010	Roll revision number due to work on the Data Brief; no other changes.

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Introduction

The SiI9187B HDMI Port Processor is the second generation of HDMI® devices that support the HDMI Specification. With four HDMI inputs and a single output, the SiI9187B port processor enhances the functionality of digital TVs using single system on a chip (SoC) solutions with integrated HDMI receivers. The port processor provides a simple, low-cost method of retransmitting digital audio and video to give consumers a truly all-digital experience. Built-in backward compatibility with DVI 1.0 allows HDMI systems to connect to any DVI 1.0 source.

Features

The SiI9187B device brings cutting edge innovations, such as:

- Enhanced cable equalization for long cable support, even at Deep Color resolutions that enables the SiI9187B device to work with noisy signals and many sources, making the sink devices highly interoperable
- Integrated EDID and CEC functions
- Improved ESD protection on all signals connected to the HDMI connector.

HDMI Inputs and Output

- Four HDMI input ports and single output port
- HDMI, HDCP, and DVI compatibility
- TMDS™ cores run at 25–225 MHz
- Supports video resolutions up to 1080p, 60 Hz, 12-bit or 720p/1080i, 120 Hz, 12-bit.

Control Capability

- Consumer Electronics Control (CEC) interface incorporates an HDMI-compliant CEC I/O and an integrated CEC Programming Interface (CPI); these simplify design and lower cost and software overhead
- Integrated EDID and DDC support for 4 HDMI/DVI ports and 1 VGA port with a 256-byte NVRAM shared between ports that loads into separate 256-byte SRAM for each of 5 ports
- Individual control of Hot Plug Detect (HPD) for each of the 4 HDMI/DVI ports
- TPWR (TMDS clock detect) output to help speed soft mute of audio while plugging and unplugging cables
- Controllable by the local I^2C bus.

Power Management

- Flexible power management provides extremely low standby power consumption
- Standby power can be supplied from a separate +3.3 V or 5 V standby power pin
- Port power only can be used to read EDID
- Single power 3.3-V source
- Integrated 5 V to 3.3 V Voltage regulator.

Package

- 72-pin, 10 mm x 10 mm, 0.5 mm pitch QFN package with enhanced ePad™.

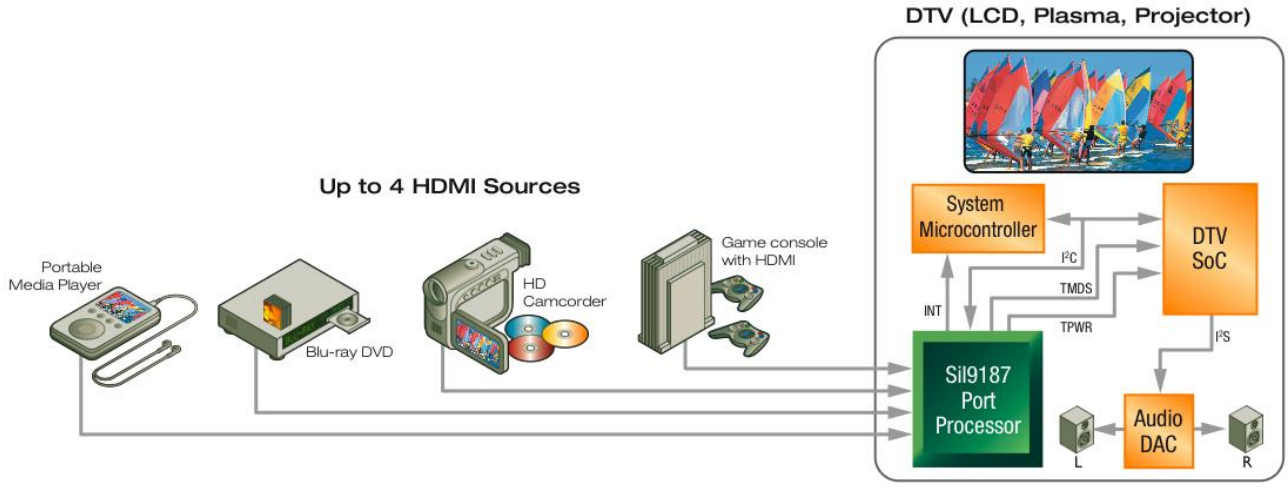

Figure 1. Typical Application of SiI9187B HDMI Port Processor

Pin Diagram

Figure 2 shows the pin diagram for the SiI9187B port processor. A description of the pin functions is in the Pin Descriptions section beginning on page 13. The ePad ***must*** be soldered to ground.

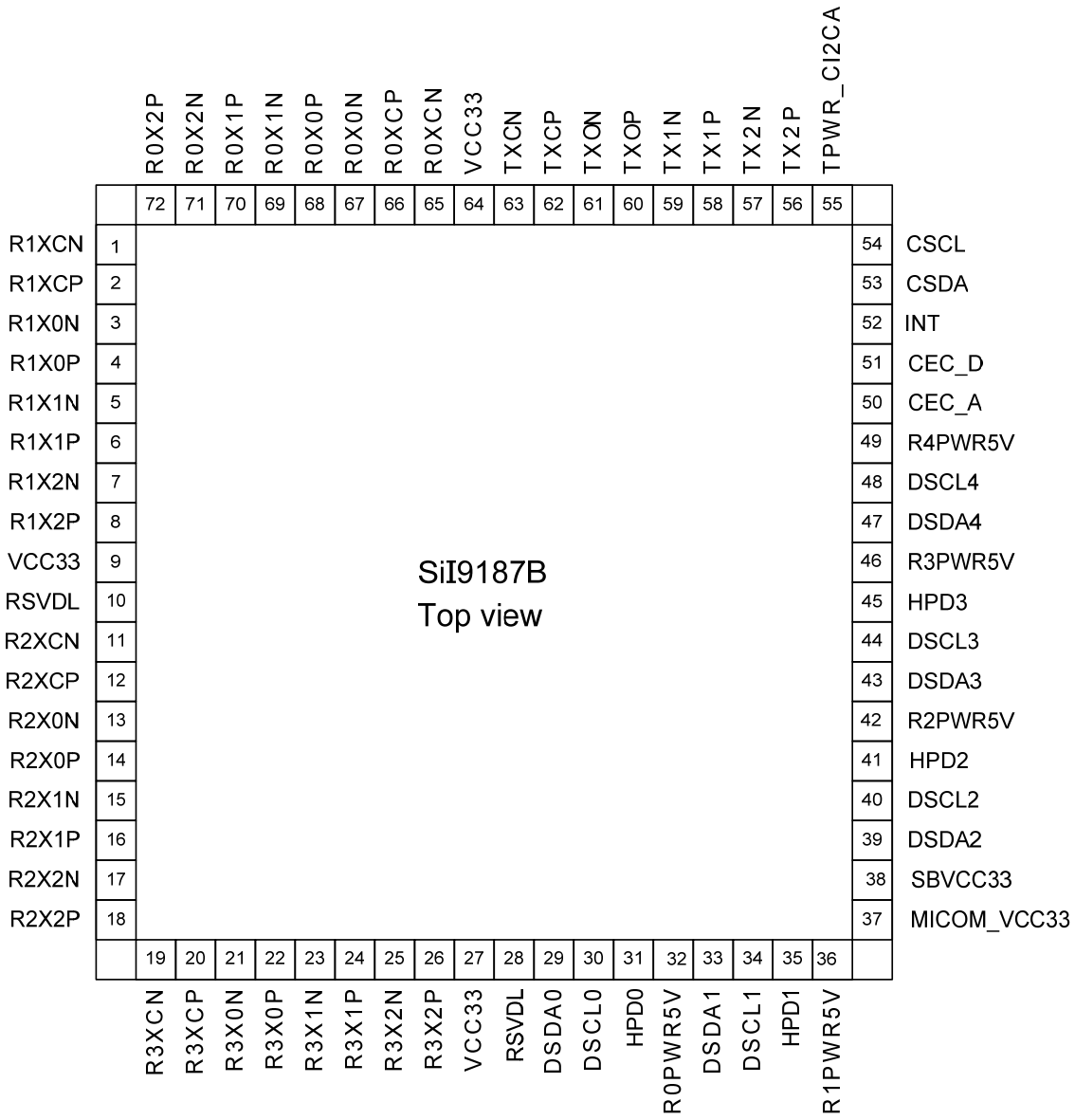

Figure 2. Pin Diagram (Top View)

Functional Description

Figure 3 shows typical signal connections when the SiI9187B port processor is incorporated in a DTV. Figure 4 on the next page shows the functional block diagram of the device.

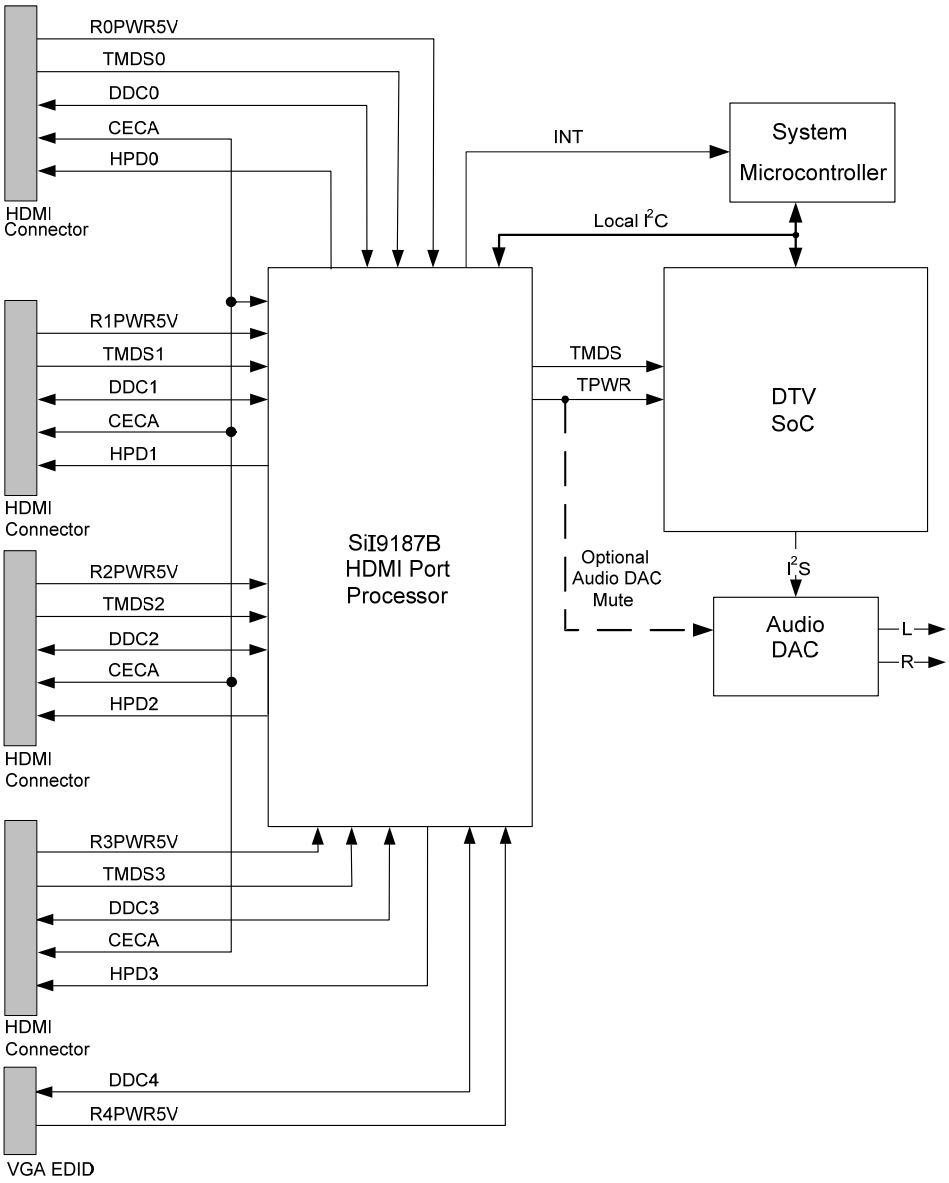

Figure 3. System Architecture

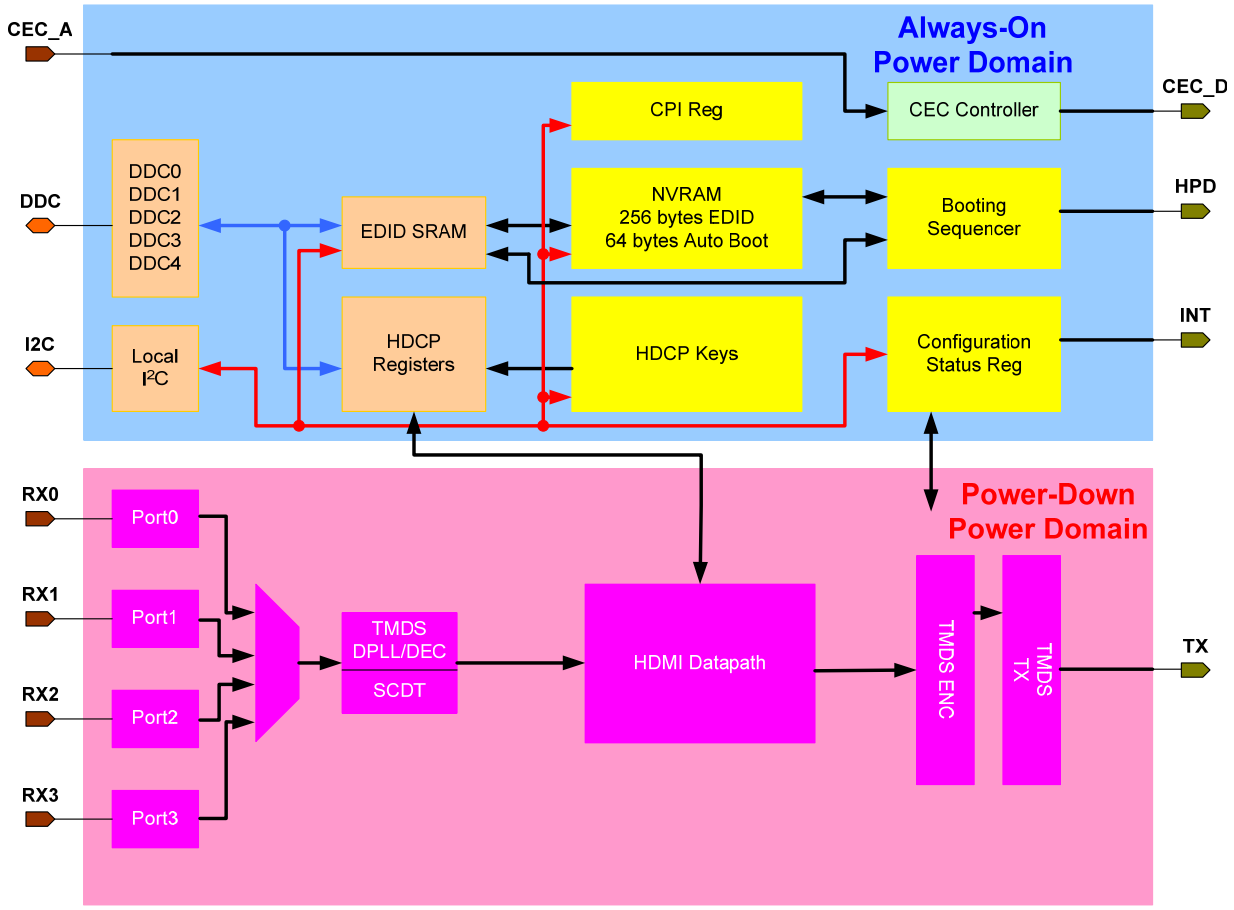

Figure 4. Functional Block Diagram

Receiver Block

The four HDMI/DVI receiver ports are defined as Port 0, Port 1, Port 2, and Port 3. Each of the ports is terminated separately and equalized under the control of the receiver digital block and is controlled by the local I^2C bus.

TMDS Transmitter Block

The transmitter block sends an HDMI content stream based on the content delivered from the selected source. Internal source termination eliminates the need for external R-C components for signal shaping. The internal source termination can be disabled by using a register setting.

CEC Interface Block

The Consumer Electronics Control (CEC) interface block provides CEC-compliant signals between CEC devices and a CEC master. It translates the LVTTL signals of an external microcontroller (CEC host-side or transmit-side) to CEC signal levels for CEC devices at the receive-side, and vice versa.

A CEC controller compatible with the Silicon Image CEC API is included on-chip. This controller has a high-level register interface accessible through the I^2C interface, and can be used to send and receive CEC commands. This controller makes CEC transactions easy and straightforward, removing the burden of performing these low-level transactions on the CEC bus from the host processor.

NVRAM and EDID RAM Block

The port processor has 256 bytes of NVRAM for storing common EDID data that can be used by each of the ports. An additional 64-byte block of NVRAM is used by the Auto-Boot feature, which initializes some of the registers used to enable the EDID for the respective port and asserts HOTPLUG after the EDID has loaded properly into the SRAM. For example, by changing the data in the NVRAM Auto-Boot portion, EDID loading and automatic HOTPLUG control can be enabled in 3 of the HDMI ports while disabling this feature in the fourth port. More detail about the format of the NVRAM Auto-Boot feature is described in the Programmer's Reference (refer to Table 11). The EDID block consists of 1280 bytes of SRAM. Each port has a block of 256 bytes of SRAM for EDID data, allowing all ports to be read simultaneously from five different sources connected to the SiI9187B device. Both the NVRAM EDID data and NVRAM Auto-Boot data should be initialized by software using the local I^2C bus at least once during time of manufacture.

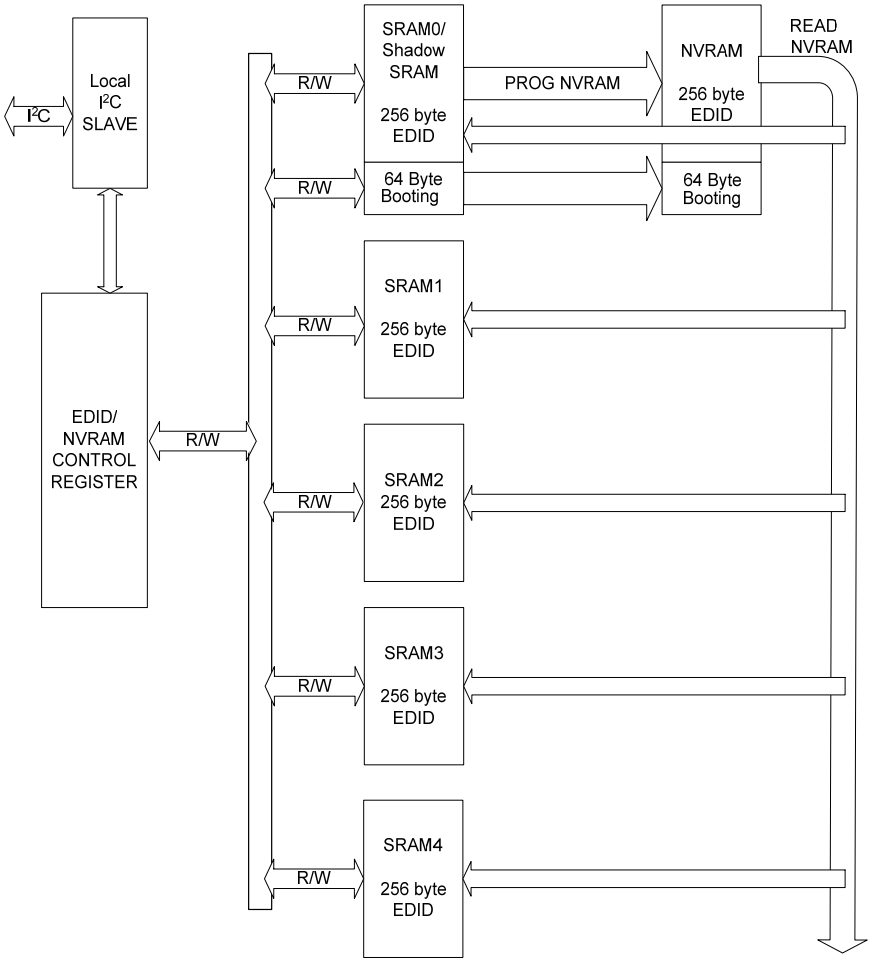

Figure 5. EDID Block Diagram

Configuration, I²C Slave, and Interrupt Blocks

The configuration block is used to set up and control the operation of the port processor.

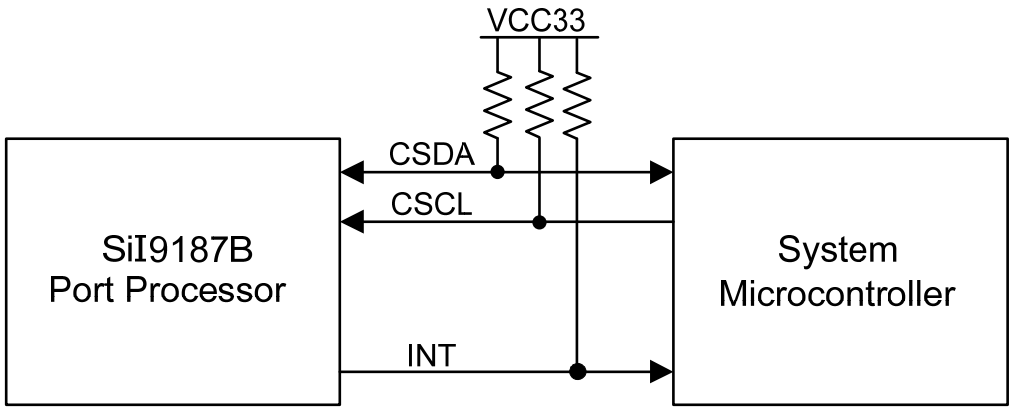

Figure 6. I²C Control Mode Configuration

The local slave I²C interface on SiI9187B pins CSCL and CSDA can run at up to 400 kHz. This bus configures the device by reading from and writing to necessary registers.
The power-on-reset (POR) circuit of the SiI9187B performs the following functions:

- Issue a reset to all internal logic after power up
- Read the level on the TPWR/CI2CA pin during reset time (this determines the primary slave I²C address).

Table 1 lists the local I²C interface slave addresses. By setting the level of the CI2CA pin with the PCB strapping option, the user can select either 0xB0 or 0xB2 as the primary I²C slave address for the port processor. The secondary I²C slave addresses such 0xC0 and 0xE0 are not affected. For complete registers information, Refer to the Programmer's Reference.

Table 1. Control of the Default I²C Addresses with the CI2CA Pin

CI2CA	I²C Slave Address	Accessed Through
CI2CA = 0	0xB0	Local I²C
CI2CA = 1	0xB2	Local I²C

Standby and HDMI Port Power Supplies

The port processor contains two separate power domains: the *always-on domain*, and the *power-down (VCC33) domain*. The always-on domain must always have power for the device to function. This is also the only power source needed to power the EDID and CEC functions. The power-down domain can be powered off at any time; however, when powered off, only the EDID and CEC functions are operational, along with the local I²C registers used to control these functions. The VCC33 power domain should never be powered on when the always-on domain is powered off.

The always-on domain incorporates a power multiplexer that selects power from one of six sources: pins SBVCC33, R0PWR5V, R1PWR5V, R2PWR5V, R3PWR5V or R4PWR5V. As long as 5 V is available at one of the R*n*PWR5V pins or 3.3V is available at pin SBVCC33, the always-on domain will have power and the EDID and CEC functions will operate correctly. Note that the SBVCC33 is supplied from a 3.3 V power supply. As long as one of these inputs has power, the other inputs can be left unpowered.

Standby power supply SBVCC33 pin can be supplied with 3.3 V from the display when the device is in power-down mode. Alternatively, one of the R*n*PWR5V pins can receive power from HDMI port *n* for standby power when the display device is off. The R4PWR5V has the highest priority and when in standby mode current is used from this port. Therefore, if there is a 5 V standby power supply from the display, it can be connected to R4PWR5V.

Table 2 summarizes the power modes available in the port processor. Figure 7 shows a block diagram of the standby power supply sources and the always-on power island.

Table 2. Description of Power Modes

Power mode	Description	SBVCC33	R4PWR5V	R[0-3]PWR5V	VCC33
Power-On mode 3.3 V Standby	All power supplies to the SiI9187B chip are on. All functions are available. The standby power supply is 3.3 V. MICOM_VCC33 cannot be used in this mode. The TMDS transmitter must be connected to a terminated receiver.	3.3 V	No connection	Don't Care	3.3 V
Power-On mode 5 V Standby	All power supplies to the SiI9187B chip are on. All functions are available. The standby power supply is 5 V. The TMDS transmitter must be connected to a terminated receiver.	No connection	5 V	Don't Care	3.3 V
Standby power mode. 3.3 V Standby	The always-on power domain is on, supplied from the internal power MUX; all other supplies are off. The standby power supply is 3.3 V. MICOM_VCC33 cannot be used in this mode. In this mode, EDID and CEC are functional, but video and audio processing is not performed and all outputs are off.	3.3 V	No connection	Don't Care	Off
Standby power mode. 5 V Standby	The always-on power domain is on, supplied from the internal power MUX; all other supplies are off. The standby power supply is 5 V. In this mode, EDID and CEC are functional, but video and audio processing is not performed and all outputs are off.	No connection	5 V	Don't Care	Off
HDMI Port Power only 3.3 V Standby	Power is off to the device. HDMI +5 V from the HDMI cable is the only power source. For example, if the TV is unplugged from AC wall outlet, EDID and CEC are functional in this mode.	Off	No connection	5 V on any input	Off
HDMI Port Power only 5 V Standby	Power is off to the device. HDMI +5 V from the HDMI cable is the only power source. For example, if the TV is unplugged from AC wall outlet, EDID and CEC are functional in this mode.	No connection	Off	5 V on any input	Off
VGA Port Power only 3.3 V Standby	Power is off to the device. VGA +5 V from the VGA cable is the only power source. For example, if the TV is unplugged from AC wall outlet, EDID is functional in this mode.	Off	5 V	Off	Off

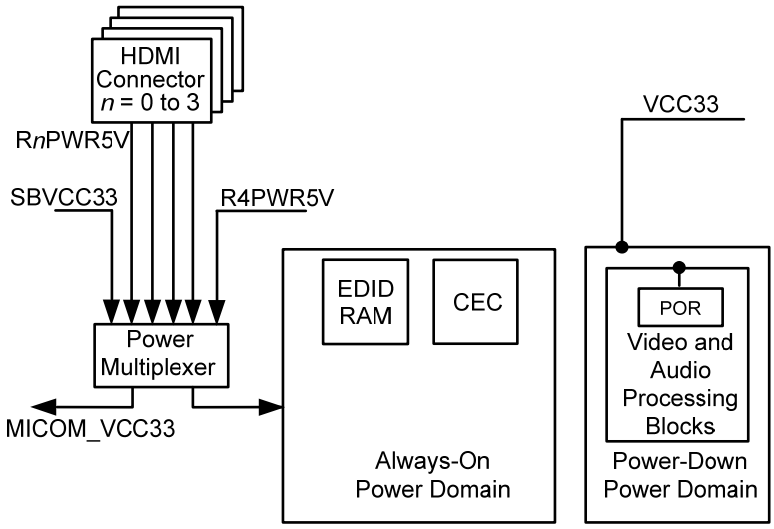

Figure 7. Standby Power Supply Diagram

HDMI Port Power

If all power to the system is off, as when the TV is unplugged from the AC electrical outlet, the EDID can still be read from the source by using power from the HDMI connector +5 V signal. In this case, the internal power MUX automatically switches to the power from the HDMI connector for powering the EDID logic. In this mode, only the EDID and CEC blocks are functional; all other functions of the device are in power-off mode. Also, the EDID RAM block that is read from the DDC port of the HDMI connector is loaded from non-volatile memory (NVRAM) once the 5 V is applied from the HDMI connector. No damage will occur to the device in this mode.

HDCP, CEC Programming Interface (CPI), and Configuration Registers

Refer to the Programmer's Reference (see Table 11) for register descriptions.

Power-On Reset Timing

Figure 8 shows the SiI9187B power up sequence. As soon as either Port Power or the TV standby power is available, the power up sequence starts and takes about 100 ms. HPD for each port is asserted when the power up sequence is completed.

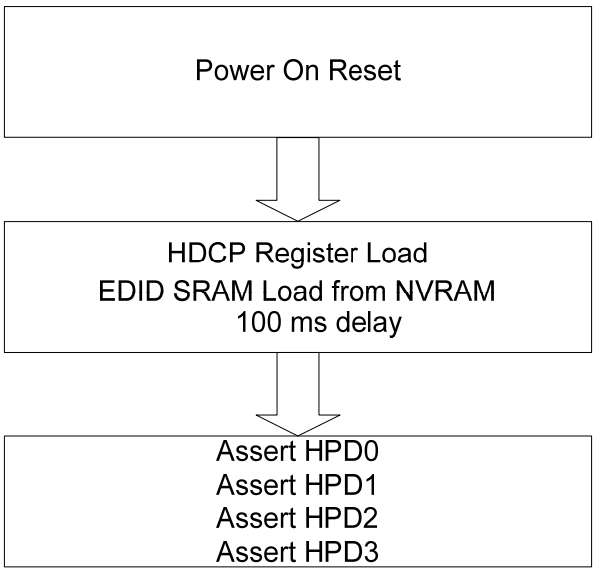

Figure 8. POR Minimum Timings

Electrical Specifications

Specifications are for the Commercial Temperature range, 0 °C to +70 °C, unless otherwise specified.

Table 3. Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
VCC33	Analog and digital core supply voltage	−0.3	—	4.0	V	1, 2
SBVCC33	3.3 V standby power supply voltage	−0.3	—	4.0	V	1, 2
R[0–3]PWR5V	5 V input from Power pin of HDMI connector	−0.3	—	5.7	V	1,2
R4PWR5V	5 V standby power or input from Power pin of VGA connector	−0.3	—	5.7	V	1,2
V_I	Input voltage	−0.3	—	6.0	V	1, 2, 3
V_O	Output voltage	−0.3	—	4.0	V	1, 2
T_J	Junction temperature	0	—	125	°C	—
T_{STG}	Storage temperature	−65	—	150	°C	—

Notes:

1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.
3. All input signal pins except those for the TMDS signals.

Table 4. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
VCC33	Analog and digital core supply voltage	3.135	3.3	3.465	V	—
SBVCC33	3.3 V standby power supply voltage	3.0	3.3	3.6	V	—
R[0–3]PWR5V	5 V input from Power pin of HDMI connector	4.5	5.0	5.5	V	—
R4PWR5V	5 V standby power or input from Power pin of VGA connector	4.5	5.0	5.5	V	—
V_{CCN}	Supply voltage noise	—	—	100	mV_{P-P}	1
MICOM_VCC33	Voltage	3.0	3.3	3.6	V	2
MICOM_VCC33	Output current	—	—	30	mA	2
T_A	Ambient temperature (with power applied)	0	+25	+70	°C	—
Θ_{ja}	Ambient thermal resistance (Theta JA)	—	—	27	°C/W	3
Θ_{jc}	Junction to case resistance (Theta JC)	—	—	13	°C/W	3

Notes:

1. The supply voltage noise is measured at test point VCC. See Figure 9. The ferrite bead provides filtering of power supply noise. The figure is representative and applies to other VCC33 pins as well.
2. MICOM_VCC33 can only be used in 5 V Standby.
3. The ePad ***must*** be soldered to ground.

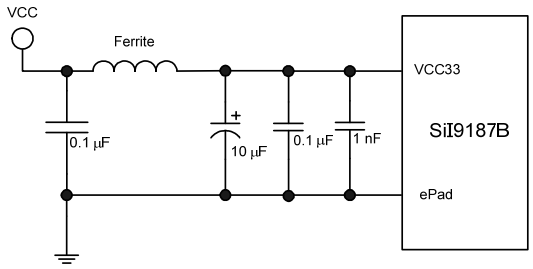

Figure 9. Test Point VCC for VCC33 Noise Tolerance Spec

DC Specifications

Table 5. Digital I/O Specifications

Symbol	Parameter	Pin Type	Conditions	Min	Typ	Max	Units
V_{IH}	HIGH-level input voltage	LVTTL	—	2.0	—	—	V
V_{IL}	LOW-level input voltage	LVTTL	—	—	—	0.8	V
$V_{TH+I2CD}$	LOW to HIGH threshold, DDC I^2C Bus	Schmitt	—	3.0	—	—	V
$V_{TH-I2CD}$	HIGH to LOW threshold, DDC I^2C Bus	Schmitt	—	—	—	1.5	V
$V_{TH+I2CL}$	LOW to HIGH threshold, Local I^2C Bus	Schmitt	—	2.0	—	—	V
$V_{TH-I2CL}$	HIGH to LOW threshold, Local I^2C Bus	Schmitt	—	—	—	0.8	V
V_{OH}	HIGH-level output voltage	LVTTL	—	2.4	—	—	V
V_{OL}	LOW-level output voltage	LVTTL	—	—	—	0.4	V
I_{OL}	Output leakage current	—	High Impedance	−10	—	10	µA
V_{ID}	Differential input voltage	TMDS	—	150	—	1200	mV
I_{OD8}	8 mA Digital Output Drive	LVTTL	V_{OUT} = 2.4V	8	—	—	mA
			V_{OUT} = 0.4V	8	—	—	mA

HPD Output Signal

When a source is connected to a port using an HDMI cable, the SiI9187B device detects the presence of the +5 V supply on the cable and uses it to generate the HPD output signal. The HPD output signal driver circuit is shown in Figure 10 and the output signal specifications are shown in Table 6.

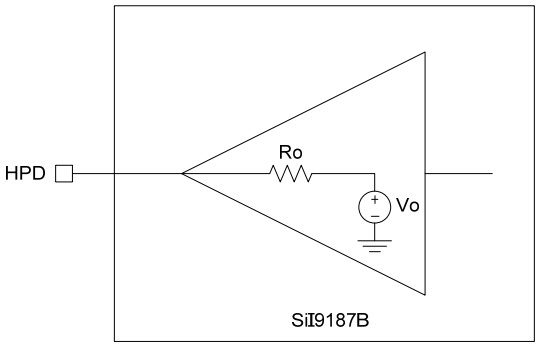

Figure 10. HPD Output Signal Driver

Table 6. HPD Output Signal Specifications

Symbol	Parameter	Pin Type	Conditions	Min	Typ	Max	Units	Notes
V_{OH}	HIGH-level output voltage	HPD	—	2.4	—	5.3	V	1
V_{OL}	LOW-level output voltage	HPD	—	0.0	—	0.4	V	—
Ro	Output Resistance	—	—	800	1000	1200	Ω	2

Notes:

1. V_{OH} is specified with R[0-3]PWR5V from the +5V pin of the HDMI connector between 4.8 V and 5.3 V.
2. Ro is the output resistance of the HPD output driver and is included in the chip.

Power Consumption

Table 7. Power

Symbol	Parameter	Min	Typ	Max	Units	Notes
VCC33 Icc	VCC33 Supply Current	—	251	330	mA	1, 2
SBVCC33 Icc	SBVCC33 Supply Current	—	—	5	mA	—
R4PWR5V Icc	R4PWR5V Supply Current with 30 mA supply for MICOM_VCC33	—	—	35	mA	—
R4PWR5V Icc	R4PWR5V Supply Current with MICOM_VCC33 not used	—	—	7	mA	—
R[0–3]PWR5V Icc	R[0-3]PWR5V Supply Current	—	—	7	mA	—

Notes:

1. Typical VCC33 Icc with one 1080p 8-bit input source and one 720p 8-bit input source with VCC33 at 3.3 V, with the 1080p 8-bit input source selected, and temperature at 25 °C.
2. Maximum VCC33 Icc with four 1080p 12-bit sources with VCC33 at 3.465 V, with one of the four input ports selected, and temperature at 70 °C.

AC Specifications

Table 8. TMDS Input Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{RXDPS}	Intra-Pair Differential Input Skew	—	—	—	0.4	T_{BIT}	—	2, 4
T_{RXCCS}	Channel to Channel Differential Input Skew	—	—	—	$0.2T_{PIXEL} + 1.78$	ns	Figure 11	2, 3
F_{RXC}	Differential Input Clock Frequency	—	25	—	225	MHz	—	—
T_{RXC}	Differential Input Clock Period	—	4.44	—	40	ns	—	—
T_{IJIT}	Differential Input Clock Jitter tolerance (0.3Tbit)	74.25 MHz	—	—	400	ps	—	2, 5, 6

Notes:

1. Under normal operating conditions unless otherwise specified, including output pin loading of $C_L = 10$ pF.
2. Guaranteed by design.
3. T_{PIXEL} is one IDCK Period (refer to the applicable Silicon Image HDMI Transmitter Data Sheet).
4. T_{BIT} is 1/10 of IDCK Period (refer to the applicable Silicon Image HDMI Transmitter Data Sheet).
5. Jitter as defined by the HDMI Specification.
6. Jitter is measured with the Clock Recovery Unit defined by the HDMI Specification. Actual jitter tolerance can be higher depending on the frequency of the jitter.

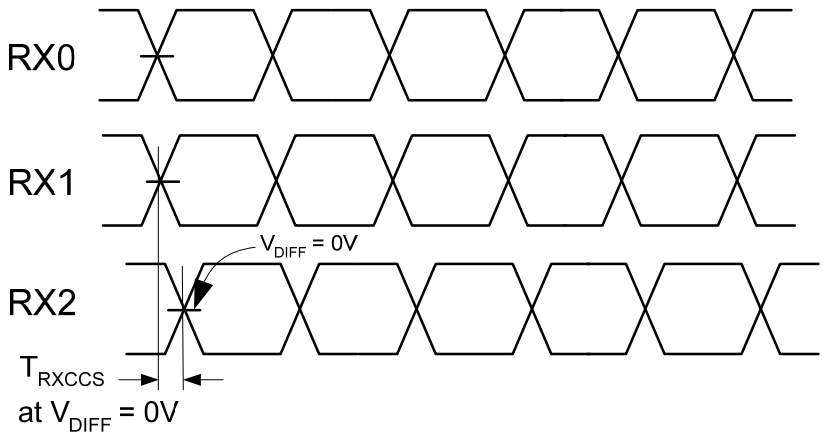

Figure 11. TMDS Channel-to-Channel Input Skew Timing

Table 9. TMDS Output Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
T_{TXDPS}	Intra-Pair Differential Output Skew	—	—	—	0.15	T_{BIT}	1
T_{TXRT}	Data/Clock Rise Time (20%–80%)	—	75	—	—	ps	—
T_{TXFT}	Data/Clock Fall Time (20%–80%)	—	75	—	—	ps	—
F_{TXC}	Differential Output Clock Frequency	—	25	—	225	MHz	—
T_{TXC}	Differential Output Clock Period	—	4.44	—	40	ns	—
T_{DUTY}	Differential Output Clock Duty Cycle	—	40%	—	60%	T_{TXC}	—
T_{OJIT}	Differential Output Clock Jitter	—	—	—	0.25	T_{BIT}	1, 2

Notes:

1. T_{BIT} is 1/10 of Output Clock Period (refer to the applicable Silicon Image HDMI Transmitter Data Sheet).
2. Jitter is defined by the HDMI Specification.

Table 10. DDC and Local I^2C Bus Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
T_{I2CDVD}	SDA Data Valid delay from SCL falling edge	C_L=400 pF	—	—	700	ns	—
F_{DDC}	Operating frequency of TMDS DDC Ports	C_L=400 pF	—	—	400	KHz	1
F_{I2C}	Operating frequency of Local I^2C Port	C_L=400 pF	—	—	400	KHz	2

Notes:

1. DDC (DSDA*n*/DSCL*n*) I^2C ports meet Standard-mode I^2C timing requirements to 400 KHz.
2. Local (CSDA/CSCL) I^2C port meets Standard-mode I^2C timing requirements to 400 KHz.

Pin Descriptions

HDMI Receiver Port Pins

Name	Pin	Type	Dir	Description
R0X0P	68	TMDS	Input	TMDS input Port 0 data pair.
R0X0N	67			
R0X1P	70			
R0X1N	69			
R0X2P	72			
R0X2N	71			
R0XCP	66	TMDS	Input	TMDS input Port 0 clock pair.
R0XCN	65			
R1X0P	4	TMDS	Input	TMDS input Port 1 data pairs.
R1X0N	3			
R1X1P	6			
R1X1N	5			
R1X2P	8			
R1X2N	7			
R1XCP	2	TMDS	Input	TMDS input Port 1 clock pair.
R1XCN	1			
R2X0P	14	TMDS	Input	TMDS input Port 2 data pairs.
R2X0N	13			
R2X1P	16			
R2X1N	15			
R2X2P	18			
R2X2N	17			
R2XCP	12	TMDS	Input	TMDS input Port 2 clock pair.
R2XCN	11			
R3X0P	22	TMDS	Input	TMDS input Port 3 data pairs.
R3X0N	21			
R3X1P	24			
R3X1N	23			
R3X2P	26			
R3X2N	25			
R3XCP	20	TMDS	Input	TMDS input Port 3 clock pair.
R3XCN	19			

HDMI Transmitter Port Pins

Name	Pin	Type	Dir	Description
TX0P	60	TMDS	Output	HDMI Output Port Data. TMDS Low Voltage Differential Signal output data pairs.
TX0N	61			
TX1P	58			
TX1N	59			
TX2P	56			
TX2N	57			
TXCP	62	TMDS	Output	HDMI Output Port Clock. TMDS Low Voltage Differential Signal output clock pair.
TXCN	63			

Input Port Control Pins

Name	Pin	Type	Dir	Description
DSDA0 DSDA1 DSDA2 DSDA3	29 33 39 43	Schmitt 5-V tolerant	Input	DDC I^2C Data for respective port. These pins are true open drain, and do not pull down to ground when power is not applied.
		Open drain	Output	
DSCL0 DSCL1 DSCL2 DSCL3	30 34 40 44	Schmitt 5-V tolerant	Input	DDC I^2C Clock for respective port.
R0PWR5V R1PWR5V R2PWR5V R3PWR5V	32 36 42 46	Power	Input	5 V Port detection input for respective port. Connect to 5 V signal from HDMI input connector. These pins require a 10 Ω series resistor and at least a 1 µF capacitor to ground. A 100 kΩ pull-down resistor is also required for these pins.
HPD0 HPD1 HPD2 HPD3	31 35 41 45	HPD*	Output	Hot Plug Detect Output for respective port. The nominal 1 kΩ output resistance is included in the chip. Connect to the HOTPLUG pin of the HDMI input connector.
DSDA4	47	Schmitt 5-V tolerant	Input	DDC I^2C Data for VGA port. This pin is a true open drain, and does not pull down to ground when power is not applied.
		Open drain	Output	
DSCL4	48	Schmitt 5-V tolerant	Input	DDC I^2C Clock for VGA port.
R4PWR5V	49	Power	Input	5 V Standby power or 5 V power from VGA port (Port 4). If this signal is connected to the VGA cable then it requires a 10 Ω series resistor and at least a 1 µF capacitor to ground. If connected to a local power supply, the resistor is not needed but a capacitor of at least 1 µF is recommended. If not used, this pin should be left unconnected.

***Note:** See the HPD Output Signal section.

Configuration Pins

Name	Pin	Type	Dir	Description
TPWR_CI2CA	55	LVTTL 5-V tolerant	Input	I^2C Slave Address input / Transmit Power Sense Output. At the end of power-on-reset (POR), this pin is used as an input to latch the I^2C sub-address. The level on this pin is latched when the POR transitions from the asserted state to the de-asserted state. After completion of POR, this pin is used as the TPWR output, indicating that the selected HDMI input port is receiving an active TMDS clock. This pin has an internal pull-up to the MICOMVCC33 power supply. If this signal is pulled-down, a 4.7 kΩ resistor should be used.
		LVTTL 8 mA	Output	
CSDA	53	Schmitt 5-V tolerant	Input	Local Configuration/Status I^2C Data. Chip configuration/status is accessed using this I^2C port. This pin is a true open drain, and does not pull down to ground when power is not applied.
		Open drain	Output	
CSCL	54	Schmitt 5-V tolerant	Input	Local Configuration/Status I^2C Clock.
INT	52	LVTTL 8 mA or Open drain	Output	Interrupt Output. Configurable as either an LVTTL push-pull output or an open drain output. This pin has an internal pull-up resistor.
RSVDL RSVDL	10 28	Reserved pin	—	These pins must be tied to ground with a 10 kΩ or less resistor during normal operation. Silicon Image recommends that these pins be connected directly to ground.

CEC Pins

Name	Pin	Type	Dir	Description
CEC_A	50	CEC Compliant 5-V tolerant	Input	HDMI compliant CEC I/O used for interfacing to CEC devices. This signal complies with the CEC specification. It connects to the CEC pins of all HDMI connectors in the system. This pin has an internal pull-up resistor.
		CEC Compliant	Output	
CEC_D	51	LVTTL Schmitt 5-V tolerant	Input	CEC interface to local system. This signal typically connects to a local CPU if the CEC functions are performed by the CPU directly, and not by the CEC controller inside the device. This pin has an internal pull-up resistor.
		Open drain	Output	

Power and Ground Pins

Name	Pin	Type	Description
VCC33	9, 27, 64	Power	Analog and digital core VCC. Must be supplied at 3.3 V.
MICOM_ VCC33	37	Output	During normal mode, this pin provides 3.3 V power to an external microcontroller. The maximum output current is 30 mA. This pin requires a 1µF capacitor to ground.
SBVCC33	38	Power	3.3 V standby power. If 3.3 V standby mode is not used, this pin should be left unconnected.
ePad	ePad	Ground	**Must be connected to ground**. All analog and digital ground planes are tied together to the ePad, which ***must*** be soldered to ground.

Design Guidelines

Downstream HDMI Receiver Equalizer Setting Recommendation

HDMI is normally sent using a standard HDMI cable connected from an HDMI transmitter to an HDMI receiver. Many HDMI receivers contain active cable equalizer circuitry to improve the quality of the HDMI signal that may have been degraded by the cable. However, the HDMI output of the SiI9187B port processor usually interfaces over a relatively short PCB trace with a downstream HDMI receiver that is integrated into the video processor of the display. A cable equalizer circuit when used in this case may actually amplify noise and prevent the receiver from sampling the TMDS data correctly. Therefore, Silicon Image recommends turning off the equalizer in the receiver connected to the output of the SiI9187B port processor, or if the equalizer cannot be disabled, setting it to the minimum value.

Decoupling

Silicon Image recommends that designers include decoupling and bypass capacitors at each power pin in the layout. An example is shown schematically in Figure 12. Place these components as close as possible to the SiI9187B device pins and avoid routing the traces through vias, if possible. Figure 13 shows an example of this layout configuration.

The recommended impedance of the ferrite is 10 Ω or more in the frequency range of 1–2 MHz.

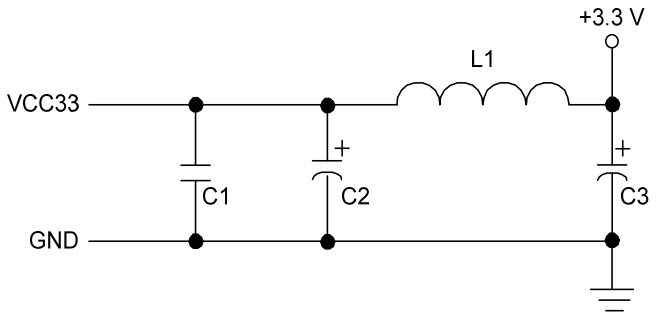

Figure 12. Decoupling and Bypass Schematic

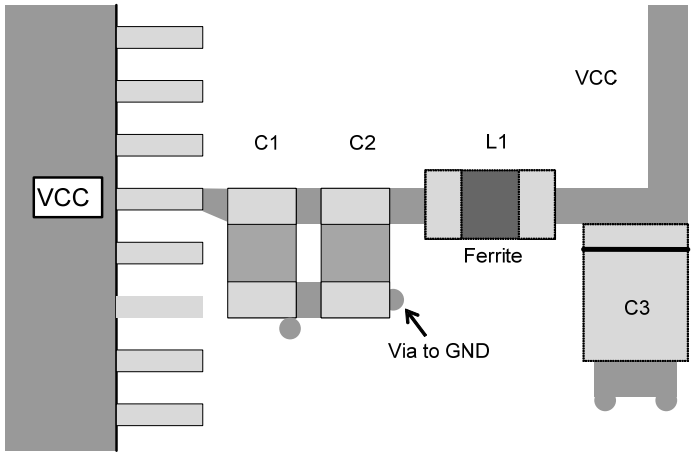

Figure 13. Decoupling and Bypass Capacitor Placement

MICOM_VCC33

MICOM_VCC33 can only be used in 5 V Standby. In this case, the MICOM_VCC33 pin is connected to the output of the internal 5 V to 3.3 V voltage regulator. A 1 µF or greater capacitor connected from this pin to ground is required for all applications, even if MICOM_VCC33 is not used by an external device. Figure 14 shows the loading of this pin.

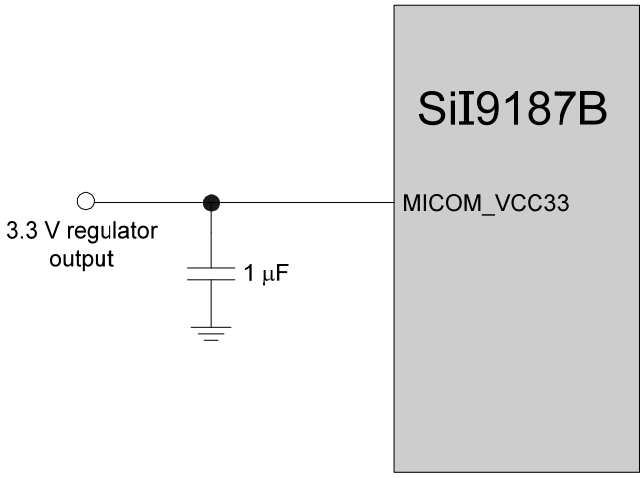

Figure 14. Schematic Showing Load on MICOM_VCC33 Pin

R*n*PWR5V Signals from HDMI Connector +5 V Pin

The R[0–3]PWR5V signals connect to the +5 V signals of the HDMI connectors. These signals carry +5 V from the HDMI source over the HDMI cable.

Whenever the R[0–3]PWR5V signals connect to the HDMI connector, a 1 µF capacitor and a 100 kΩ resistor to ground and 10 Ω ±5% series resistor is required. If a port is not used, then only the 100 kΩ pull-down resistor is required. The schematic for this circuit is shown in the lower part of Figure 15; this connection should be repeated for all HDMI ports.

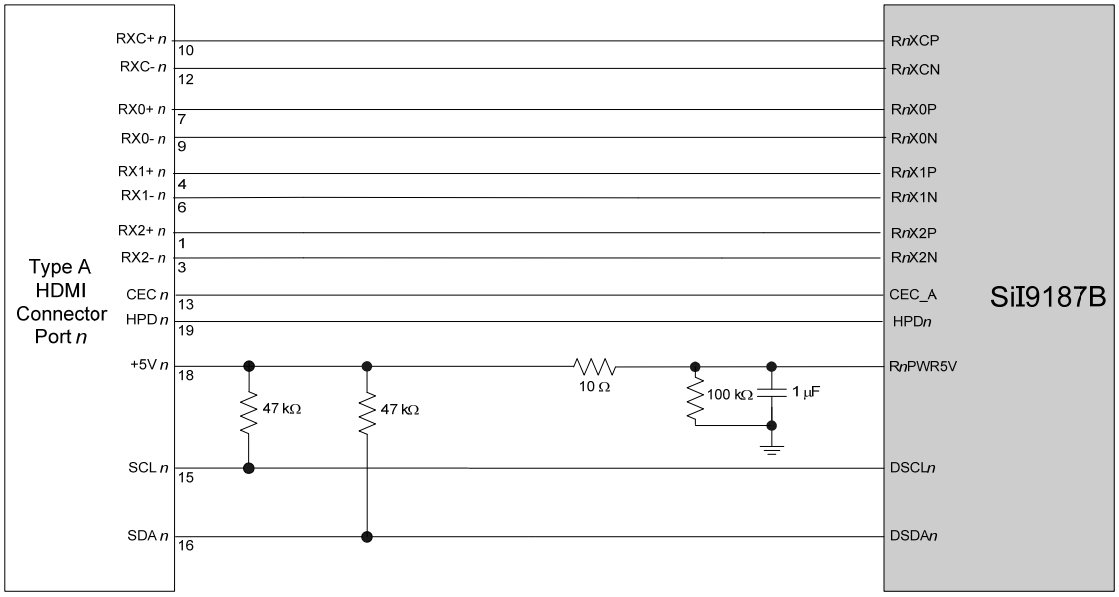

Figure 15. HDMI Port Connection Schematic

R4PWR5V Signal

The R4PWR5V signal can be used for two purposes:

- to supply standby 5 V power from the local system
- to connect to the +5 V of the analog VGA connector.

Whenever the R4PWR5V signal connects to the VGA connector +5 V power, a 1 µF capacitor and 10 Ω ±5% series resistor is required on this signal. If connected to a local power supply the resistor is not needed but a capacitor of at least 1 µF is recommended. If the R4PWR5V is not used, this pin should be left unconnected.

Layout Guidelines

The following layout guidelines help ensure signal integrity, and Silicon Image encourages the board designer to follow them whenever possible.

- Place the input connectors that carry the TMDS signals as close as possible to the chip
- Route the differential lines as directly as possible from the connector to the device when using industry-standard HDMI connectors
- Route the two traces of each differential pair together
- Minimize the number of vias through which the signal lines are routed
- Lay out the two traces of each differential pair with a controlled differential impedance of 100 Ω.

Because Silicon Image devices are tolerant of skews between differential pairs, spiral skew compensation for path length differences is not required.

EMI Considerations

Electromagnetic interference is a function of board layout, shielding, receiver component operating voltage, frequency of operation, and other factors. When attempting to control emissions, it is important not to place any passive components on the differential signal lines, except common-mode chokes and ESD protection devices as required. The differential signaling used in HDMI is inherently low in EMI if the routing recommendations noted in the Layout Guidelines section are followed.

The PCB ground plane should extend unbroken under as much of the port processor chip and associated circuitry as possible.

Package Information

ePad Requirements

The SiI9187B HDMI Port Processor is packaged in a 72-pin 10 mm x 10 mm QFN package with an ExposedPad™ (ePad) that is used for the electrical ground of the chip and for improved thermal transfer characteristics. The ePad dimensions are 4.7 mm x 4.7 mm with a tolerance of ±0.15 mm. Soldering the ePad to the ground plane of the PCB is ***required*** to meet package power dissipation requirements at full speed operation and to connect the chip circuitry to electrical ground. A clearance of at least 0.25 mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid electrical shorts.

The thermal land area on the PCB can use thermal vias to improve heat removal from the package. These thermal vias can double as ground connections, attaching internally in the PCB to the ground plane. An array of vias can be designed into the PCB beneath the package. For optimum thermal performance, Silicon Image recommends that the via diameter be 12 to 13 mils (0.30 to 0.33 mm) and the via barrel be plated with 1-ounce copper to plug the via. This plating helps avoid solder wicking inside the via during the soldering process, which can result in voids in solder between the exposed pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be tented with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1 mm) larger than the via diameter.

Package stand-off is also a consideration. For a nominal stand-off of approximately 0.1 mm the stencil thickness of 5 to 8 mils should provide a good solder joint between the ePad and the thermal land.

Figure 16 on the next page shows the package dimensions of the SiI9187B package.

Package Dimensions

These drawings are not to scale.

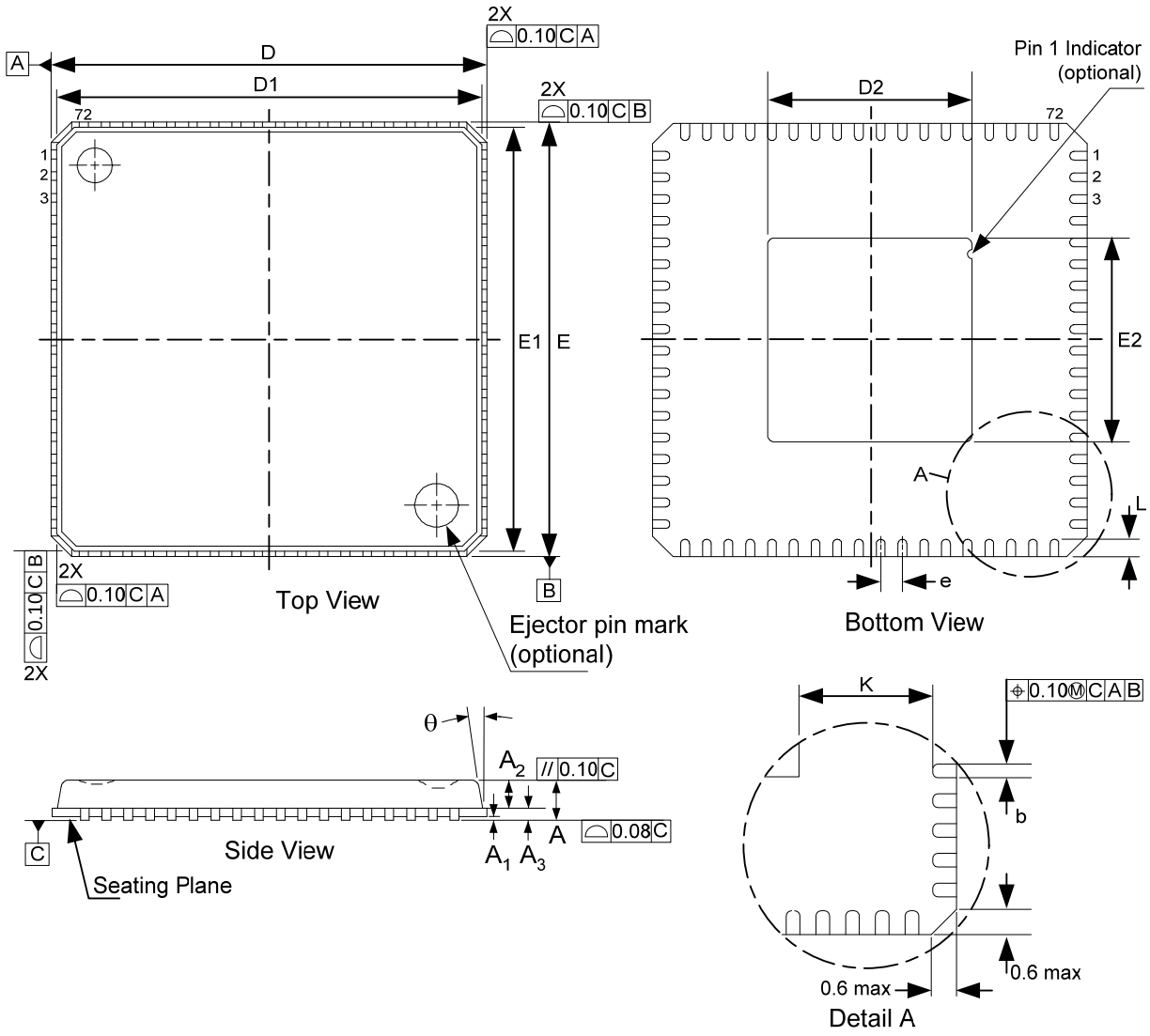

Figure 16. Package Diagram
JEDEC Package Code MO-220

Item	Description	Min	Typ	Max
A	Thickness	—	0.85	0.90
A1	Stand-off	0.00	0.01	0.05
A2	Body thickness	—	0.65	0.70
A3	Base thickness		0.20 REF	
D	Footprint		10.00 BSC	
E	Footprint		10.00 BSC	
D1	Body size		9.75 BSC	
E1	Body size		9.75 BSC	

Item	Description	Min	Typ	Max
D2	ePad size	4.55	4.70	4.85
E2	ePad size	4.55	4.70	4.85
b	Plated lead width	0.18	0.23	0.30
e	Lead pitch		0.50 BSC	
K	ePad-to-pin clearance	0.20	—	—
L	Lead foot length	0.30	0.40	0.50
θ	Lead foot angle	—	—	14°

Marking Specification

This drawing is not to scale.

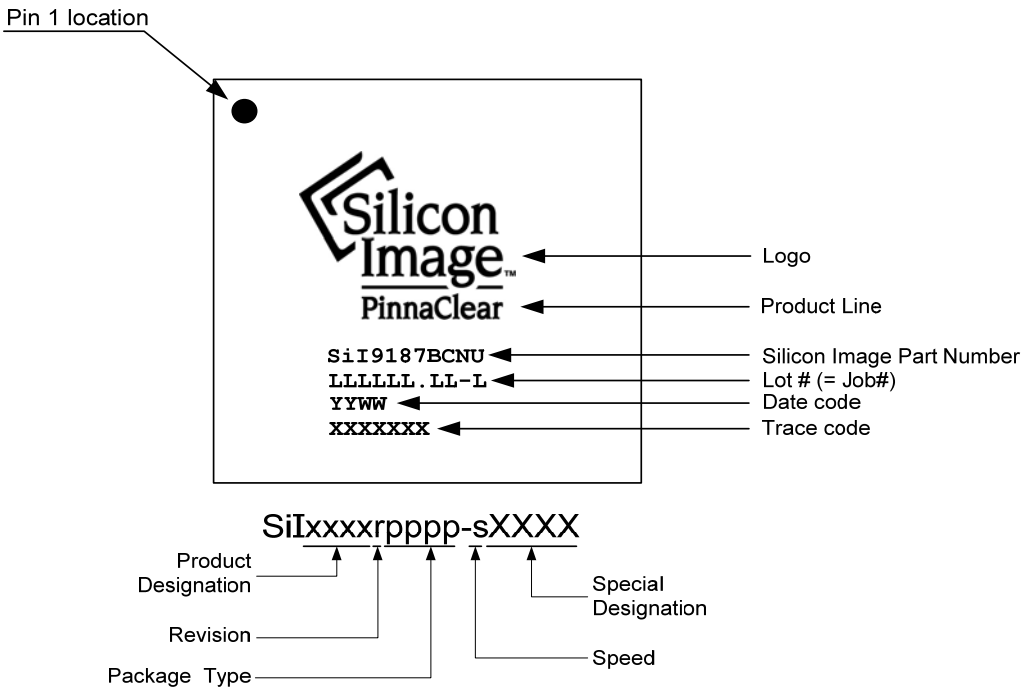

Figure 17. Marking Diagram

Ordering Information

Production Part Numbers:

Device	Part Number
Standard	SiI9187BCNU

The universal package may be used in lead-free and ordinary process lines.

References

Standards Documents

Table 9 lists the abbreviations of the standards mentioned in this document. Contact the responsible standards groups listed in Table 10 for more information on these specifications.

Table 9. Referenced Documents

Abbreviation	Standards publication, organization, and date
HDMI	*High Definition Multimedia Interface*, Revision 1.3a, HDMI Consortium; November 2006
HCTS	*HDMI Compliance Test Specification*, Revision 1.3c, HDMI Consortium; July 2008.
HDCP	*High-bandwidth Digital Content Protection*, Revision 1.3, Digital-Content Protection, LLC; December 2006.
E-EDID	*Enhanced Extended Display Identification Data Standard*, Release A Revision 1, VESA; Feb. 2000.
E-DID IG	*VESA EDID Implementation Guide*, VESA; June 2001.
EDDC	*Enhanced Display Data Channel Standard*, Version 1, VESA; September 1999.

Table 10. Standards Groups Contact Information

Standards Group	Web URL	e-mail	phone
ANSI/EIA/CEA	http://global.ihs.com	global@ihs.com	800-854-7179
VESA	http://www.vesa.org	—	408-957-9270
DVI	http://www.ddwg.org	ddwg.if@intel.com	—
HDCP	http://www.digital-cp.com	info@digital-cp.com	—
HDMI	http://www.hdmi.org	admin@hdmi.org	—

Silicon Image Documents

Table 11 lists Silicon Image documents that are available from your Silicon Image sales representative.

Table 11. Silicon Image Publications

Document	Title
SiI-PR-1038	*SiI9287B and SiI9187B Port Processors Programmer's Reference*
SiI-PR-0041	*CEC Programming Interface (CPI) Programmer's Reference*

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