Quasi-Resonant PWM Flyback Controller with Frequency Swapping and Integrated Protections

REV. 00

General Description

The LD5521D integrates a quasi-resonant PWM control function into a SOT-26 package. It takes less components counts or circuit space, especially ideal for those total solutions of low cost.

The implemented functions include low startup current, green-mode power-saving operation, leading-edge blanking of the current sensing and internal soft driving. It also features more protections like OLP (Over Load Protection) and OVP (Over Voltage Protection) to prevent circuit damage occurred under abnormal conditions.

Furthermore, the QR jitter function could reduce the noise level and thus helps the power circuit designers to easily deal with the EMI filter by spending minimum amount of component cost and developing time.

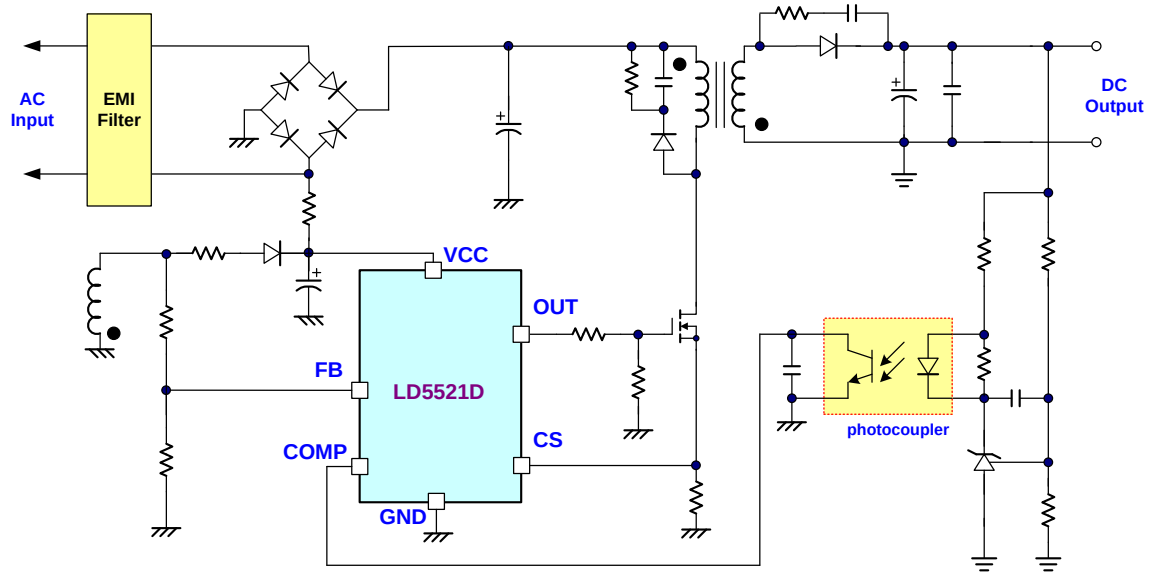
Features

- Secondary-side feedback control with quasi-resonant operation
- Low startup current (<5μA)
- 0.5mA ultra-low operating current at light load
- 130kHz maximum switching frequency
- Current mode control with cycle-by-cycle current limit
- Green mode control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS pin
- VCC OVP (Over Voltage Protection)
- Adjustable OVP (Over Voltage Protection) on FB pin.
- Output short protection by FB pin.
- OLP (Over Load Protection)
- Internal OTP (Over Temperature Protection)
- 250mA/-500mA driving capability

Applications

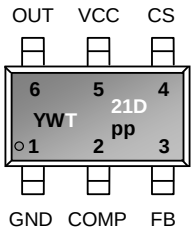
- Switching AC/DC Adaptor

Typical Application



Pin Configuration

SOT-26 (TOP VIEW)



YY, Y : Year code (D: 2004, E: 2005…..)
WW, W : Week code
PP : Production code
T21D : LD5521D

Ordering Information

Part number	Package	TOP MARK	Shipping
LD5521D GL	SOT-26	YWT/21D	3000 /tape & reel

The LD5521D is ROHS compliant/Green Packaged.

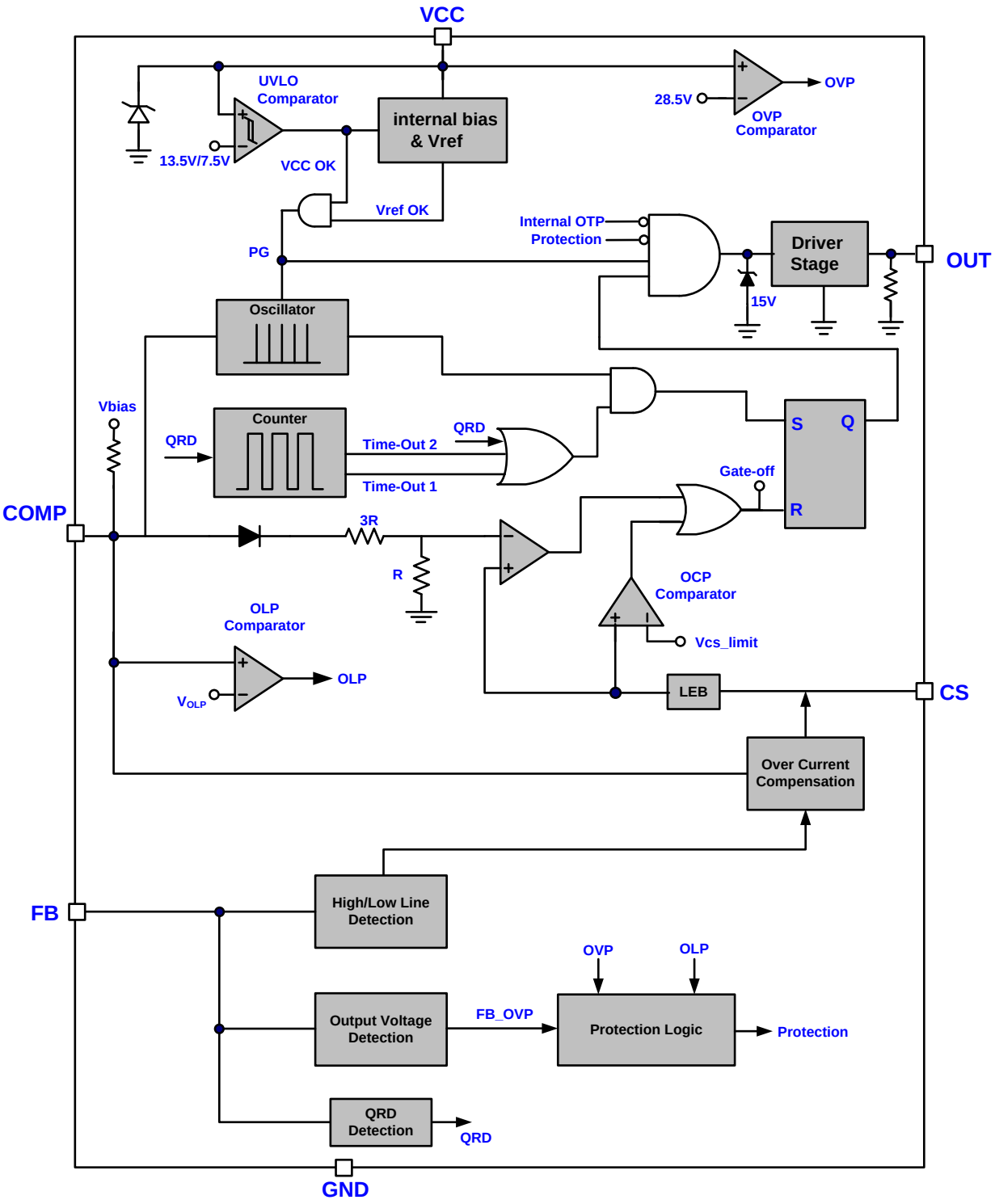
Protection Mode

Switching Freq.	VCC OVP	FB_OVP	OLP
130kHz	Auto	Latch	Auto

Pin Descriptions

PIN	NAME	FUNCTION
1	GND	Ground
2	COMP	Output of the error amplifier for voltage compensation
3	FB	Auxiliary voltage sense, brown in/out and Quasi Resonant detection
4	CS	Current sense pin, connect to sense the MOSFET current
5	VCC	Supply voltage pin
6	OUT	Gate drive output to drive the external MOSFET

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC,	-0.3V ~ 30V
OUT	-0.3V ~ VCC
COMP, FB, CS	-0.3V~ 6V
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C ~ 150°C
Package Thermal Resistance (SOT-26, θ_{JA})	200°C/W
Power Dissipation (SOT-26, at Ambient Temperature = 85°C)	200mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5 KV
ESD Voltage Protection, Machine Model	250 V

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
Supply VCC Voltage	8.0	26.5	V
VCC Capacitor	3.3	10	μF
Start-up resistor Value (AC Side, Half Wave)	400K	2M	Ω
Comp Pin Capacitor	1	10	nF
CS Pin Capacitor Value	47	470	pF

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF~0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible
2. It's also essential to connect a capacitor to COMP to filter out the undesired switching noise for stable operation.
3. The small signal components should be placed close to IC pin as possible.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, VCC=15.0V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage (VCC Pin)						
Startup Current	*	I_{CC_ST}			5	μA
Operating Current (with 1nF load on OUT pin)	*V_{COMP}=0V, OUT=1nF	I_{CC_OP1}		0.5		mA
	*V_{COMP}=3V, OUT=1nF	I_{CC_OP2}		1.5		mA
	*OLP Auto	I_{CC_OPA2}		0.55		mA
Holding Current	*VCC=10V	I_{CC_OPL2}		500		μA
UVLO(OFF)		V_{CC_OFF}	6.5	7.5	8.5	V
UVLO(ON)		V_{CC_ON}	12.5	13.5	14.5	V
Latch-Off Release Voltage		PDR	3.6	4.6	5.6	V
VCC OVP Level		V_{CC_OVP}	27	28.5	29.5	V
OVP pin de-bounce time	*Cannot share with QRD OVP counter	T_{D_VCCOVP}		8		Cycle
Voltage Feedback (COMP Pin)						
Short Circuit Current	V_{COMP}=0V	I_{COMP}	0.1	0.125	0.15	mA
Open Loop Voltage	COMP pin open	V_{COMP_OPEN}	5	5.3	5.6	V
Maximum Frequency Mode	*	V_{COMP_FMAX}		2.4		V
Green Mode Threshold	*	V_G		2		V
Burst Mode, V_{burst}	*	V_{ZDC}		1.5		V
	*Hysteresis	V_{ZDCH}		100		mV
Maximum OCP Compensation Current	*	I_{OCP_MAX}		200		μA
OCP Current Threshold	*	V_V		2.3		V
Current Sensing (CS Pin)						
Maximum Input Voltage		V_{CS_LIMIT}	0.49	0.52	0.55	V
Leading Edge Blanking Time	*	T_{LEB}		350		ns
Input impedance	*	Z_{CS}	1			MΩ
Delay to Output	*	T_{PD}		80		ns
BNO Protection (FB Pin)						
Brown In Trip Level		I_{BNI}	85	95	101.5	μA
Brown Out Trip Level		I_{BNO}	79	85	93.5	μA
Brown In/Out Hysteresis	*	I_{BNIO_HYS}	6			μA
Brown Out De-bounce Time	V_{COMP}=3V	T_{DB_BNO}	46	60	64	ms

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
QRD (Quasi Resonant Detection, FB Pin)						
OVP Trip voltage Level		V_{FB_OVP}	3.4	3.5	3.6	V
OVP De-bounce Cycle	*	T_{FB_OVP}		8		Cycle
QRD Trip Level	*	V_{QRD}		100		mV
QRD Delay Time	*	T_{QRD}		100		ns
QR Mode Time Out 1	*FT checking	T_{QR_TO1}		5		μs
Max Frequency Clamp Time Out 2	*	T_{QR_TO2}		150		μs
QR Maximum Frequency	*	$F_{QR\_MAX\_LL}$		130		kHz
Frequency Swapping	*	F_{SW_MOD}		±12%		kHz
Green Mode Frequency	*	F_{SW_GREEN}		25	27	kHz
Temp. Stability	*	F_{SW_TS}		3	5	%
Voltage Stability	*(VCC=9V~24V)	F_{SW_VS}			1	%
Maximum ON Time						
Maximum On Time	*(-20℃ ~125℃)	T_{ON_MAX}		18		μs
Gate Drive Output (OUT Pin)						
Output Low Level	*VCC=15V, I_O=20mA	V_{OL}			1	V
Output High Level	VCC=15V, I_O=20mA	V_{OH}	8		15	V
Rising Time	*VCC=15V C_L=1000pF	T_r		200	350	ns
Falling Time	*VCC=15V C_L =1000pF	T_f		80	150	ns
Output High Clamp Level	*VCC=18V	V_{O_CLAMP}		14		V
Soft Start						
Soft Start Time	*V_{CS_OFF} from 0.2V to 0.5V	T_{SS}		5		ms
Open Loop Protection						
OLP Trip Level		V_{OLP}	4.3	4.5	4.7	V
OLP delay time	*After soft-start	T_{D_OLP}		70		ms
On Chip OTP (Over Temperature)						
OTP Level (2)	*	T_{INOTP}		140		°C
OTP Hysteresis (2)	*	T_{INOTP_HYS}		30		°C

Notes:

1. *: Guaranteed by design.
2. The threshold temperature for enabling the output again and resetting the latch after OTP has been activated.

Typical Performance Characteristics

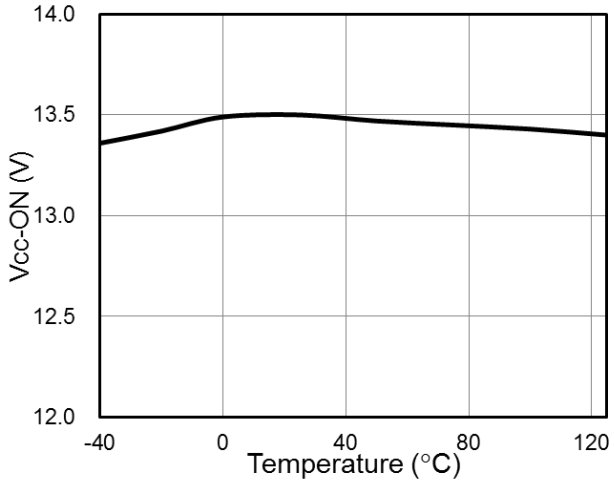


Fig. 1 UVLO on level vs.Temperature

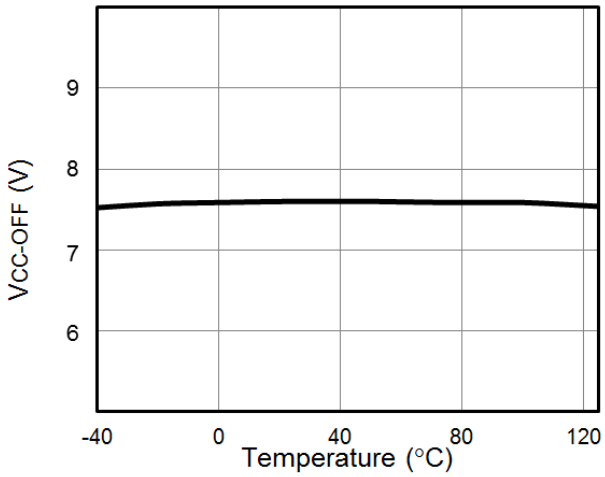


Fig. 2 UVLO off level vs.Temperature

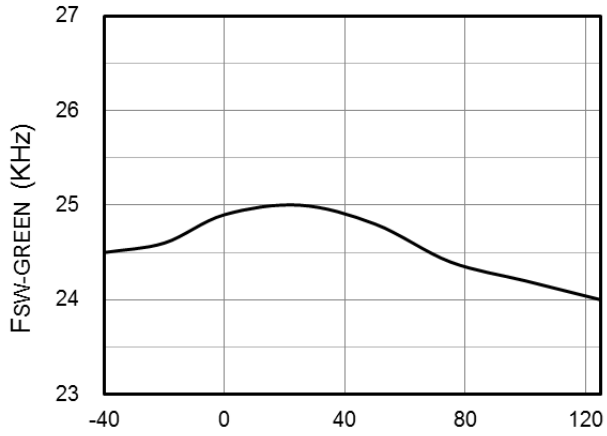


Fig. 3 Green Mode Frequency vs.Temperature

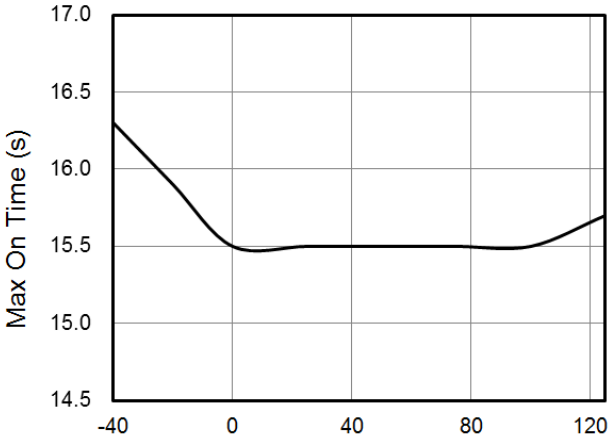


Fig. 4 Max On Time vs.Temperature

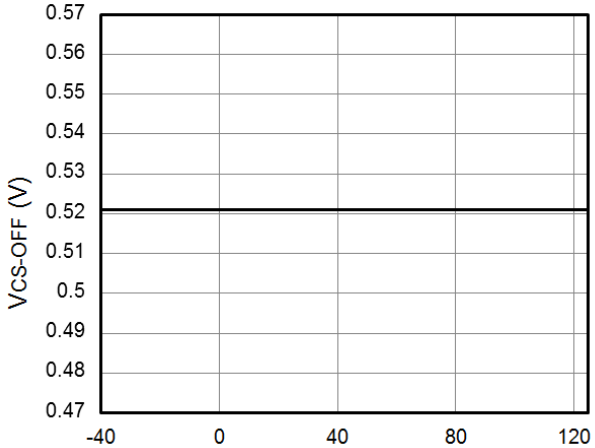


Fig. 5 VCS Limit level vs.Temperature

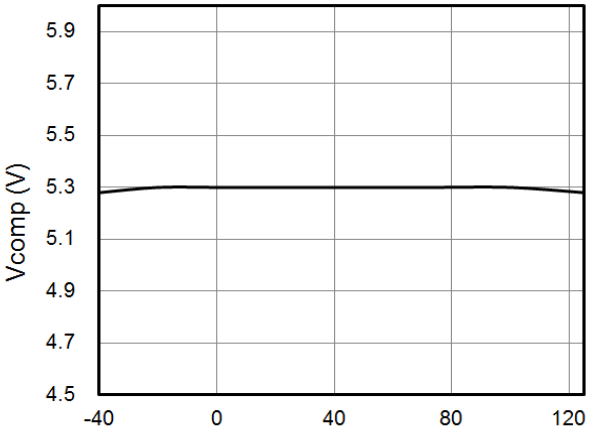


Fig. 6 Open Loop Voltage Level vs.Temperature

Application Information

Operation Overview

The LD5521D meets the green-power requirement and is intended for the use in those modern switching power suppliers and adaptors that demand higher power efficiency and power-saving by QR control. It integrated more functions to reduce the external components counts and the size. Its major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the LD5521D PWM controllers and further to drive the power MOSFET. As shown in Fig. 7, a hysteresis is built in to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16.0V and 7.5V, respectively.

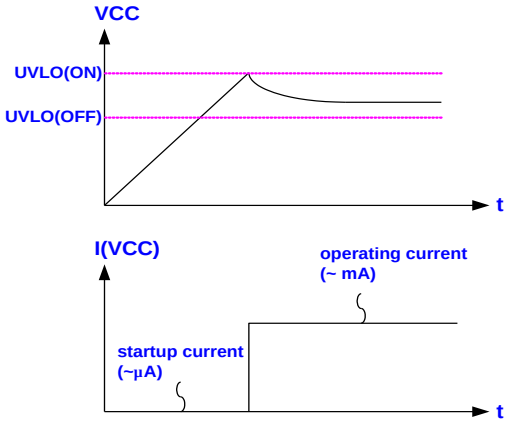


Fig. 7

Startup Current and Startup Circuit

The typical startup circuit to generate the LD5521D VCC is shown in Fig. 8. During the startup transient, the VCC is lower than the UVLO threshold thus there is no gate pulse produced from LD5521D to drive power MOSFET. Therefore, the current through R1 will provide the startup current and to charge the capacitor C1. Whenever the VCC voltage is high enough to turn on the LD5521D and further to deliver the gate drive signal, the supply current is provided from the auxiliary winding of the transformer.

Lower startup current requirement on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current of LD5521D is only 5μA. If a higher resistance value of R1 is chosen, it usually takes more time to start up. To select the value of R1 and C1 carefully will optimize the power consumption and startup time.

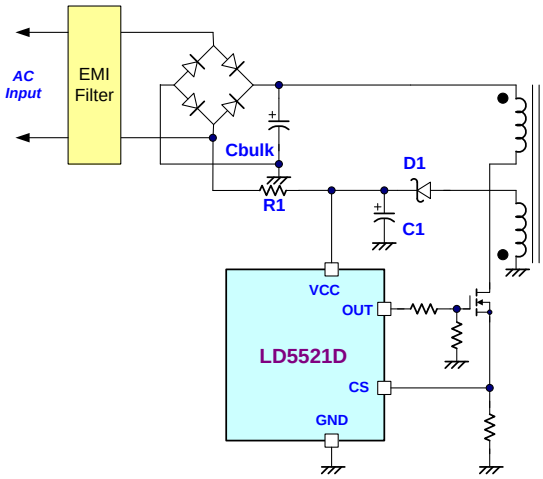


Fig. 8

QR Mode Detection

The transformer will be demagnetized after the main power MOSFET turns off. A quasi resonant signal will be detected from auxiliary winding by FB pin through the external resister.

As soon as the current of the secondary side diode is down to zero during MOSFET-off period, the transformer's core is demagnetized completely. V_{DS} of MOSFET will resonate in discontinuous current mode. The resonance frequency (F_{QR}) will be obtained as below.

$$F_{QR} = \frac{1}{2\pi\sqrt{L_m * C_R}} (Hz)$$

L_M = Inductance of primary winding

C_R = Resonance equivalent parasitic capacitance

If V_{DS} voltage falls to resonant valley level from max plateau value, the QRD comparator will be tripped while FB pin voltage is close to 100mV.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 at the secondary side through the photo-coupler to the COMP pin of the LD5521D. Similar to UC3842, the LD5521D would without voltage offset to feed the voltage divider at the ratio of RA and RB, that is,

$$V_{(PWM_{COMPARATOR})} = \frac{R}{3R+R} \times V_{COMP}$$

A pull-high resistor is embedded internally and therefore no external one is required.

Current Sensing, Leading Edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. The LD5521D detect the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin sets at 0.5V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.5V}{R_{CS}}$$

A 350nS leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. In the low power application, if the total pulse width of the turn-on spike is less than 250nS and the negative spike on the CS pin doesn't exceed -0.3V, it could remote the R-C filter (as shown in Fig. 9).

However, the total pulse width of the turn-on spike is decided by the output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter (as shown in Fig. 10) for higher power application to avoid the CS pin being damaged by the negative turn-on spike.

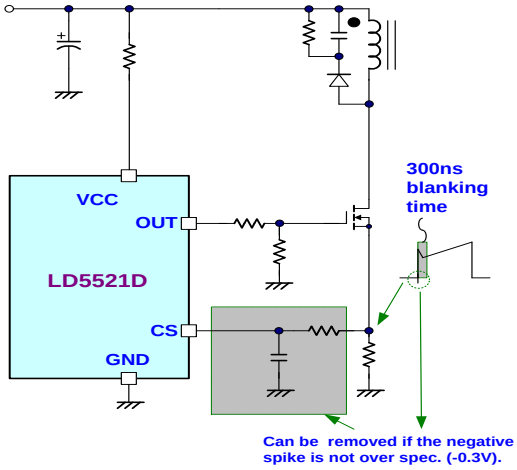


Fig. 9

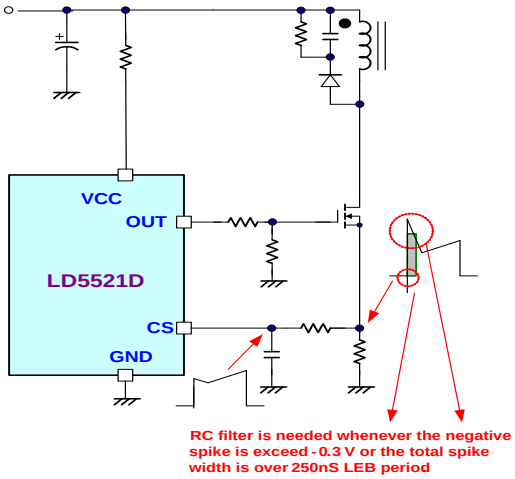


Fig. 10

Output Stage and Maximum on Time

An output stage of a CMOS buffer, with typical 250mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum on time of LD5521D is limited to 18μs to limit the minimum frequency of the system.

Maximum Switching Frequency Clamp

According to the QR operation principle, the switching frequency is inversely proportional to the output power. Therefore, as the output power decreases, the switching

frequency can become rather high without limiting. The maximum switching frequency of LD5521D is clamped at 130 kHz internally to provide the optimized operations by considering the EMI performance, thermal treatment, component sizes and transformer design.

OVP (Over Voltage Protection) on VCC - Auto Recovery

The V_{GS} ratings of the nowadays power MOSFETs are often limited up to max. 28.5V. To prevent the V_{GS} from the fault condition, LD5521D is implemented with an OVP function on VCC. Whenever the VCC voltage is higher than the OVP threshold voltage, the output gate drive circuit will be shutdown simultaneously thus to stop the switching of the power MOSFET until the next UVLO(ON).

The VCC OVP function in LD5521D is an auto-recovery type protection. The Fig. 11 shows its operation.

On the other hand, if the OVP condition is removed, the VCC level will get back to normal level and the output will automatically return to the normal operation.

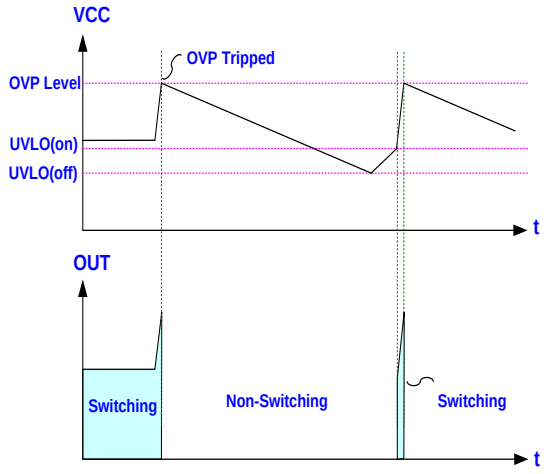


Fig.11

Over Load Protection (OLP) - Auto Recovery

To protect the circuit from damage due to over-load condition and short or open-loop condition, the LD5521D is implemented with smart OLP function. It also features auto –recovery function, see Fig. 12 for the waveform. In case of fault condition, the feedback system will force the voltage loop toward the saturation and then pull the voltage high on COMP pin (VCOMP). When the V_{COMP} ramps up to the OLP threshold of 4.5V and continues over OLP delay time, the protection will be activated and then turn off the gate output to stop the switching of power circuit.

With the protection mechanism, the average input power will be minimized to remain the component temperature and stress within the safe operating area.

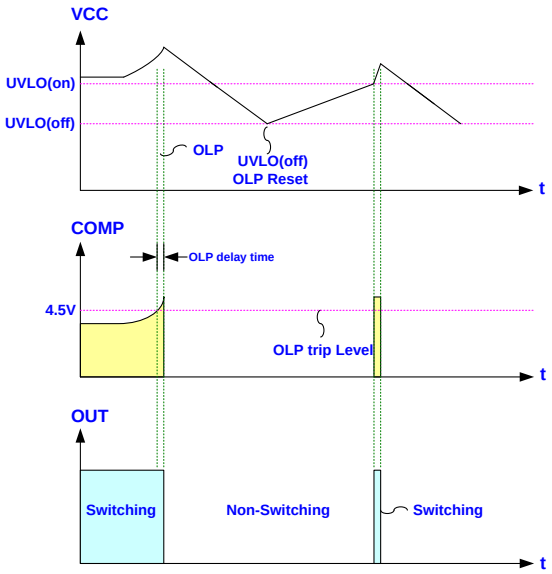


Fig. 12

Adjustable Over Current Compensation (FB Pin)

For compensating the differential input current from high/low line conditions on current sensing resistor, LD5521D mirrors compensation current I_{OCP} from I_{FB} to CS pin. The relationship of compensation current I_{OCP} and I_{FB} is expressed by following equation and shown in Fig. 13.

$$I_{OCP} = K \times I_{FB}, \text{ where } K = 0.5$$

K is the mirror current ratio of FB pin, and the I_{OCP} follows to the input voltage.

The compensation current I_{OCP} supplies an offset voltage by external resistor R_{OCP}, which is series between the current sensing resistor R_S and CS pin. By selecting a proper value of the resistor R_{OCP} in series with the CS pin, the amount of compensation can be adjusted.

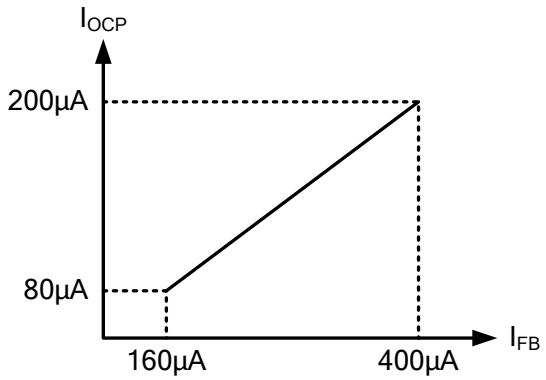


Fig. 13

FB Pin Over-Voltage Protection (FB OVP) - Latch

An output overvoltage protection is implemented in the LD5521D. The auxiliary winding voltage can be reflected from secondary winding, in which the FB pin voltage is proportional to output voltage during the gate off time. OVP is worked by sensing the auxiliary voltage via the divided resistors R2, refereeing to Fig. 14. The equation of FB OVP is shown as follows.

$$R_2 = \frac{R_1 \cdot V_{FB\_OVP}}{V_a - V_{FB\_OVP}} \qquad V_a = \frac{N_a}{N_S} \cdot (V_O + V_F)$$

, where

V_{FB_OVP} is the FB pin OVP trip voltage level. V_a is the auxiliary winding voltage which reflects from the forward voltage V_F of Schottky diode and output voltage V_O. N_S is turns ration of secondary-side winding.

If V_{FB} overs the FB OVP trip level, the internal counter starts counting 8 cycles, and then LD5521D goes to latch protection mode.

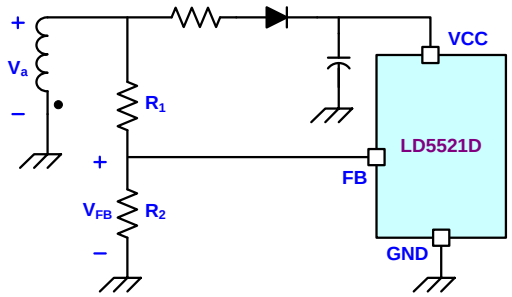


Fig. 14

Oscillator and Switching Frequency

The LD5521D is implemented with Frequency Swapping function which helps the power supply designers to both optimize EMI performance and lower system cost.

Green Mode Operation

By using the green-mode control, the switching frequency can be reduced under the light load condition. This feature helps to improve the efficiency in light load conditions. The green-mode control is Leadtrend Technology's own property.

Fault Protection

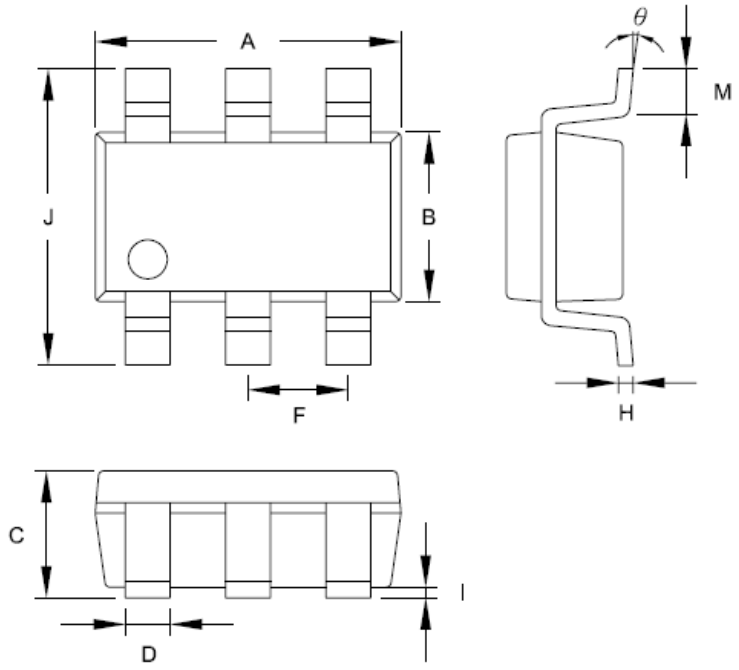
There are several critical protections integrated in the LD5521D to prevent from damage to the power supply. Those damages usually come from open or short conditions on the pins of LD5521D.

In case under such conditions listed below, the gate output will turn off immediately to protect the power circuit.

1. CS pin floating
2. COMP pin floating

Package Information

SOT-26



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-------	1.450	-------	0.057
D	0.300	0.500	0.012	0.020
F	0.95 TYP		0.037 TYP	
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

REV.	Date	Change Notice
00	05/04/2017	Original Specification.

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