High Power Factor Flyback LED Controller with HV Start-up

REV: 01a

General Description

The LD7830 is a HV start-up Flyback PFC controller, specially designed for LED lighting appliances. It operates in transition(TM) mode and integrates with complete protections required for safety and therefore it's an excellent solution to minimize the components counts. Those make it ideal for cost- effective applications.

With HV start-up technology, high power factor and TM control, the start-up time and resistor loss could be minimized efficiently. The circuit can easily achieve PF>0.90 to meet most of the international standard requirements.

With completed protection built inside this IC, such as over voltage protection (OVP), over current protection (OCP), over load protection (OLP), over temperature protection (OTP), and short circuit protection (SCP), It enable the circuit to meet most safety requirements either in normal and abnormal test.

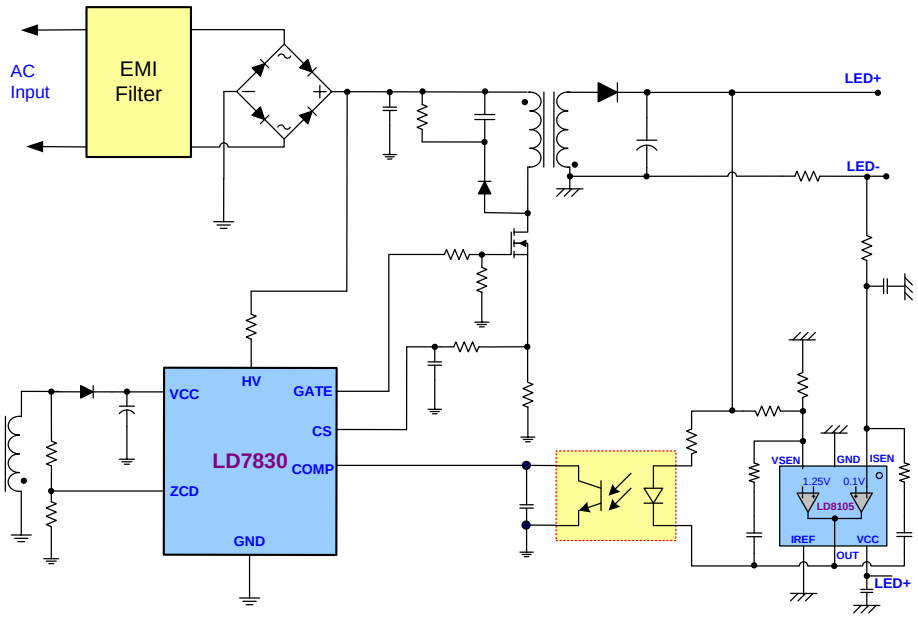
Features

- High voltage (600V) startup circuit
- High Power Factor Flyback PFC controller
- High-efficiency Transition mode operation
- Wide UVLO (16Von and 7.5 Voff)
- VCC OVP (Over Voltage Protection)
- OLP (Over Load Protection)
- OCP (Cycle by cycle current limiting) Vcs=0.5V
- Internal OTP (Over Temperature Protection)
- 500/-800mA Driving Capability
- Internal OTP function

Applications

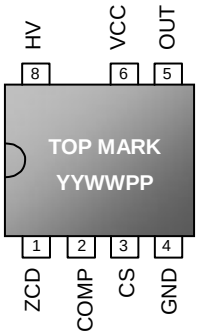
- LED Power Supply
- Flyback PFC Power Supply

Typical Application

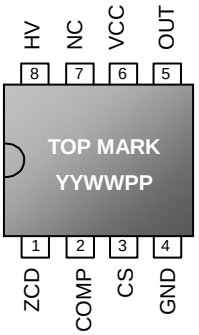


Pin Configuration

SOP-7 (TOP VIEW)



SOP-8 / DIP-8 (TOP VIEW)



YY: Year code
WW: Week code
PP: Production code

Ordering Information

Part number	Package	Top Mark	Shipping
LD7830 GR	SOP-7	LD7830GR	2500 /tape & reel
LD7830 GS	SOP-8	LD7830GS	2500 /tape & reel
LD7830 GN	DIP-8	LD7830GN	3600 /tube /Carton

The LD7830 is green packaged.

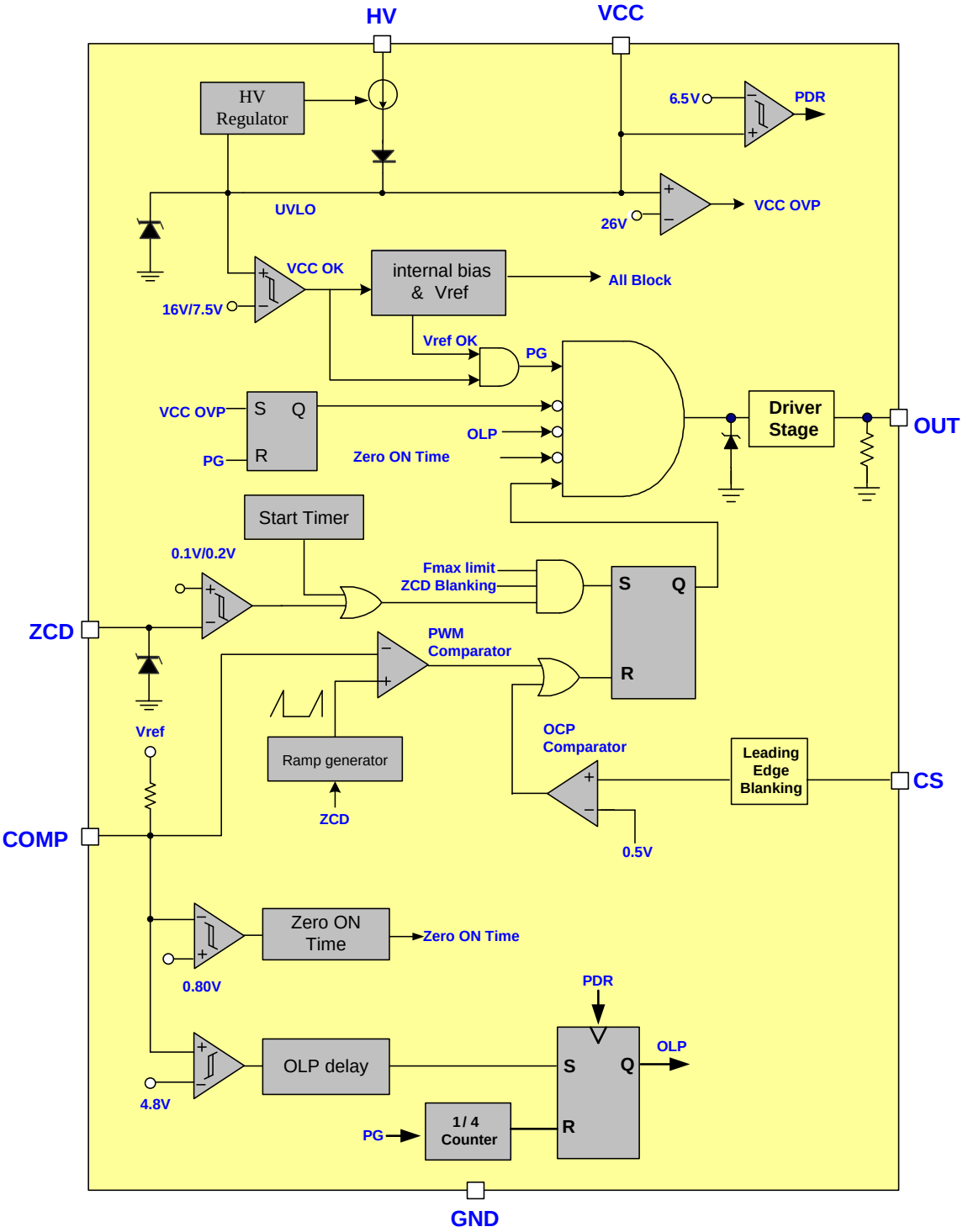
Protection Mode

Part number	VCC OVP	OLP
LD7830	Auto recovery	Auto recovery

Pin Descriptions

Pin	NAME	FUNCTION
1	ZCD	Quasi resonance detector and programmable maximum ON-time.
2	COMP	Feedback pin. Connect a photo-coupler to close the control loop to achieve regulation.
3	CS	Current sense pin, connect it to sense the MOSFET current for OCP
4	GND	Ground
5	OUT	Gate drive output to drive the external MOSFET
6	VCC	Power source VCC pin
7	NC	No connecting.
8	HV	Connect this pin to positive terminal of main bulk cap to provide startup current for controller. Once Vcc is UVLO on, the HV loop will open and turn off internal current source to minimize the power loss.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3 ~30V
High voltage pin, HV	-0.3~600V
OUT	-0.3 ~VCC +0.3V
COMP, CS, ZCD	-0.3 ~6V
Maximum Junction Temperature	150°C
Operating Junction Temperature Range	-40°C to 125°C
Operating Ambient Temperature Range	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8, SOP-7 θ_{JA})	160°C/W
Package Thermal Resistance (DIP-8, θ_{JA})	100°C/W
Power Dissipation (SOP-8, SOP-7, at Ambient Temperature = 85°C)	250mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	400mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (except HV pin)	2.5KV
ESD Voltage Protection, Machine Model	250V
ESD Voltage Protection, Human Body Model (HV pin only)	1KV

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Vcc pin capacitor	4.7	47	μF
Comp pin capacitor	1	10	μF

Electrical Characteristics

(V_{CC}=15.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High voltage Supply(HV Pin)					
High-voltage current Source	VCC=4V , HV=80V	1.0	1.3	1.6	mA
	VCC=9V,HV=80V	2.6	3.1	3.6	mA
Off-state Leakage current	VCC>UVLO(ON), HV=500V	0		35	μA
Supply Voltage (VCC Pin)					
Startup Current	VCC<UVLO ON	55	75	95	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V, ZCD=0		1		mA
	V_{COMP}=3V, ZCD=0		1.45		mA
	V_{CC} OVP		0.3		mA
	OLP		0.3		mA
UVLO (OFF)		6.9	7.5	8.1	V
UVLO (ON)		15.0	16	17.0	V
HV Self Bias (Linear Regulator)		8.1	8.8	9.5	V
De-Latch VCC Voltage	PDR(Power Down Reset)	6.0	6.5	7.0	V
VCC OVP Level		25	26	27	V
Voltage Feedback(Comp Pin)					
Short circuit current	V_{COMP}=0	0.4	0.5	0.6	mA
Open loop voltage		5.0	5.3	5.8	V
OLP Trip Level		4.65	4.8	4.95	V
Zero ON-time Threshold			0.8		V
Zero ON-time Hysteresis			25		mV
OLP Delay Time		225	270	315	ms
OLP De-Latch Counter			4		Cycle
Current Sensing (CS Pin)					
Current Sense Input Threshold Voltage	I_{ZCD}<110μA	0.47	0.5	0.53	V
	I_{ZCD}>440μA	0.322	0.35	0.378	V
Soft Start Time	*		8		ms
Input bias current	V_{CS}=0V~0.5V	0		1.5	μA
LEB time		240	300	360	ns

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Current Detector (ZCD Pin)					
Upper Clamp Voltage	I_{DET}=100μA	5.0	5.6	6.0	V
Lower Clamp Voltage	$I_{DET=}$-2mA	0		-0.35	V
Input Voltage Threshold		0.05	0.1	0.15	V
	Hysteresis	0.05	0.15	0.2	V
Input bias current	V_{ZCD}=1V~4V, OUT=OFF	0.0		1.0	μA
Programming Maximum ON-Time, Ton-max (ZCD Pin)					
Programming Maximum ON-time	ZCD R_{ZCD}=6kΩ,	4.8	5.82	6.8	μs
Maximum ON-time	ZCD R_{ZCD}≥34kΩ,	13.6	16	18.4	μs
Minimum (ON+OFF)-Time					
Minimum (ON+OFF)-Time	Fmax(250kHz),	3.2	4	4.8	μs
Minimum OFF-Time		1.2	1.6	2.0	μs
Gate Drive Output (OUT Pin)					
Output Low Level	V_{CC}=15V, I_{SINK}=20mA	0		0.5	V
Output High Level	V_{CC}=15V, I_{SOURCE}=20mA	10		VCC	V
Output High Clamp Level	V_{CC}=16V		13		V
Rising Time	V_{CC} =15V, CL=1000pF		75	150	ns
Falling Time	V_{CC} =15V, CL=1000pF		25	50	ns
Starter					
Start Timer Period		100	150	200	μs
Internal OTP (Over Temp. Protection)					
OTP Trip level	*		140		°C
OTP Hysteresis	*		30		°C

*: These parameters are guaranteed by design only.

Typical Performance Characteristics

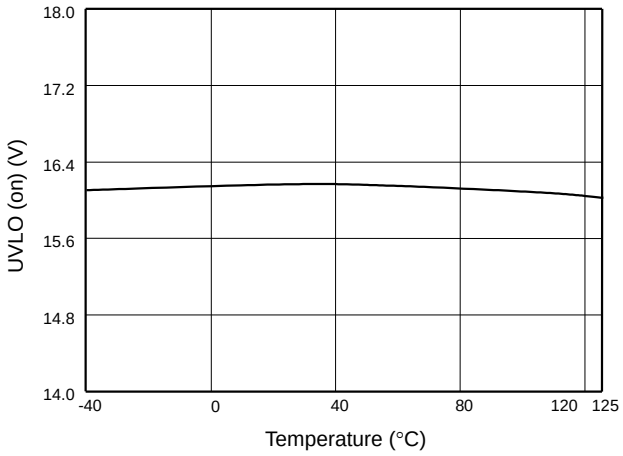


Fig. 1 UVLO (on) vs. Temperature

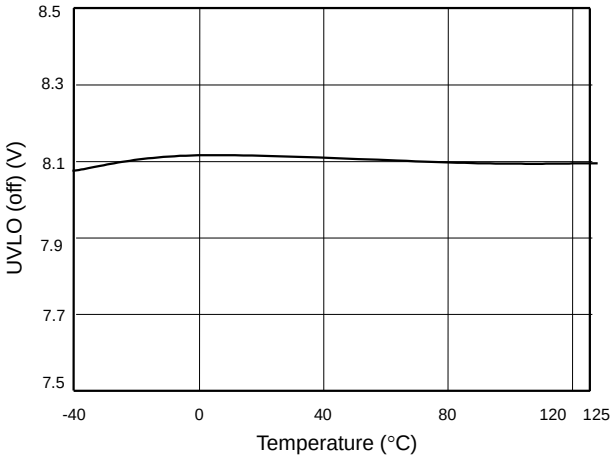


Fig. 2 UVLO (off) vs. Temperature

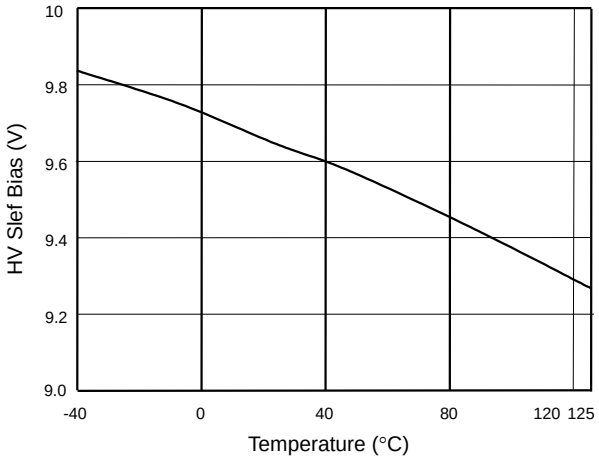


Fig. 3 HV Slef Bias vs. Temperature

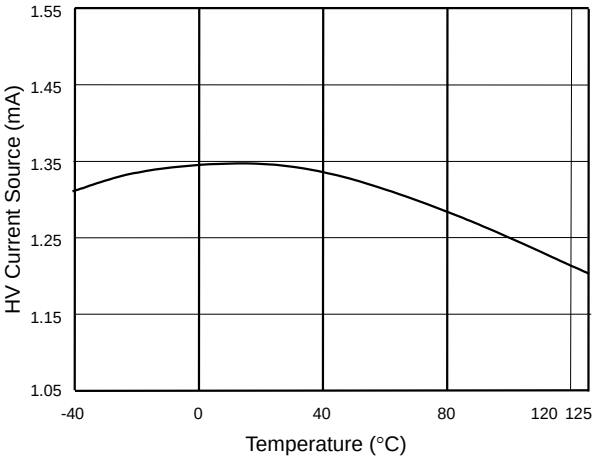


Fig. 4 HV Current source(Vcc=4V) vs. Temperature

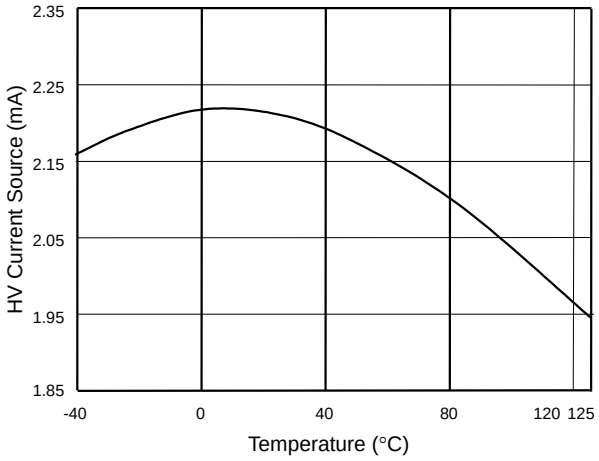


Fig. 5 HV Current source(Vcc=9V) vs. Temperature

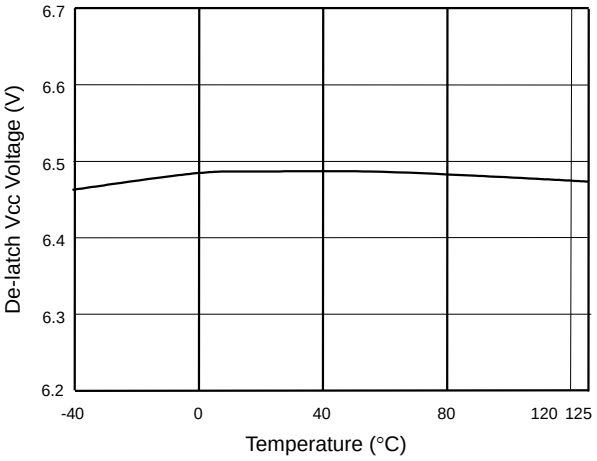


Fig. 6 De-latch Vcc Voltage vs. Temperature

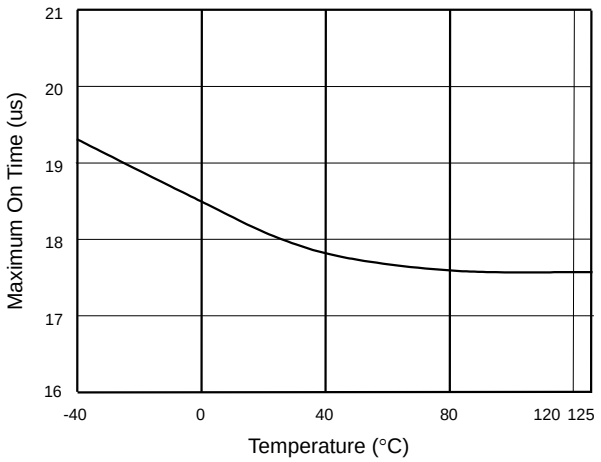


Fig. 7 Maximum On Time vs. Temperature

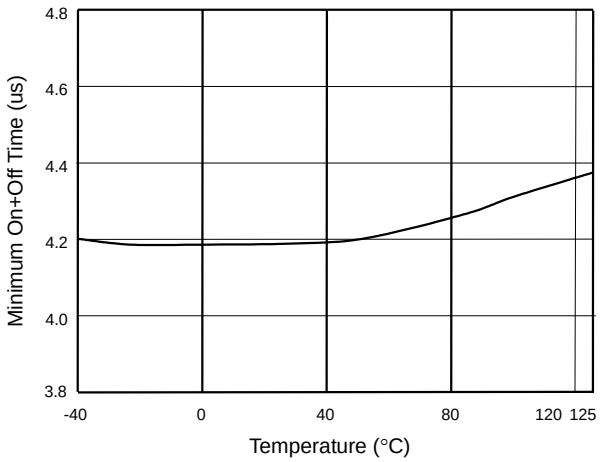


Fig. 8 Minimum On+Off Time vs. Temperature

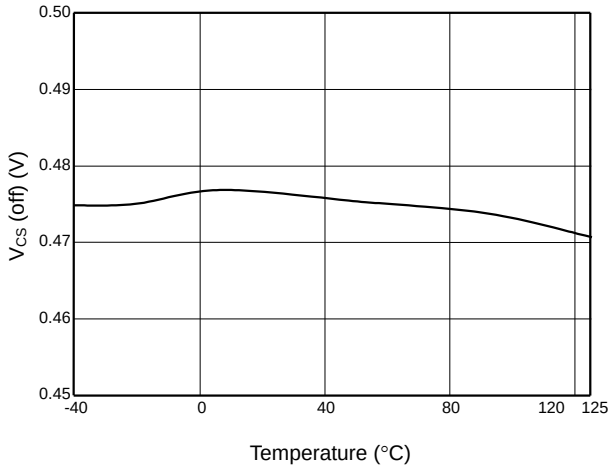


Fig. 9 V_{CS} (off) vs. Temperature

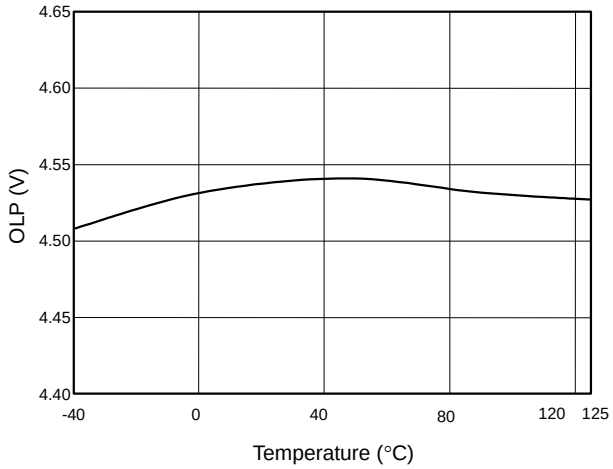


Fig. 10 OLP-Trip Level vs. Temperature

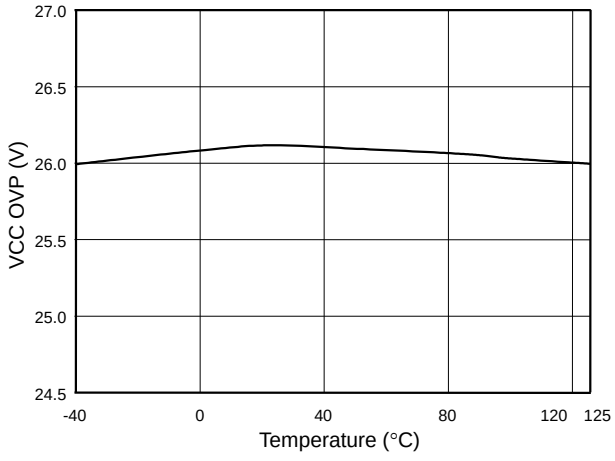


Fig. 11 VCC OVP vs. Temperature

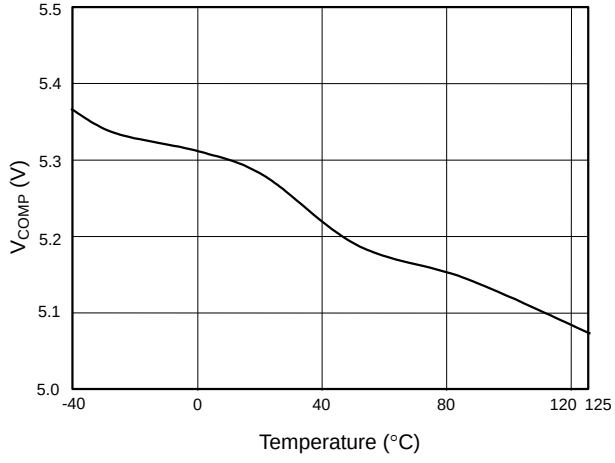


Fig. 12 V_{COMP} open loop voltage vs. Temperature

Application Information

Operation Overview

The LD7830 is an excellent single-stage Flyback PFC controller for LED lighting applications. It integrates more functions to reduce the external components counts and the size. Its major features are described as below.

The LD7830 is a voltage-mode TM PFC controller. The turn-on time of the switch is fixed while the turn-off time is varied in steady state. Therefore, the switching frequency varies in accordance with the input voltage variation. The LD7830 features over load protection, over voltage protection, over current protection, under voltage lockout and LEB of the current sensing. Also, the LD7830 requires no mains voltage sensing unlike what the other traditional current mode PFC controllers behave for power saving.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The traditional circuit provides the startup current through a startup resistor to power up the PWM controller. However, it consumes significant power to meet the power saving requirement. In most cases, startup resistors carry large resistance. And, a larger resistor will spend more time to start up.

To achieve optimized topology, as shown in Fig. 13, LD7830 is implemented with a high-voltage startup circuit to enhance it. During startup, a high-voltage current source sinks current from the full-bridge rectifier to provide the startup current and charge Vcc capacitor C1 at the same time. On condition of VCC below PDR, the charge current will remain at 1.3mA to protect the circuit from being damaged, even in case VCC pin is shorted to ground. In contrast, the charge current will increases to 3.1mA once VCC rises above PDR voltage threshold during start up. Meanwhile, it consumes only 75μA for Vcc supply current, that most of the HV current is reserved to charge the Vcc capacitor. In using such configuration, the turn-on delay time will be almost no difference either in low-line or high-line conditions.

Once the Vcc voltage rises higher than UVLO(on) to power on the LD7830 and further to deliver the gate drive signal, the high-voltage current source will be disabled and the supply current is provided from the auxiliary winding of the transformer. Therefore, it would eliminate the power loss on the startup circuit and perform highly power saving.

An UVLO comparator is embedded to detect the voltage on the Vcc pin to ensure the supply voltage enough to power on the LD7830 PWM controller and in addition to drive the power MOSFET. As shown in Fig. 14, a hysteresis is provided to prevent the shutdown from the voltage dip during startup.

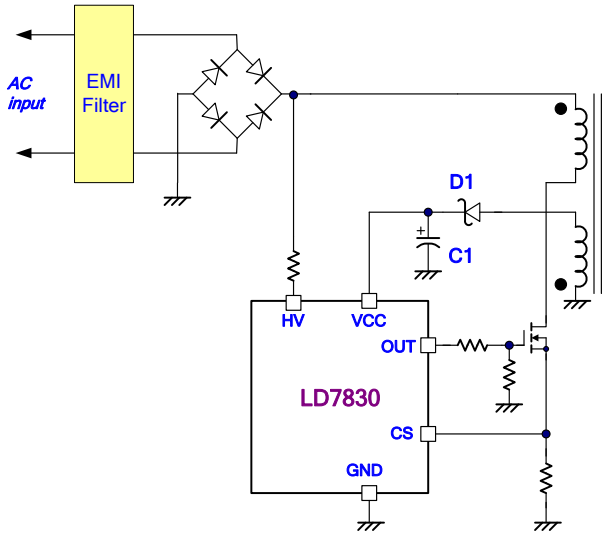


Fig. 13

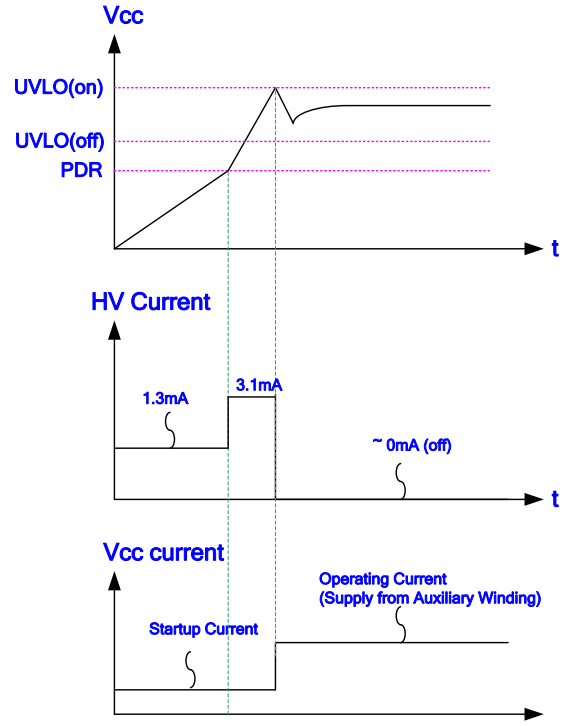


Fig. 14

Ramp Generator Block and Zero Current Detection (ZCD)

Fig. 15 shows typical ramp generator block and ZCD block. The comp pin voltage and the output of the ramp generator block are compared to determine the MOSFET ON-time, as shown in Fig. 16.

A greater comp voltage produces more ON-time. Using an external resistor connected to ZCD pin to set the desired slope of the internal ramp, the user may program the maximum ON-time. Alternatively, the ON-time will also achieve its maximum when COMP pin voltage trip OLP trigger point.

The maximum ON-time should be set according to the condition of the transformer, lowest AC line voltage, and maximum output power. A choice of optimum resistor value would result in best performance.

It shuts down the drive output if COMP pin voltage falls below zero ON-time threshold. This optimizes the efficiency in power saving in most conditions.

The Zero Current Detection block will detect auxiliary winding signal to drive MOSFET as ZCD pin voltage drops to 0.1V. As ZCD pin voltage drop to 0.1V, the current through the transformer is below zero. This feature enables transition-mode operation. The ZCD comparator would not operate if ZCD pin voltage remains at above 0.2V. Once it drops below 0.1V, the zero current detector will act to turn on the MOSFET.

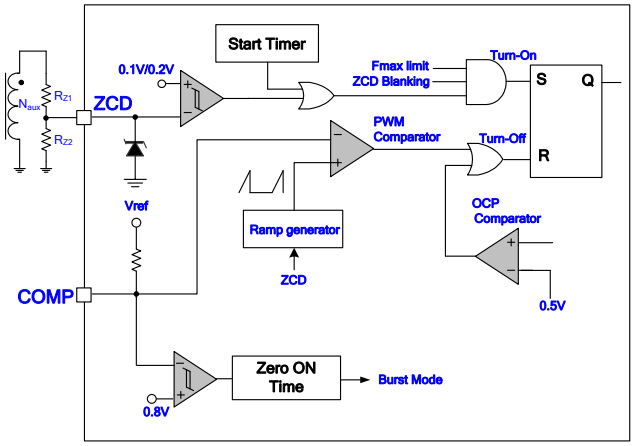


Fig. 15

The 150μs timer generates a MOSFET turn-on signal if the driver output drops to low level for more than 150μs from the falling edge of the driver output. Fig. 16 shows typical ZCD-related waveforms. Since ZCD pin carries some capacitance, it produces some delay to the turn-on time caused from Rz1. During delay time, the junction capacitor of the MOSFET resonates with the primary inductor of the transformer and the drain-source voltage (V_{DS}) decreases accordingly. So, the MOSFET consumes less voltage to turn on and it therefore minimizes the power dissipation.

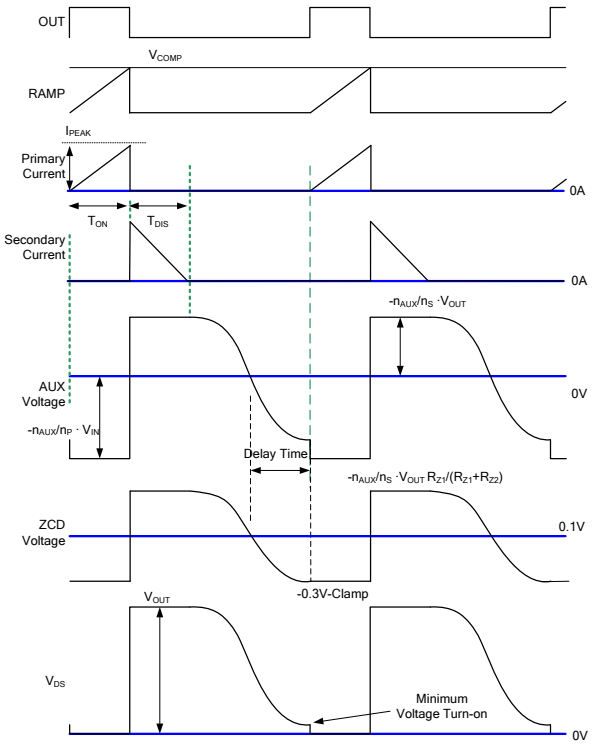
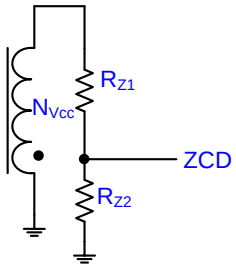


Fig. 16

Programming Maximum ON-time

LD7830 features adjustable maximum ON-time to limit power output in abnormal operation. The selection of maximum ON-time is subject to ZCD resistance as shown in Fig. 17. ZCD resistance can be obtained from below:



$$R_{ZCD} = \frac{R_{Z1} \cdot R_{Z2}}{R_{Z1} + R_{Z2}}$$

Fig. 17

The following table is a suggestion for maximum ON-time setting.

R_{ZCD}	Max. Ton (Typ.)	Suggestion
32k<R_{ZCD}	16μs	36k
28k<R_{ZCD}<32k	12.8μs	30k
24k<R_{ZCD}<28k	10.7μs	26k
20k<R_{ZCD}<24k	9.1μs	22k
16k<R_{ZCD}<20k	8.0μs	18k
12k<R_{ZCD}<16k	7.1μs	14k
8k<R_{ZCD}<12k	6.4μs	10k
R_{ZCD}<8k	5.8μs	6k

High/ Low Line OCP Compensation

LD7830 supports high/low line OCP compensation through aux-winding to reflect the magnitude of input voltage. When gate turns on, ZCD pin will source the current I_{ZCD} to clamp the voltage to zero as shown in Fig.18. According to this current information, OCP trigger level V_{CS-OFF} will be determined by R_{Z1} and input voltage. In order to avoid ZCD pin over rating, I_{ZCD} must be set less than 2mA. $I_{ZCD-max}$ can be calculated as below:

$$I_{ZCD-MAX} = \frac{V_{IN-PK}}{N_P / N_{VCC} \cdot R_{Z1}} < 2mA$$

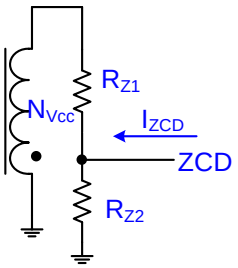


Fig. 18

The relation (typical) of V_{CS-OFF} and I_{ZCD} is shown in Table 1.

I_{ZCD} (μA)	V_{CS-OFF} (V)
160	0.5
160~200	0.475
200~240	0.4625
240~290	0.45
290~350	0.425
350~390	0.4
390~450	0.375
>450	0.35

Table 1

Output Drive Stage

With typical 500mA/-800mA driving capability, an output stage of a CMOS buffer is incorporated to drive a power MOSFET directly. The output voltage is clamped at 13V to protect the MOSFET gate even when the VCC voltage is higher than 13V.

Current Sensing and Leading-edge Blanking

The LD7830 detects the primary MOSFET current from the CS pin, which is for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.5V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.5V}{R_S}$$

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. In the low power application, if the total pulse width of the turn-on spikes is less than and the negative spike on the CS pin doesn't exceed -0.3V, it could eliminated the R-C filter.

However, the total pulse width of the turn-on spike is determined by the output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter for higher power application to avoid the CS pin being damaged by the negative turn-on spike.

Over Load Protection (OLP) - Auto Recovery

To protect the circuit from damage due to overload condition or output short condition, a smart OLP function is implemented in the LD7830 for it. The OLP function is an auto-recovery type protection. Fig. 19 shows the waveforms of the OLP operation. Under such fault condition, the feedback system will force the voltage loop toward saturation and thus pull up the voltage of COMP pin (VCOMP). If the VCOMP trips the OLP threshold of 4.8V and stays for over OLP delay time, the protection will be activated to turn off the gate output and to shut down the switching of power circuit. The OLP delay time is to prevent the false-trigger during the power-on and turn-off transient.

A divided-by-4 counter is implemented to reduce the average power consumption under OLP behavior. Whenever OLP is activated, the output is latched off and the divided-by-4 counter starts to count the number of UVLO(off). The latch will be released if the 4nd UVLO(off) point is counted, and then the output recovers switching again.

By using such protection mechanism, the average input power can be reduced to a very low level so that the component temperature and stress can be controlled within a safe operating area.

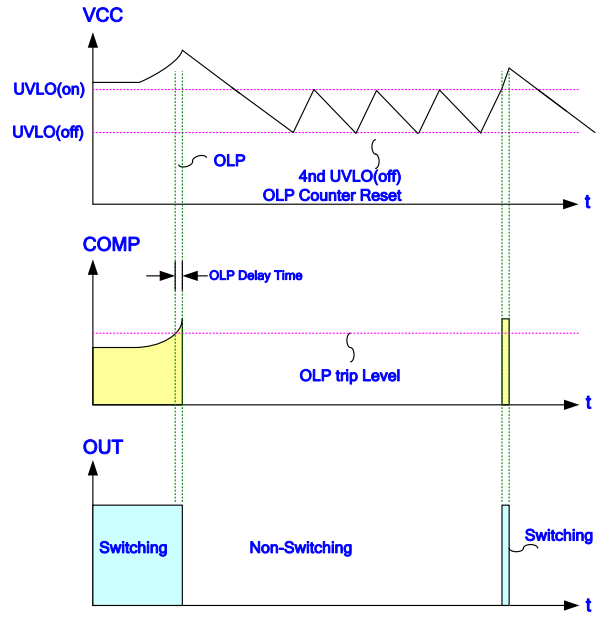


Fig. 19

OVP (Over Voltage Protection) on Vcc

The maximum rating of the VCC pin is limited below 29V. To prevent VCC from the fault condition, the LD7830 is implemented with OVP function on Vcc pin. As soon as the Vcc voltage is over OVP threshold voltage, the output gate drive circuit will be shutdown simultaneously thus to stop the switching of the power MOSFET until the next UVLO(on). The Vcc OVP function of the LD7830 is an auto-recovery protection. The Fig. 20 shows its operation. Upon removal of the OVP condition will resume the Vcc level and the output operation

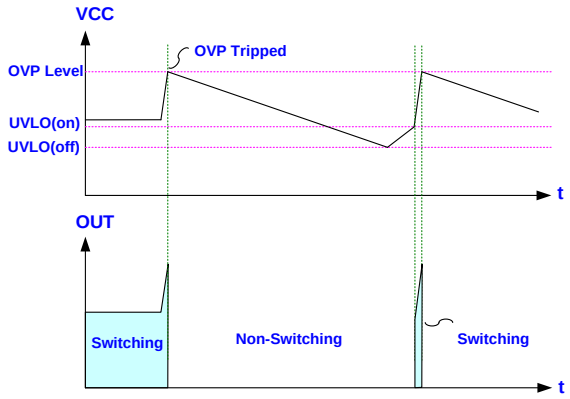


Fig. 20

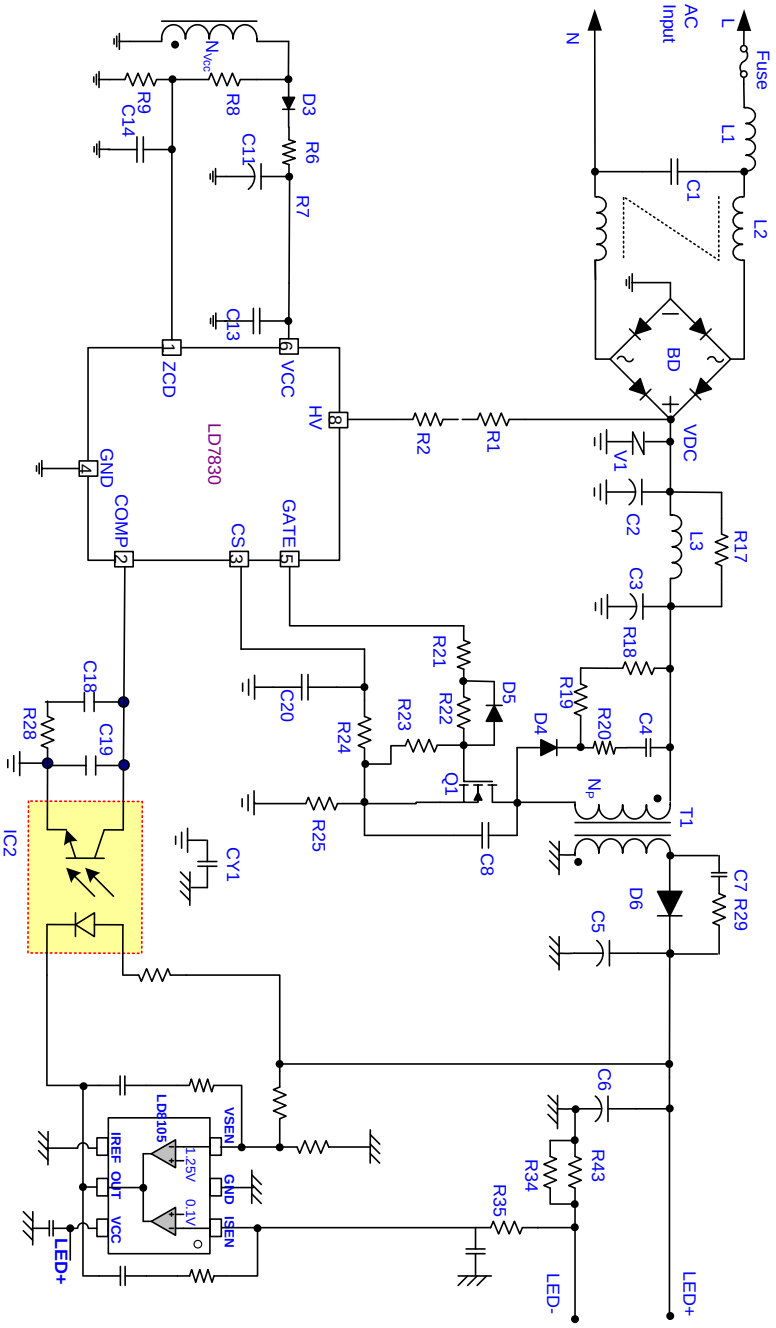
Fault Protection

There are several critical protections were integrated in the LD7830 to prevent the power supply or adapter from being damaged. Those damages usually come from open or short condition caused to LD7830.

Once it happens in below condition, the gate output will turn off immediately to protect the power circuit ---

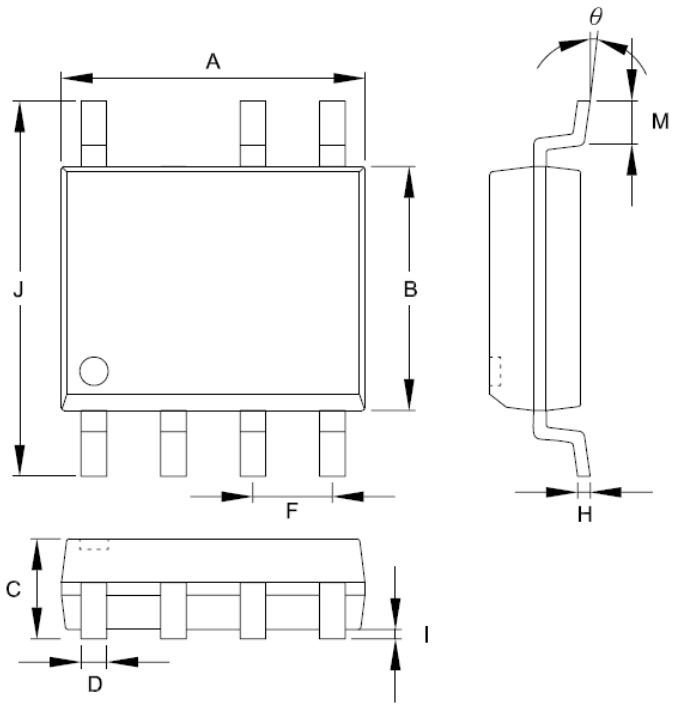
1. Comp pin floating
2. CS pin floating

Reference Application Circuit --- LED -24V/700mA (90~264V_{AC})



Package Information

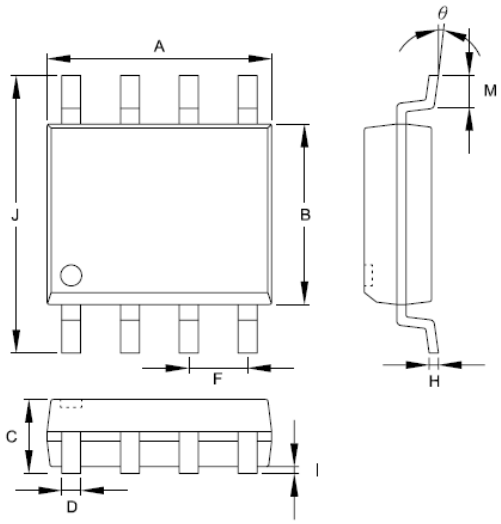
SOP-7



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

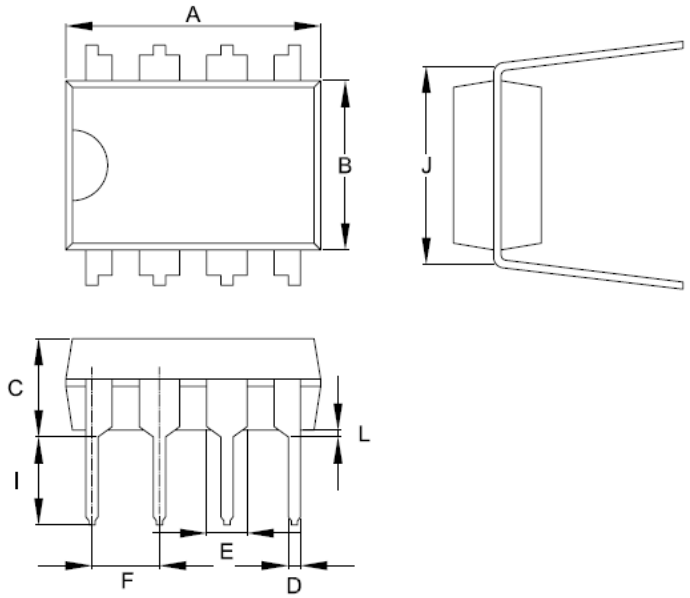
SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.229	0.007	0.009
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	2/3/2012	Original Specification
01	6/21/2012	High Voltage (600V)
01a	8/17/2012	HV ESD Level(1KV) SOP-8 Dimension: “H”

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