LEOPARD IMAGING INC

Rev. 1.1

LI-IMX274-MIPI-M12 Data Sheet

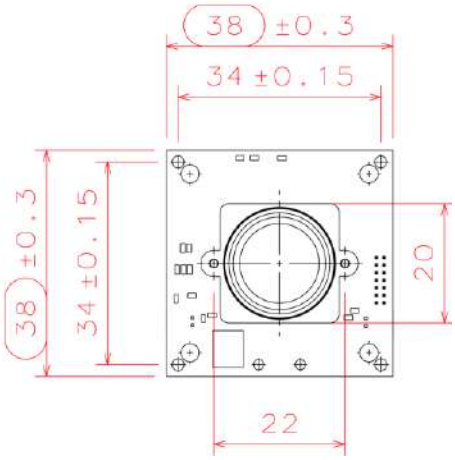
Key Features

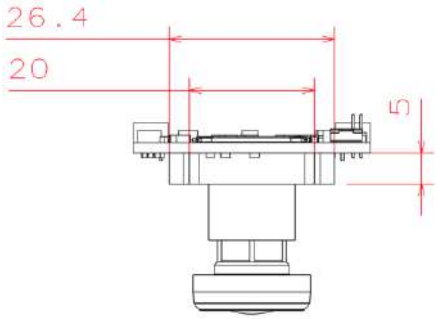
- Sony Diagonal 7.20 mm (Type 1/2.5) CMOS Image Sensor IMX274
- Active pixels: 3864H x 2196V
- Pixel size: 1.62 um x 1.62 um
- Color sensor
- Interface: MIPI output
- Support M12 lens
- Module Size: 38mmx38mm
- Weight: 12 g
- Part#: LI-IMX274-MIPI-M12

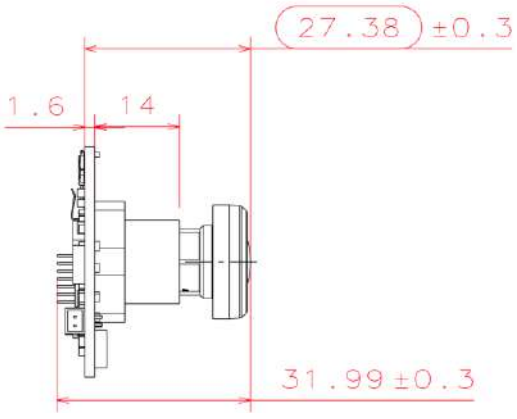
Lens Spec

- Model: SYD1201A
- Focal length: 3.7 mm
- Aperture, F/#: 2.8 +/- 5%
- Built in 650nm IR cut filter
- FOV (D/H/V): 92° / 83° /53°
- TV Distortion: -1.0 %
- Mount: M12 x P0.5

Dimensions







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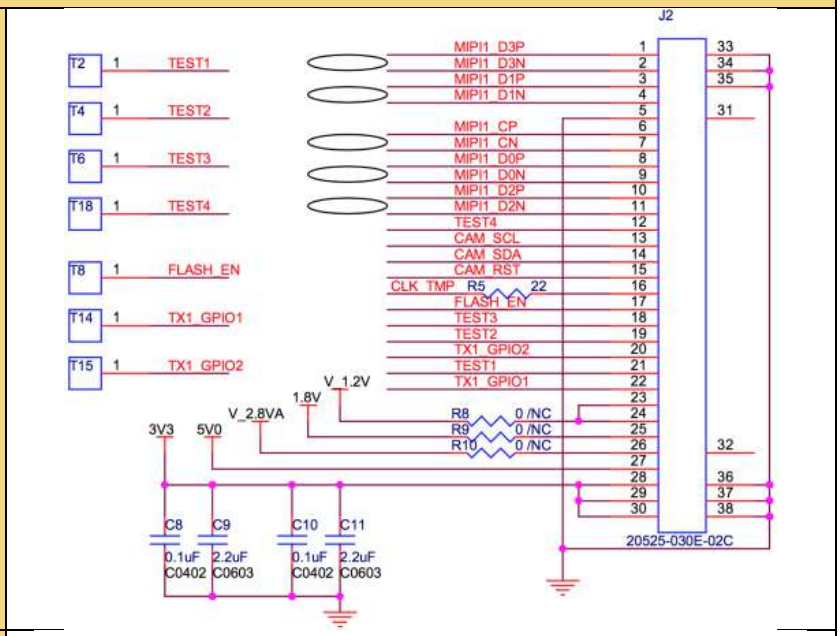
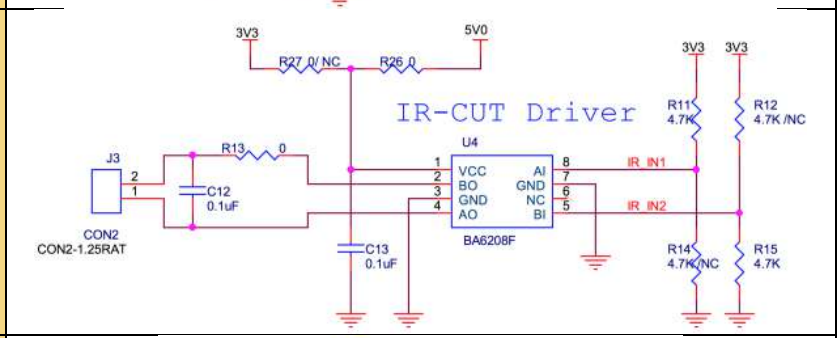
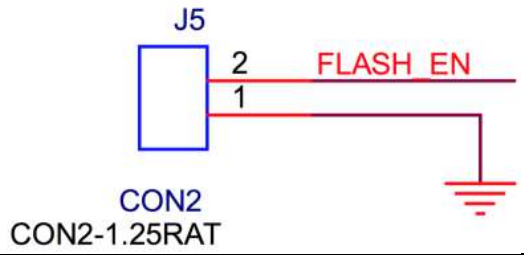
Interfaces

Interfaces	
Interface J2: ▪ Part#: 20525-030E-02C ▪ Number of Positions: 30 ▪ Pitch: 0.4mm ▪ Mating I-PEX cable: LI-FAW-1233-T1 (200mm)	
Interface J3: ▪ Part#: 1734829-2 ▪ Number of Positions: 2 ▪ Pitch: 1.25mm	
Interface J5: ▪ Part#: 1734829-2 ▪ Number of Positions: 2 ▪ Pitch: 1.25mm	

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Absolute Maximum Ratings

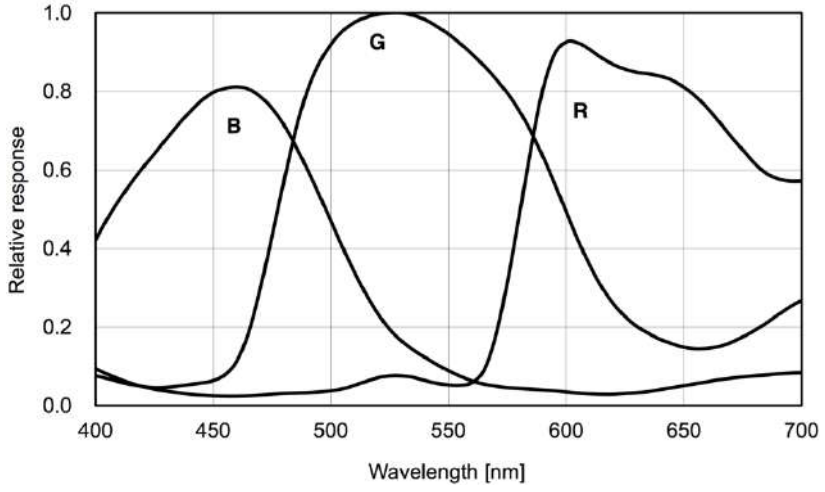
Item	Symbol	Ratings	Unit
Supply voltage (Analog)	V_{ADD} *1	–0.3 to +3.3	V
Supply voltage (Digital 1)	V_{DDD1} *2	–0.5 to +2.0	V
Supply voltage (Digital 2)	V_{DDD2} *3	–0.5 to +3.3	V
Input voltage (Digital)	V_I	–0.3 to V_{DDD2} + 0.3	V
Output voltage (Digital)	V_O	–0.3 to V_{DDD2} + 0.3	V
Guaranteed operating temperature	T_{OPR}	–30 to +75	˚C
Storage guarantee temperature	T_{STG}	–30 to +80	˚C
Performance guarantee temperature	T_{SPEC}	–10 to +60	˚C

Recommended Operating Conditions

Item	Symbol	Rating	Unit
Supply voltage (Analog)	V_{ADD} *1	2.8 ± 0.1	V
Supply voltage (Digital 1)	V_{DDD1} *2	1.2 ± 0.1	V
Supply voltage (Digital 2)	V_{DDD2} *3	1.8 ± 0.1	V
Input voltage (Digital)	V_I	–0.1 to V_{DDD2} + 0.1	V

*1 V_{ADD}: V_{DD}SUB, V_{DD}HCM, V_{DD}HPX, V_{DD}HDA, V_{DD}HCP (2.8 V power supply)
*2 V_{DDD1}: V_{DD}LCN, V_{DD}LSC1 to 2, V_{DD}LPA, V_{DD}LPL1, V_{DD}LPL2 to 3, V_{DD}LIF (1.2 V power supply)
*3 V_{DDD2}: V_{DD}MIO, V_{DD}MIF (1.8 V power supply)

Spectral Sensitivity Characteristics



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DC Characteristics

Current Consumption and Gain Variable Range

(V_{ADD} = 2.9 V, V_{DDD1} = 1.3 V, V_{DDD2} = 1.9 V, Tj = 60 ˚C, Reference Gain (0 dB)
All pixel scan mode (MODE0), 29.97 frame/s)

Item	Symbol	Min.	Typ.	Max	Unit	Remarks
Current consumption (Analog)	I_{ADD}	—	—	62	mA	
Current consumption (Digital 1)	I_{DDD1}	—	—	190	mA	
Current consumption (Digital 2)	I_{DDD2}	—	—	1	mA	
Standby current (Analog)	I_{ADDSTB}	—	—	35	μA	In the dark
Standby current (Digital 1)	$I_{DDD1STB}$	—	—	13	mA	In the dark
Standby current (Digital 2)	$I_{DDD2STB}$	—	—	20	μA	In the dark
PGA gain variable range	PGAG	0	—	27	dB	

Supply Voltage and I/O Voltage

Item		Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Analog	V_{DD}SUB, V_{DD}HCM, V_{DD}HPX, V_{DD}HDA, V_{DD}HCP	V_{ADD}	2.70	2.80	2.90	V
	Digital 1	V_{DD}LCN, V_{DD}LSC1 to 2, V_{DD}LPL1, V_{DD}LPA, V_{DD}LPL2 to 3, V_{DD}LIF	V_{DDD1}	1.10	1.20	1.30	V
	Digital 2	V_{DD}MIO, V_{DD}MIF	V_{DDD2}	1.70	1.80	1.90	V
Digital input voltage		SDA, SCL	V_{IH1}	0.7 × V_{DDD2}	—	1.9	V
			V_{IL1}	–0.3	—	0.3 × V_{DDD2}	V
		XCLR, INCK	V_{IH2}	0.65 × V_{DDD2}	—	V_{DDD2} + 0.3	V
			V_{IL2}	–0.3	—	0.35 × V_{DDD2}	V
Digital output voltage		XHS, XVS	V_{HVOUT}	—	V_{DDD2}	—	V

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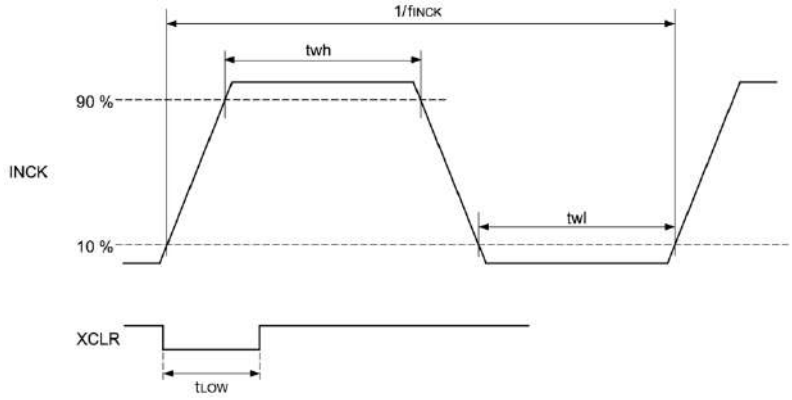
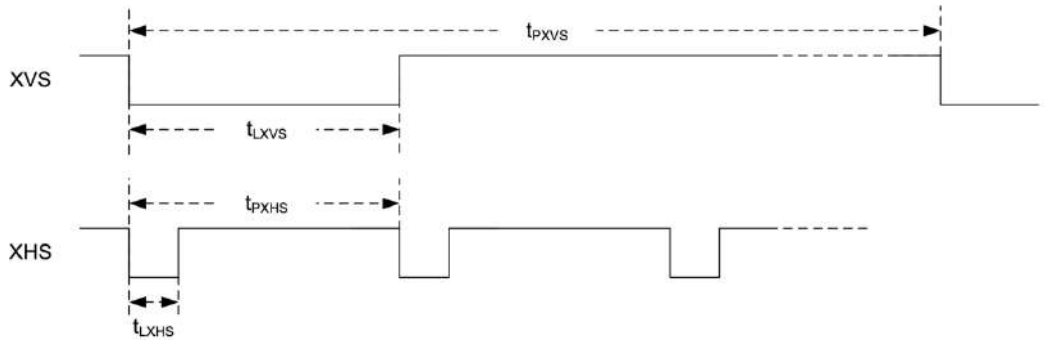
AC Characteristics

INCK, XCLR



Item	Symbol	Min.	Typ.	Max.	Unit
INCK clock frequency	f_{INCK}	6	—	27	MHz
INCK Low level pulse width	twl	5	—	—	ns
INCK High level pulse width	twh	5	—	—	ns
Clock duty	—	40	50	60	%
XCLR Low level pulse width	t_{LOW}	100	—	—	ns

XHS, XVS (Output)



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XHS Low level pulse width	t_{LXHS}		222		ns	16 clk@72MHz
XHS pulse period	t_{PXHS}		HMAX*1		clk@72MHz	
XVS Low level pulse width	t_{LXVS}		t_{PXHS}		clk@72MHz	
XVS pulse period	t_{PXVS}		HMAX*1 × VMAX*2		clk@72MHz	

*1 The value set as HMAX (address 30F6h, bit [7:0] and address 30F7h, bit [7:0])
*2 The value set as VMAX (address 30F8h, bit [7:0], address 30F9h, bit [7:0] and address 30FAh, bit [3:0]).

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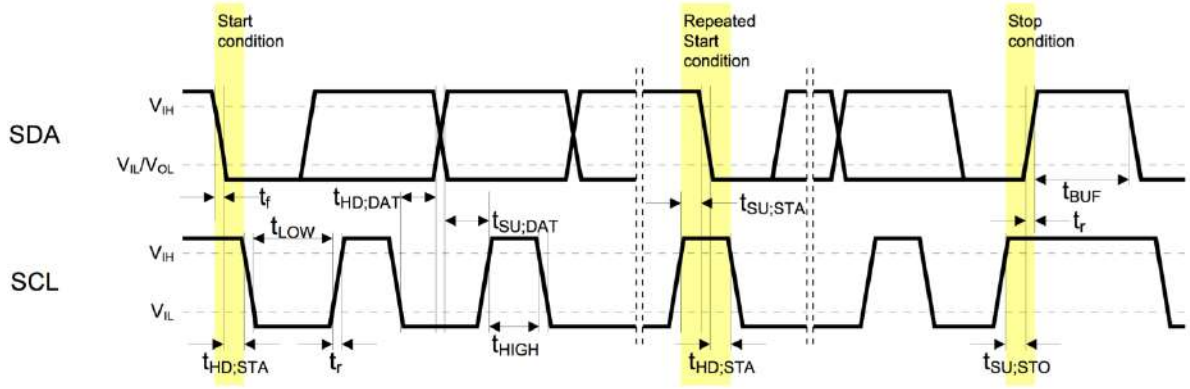
I²C Communication



I²C Specification

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Low level input voltage	V_{IL}	−0.3	—	0.3 × V_{DDD2}	V	
High level input voltage	V_{IH}	0.7 × V_{DDD2}	—	1.9	V	
Low level output voltage	V_{OL}	0	—	0.2 × V_{DDD2}	V	V_{DDD2} < 2 V, Sink 3 mA
Output fall time	tof	—	—	250	ns	Load 10 pF to 400 pF, 0.7 × V_{DDD2} to 0.3 × V_{DDD2}
Input current (SCL, SDA, XCLR, INCK)	Ii	-10	—	10	µA	0.1 × V_{DDD2} to 0.9 × V_{DDD2}
Input capacitance of SCL / SDA	Ci	—	—	10	pF	

I²C AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	0	—	400	kHz
Hold time (Start Condition)	$t_{HD;STA}$	0.6	—	—	µs
Low period of the SCL clock	t_{LOW}	1.3	—	—	µs
High period of the SCL clock	t_{HIGH}	0.6	—	—	µs
Set-up time (Repeated Start Condition)	$t_{SU;STA}$	0.6	—	—	µs
Data hold time	$t_{HD;DAT}$	0	—	0.9	µs
Data set-up time	$t_{SU;DAT}$	100	—	—	ns
Rise time of both SDA and SCL signals	t_r	—	—	300	ns
Fall time of both SDA and SCL signals	t_f	—	—	300	ns
Set-up time (Stop Condition)	$t_{SU;STO}$	0.6	—	—	µs
Bus free time between a STOP and START Condition	t_{BUF}	1.3	—	—	µs

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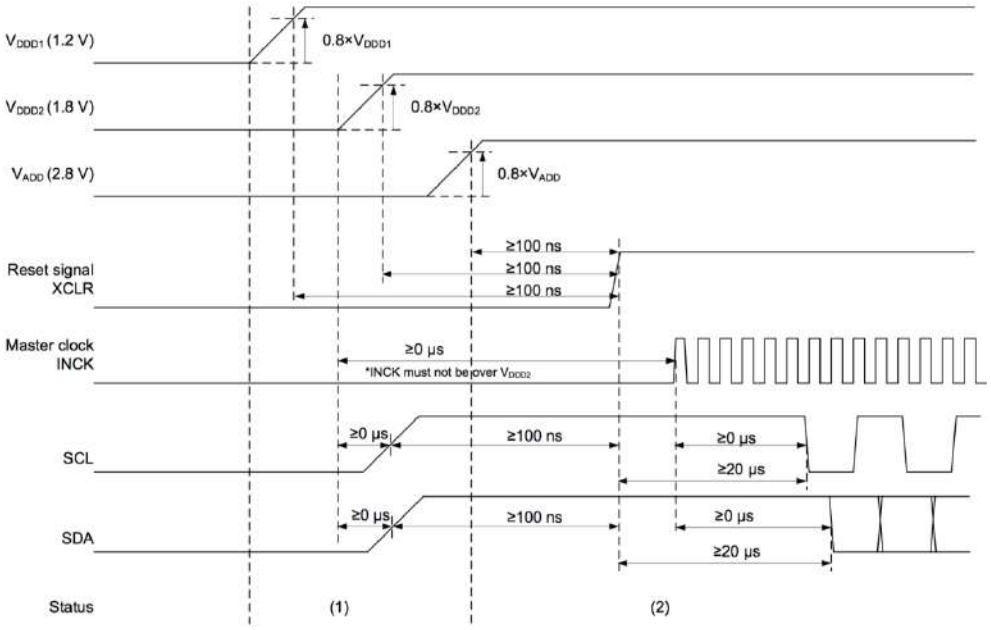
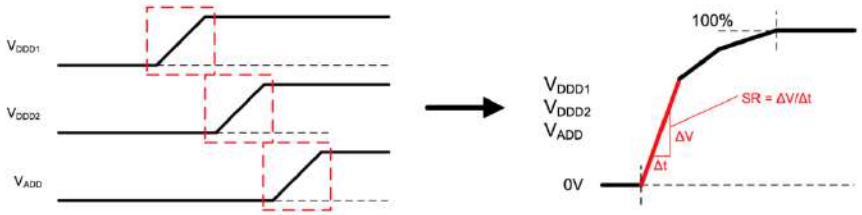
Power-on Sequence



Period name	Remarks
(1) Power stabilization period	All input signals are set to Low level. There are no constraints of the power-on sequence with V_{ADD}, V_{DDD1}, and V_{DDD2}.
(2) Register communication period for standby cancel	Wait 100 ns after the last power supply in V_{ADD}, V_{DDD1} and V_{DDD2}. Then set XCLR to "H" and start the standby cancel sequence.

Slew Rate Limitation of Power-on Sequence

Conform to the slew rate limitation shown below when power supply change 0 V to each voltage (0 % to 100 %) in power-on sequence.



Item	Symbol	Power supply	Min.	Max.	Unit	Remarks
Slew rate	SR	V_{DDD1} (1.2 V)	—	25	mV/us	
		V_{DDD2} (1.8 V)	—	25	mV/us	
		V_{ADD} (2.8 V)	—	25	mV/us	

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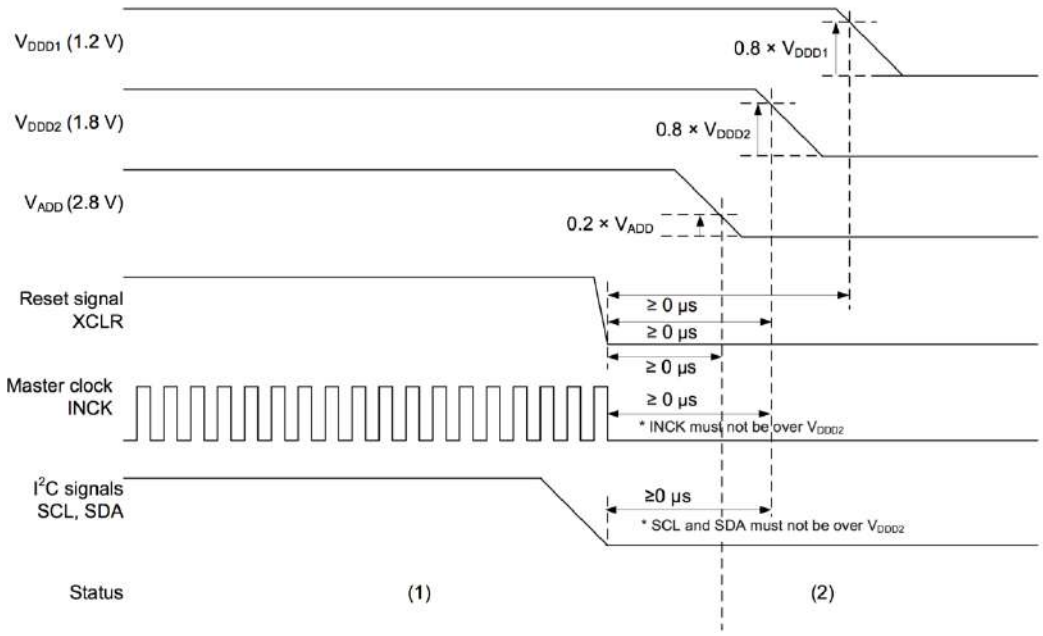
Power-off Sequence



Period name	Remarks
(1) Pixel output period	Pixel signal output period
(2) Power-off period	Turn the power supplies off after all input signals are set to "Low" level except SCL and SDA. Set SCL and SDA to "Low" level at the same time with turning off the power supply of V_{DDD2}. There are no constraints of the power-off sequence with V_{ADD}, V_{DDD1}, and V_{DDD2}.

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