



LEOPARD IMAGING INC

LI-M021C-MIPI

Data Sheet

Key Features

- Aptina 1/3" CMOS Digital Image Sensor MT9M021
- Optical format: 1/3"
- Active pixels: 1280H x 960V
- Pixel size: 3.75 μm x 3.75 μm
- Global shutter
- Color filter array: RGB Bayer
- Responsivity: 5.3V/lux-sec
- Support M8 lens
- Module Size: 18.5mm x 15mm
- Weight: 2 g
- Part#: **LI-M021C-MIPI**



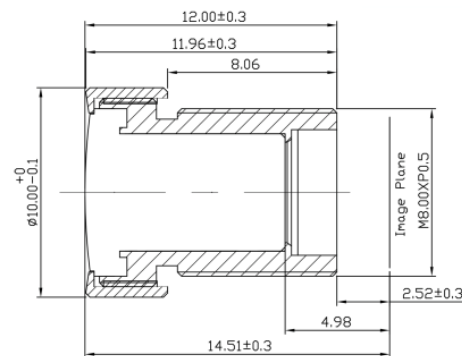
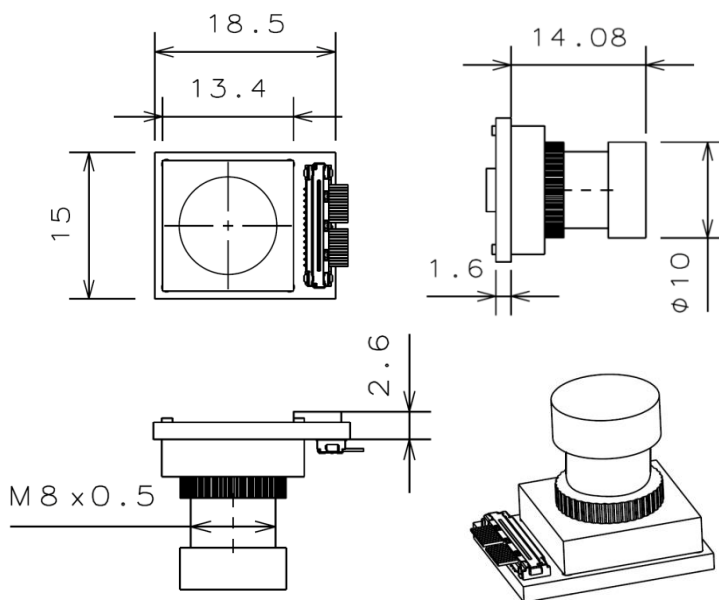
Interface

- Part#: 20498-026E-41
- Number of Positions: 26
- Shell Plating: Sn
- Vacuum Clip: With

Lens Spec

- Part#: HK-8110-131-1-M8
- Sensor size: 1/3"
- Focal Length: 3 mm
- Aperture, F/#: 2.8
- Built in 650 nm IR cut filter
- FOV (D/H/V): 117 %/90 %/67 °
- Mount: M8 x P0.5 – 6g

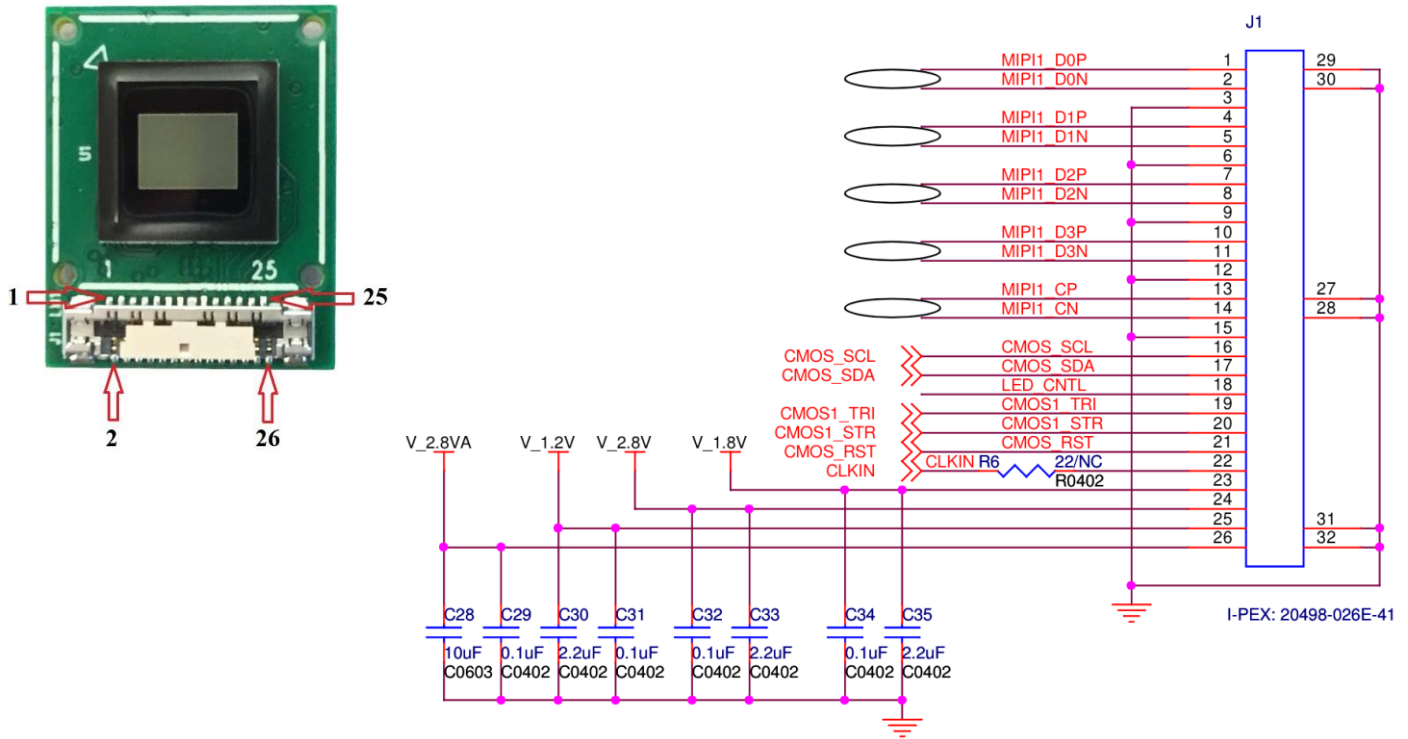
Dimensions



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Pin Assignment



Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{SUPPLY}	Power supply voltage (all supplies)	-0.3	4.5	V
I_{SUPPLY}	Total power supply current	-	200	mA
I_{GND}	Total ground current	-	200	mA
V_{IN}	DC input voltage	-0.3	$V_{DD} IO + 0.3$	V
V_{OUT}	DC output voltage	-0.3	$V_{DD} IO + 0.3$	V
T_{STG}^1	Storage temperature	-40	+85	°C

Note: 1. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



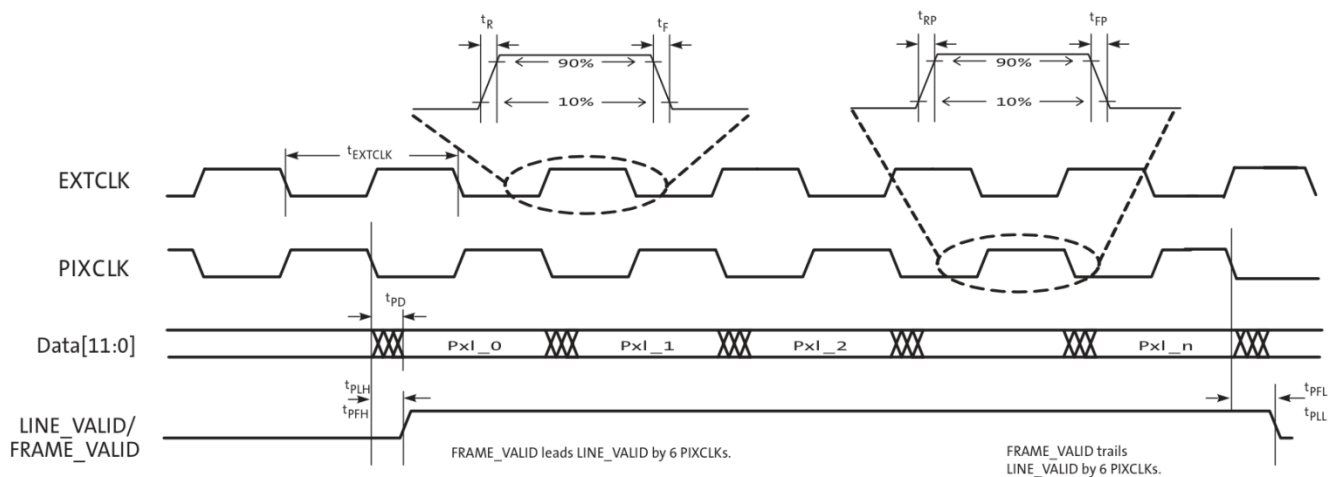
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DC Electrical Characteristics

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{DD}	Core digital voltage		1.7	1.8	1.95	V
V_{DD_IO}	I/O digital voltage		1.7/2.5	1.8/2.8	1.9/3.1	V
V_{AA}	Analog voltage		2.5	2.8	3.1	V
V_{AA_PIX}	Pixel supply voltage		2.5	2.8	3.1	V
V_{DD_PLL}	PLL supply voltage		2.5	2.8	3.1	V
V_{DD_SLVS}	HiSPi supply voltage		0.3	0.4	0.6	V
V_{IH}	Input HIGH voltage		$V_{DD_IO} * 0.7$	-	-	V
V_{IL}	Input LOW voltage		-	-	$V_{DD_IO} * 0.3$	V
I_{IN}	Input leakage current	No pull-up resistor; $V_{IN} = V_{DD_IO}$ or D_{GND}	20	-	-	uA
V_{OH}	Output HIGH voltage		$V_{DD_IO} - 0.3$	-	-	V
V_{OL}	Output LOW voltage	$V_{DD_IO} = 2.8V$	-	-	0.4	V
I_{OH}	Output HIGH current	At specified V_{OH}	-22	-	-	mA
I_{OL}	Output LOW current	At specified V_{OL}	-	-	22	mA

I/O Timing Diagram



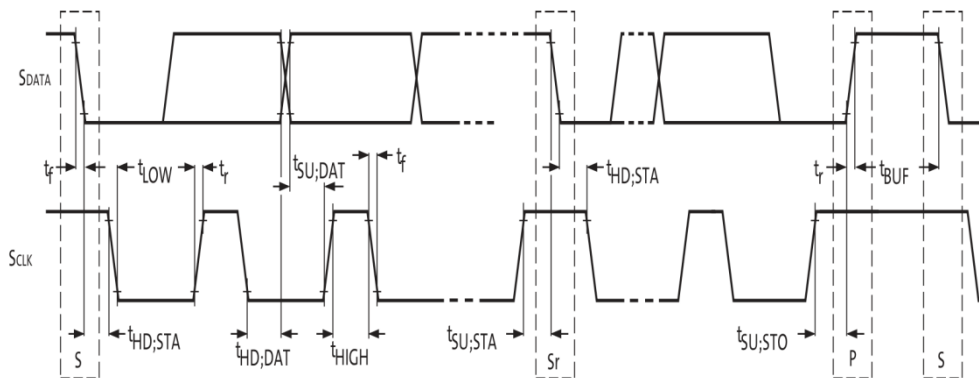
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I/O Timing Characteristics

Parallel Output									
Symbol	Definition	Condition	VDD_IO=2.8V			VDD_IO=1.8V			Unit
			Min	Typ	Max	Min	Typ	Max	
f_{EXTCLK}	Input clock frequency		6		50	6		50	MHz
t_{EXTCLK}	Input clock period		20		166	20		166	ns
t_R	Input clock rise time	PLL enabled		3	4		3	4	ns
t_F	Input clock fall time	PLL enabled		3	4		3	4	ns
t_{RP}	PIXCLK rise time	Slew setting = 4 (default)	2.3		4.6	2.3		4.6	ns
t_{FP}	PIXCLK fall time	Slew setting = 4 (default)	3		4.4	3		4.4	ns
	PIXCLK duty cycle		40	50	60	40	50	60	%
f_{PIXCLK}	PIXCLK frequency	Nominal voltages, PLL Enabled	6		74.25	6		74.25	MHz
t_{PD}	PIXCLK to data valid	Nominal voltages, PLL Enabled	-3	2.3	4	-3	2.3	4.5	ns
t_{PFH}	PIXCLK to FV HIGH	Nominal voltages, PLL Enabled	-3	1.5	4	-3	1.5	4.5	ns
t_{PLH}	PIXCLK to LV HIGH	Nominal voltages, PLL Enabled	-3	2.3	4	-3	2.3	4.5	ns
t_{PFL}	PIXCLK to FV LOW	Nominal voltages, PLL Enabled	-3	1.5	4	-3	1.5	4.5	ns
t_{PLL}	PIXCLK to LV LOW	Nominal voltages, PLL Enabled	-3	2	4	-3	2	4.5	ns

Two-Wire Serial Bus Timing Parameters



Note: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.



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Two-Wire Serial Bus Characteristics

$f_{EXTCLK} = 27 \text{ MHz}$; $VDD = 1.8\text{V}$; $VDD_{IO} = 2.8\text{V}$; $VAA = 2.8\text{V}$; $VAA_{PIX} = 2.8\text{V}$; $VDD_{PLL} = 2.8\text{V}$; $T_A = 25 \text{ }^\circ\text{C}$

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
S _{CLK} Clock Frequency	f_{SCL}	0	100	0	400	KHz
Hold time (repeated) START condition						
After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	-	0.6	-	us
LOW period of the SCLK clock	t_{LOW}	4.7	-	1.3	-	us
HIGH period of the SCLK clock	t_{HIGH}	4.0	-	0.6	-	us
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	us
Data hold time	$t_{HD;DAT}$	0 ⁴	3.45 ⁵	0 ⁶	0.9 ⁵	us
Data set-up time	$t_{SU;DAT}$	250	-	100 ⁶	-	ns
Rise time of both S _{DATA} and S _{CLK} signals	t_r	-	1000	20 + 0.1Cb7	300	ns
Fall time of both S _{DATA} and S _{CLK} signals	t_f	-	300	20 + 0.1Cb7	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	us
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	us
Capacitive load for each bus line	Cb	-	400	-	400	pF
Serial interface input pin capacitance	C _{IN_SI}	-	3.3	-	3.3	pF
S _{DATA} max load capacitance	C _{LOAD_SD}	-	30	-	30	pF
S _{DATA} pull-up resistor	R _{SD}	1.5	4.7	1.5	4.7	K Ω

Note: 1. This table is based on I²C standard (v2.1 January 2000). Philips Semiconductor.

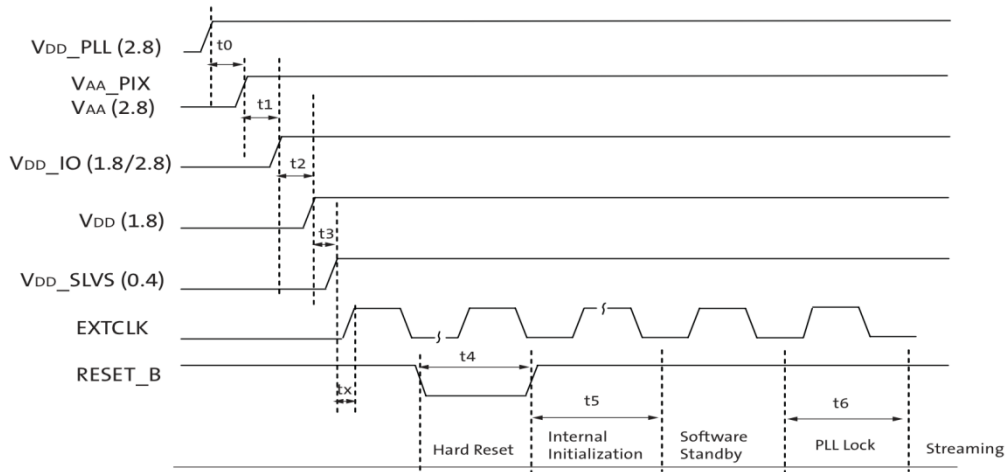
- Two-wire control is I²C-compatible.
- All values referred to $V_{IHmin} = 0.9 VDD$ and $V_{ILmax} = 0.1 VDD$ levels. Sensor EXCLK = 27MHz.
- A device must internally provide a hold time of at least 300 ns for the S_{DATA} signal to bridge the unde-fined region of the falling edge of SCLK.
- The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCLK signal.
- A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU;DAT}$ 250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must out- put the next data bit to the S_{DATA} line $t_r \text{ max} + t_{SU;DAT} = 1000 + 250 = 1250 \text{ ns}$ (according to the Stan- dard-mode I²C-bus specification) before the SCLK line is released.
- Cb = total capacitance of one bus line in pF.



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Power-Up Sequence

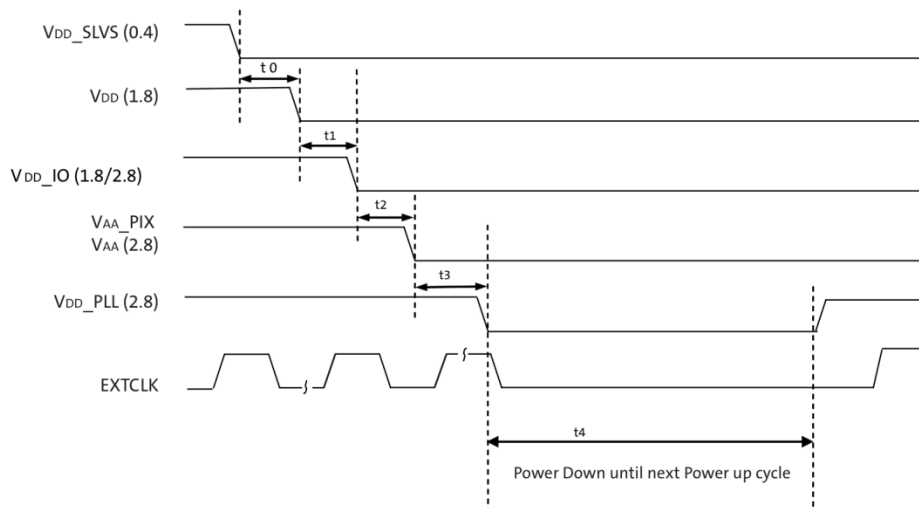


Definition	Symbol	Minimum	Typical	Maximum	Unit
V _{DD_PLL} to V _{AA_PIX} /V _{AA_PIX}	t ₀	0	10	-	us
V _{AA_PIX} /V _{AA_PIX} to V _{DD_IO}	t ₁	0	10	-	us
V _{DD_IO} to V _{DD}	t ₂	0	10	-	us
V _{DD} to V _{DD_SLVS}	t ₃	0	10	-	us
Xtal settle time	t _x	-	30 ¹	-	ms
Hard Reset	t ₄	1 ²	-	-	ms
Internal Initialization	t ₅	150000	-	-	EXTCLKs
PLL Lock Time	t ₆	1	-	-	ms

Note: 1. Xtal settling time is component-dependent, usually taking about 10 – 100 ms.

2. Hard reset time is the minimum time required after power rails are settled. In a circuit where Hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.

Power-Down Sequence



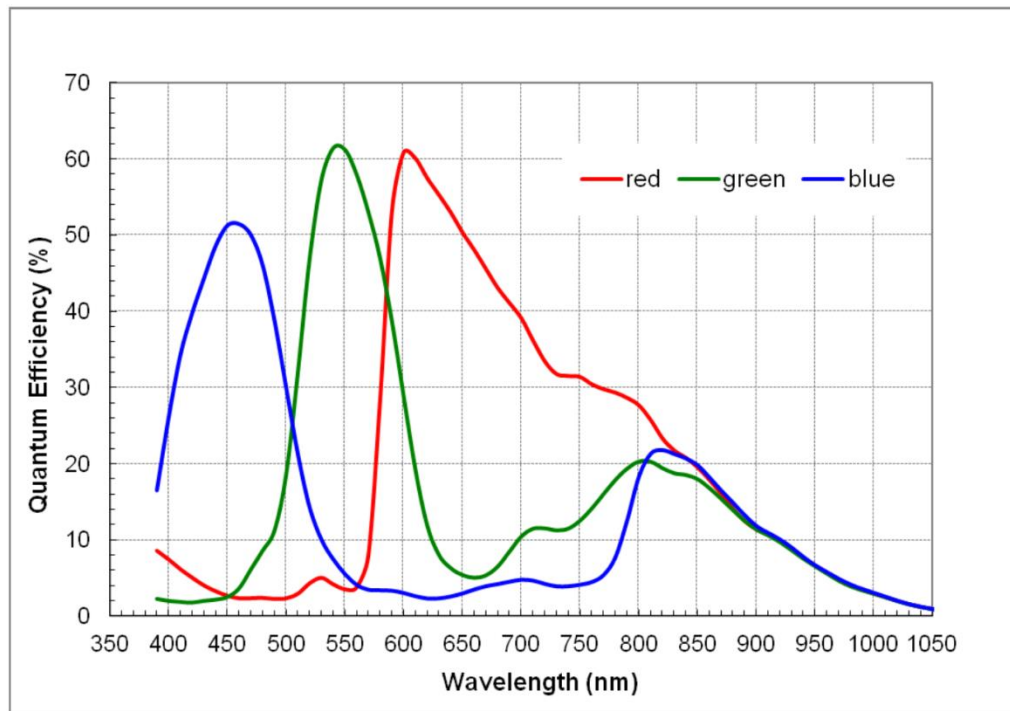
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Definition	Symbol	Minimum	Typical	Maximum	Unit
V_{DD_SLVS} to V_{DD}	t0	0	-	-	us
V_{DD} to V_{DD_IO}	t1	0	-	-	us
V_{DD_IO} to V_{AA}/V_{AA_PIX}	t2	0	-	-	us
V_{AA}/V_{AA_PIX} to V_{DD_PLL}	t3	0	-	-	us
PwrDn until Next PwrUp Time	t4	100	-	-	ms

Note: t4 is required between power down and next power up time; all decoupling caps from regulators must be completely discharged.

Quantum Efficiency – Color Sensor



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