



LEOPARD IMAGING INC

Rev 1.1

LI-TX1-KIT-IMX274M12

Data Sheet

Key Features

- Compatible with Nvidia Jetson TX1
- MIPI interface
- Support up to three IMX274 cameras
- Sony Diagonal 7.20 mm (Type 1/2.5) CMOS Image Sensor IMX274
- Active pixels: 3864H x 2196V
- Length of the I-PEX cable: 300mm
- Support M12 lens
- Provide customization services
- Weight: 34 g
- Part#: **LI-TX1-KIT-IMX274M12**



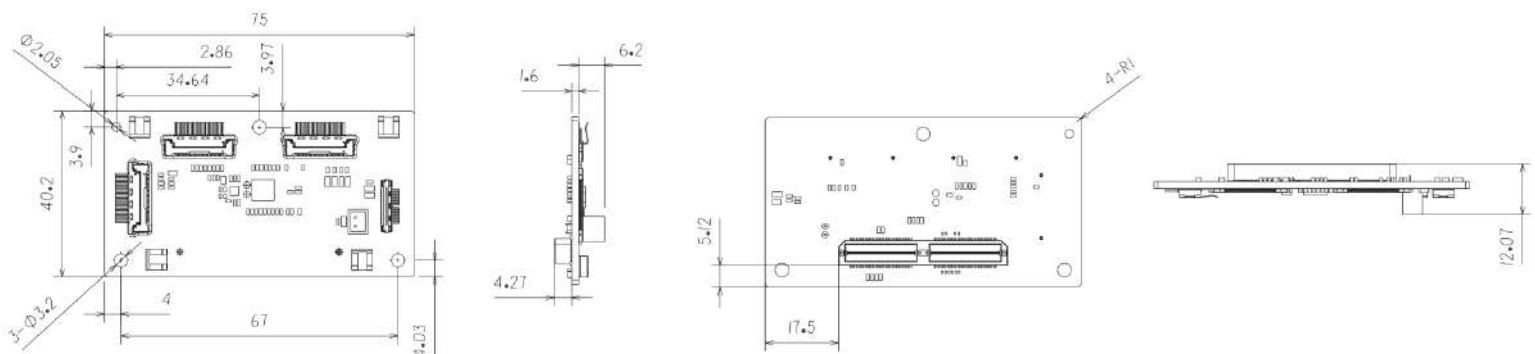
Lens Spec

- Model: YC-172
- Focal length: 4.0 mm
- Aperture, F/#: 1.8
- Built in 650nm IR cut filter
- FOV (D/H/V): 112° / 96° / 51°
- TV Distortion: < 20%
- Mount: M12 x P0.5

BOM

| # | Items | QTY |
|---|--------------------|-----|
| 1 | LI-JTX1-MIPI-ADPT | 1 |
| 2 | LI-IMX274-MIPI-M12 | 1 |
| 3 | FAW-1233-03 cable | 1 |

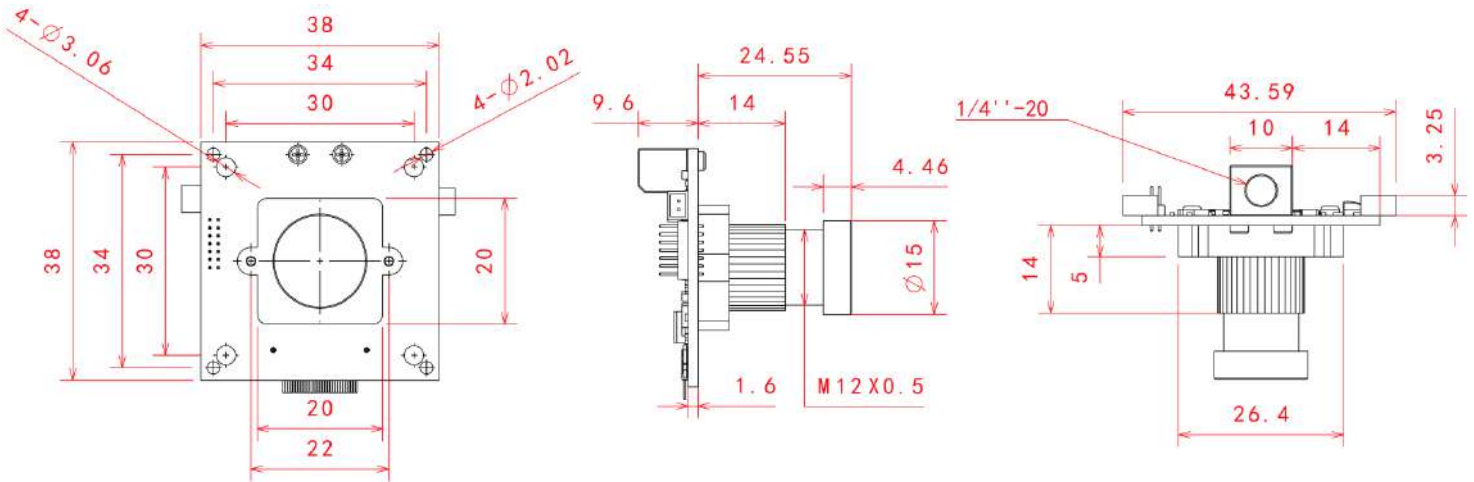
Dimensions (LI-JTX1-MIPI-ADPT)



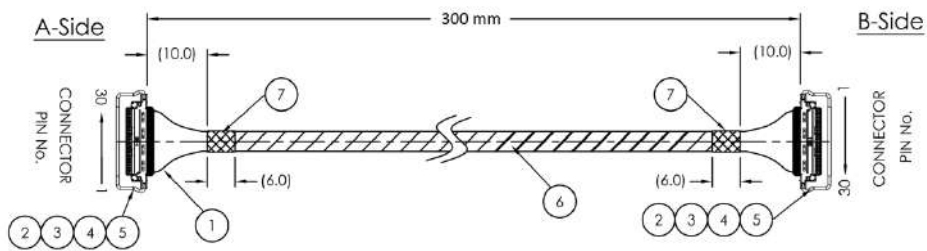
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Dimensions (LI-IMX274-MIPI-M12)



Dimensions (FAW-1233-03)



Work on Nvidia Jetson TX1



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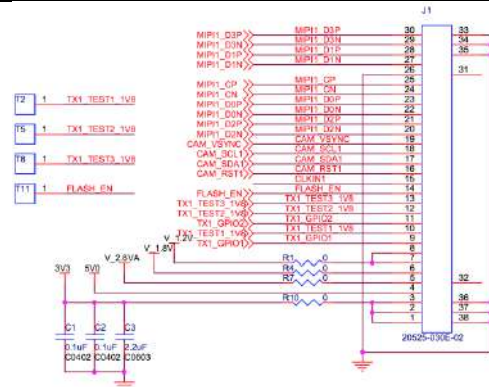
LI-JTX1-MIPI-ADPT



Interfaces

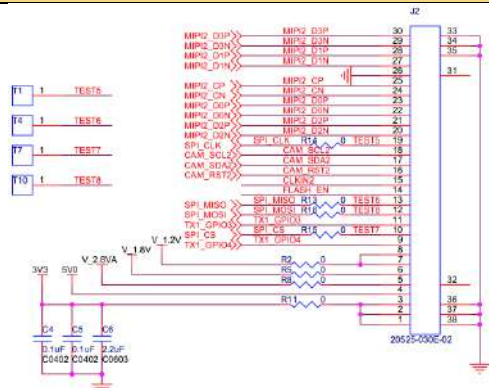
Interface J1

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



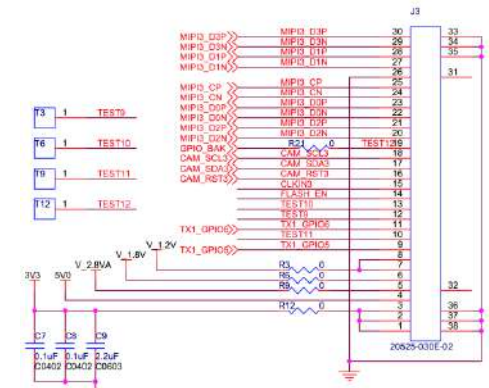
Interface J2

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



Interface J3

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



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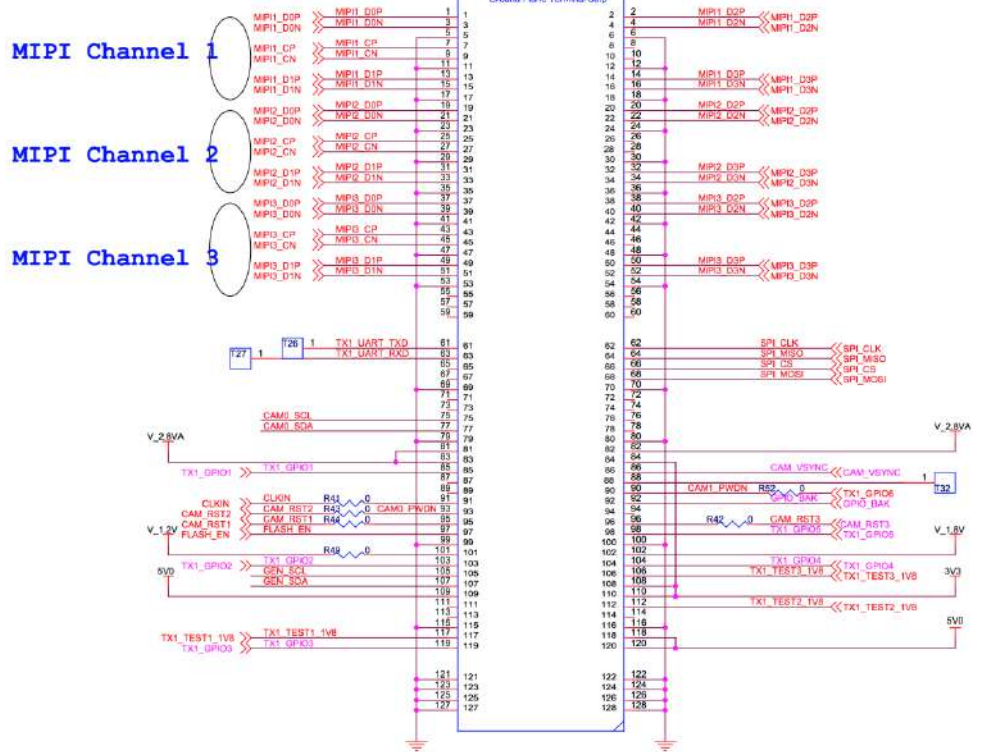


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Interface J10

- Part#: QTH-060-01-L-D-A
- Number of Positions: 120
- Number of Rows: 2
- Pitch: 0.5 mm

Vertical Mating Connector of Jetson TX1 J22



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LI-IMX274-MIPI-M12



| | |
|--|---|
| Camera Spec | |
| Image Sensor | Sony Diagonal 7.20 mm (Type 1/2.5) CMOS Image Sensor IMX274 |
| Optical format | 1/2.5" |
| Number of active pixels | 3864 (H) x 2196 (V) |
| Pixel size | 1.62um (H) x 1.62um (V) |
| Color or Mono | Color |
| Interface | MIPI interface |
| Lens mount | M12 |
| Weight | 14 g |
| Interfaces | |
| Interface J2: <ul style="list-style-type: none"> Part#: 20525-030E-02C Number of Positions: 30 Pitch: 0.4mm Mating I-PEX cable: FAW-1233-03 (300mm) | |
| Interface J3: <ul style="list-style-type: none"> Part#: 1734829-2 Number of Positions: 2 Pitch: 1.25mm | |
| Interface J5: <ul style="list-style-type: none"> Part#: 1734829-2 Number of Positions: 2 Pitch: 1.25mm | |



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Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit |
|-----------------------------------|-----------------|--------------------------|------|
| Supply voltage (Analog) | V_{ADD}^{*1} | -0.3 to +3.3 | V |
| Supply voltage (Digital 1) | V_{DDD1}^{*2} | -0.5 to +2.0 | V |
| Supply voltage (Digital 2) | V_{DDD2}^{*3} | -0.5 to +3.3 | V |
| Input voltage (Digital) | V_I | -0.3 to $V_{DDD2} + 0.3$ | V |
| Output voltage (Digital) | V_O | -0.3 to $V_{DDD2} + 0.3$ | V |
| Guaranteed operating temperature | T_{OPR} | -30 to +75 | °C |
| Storage guarantee temperature | T_{STG} | -30 to +80 | °C |
| Performance guarantee temperature | T_{SPEC} | -10 to +60 | °C |

Recommended Operating Conditions

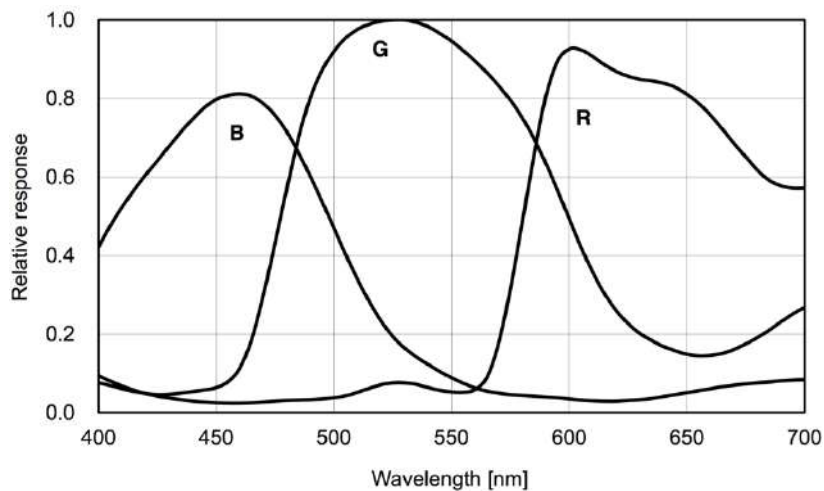
| Item | Symbol | Rating | Unit |
|----------------------------|-----------------|--------------------------|------|
| Supply voltage (Analog) | V_{ADD}^{*1} | 2.8 ± 0.1 | V |
| Supply voltage (Digital 1) | V_{DDD1}^{*2} | 1.2 ± 0.1 | V |
| Supply voltage (Digital 2) | V_{DDD2}^{*3} | 1.8 ± 0.1 | V |
| Input voltage (Digital) | V_I | -0.1 to $V_{DDD2} + 0.1$ | V |

*1 V_{ADD} : V_{DDSUB} , V_{DDHCM} , V_{DDHPX} , V_{DDHDA} , V_{DDHCP} (2.8 V power supply)

*2 V_{DDD1} : $V_{DDL CN}$, $V_{DDL SC1}$ to 2, $V_{DDL PA}$, $V_{DDL PL1}$, $V_{DDL PL2}$ to 3, $V_{DDL IF}$ (1.2 V power supply)

*3 V_{DDD2} : V_{DDMIO} , V_{DDMIF} (1.8 V power supply)

Spectral Sensitivity Characteristics



DC Characteristics

Current Consumption and Gain Variable Range

($V_{ADD} = 2.9\text{ V}$, $V_{DDD1} = 1.3\text{ V}$, $V_{DDD2} = 1.9\text{ V}$, $T_j = 60\text{ }^\circ\text{C}$, Reference Gain (0 dB)
All pixel scan mode (MODE0), 29.97 frame/s)

| Item | Symbol | Min. | Typ. | Max | Unit | Remarks |
|---------------------------------|---------------|------|------|-----|---------------|-------------|
| Current consumption (Analog) | I_{ADD} | — | — | 62 | mA | |
| Current consumption (Digital 1) | I_{DDD1} | — | — | 190 | mA | |
| Current consumption (Digital 2) | I_{DDD2} | — | — | 1 | mA | |
| Standby current (Analog) | I_{ADDSTB} | — | — | 35 | μA | In the dark |
| Standby current (Digital 1) | $I_{DDD1STB}$ | — | — | 13 | mA | In the dark |
| Standby current (Digital 2) | $I_{DDD2STB}$ | — | — | 20 | μA | In the dark |
| PGA gain variable range | PGAG | 0 | — | 27 | dB | |

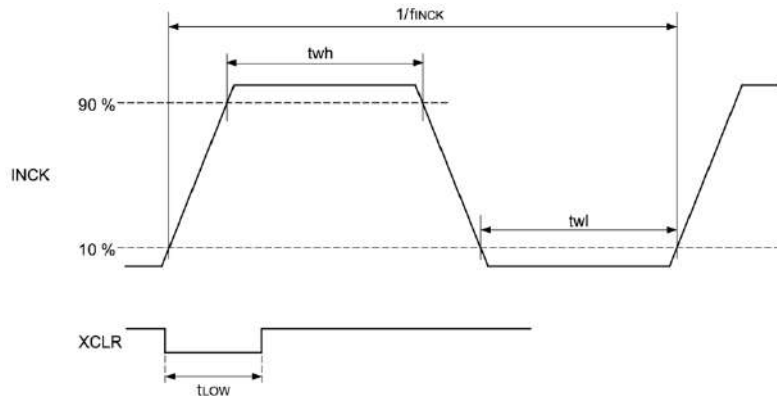
Supply Voltage and I/O Voltage

| Item | Pins | Symbol | Min. | Typ. | Max. | Unit |
|------------------------|---|-------------|------------------------|------------|------------------------|------|
| Supply voltage | Analog V_{DDSUB} , V_{DDHCM} , V_{DDHPX} , V_{DDHDA} , V_{DDHCP} | V_{ADD} | 2.70 | 2.80 | 2.90 | V |
| | Digital 1 $V_{DDL CN}$, V_{DDLSC1} to 2, V_{DDLPL1} , V_{DDLPA} , V_{DDLPL2} to 3, V_{DDLIF} | V_{DDD1} | 1.10 | 1.20 | 1.30 | V |
| | Digital 2 V_{DDMIO} , V_{DDMIF} | V_{DDD2} | 1.70 | 1.80 | 1.90 | V |
| Digital input voltage | SDA, SCL | V_{IH1} | $0.7 \times V_{DDD2}$ | — | 1.9 | V |
| | | V_{IL1} | -0.3 | — | $0.3 \times V_{DDD2}$ | V |
| | XCLR, INCK | V_{IH2} | $0.65 \times V_{DDD2}$ | — | $V_{DDD2} + 0.3$ | V |
| | | V_{IL2} | -0.3 | — | $0.35 \times V_{DDD2}$ | V |
| Digital output voltage | XHS, XVS | V_{HVOUT} | — | V_{DDD2} | — | V |



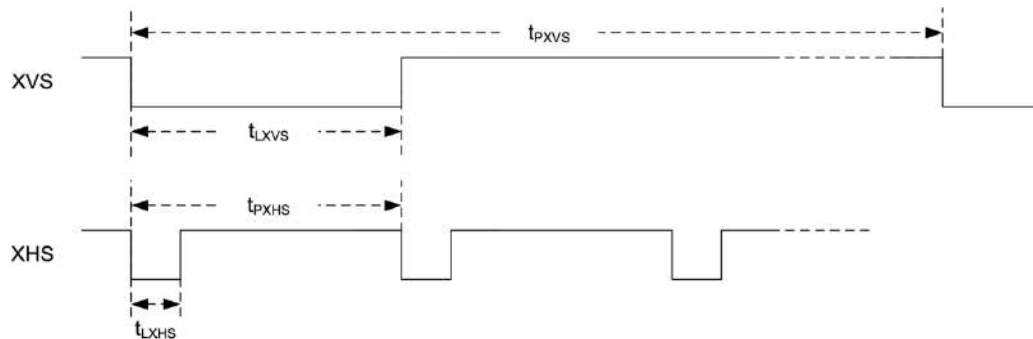
AC Characteristics

INCK, XCLR



| Item | Symbol | Min. | Typ. | Max. | Unit |
|-----------------------------|------------|------|------|------|------|
| INCK clock frequency | f_{INCK} | 6 | — | 27 | MHz |
| INCK Low level pulse width | t_{wl} | 5 | — | — | ns |
| INCK High level pulse width | t_{wh} | 5 | — | — | ns |
| Clock duty | — | 40 | 50 | 60 | % |
| XCLR Low level pulse width | t_{LOW} | 100 | — | — | ns |

XHS, XVS (Output)



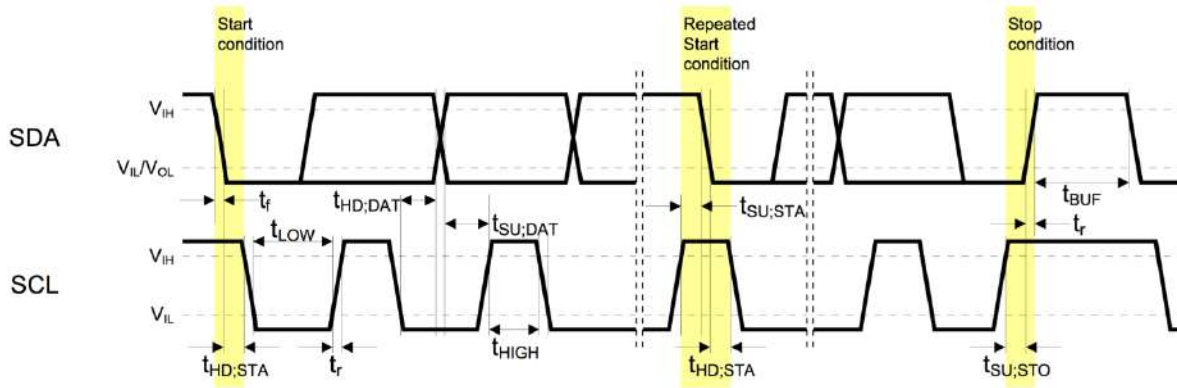
| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---------------------------|------------|------|------------------------------|------|-----------|--------------|
| XHS Low level pulse width | t_{LXHS} | | 222 | | ns | 16 clk@72MHz |
| XHS pulse period | t_{PXHS} | | $HMAX^{*1}$ | | clk@72MHz | |
| XVS Low level pulse width | t_{LXVS} | | t_{PXHS} | | clk@72MHz | |
| XVS pulse period | t_{PXVS} | | $HMAX^{*1} \times VMAX^{*2}$ | | clk@72MHz | |

*1 The value set as HMAX (address 30F6h, bit [7:0] and address 30F7h, bit [7:0])

*2 The value set as VMAX (address 30F8h, bit [7:0], address 30F9h, bit [7:0] and address 30FAh, bit [3:0]).



I²C Communication



I²C Specification

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|--------------------------------------|----------|----------------------|------|----------------------|---------|---|
| Low level input voltage | V_{IL} | -0.3 | — | $0.3 \times V_{DD2}$ | V | |
| High level input voltage | V_{IH} | $0.7 \times V_{DD2}$ | — | 1.9 | V | |
| Low level output voltage | V_{OL} | 0 | — | $0.2 \times V_{DD2}$ | V | $V_{DD2} < 2V$, Sink 3 mA |
| Output fall time | tof | — | — | 250 | ns | Load 10 pF to 400 pF, $0.7 \times V_{DD2}$ to $0.3 \times V_{DD2}$ |
| Input current (SCL, SDA, XCLR, INCK) | li | -10 | — | 10 | μA | $0.1 \times V_{DD2}$ to $0.9 \times V_{DD2}$ |
| Input capacitance of SCL / SDA | Ci | — | — | 10 | pF | |

I²C AC Characteristics

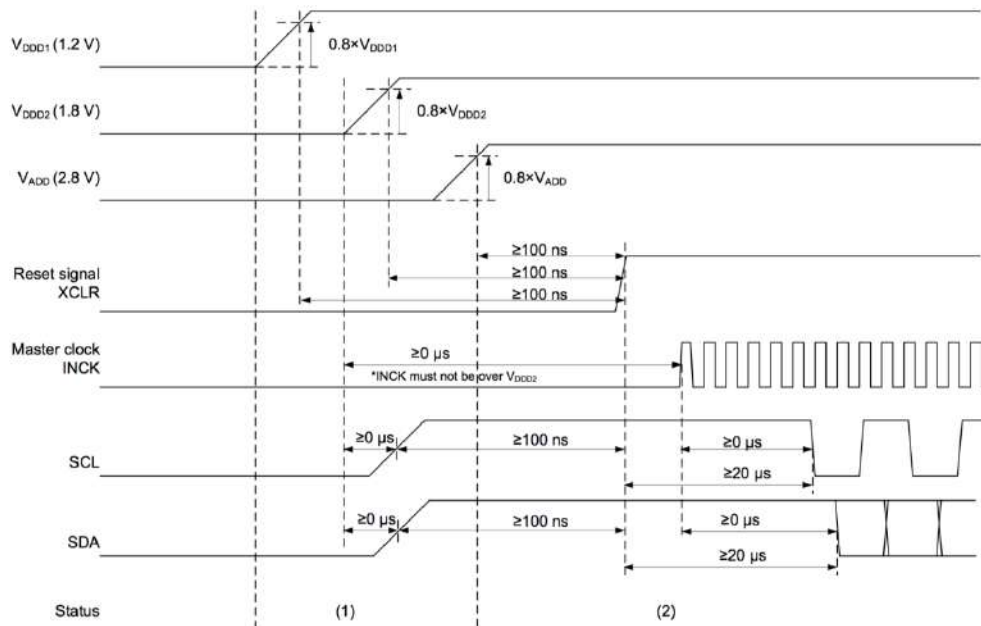
| Item | Symbol | Min. | Typ. | Max. | Unit |
|--|--------------|------|------|------|---------|
| SCL clock frequency | f_{SCL} | 0 | — | 400 | kHz |
| Hold time (Start Condition) | $t_{HD,STA}$ | 0.6 | — | — | μs |
| Low period of the SCL clock | t_{LOW} | 1.3 | — | — | μs |
| High period of the SCL clock | t_{HIGH} | 0.6 | — | — | μs |
| Set-up time (Repeated Start Condition) | $t_{SU,STA}$ | 0.6 | — | — | μs |
| Data hold time | $t_{HD,DAT}$ | 0 | — | 0.9 | μs |
| Data set-up time | $t_{SU,DAT}$ | 100 | — | — | ns |
| Rise time of both SDA and SCL signals | t_r | — | — | 300 | ns |
| Fall time of both SDA and SCL signals | t_f | — | — | 300 | ns |
| Set-up time (Stop Condition) | $t_{SU,STO}$ | 0.6 | — | — | μs |
| Bus free time between a STOP and START Condition | t_{BUF} | 1.3 | — | — | μs |



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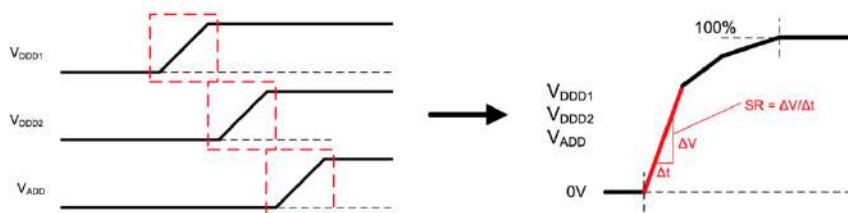
Power-on Sequence



| Period name | Remarks |
|--|--|
| (1) Power stabilization period | All input signals are set to Low level. There are no constraints of the power-on sequence with V _{ADD} , V _{DD1} , and V _{DD2} . |
| (2) Register communication period for standby cancel | Wait 100 ns after the last power supply in V _{ADD} , V _{DD1} and V _{DD2} . Then set XCLR to "H" and start the standby cancel sequence. |

Slew Rate Limitation of Power-on Sequence

Conform to the slew rate limitation shown below when power supply change 0 V to each voltage (0 % to 100 %) in power-on sequence.



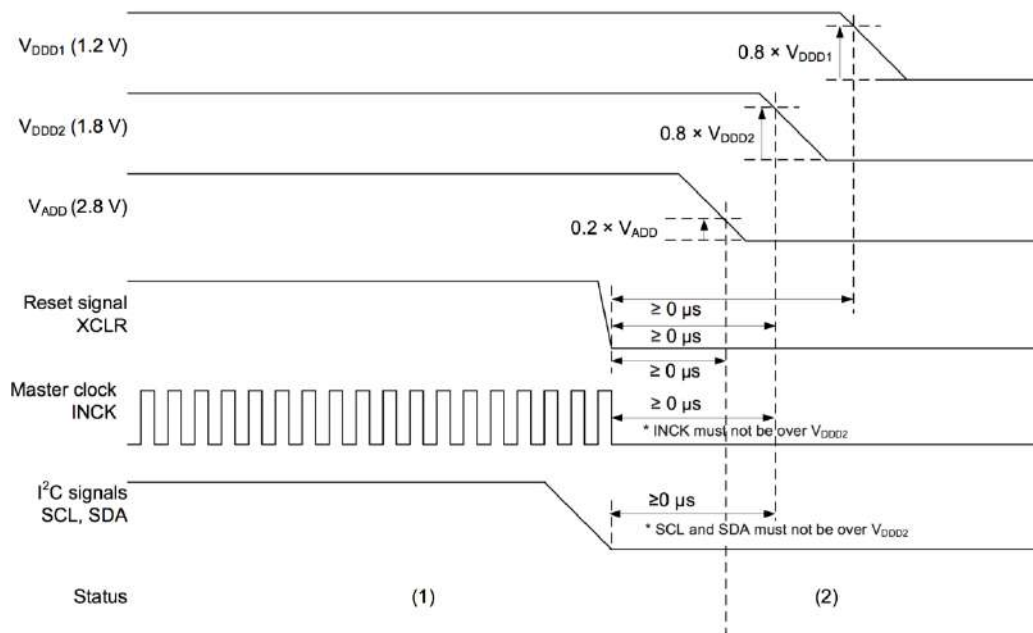
| Item | Symbol | Power supply | Min. | Max. | Unit | Remarks |
|-----------|--------|--------------------------|------|------|-------|---------|
| Slew rate | SR | V _{DD1} (1.2 V) | — | 25 | mV/us | |
| | | V _{DD2} (1.8 V) | — | 25 | mV/us | |
| | | V _{ADD} (2.8 V) | — | 25 | mV/us | |



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Power-off Sequence



| Period name | Remarks |
|-------------------------|---|
| (1) Pixel output period | Pixel signal output period |
| (2) Power-off period | Turn the power supplies off after all input signals are set to "Low" level except SCL and SDA. Set SCL and SDA to "Low" level at the same time with turning off the power supply of V_{DD2} . There are no constraints of the power-off sequence with V_{ADD} , V_{DD1} , and V_{DD2} . |



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