

# Small Signal MOSFET

## 30 Volts

### N-Channel SOT-23

- We declare that the material of product are Halogen Free and compliance with RoHS requirements.

#### FEATURES

- $R_{DS(ON)} \leq 8\Omega @ V_{GS}=4V$
- $R_{DS(ON)} \leq 13\Omega @ V_{GS}=2.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Capable doing Cu wire bonding
- ESD Protected:1000V

#### APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch

#### THERMAL CHARACTERISTICS

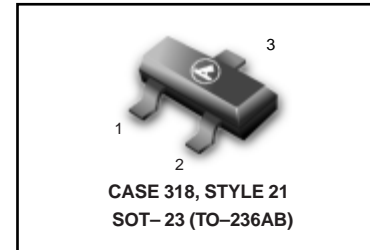
Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board (Note 1.) $T_A = 25^\circ C$ Derate above $25^\circ C$	$P_D$	225 1.8	mW mW/ $^\circ C$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	$^\circ C/W$
Total Device Dissipation Alumina Substrate, (Note 2.) $T_A = 25^\circ C$ Derate above $25^\circ C$	$P_D$	300 2.4	mW mW/ $^\circ C$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	417	$^\circ C/W$
Junction and Storage Temperature	$T_J, T_{stg}$	-55 to +150	$^\circ C$

1. FR-5 = 1.0 x 0.75 x 0.062 in.
2. Alumina = 0.4 x 0.3 x 0.025 in 99.5% alumina.

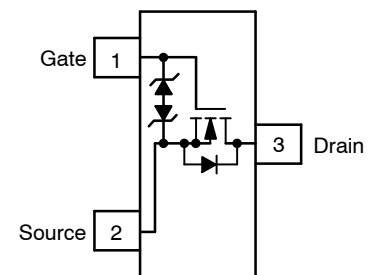
#### ORDERING INFORMATION

Device	Marking	Shipping
L2N7002FLT1G	72F	3000 Tape & Reel
L2N7002FLT3G	72F	10000 Tape & Reel

## L2N7002FLT1G

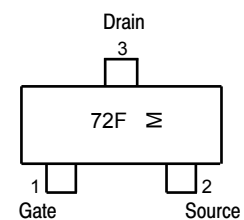


#### Simplified Schematic



(Top View)

#### MARKING DIAGRAM & PIN ASSIGNMENT



72F = Device Code  
M = Month Code

**L2N7002FLT1G**

**Absolute Maximum Ratings** (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V <sub>DS</sub>	30	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V

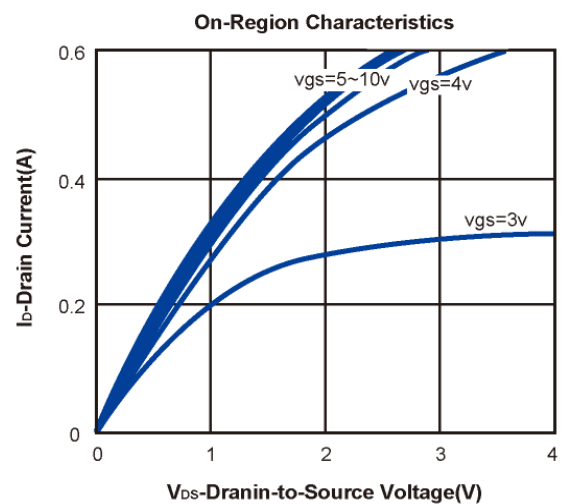
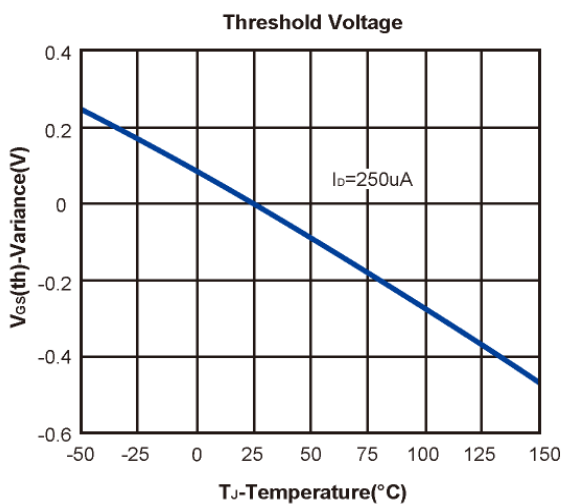
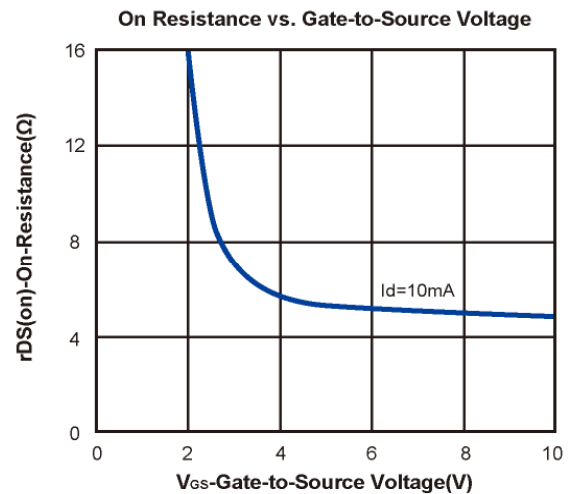
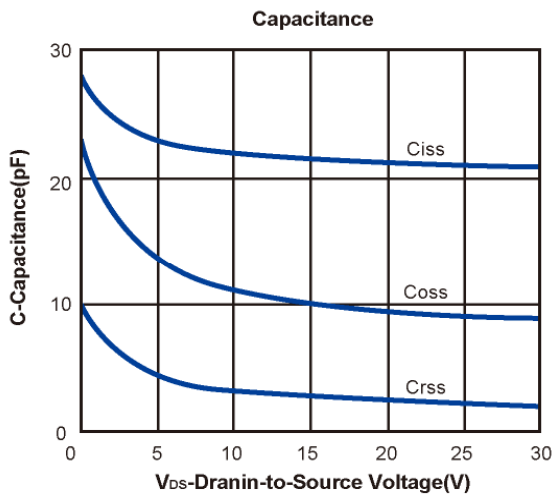
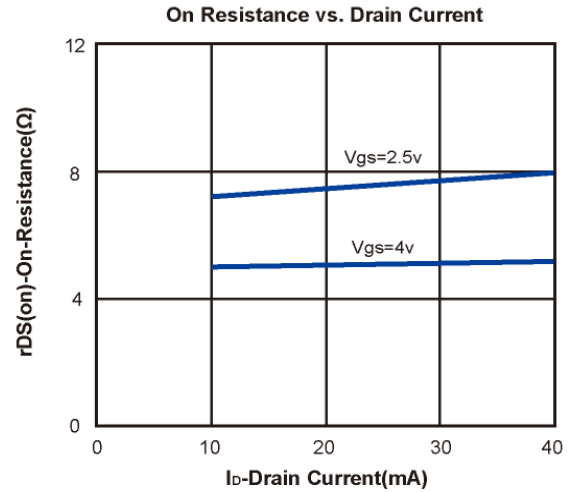
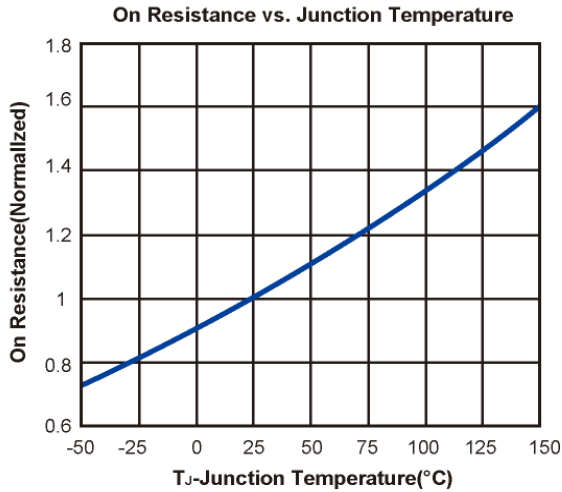
**Electrical Characteristics** (T<sub>j</sub>=25°C Unless Otherwise Specified)

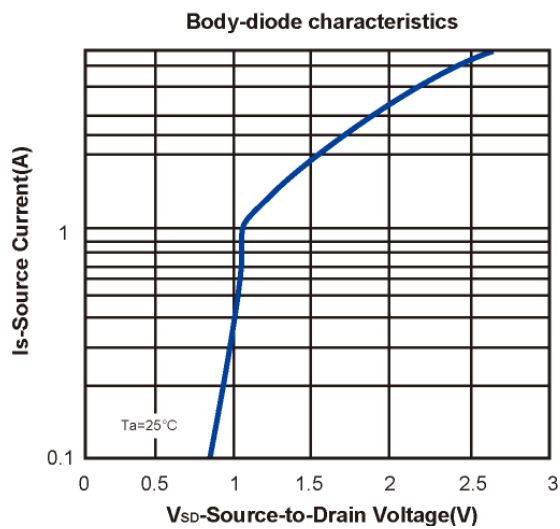
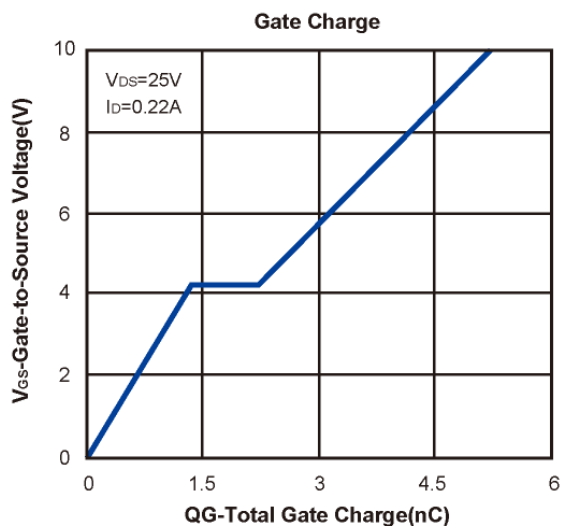
Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250 μA	30			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 μA	0.8		1.5	V
I <sub>GSS</sub>	Gate-Body Leakage	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±10	μA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V			1	μA
R <sub>DS(ON)</sub>	Drain-Source On-Resistance*	V <sub>GS</sub> =4V, I <sub>D</sub> =10mA		5	8	Ω
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =1mA		7	13	
V <sub>SD</sub>	Diode Forward Voltage *	I <sub>S</sub> =200mA, V <sub>GS</sub> =0V			1.2	V
<b>DYNAMIC</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =25V, V <sub>GS</sub> =10V, I <sub>D</sub> =0.22A		4.9		nC
Q <sub>gs</sub>	Gate-Source Charge			2.1		
Q <sub>gd</sub>	Gate-Drain Charge			0.6		
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz		21		pF
C <sub>oss</sub>	Output Capacitance			10		
C <sub>rss</sub>	Reverse Transfer Capacitance			2		
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =5V, R <sub>L</sub> =500Ω V <sub>GES</sub> =5V, R <sub>G</sub> =10Ω		10.1		ns
t <sub>r</sub>	Turn-On Rise Time			7.3		
t <sub>d(off)</sub>	Turn-Off Delay Time			31.3		
t <sub>f</sub>	Turn-Off Fall Time			28.2		

Notes: \*. Pulse test; pulse width ≤ 300us, duty cycle ≤ 2%.

L2N7002FLT1G

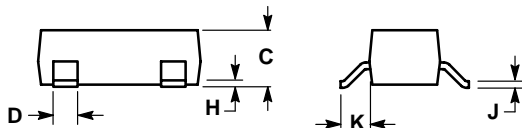
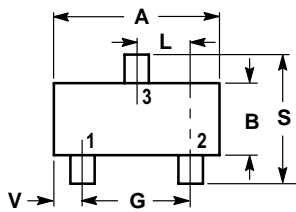
Typical Characteristics (T<sub>J</sub> =25°C Noted)



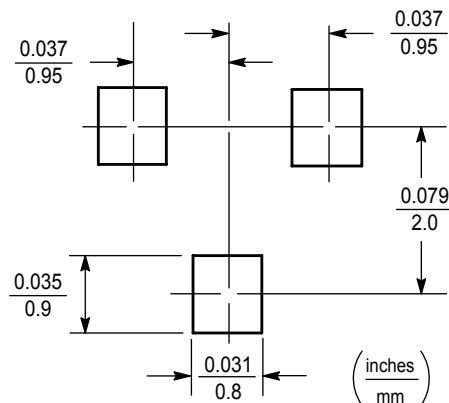
**L2N7002FLT1G**
**Typical Characteristics (T<sub>J</sub> =25°C Noted)**


**L2N7002FLT1G**
**SOT-23**
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: INCH.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60



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