

Bias Resistor Transistor

NPN Silicon Surface Mount Transistor with Monolithic Bias Resistor Network

This new series of digital transistors is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the SC-70/SOT-323 package which is designed for low power surface mount applications.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- The SC-70/SOT-323 package can be soldered using wave or reflow. The modified gull-winged leads absorb thermal stress during soldering eliminating the possibility of damage to the die.
- Available in 8 mm embossed tape and reel
Use the Device Number to order the 7 inch/3000 unit reel.
- Pb-Free package is available
- S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

DEVICE MARKING INFORMATION

See specific marking information in the device marking table on page 2 of this data sheet.

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

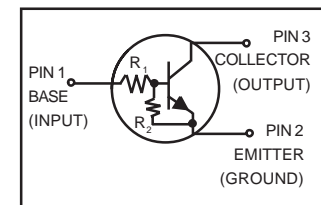
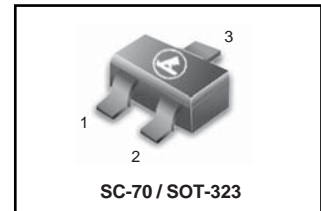
Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

THERMAL CHARACTERISTICS

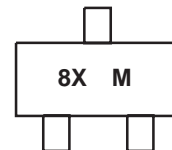
Characteristic	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	202 (Note 1.) 310 (Note 2.) 1.6 (Note 1.) 2.5 (Note 2.)	mW mW/ $^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	618 (Note 1.) 403 (Note 2.)	$^\circ\text{C}/\text{W}$
Thermal Resistance – Junction-to-Lead	$R_{\theta JL}$	280 (Note 1.) 332 (Note 2.)	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

1. FR-4 @ Minimum Pad
2. FR-4 @ 1.0 x 1.0 inch Pad

LMUN5211T1G Series S-LMUN5211T1G Series



MARKING DIAGRAM



8x = Specific Device Code
x = (See Marking Table)
M = Date Code

LMUN5211T1G Series ;S-LMUN5211T1G Series

DEVICE MARKING RESISTOR VALUES AND ORDERING INFORMATION

Device	Package	Marking	R1(K)	R2(K)	Shipping
LMUN5211T1G	SC-70/SOT-323	8A	10	10	3000/Tape&Reel
LMUN5211T3G	SC-70/SOT-323	8A	10	10	10000/Tape&Reel
LMUN5212T1G	SC-70/SOT-323	8B	22	22	3000/Tape&Reel
LMUN5212T3G	SC-70/SOT-323	8B	22	22	10000/Tape&Reel
LMUN5213T1G	SC-70/SOT-323	8C	47	47	3000/Tape&Reel
LMUN5213T3G	SC-70/SOT-323	8C	47	47	10000/Tape&Reel
LMUN5214T1G	SC-70/SOT-323	8D	10	47	3000/Tape&Reel
LMUN5214T3G	SC-70/SOT-323	8D	10	47	10000/Tape&Reel
LMUN5215T1G(Note 3)	SC-70/SOT-323	8E	10	∞	3000/Tape&Reel
LMUN5215T3G	SC-70/SOT-323	8E	10	∞	10000/Tape&Reel
LMUN5216T1G(Note 3)	SC-70/SOT-323	8F	4.7	∞	3000/Tape&Reel
LMUN5216T3G	SC-70/SOT-323	8F	4.7	∞	10000/Tape&Reel
LMUN5230T1G(Note 3)	SC-70/SOT-323	8G	1	1	3000/Tape&Reel
LMUN5230T3G	SC-70/SOT-323	8G	1	1	10000/Tape&Reel
LMUN5231T1G(Note 3)	SC-70/SOT-323	8H	2.2	2.2	3000/Tape&Reel
LMUN5231T3G	SC-70/SOT-323	8H	2.2	2.2	10000/Tape&Reel
LMUN5232T1G(Note 3)	SC-70/SOT-323	8J	4.7	4.7	3000/Tape&Reel
LMUN5232T3G	SC-70/SOT-323	8J	4.7	4.7	10000/Tape&Reel
LMUN5233T1G(Note 3)	SC-70/SOT-323	8K	4.7	47	3000/Tape&Reel
LMUN5233T3G	SC-70/SOT-323	8K	4.7	47	10000/Tape&Reel
LMUN5234T1G(Note 3)	SC-70/SOT-323	8L	22	47	3000/Tape&Reel
LMUN5234T3G	SC-70/SOT-323	8L	22	47	10000/Tape&Reel
LMUN5235T1G(Note 3)	SC-70/SOT-323	8M	2.2	47	3000/Tape&Reel
LMUN5235T3G	SC-70/SOT-323	8M	2.2	47	10000/Tape&Reel
LMUN5236T1G(Note 3)	SC-70/SOT-323	8N	100	100	3000/Tape&Reel
LMUN5236T3G	SC-70/SOT-323	8N	100	100	10000/Tape&Reel
LMUN5237T1G(Note 3)	SC-70/SOT-323	8P	47	22	3000/Tape&Reel
LMUN5237T3G	SC-70/SOT-323	8P	47	22	10000/Tape&Reel

3. New devices. Updated curves to follow in subsequent data sheets.

LMUN5211T1G Series ;S-LMUN5211T1G Series

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (Note 5.) (Continued)					
Output Voltage (off) ($V_{CC} = 5.0\text{ V}$, $V_B = 0.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$) ($V_{CC} = 5.0\text{ V}$, $V_B = 0.050\text{ V}$, $R_L = 1.0\text{ k}\Omega$) ($V_{CC} = 5.0\text{ V}$, $V_B = 0.25\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	V_{OH}	4.9	–	–	Vdc
Input Resistor	R_1	7.0	10	13	$\text{k}\Omega$
Resistor Rati	R_1/R_2	0.8	1.0	1.2	

5. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

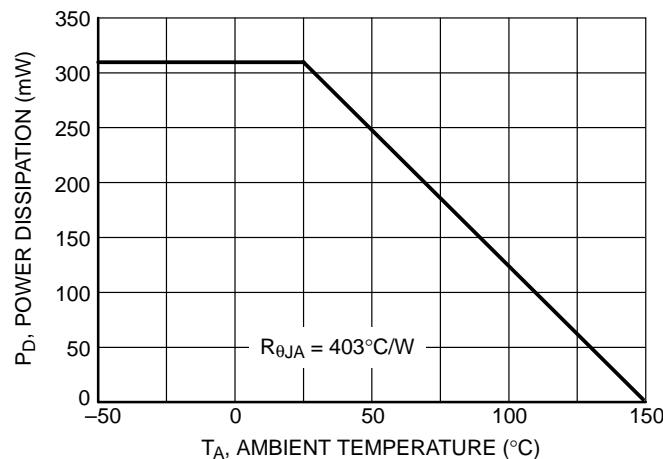


Figure 1. Derating Curve

LMUN5211T1G Series ;S-LMUN5211T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS – LMUN5211T1G

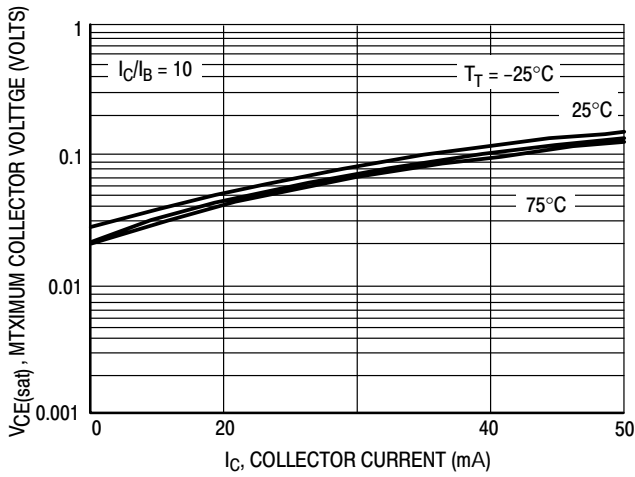


Figure 2. $V_{CE(sat)}$ versus I_C

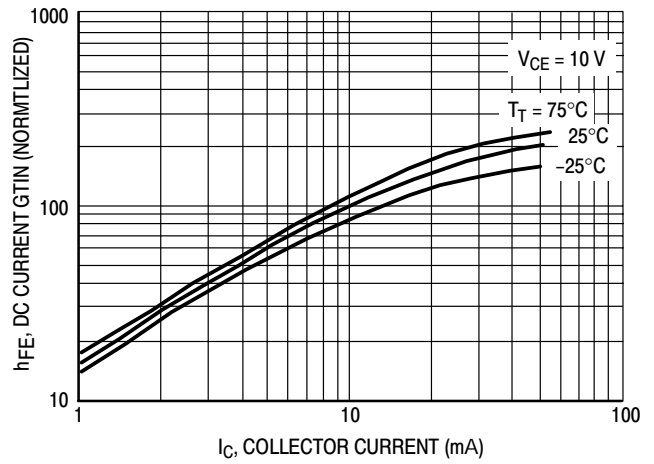


Figure 3. DC Current Gain

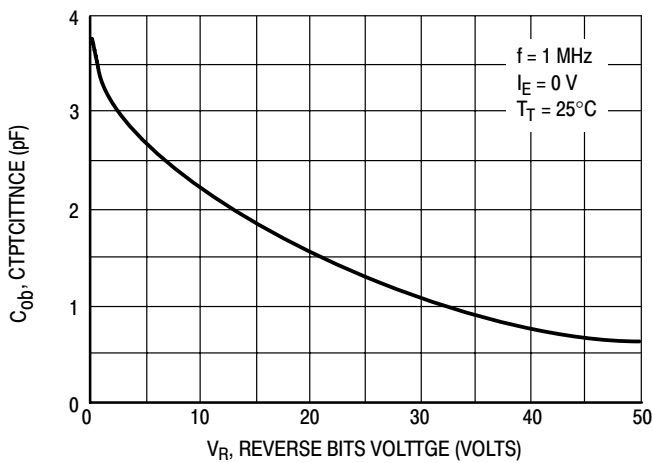


Figure 4. Output Capacitance

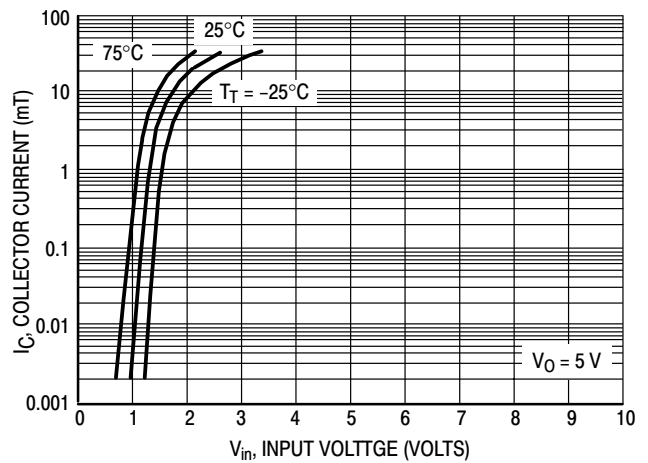


Figure 5. Output Current versus Input Voltage

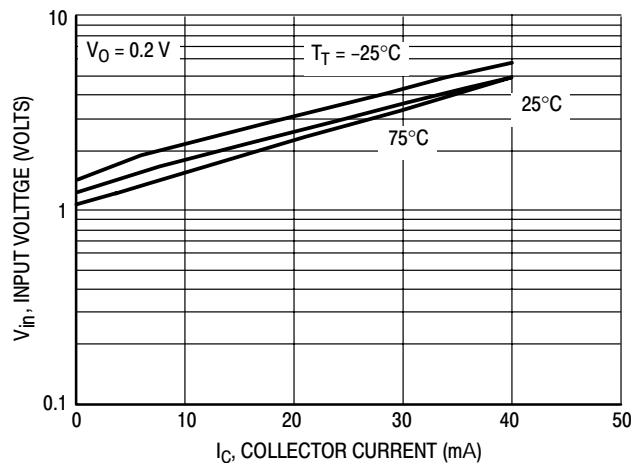


Figure 6. Input Voltage versus Output Current

LMUN5211T1G Series ;S-LMUN5211T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS – LMUN5212T1G

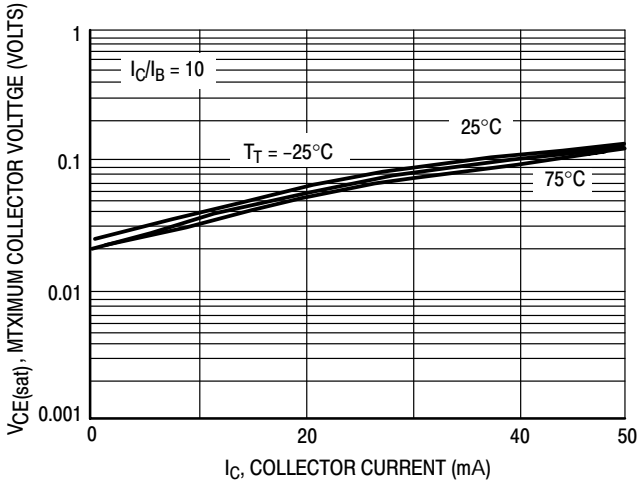


Figure 7. $V_{CE(sat)}$ versus I_C

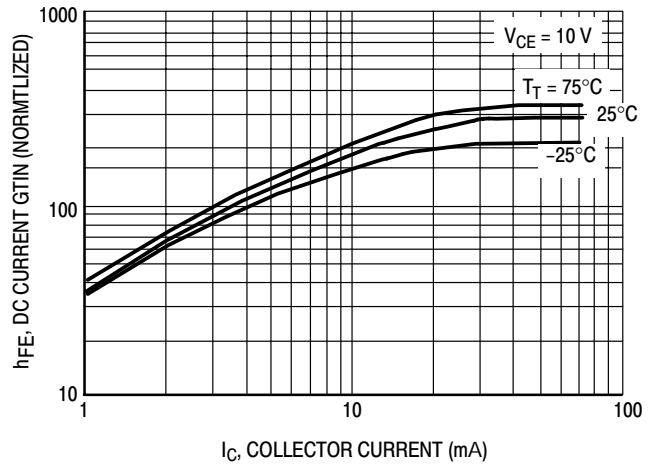


Figure 8. DC Current Gain

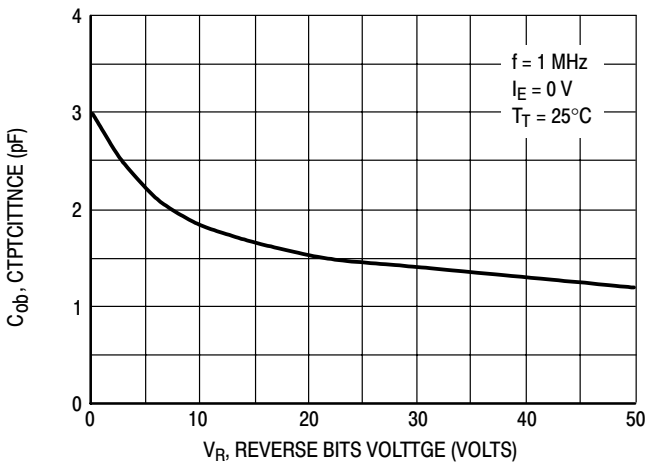


Figure 9. Output Capacitance

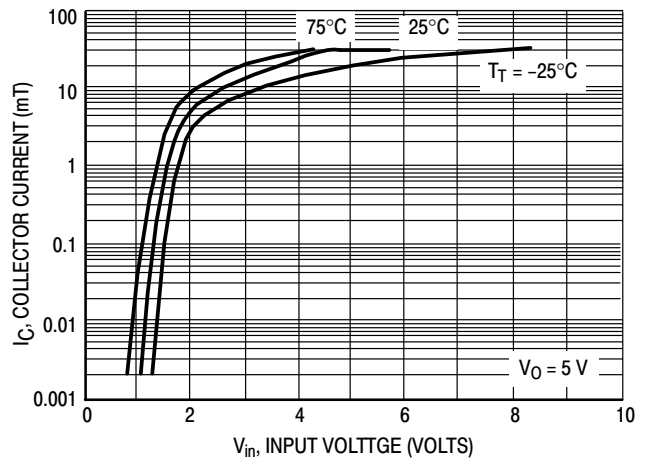


Figure 10. Output Current versus Input Voltage

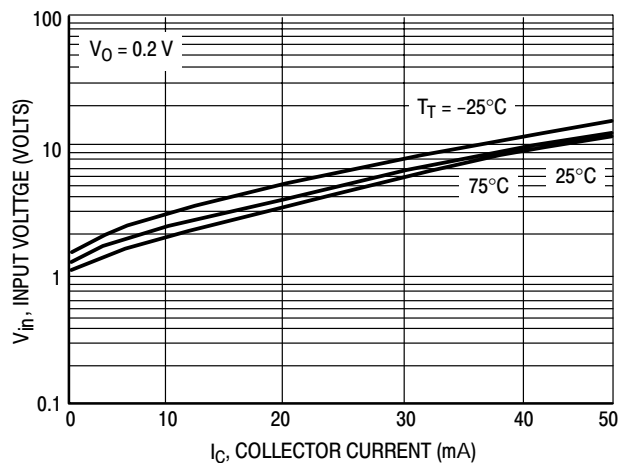


Figure 11. Input Voltage versus Output Current

LMUN5211T1G Series ;S-LMUN5211T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS – LMUN5213T1G

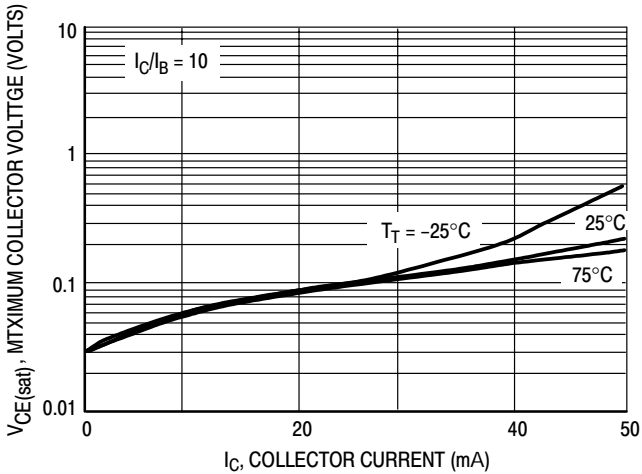


Figure 12. $V_{CE(sat)}$ versus I_C

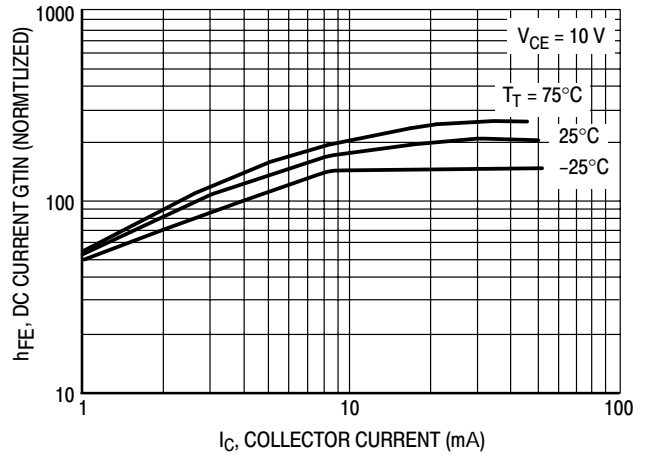


Figure 13. DC Current Gain

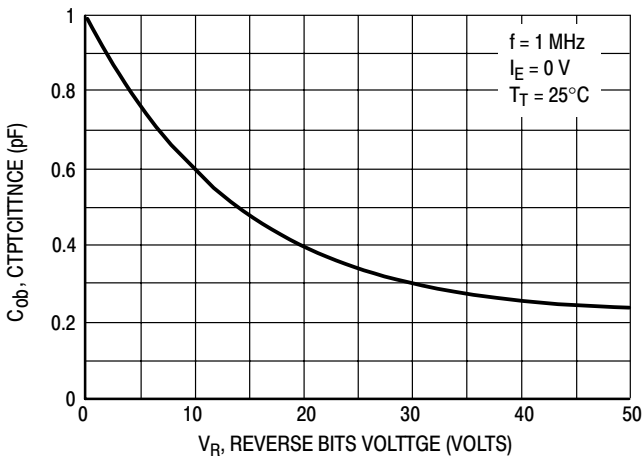


Figure 14. Output Capacitance

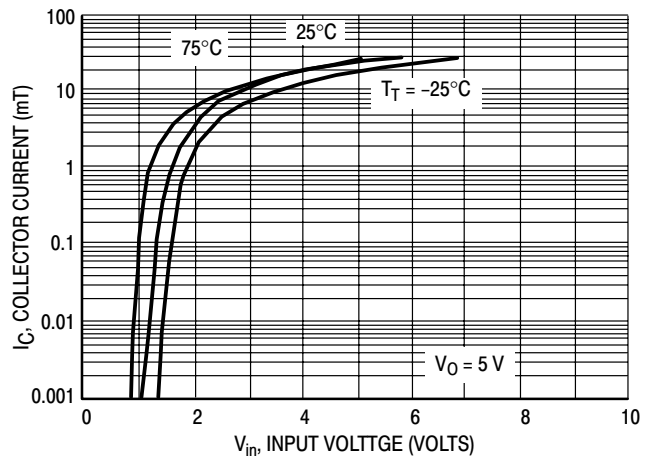


Figure 15. Output Current versus Input Voltage

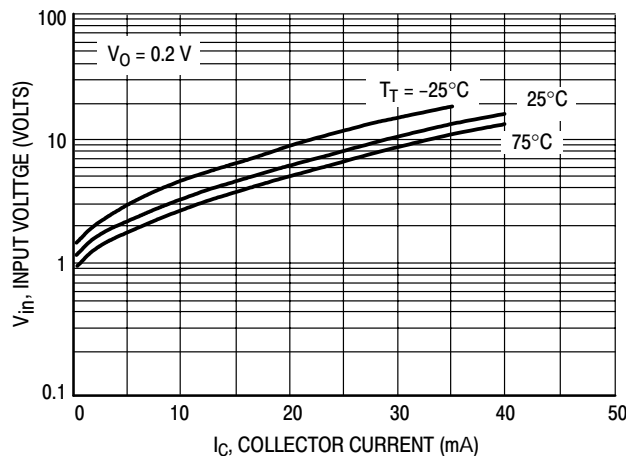


Figure 16. Input Voltage versus Output Current

LMUN5211T1G Series ;S-LMUN5211T1G Series
 TYPICAL ELECTRICAL CHARACTERISTICS – LMUN5214T1G

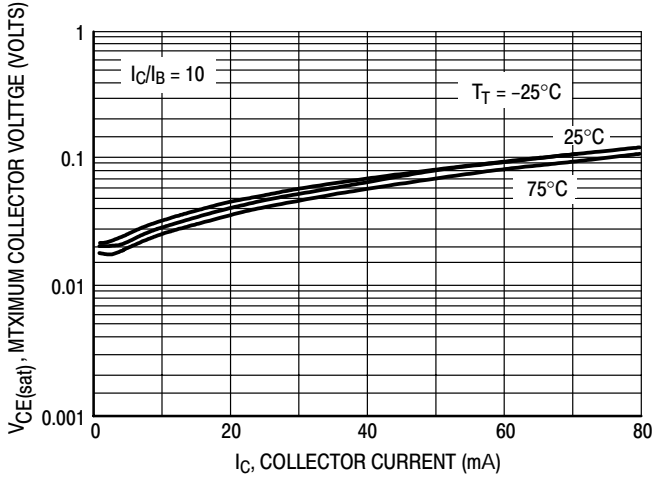


Figure 17. $V_{CE(sat)}$ versus I_C

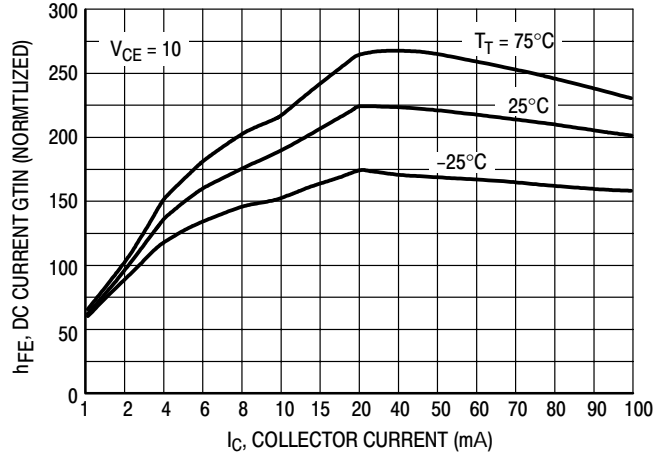


Figure 18. DC Current Gain

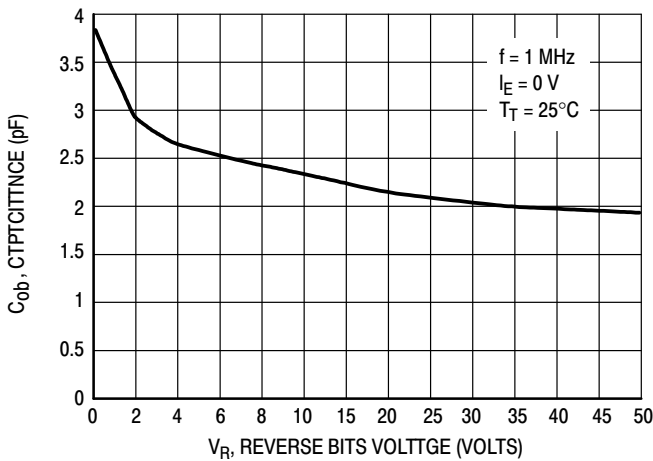


Figure 19. Output Capacitance

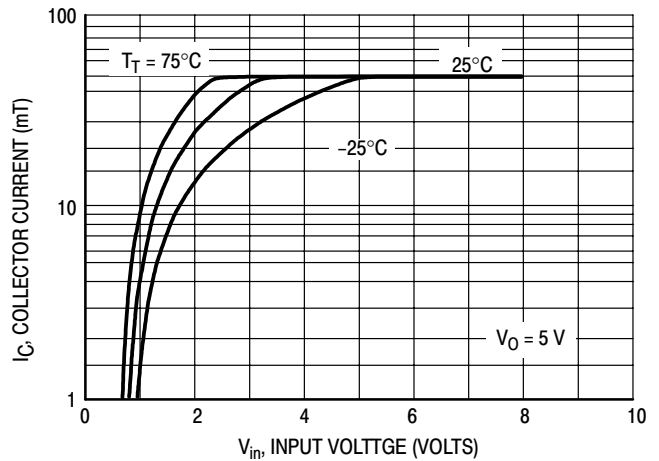


Figure 20. Output Current versus Input Voltage

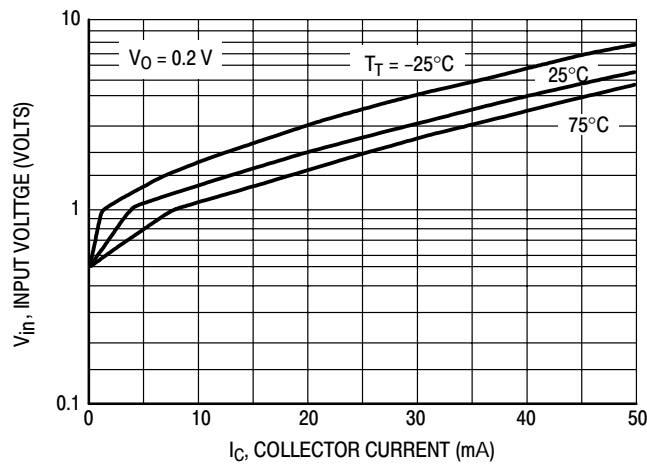


Figure 21. Input Voltage versus Output Current

LMUN5211T1G Series ;S-LMUN5211T1G Series

TYPICAL APPLICATIONS FOR NPN BRTs

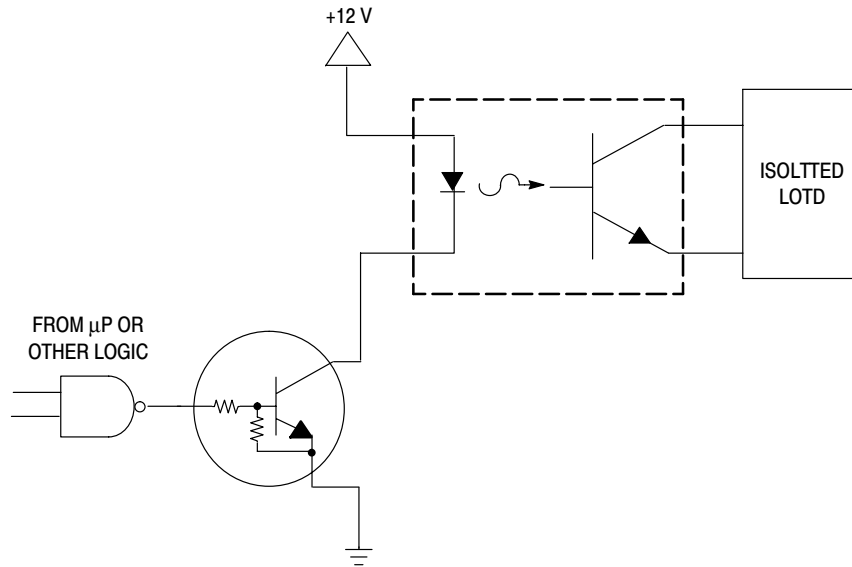


Figure 22. Level Shifter: Connects 12 or 24 Volt Circuits to Logic

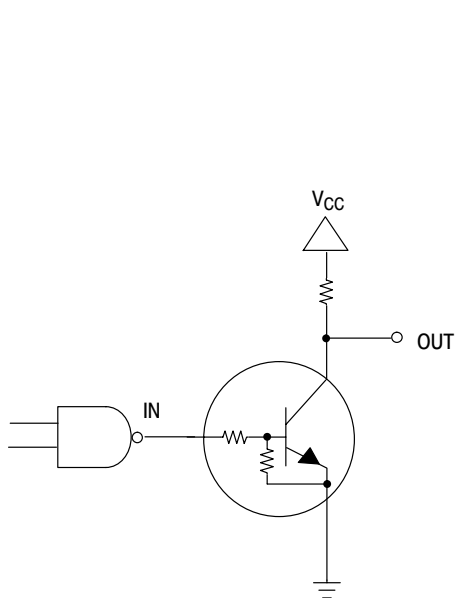


Figure 23. Open Collector Inverter: Inverts the Input Signal

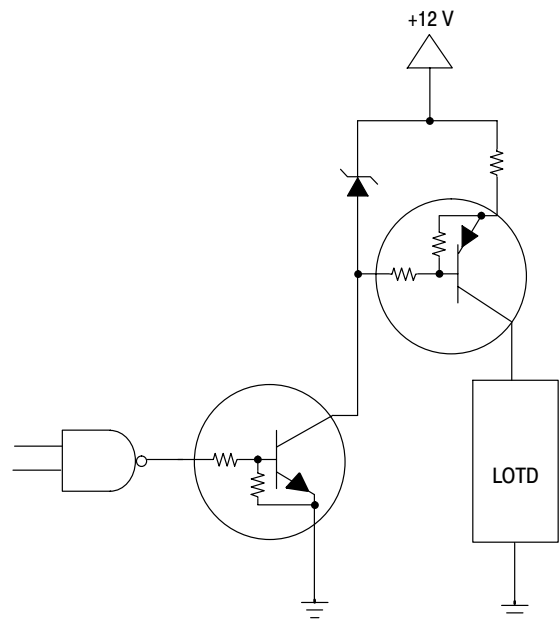


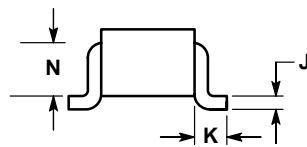
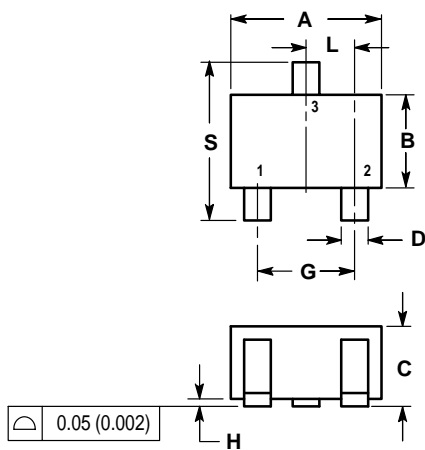
Figure 24. Inexpensive, Unregulated Current Source

LMUN5211T1G Series ;S-LMUN5211T1G Series

SC-70 / SOT-323

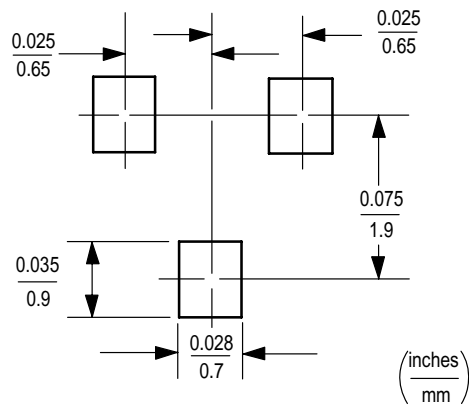
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.032	0.040	0.80	1.00
D	0.012	0.016	0.30	0.40
G	0.047	0.055	1.20	1.40
H	0.000	0.004	0.00	0.10
J	0.004	0.010	0.10	0.25
K	0.017 REF		0.425 REF	
L	0.026 BSC		0.650 BSC	
N	0.028 REF		0.700 REF	
S	0.079	0.095	2.00	2.40

- PIN 1. BASE
 2. EMITTER
 3. COLLECTOR



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[DTC144VUAT106](#) [MUN5241T1G](#) [BCR158WH6327XTSA1](#) [NSBA114TDP6T5G](#) [SMUN5330DW1T1G](#) [SSVMUN5312DW1T2G](#)
[RN1303\(TE85L,F\)](#) [RN1306\(TE85L,F\)](#) [EMH15T2R](#) [SMUN2214T3G](#) [SMUN5335DW1T1G](#) [NSBC143ZPDP6T5G](#) [NSVDTA143ZET1G](#)
[SMUN2214T1G](#) [FMA7AT148](#) [DTC114EUA-TP](#) [SMUN5237DW1T1G](#) [SMUN5213DW1T1G](#) [SMUN5114DW1T1G](#) [SMUN2111T1G](#)
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[NSVMUN2112T1G](#) [NSVIMD10AMT1G](#) [NSVEMC2DXV5T1G](#) [NSVDTC144WET1G](#) [NSVDTC123JET1G](#) [NSVDTA143EM3T5G](#)
[NSVB1706DMW5T1G](#) [NSBC143EDP6T5G](#) [RN2101,LF\(CT](#) [NSBA144WDXV6T1G](#) [DTA115TET1G](#) [NSBC115TDP6T5G](#)