

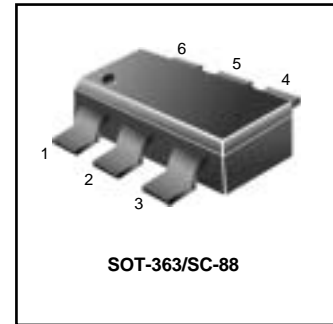
Dual Bias Resistor Transistors

NPN and PNP Silicon Surface Mount

Transistors with Monolithic Bias

Resistor Network

LMUN5311DW1T1G
Series

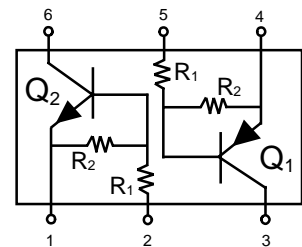


The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the LMUN5311DW1T1G series, two complementary BRT devices are housed in the SOT-363 package which is ideal for low power surface mount applications where board space is at a premium.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- We declare that the material of product compliance with RoHS requirements.

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted, common for Q 1 and Q 2, – minus sign for Q 1 (PNP) omitted)

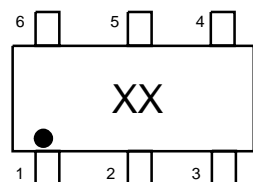
Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc



THERMAL CHARACTERISTICS

Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$	P_D	187 (Note 1.) 256 (Note 2.)	mW
Derate above 25°C		1.5 (Note 1.) 2.0 (Note 2.)	mW/ $^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	670 (Note 1.) 490 (Note 2.)	$^\circ\text{C}/\text{W}$
Characteristic (Both Junctions Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$	P_D	250 (Note 1.) 385 (Note 2.)	mW
Derate above 25°C		2.0 (Note 1.) 3.0 (Note 2.)	mW/ $^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	493 (Note 1.) 325 (Note 2.)	$^\circ\text{C}/\text{W}$
Thermal Resistance – Junction-to-Lead	$R_{\theta JL}$	188 (Note 1.) 208 (Note 2.)	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

MARKING DIAGRAM



xx = Device Marking
(See Page 2)

DEVICE MARKING INFORMATION

See specific marking information in the device marking table on page 2 of this data sheet.

1. FR-4 @ Minimum Pad 2. FR-4 @ 1.0 x 1.0 inch Pad

LMUN5311DW1T1G Series

ORDERING, SHIPPING, DEVICE MARKING AND RESISTOR VALUES

Device	Package	Marking	R1(K)	R2(K)	Shipping
LMUN5311DW1T1G	SOT-363	11	10	10	3000/Tape&Reel
LMUN5311DW1T3G	SOT-363	11	10	10	10000/Tape&Reel
LMUN5312DW1T1G	SOT-363	12	22	22	3000/Tape&Reel
LMUN5312DW1T3G	SOT-363	12	22	22	10000/Tape&Reel
LMUN5313DW1T1G	SOT-363	13	47	47	3000/Tape&Reel
LMUN5313DW1T3G	SOT-363	13	47	47	10000/Tape&Reel
LMUN5314DW1T1G	SOT-363	14	10	47	3000/Tape&Reel
LMUN5314DW1T3G	SOT-363	14	10	47	10000/Tape&Reel
LMUN5315DW1T1G	SOT-363	15	10	∞	3000/Tape&Reel
LMUN5315DW1T3G	SOT-363	15	10	∞	10000/Tape&Reel
LMUN5316DW1T1G	SOT-363	16	4.7	∞	3000/Tape&Reel
LMUN5316DW1T3G	SOT-363	16	4.7	∞	10000/Tape&Reel
LMUN5330DW1T1G	SOT-363	30	1	1	3000/Tape&Reel
LMUN5330DW1T3G	SOT-363	30	1	1	10000/Tape&Reel
LMUN5331DW1T1G	SOT-363	31	2.2	2.2	3000/Tape&Reel
LMUN5331DW1T3G	SOT-363	31	2.2	2.2	10000/Tape&Reel
LMUN5332DW1T1G	SOT-363	32	4.7	4.7	3000/Tape&Reel
LMUN5332DW1T3G	SOT-363	32	4.7	4.7	10000/Tape&Reel
LMUN5333DW1T1G	SOT-363	33	4.7	47	3000/Tape&Reel
LMUN5333DW1T3G	SOT-363	33	4.7	47	10000/Tape&Reel
LMUN5334DW1T1G	SOT-363	34	22	47	3000/Tape&Reel
LMUN5334DW1T3G	SOT-363	34	22	47	10000/Tape&Reel
LMUN5335DW1T1G	SOT-363	35	2.2	47	3000/Tape&Reel
LMUN5335DW1T3G	SOT-363	35	2.2	47	10000/Tape&Reel

LMUN5311DW1T1G Series

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted, common for Q₁ and Q₂, – minus sign for Q₁ (PNP) omitted) (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit	
ON CHARACTERISTICS (Note 4)						
DC Current Gain (V _{CE} = 10 V, I _C = 5.0 mA)	LMUN5311DW1T1G LMUN5312DW1T1G LMUN5313DW1T1G LMUN5314DW1T1G LMUN5315DW1T1G LMUN5316DW1T1G LMUN5330DW1T1G LMUN5331DW1T1G LMUN5332DW1T1G LMUN5333DW1T1G LMUN5334DW1T1G LMUN5335DW1T1G	h _{FE}	35 60 80 80 160 160 3.0 8.0 15 80 80 80	60 100 140 140 350 350 5.0 15 30 200 150 140	– – – – – – – – – – – –	
Collector-Emitter Saturation Voltage (I _C = 10 mA, I _B = 0.3 mA) (I _C = 10 mA, I _B = 5 mA) LMUN5330DW1T1G/LMUN5331DW1T1G (I _C = 10 mA, I _B = 1 mA) LMUN5315DW1T1G/LMUN5316DW1T1G LMUN5332DW1T1G/LMUN5333DW1T1G/LMUN5334DW1T1G		V _{CE(sat)}	–	–	0.25	Vdc
Output Voltage (on) (V _{CC} = 5.0 V, V _B = 2.5 V, R _L = 1.0 kΩ)	LMUN5311DW1T1G LMUN5312DW1T1G LMUN5314DW1T1G LMUN5315DW1T1G LMUN5316DW1T1G LMUN5330DW1T1G LMUN5331DW1T1G LMUN5332DW1T1G LMUN5333DW1T1G LMUN5334DW1T1G LMUN5335DW1T1G LMUN5313DW1T1G	V _{OL}	– – – – – – – – – – – –	– – – – – – – – – – – –	0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2	Vdc
Output Voltage (off) (V _{CC} = 5.0 V, V _B = 0.5 V, R _L = 1.0 kΩ) (V _{CC} = 5.0 V, V _B = 0.050 V, R _L = 1.0 kΩ) LMUN5330DW1T1G (V _{CC} = 5.0 V, V _B = 0.25 V, R _L = 1.0 kΩ) LMUN5315DW1T1G LMUN5316DW1T1G LMUN5333DW1T1G		V _{OH}	4.9	–	–	Vdc
Input Resistor	LMUN5311DW1T1G LMUN5312DW1T1G LMUN5313DW1T1G LMUN5314DW1T1G LMUN5315DW1T1G LMUN5316DW1T1G LMUN5330DW1T1G LMUN5331DW1T1G LMUN5332DW1T1G LMUN5333DW1T1G LMUN5334DW1T1G LMUN5335DW1T1G	R1	7.0 15.4 32.9 7.0 7.0 3.3 0.7 1.5 3.3 3.3 15.4 1.54	10 22 47 10 10 4.7 1.0 2.2 4.7 4.7 22 2.2	13 28.6 61.1 13 13 6.1 1.3 2.9 6.1 6.1 28.6 2.86	k Ω
Resistor Ratio	LMUN5311DW1T1G/LMUN5312DW1T1G/LMUN5313DW1T1G LMUN5314DW1T1G LMUN5315DW1T1G/LMUN5316DW1T1G LMUN5330DW1T1G/LMUN5331DW1T1G/LMUN5332DW1T1G LMUN5333DW1T1G LMUN5334DW1T1G LMUN5335DW1T1G	R1/R2	0.8 0.17 – 0.8 0.055 0.38 0.038	1.0 0.21 – 1.0 0.1 0.47 0.047	1.2 0.25 – 1.2 0.185 0.56 0.056	

4. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

LMUN5311DW1T1G Series

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise noted, common for Q_1 and Q_2 , – minus sign for Q_1 (PNP) omitted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Cutoff Current ($V_{CB} = 50\text{ V}, I_E = 0$)	I_{CBO}	–	–	100	nAdc
Collector-Emitter Cutoff Current ($V_{CE} = 50\text{ V}, I_B = 0$)	I_{CEO}	–	–	500	nAdc
Emitter-Base Cutoff Current ($V_{EB} = 6.0\text{ V}, I_C = 0$)	LMUN5311DW1T1G	–	–	0.5	mAdc
	LMUN5312DW1T1G	–	–	0.2	
	LMUN5313DW1T1G	–	–	0.1	
	LMUN5314DW1T1G	–	–	0.2	
	LMUN5315DW1T1G	–	–	0.9	
	LMUN5316DW1T1G	–	–	1.9	
	LMUN5330DW1T1G	–	–	4.3	
	LMUN5331DW1T1G	–	–	2.3	
	LMUN5332DW1T1G	–	–	1.5	
	LMUN5333DW1T1G	–	–	0.18	
	LMUN5334DW1T1G	–	–	0.13	
LMUN5335DW1T1G	–	–	0.2		
Collector-Base Breakdown Voltage ($I_C = 10\ \mu\text{A}, I_E = 0$)	$V_{(BR)CBO}$	50	–	–	Vdc
Collector-Emitter Breakdown Voltage (Note 3) ($I_C = 2.0\text{ mA}, I_B = 0$)	$V_{(BR)CEO}$	50	–	–	Vdc

3. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

ALL LMUN5311DW1T1G SERIES DEVICES

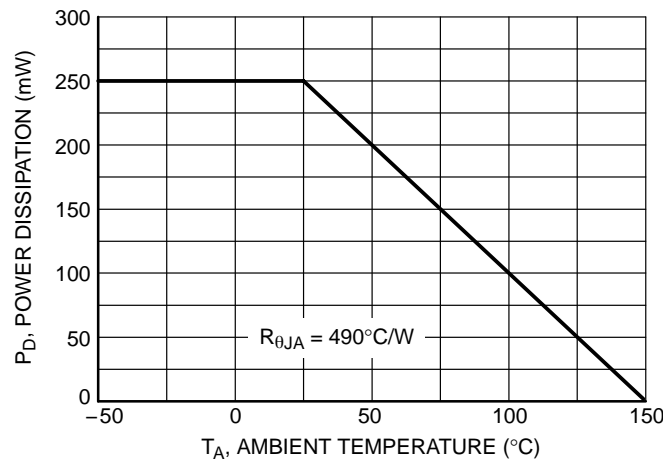


Figure 1. Derating Curve

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS – LMUN5311DW1T1G NPN TRANSISTOR

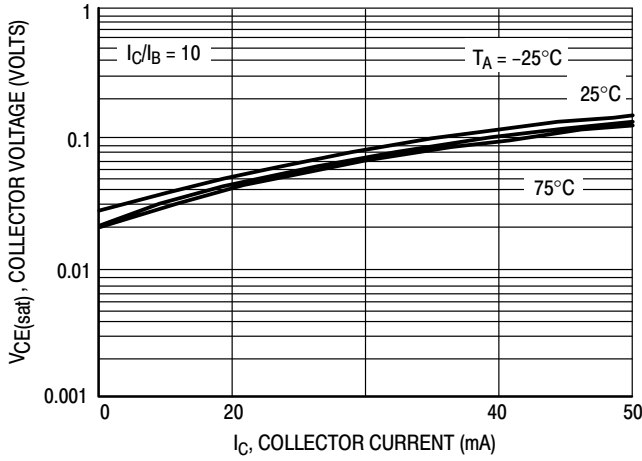


Figure 2. $V_{CE(sat)}$ versus I_C

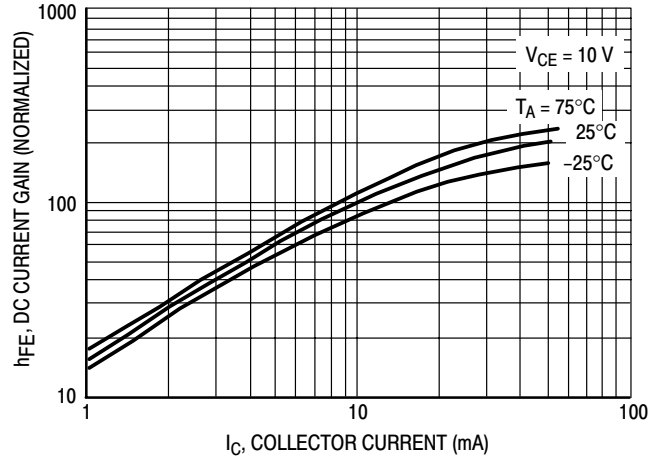


Figure 3. DC Current Gain

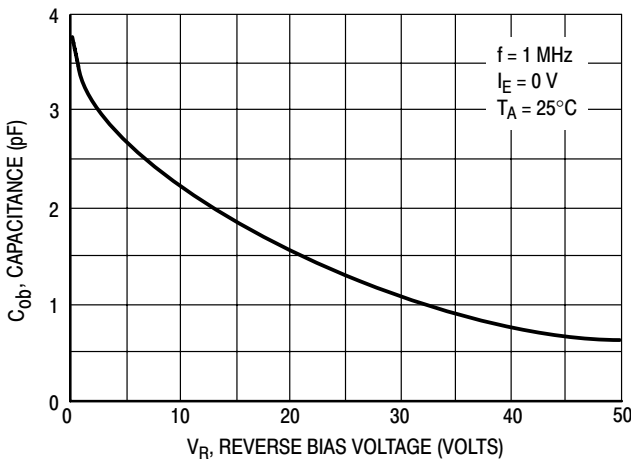


Figure 4. Output Capacitance

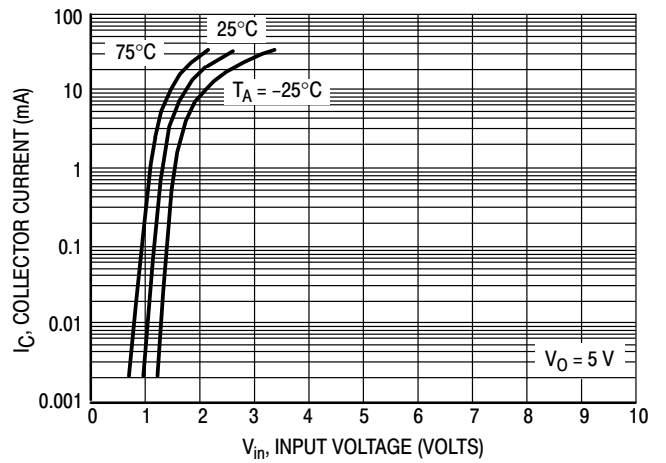


Figure 5. Output Current versus Input Voltage

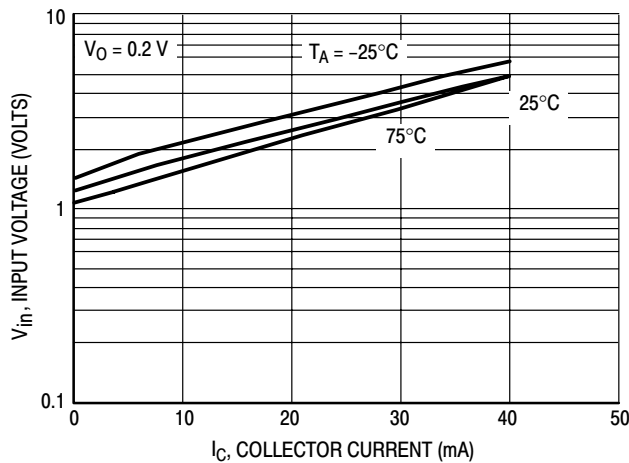


Figure 6. Input Voltage versus Output Current

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS – LMUN5311DW1T1G PNP TRANSISTOR

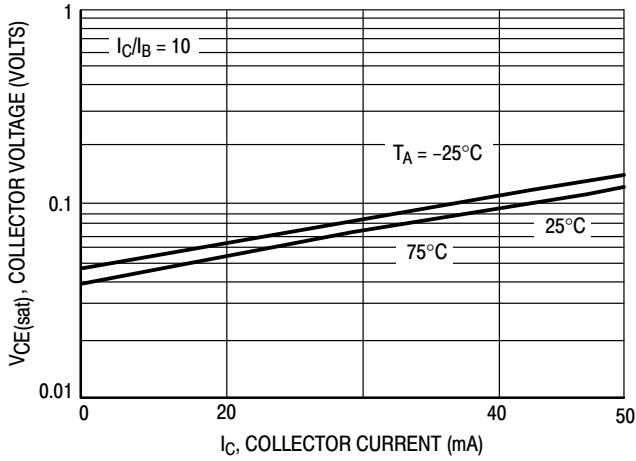


Figure 7. $V_{CE(sat)}$ versus I_C

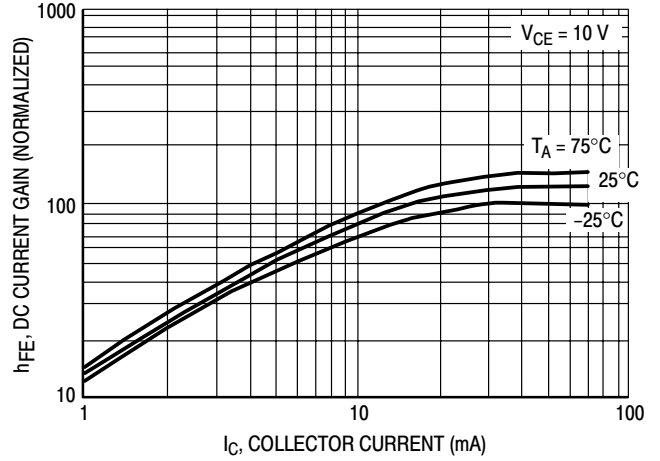


Figure 8. DC Current Gain

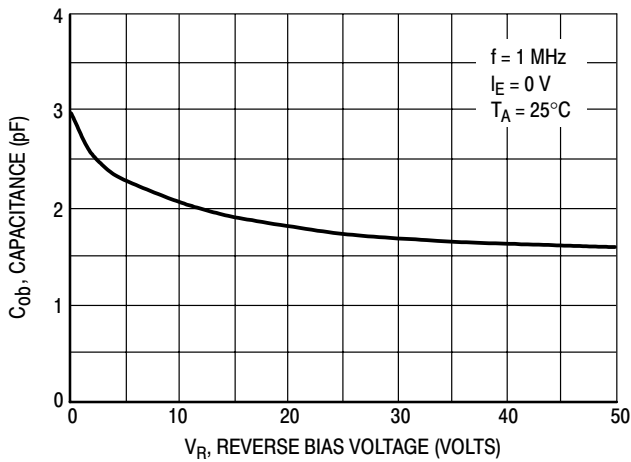


Figure 9. Output Capacitance

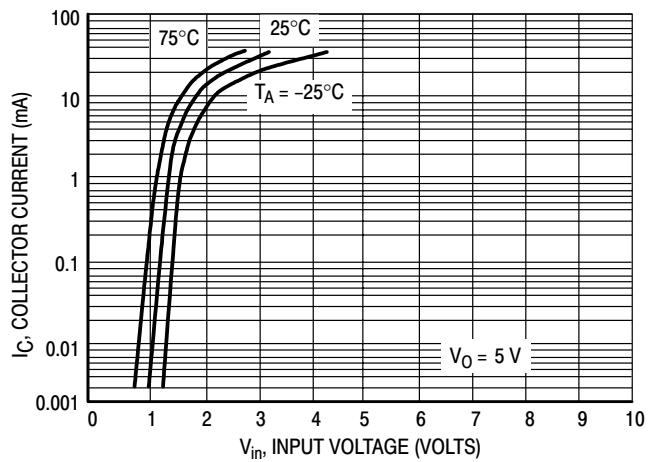


Figure 10. Output Current versus Input Voltage

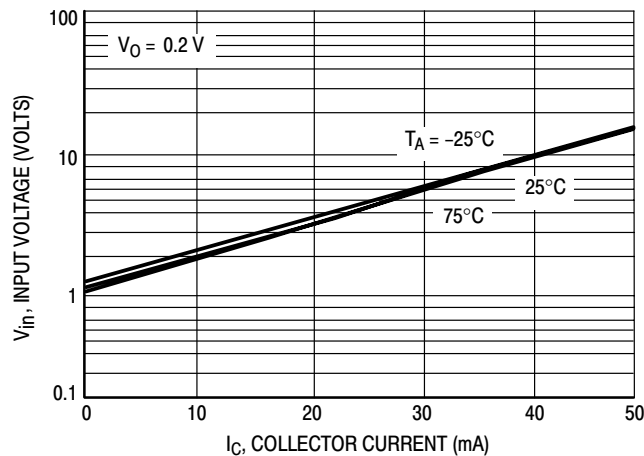


Figure 11. Input Voltage versus Output Current

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS – LMUN5312DW1T1G NPN TRANSISTOR

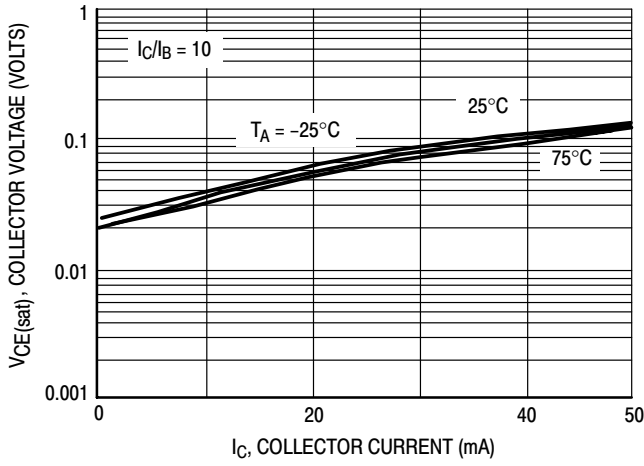


Figure 12. $V_{CE(sat)}$ versus I_C

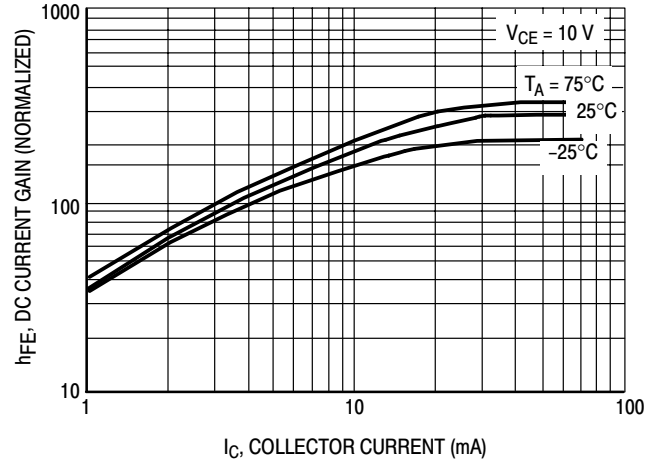


Figure 13. DC Current Gain

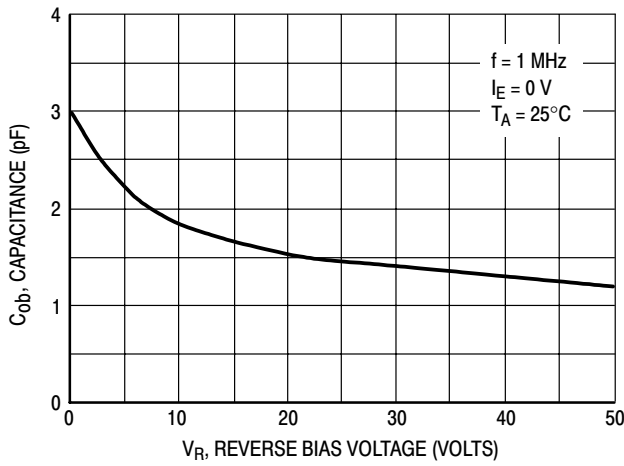


Figure 14. Output Capacitance

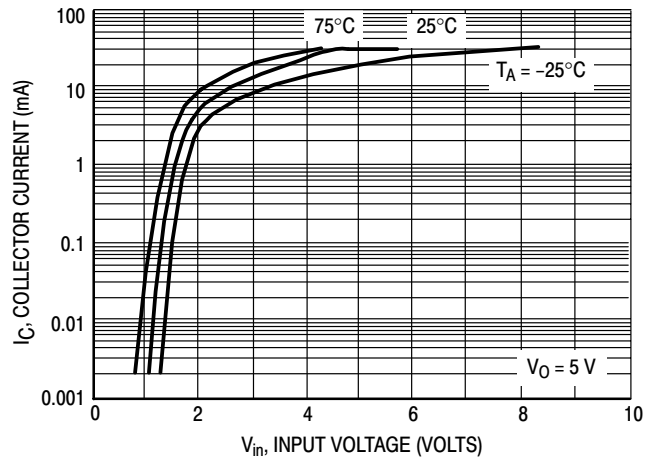


Figure 15. Output Current versus Input Voltage

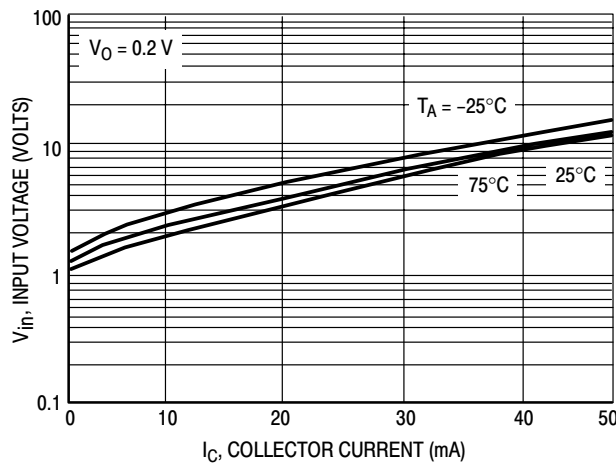


Figure 16. Input Voltage versus Output Current

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS – LMUN5312DW1T1G PNP TRANSISTOR

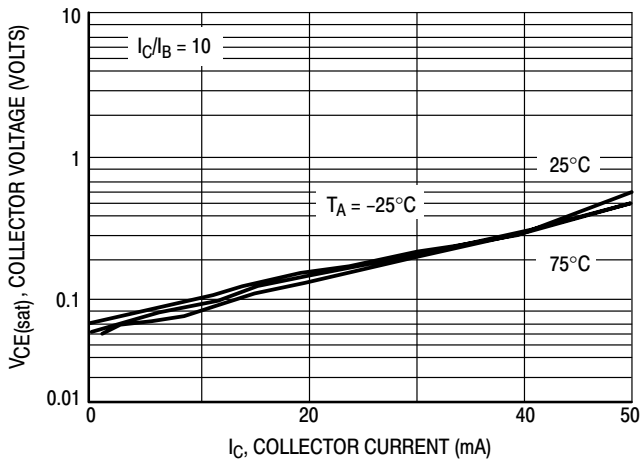


Figure 17. $V_{CE(sat)}$ versus I_C

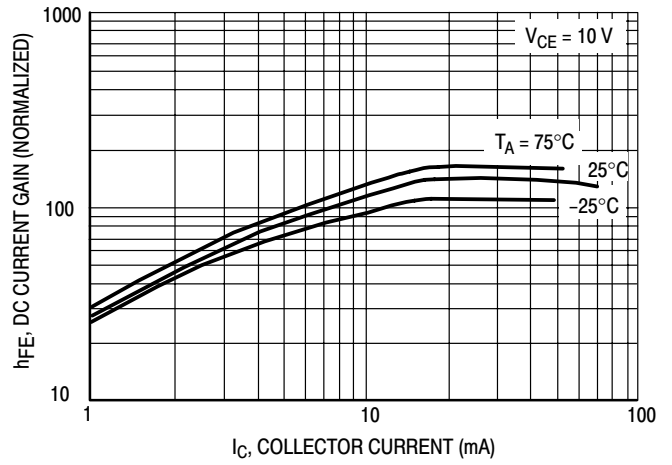


Figure 18. DC Current Gain

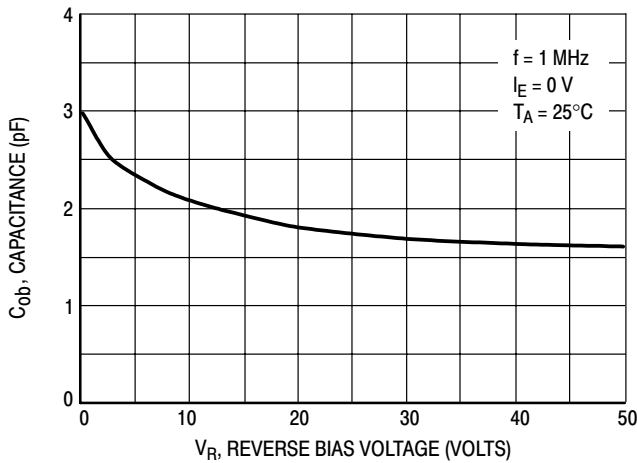


Figure 19. Output Capacitance

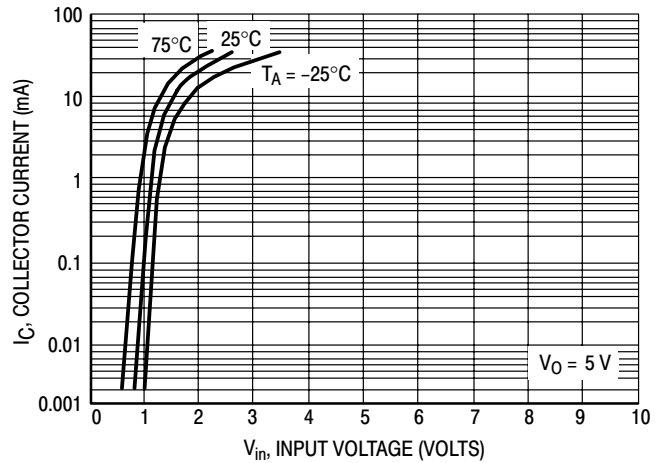


Figure 20. Output Current versus Input Voltage

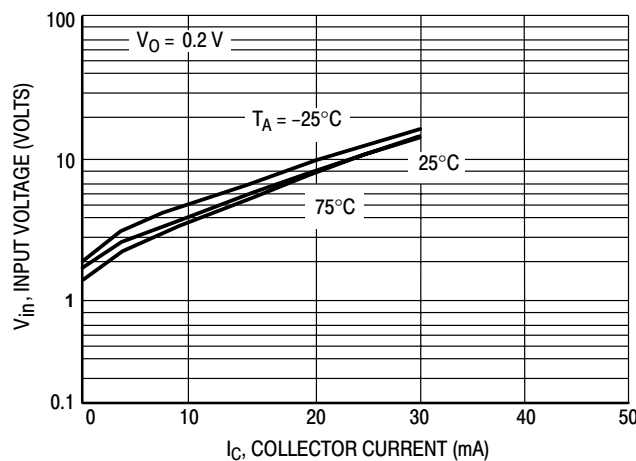


Figure 21. Input Voltage versus Output Current

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS – LMUN5313DW1T1G NPN TRANSISTOR

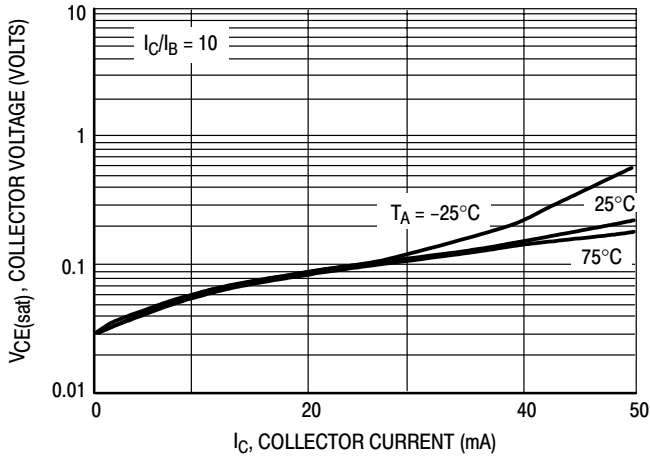


Figure 22. $V_{CE(sat)}$ versus I_C

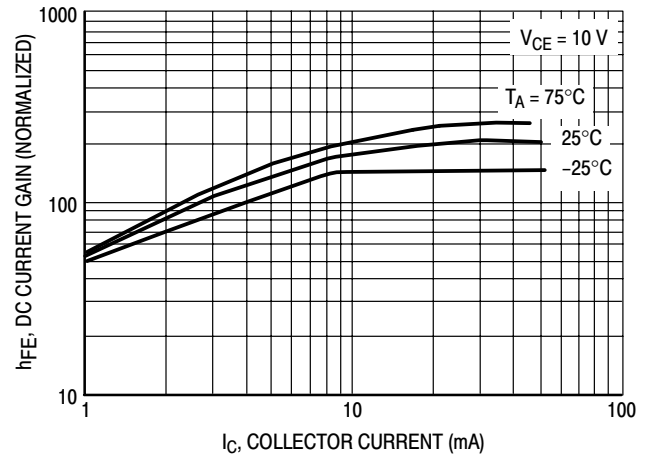


Figure 23. DC Current Gain

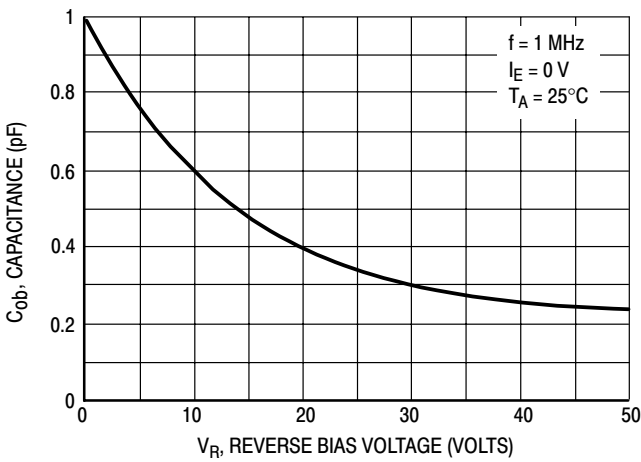


Figure 24. Output Capacitance

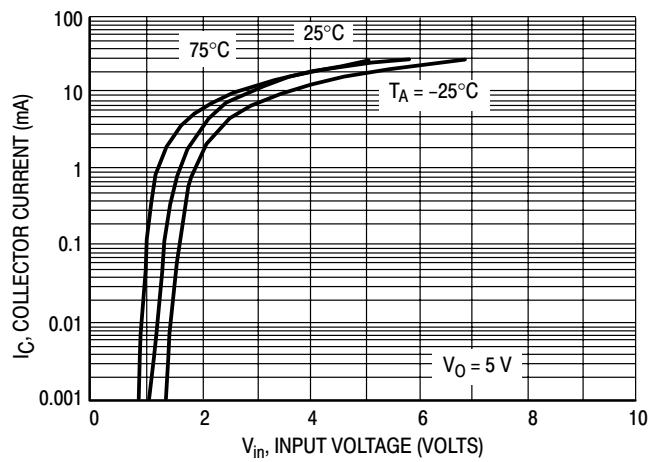


Figure 25. Output Current versus Input Voltage

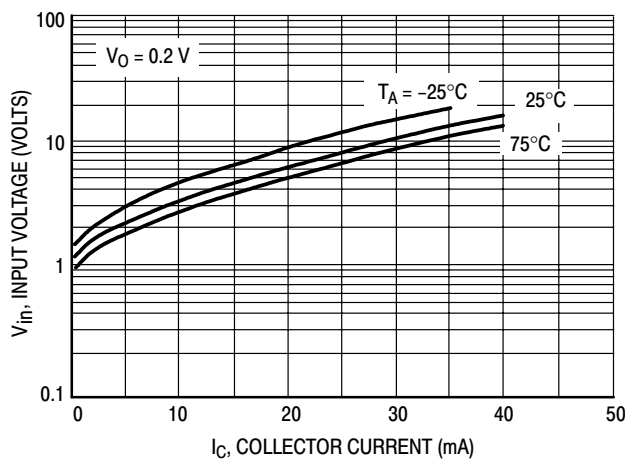


Figure 26. Input Voltage versus Output Current

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS – LMUN5313DW1T1G PNP TRANSISTOR

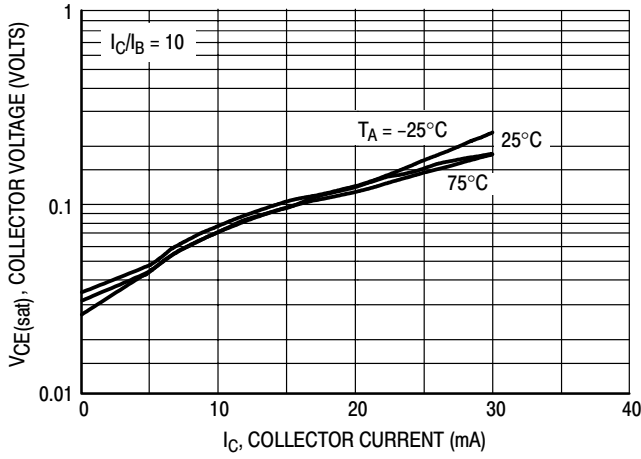


Figure 27. $V_{CE(sat)}$ versus I_C

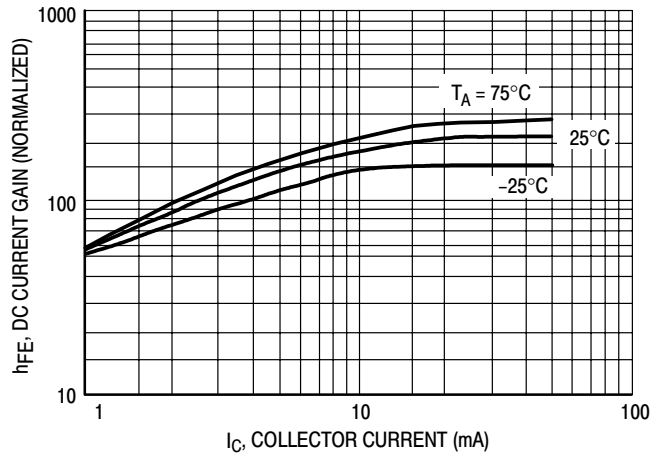


Figure 28. DC Current Gain

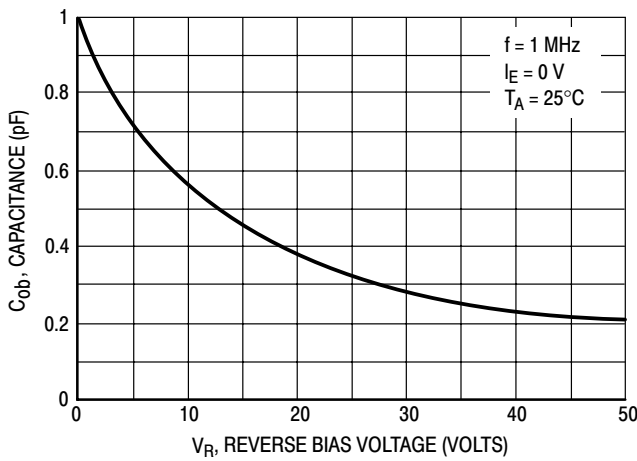


Figure 29. Output Capacitance

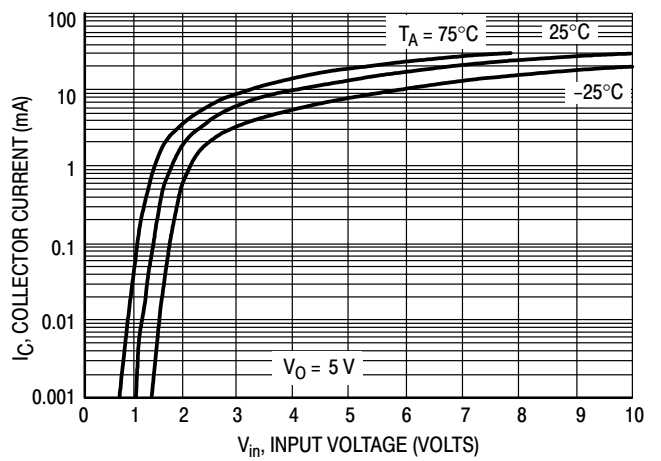


Figure 30. Output Current versus Input Voltage

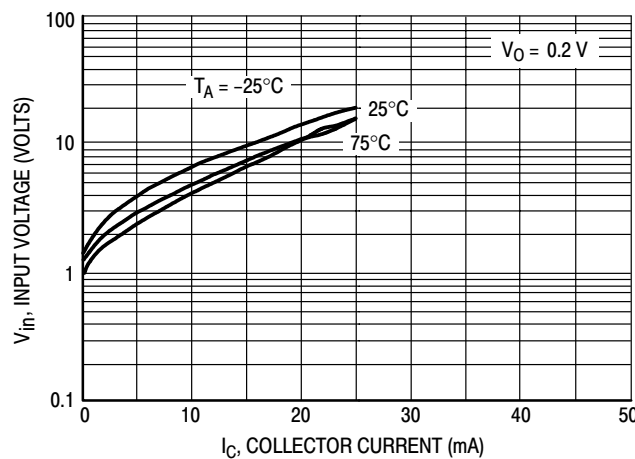


Figure 31. Input Voltage versus Output Current

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS – LMUN5314DW1T1G NPN TRANSISTOR

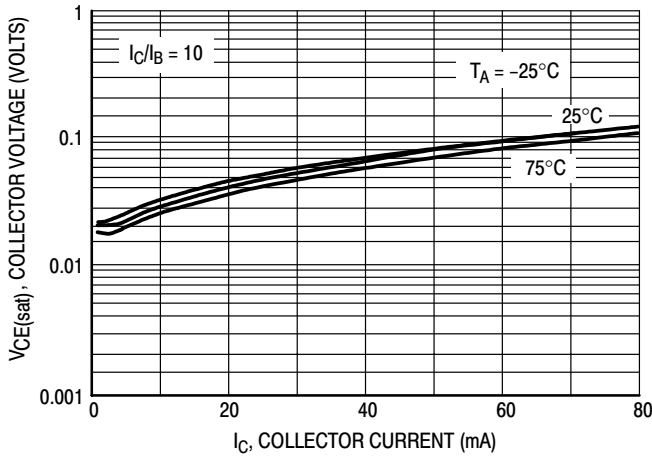


Figure 32. $V_{CE(sat)}$ versus I_C

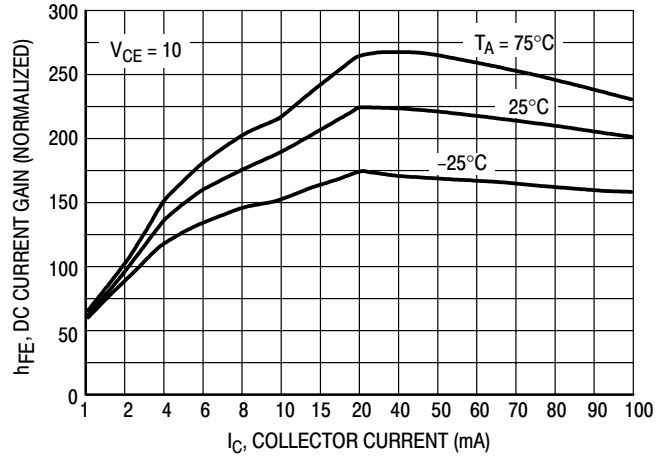


Figure 33. DC Current Gain

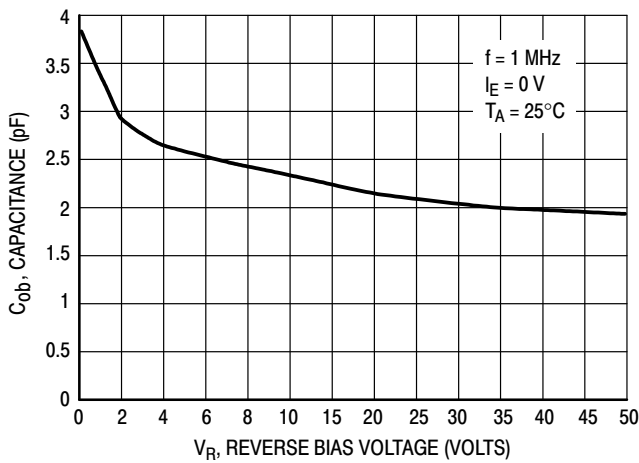


Figure 34. Output Capacitance

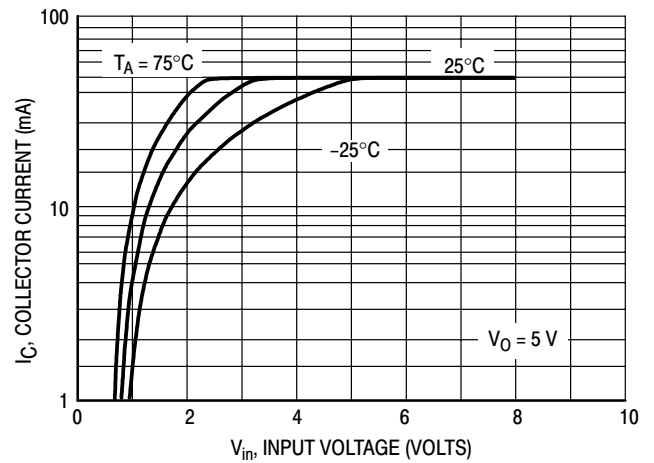


Figure 35. Output Current versus Input Voltage

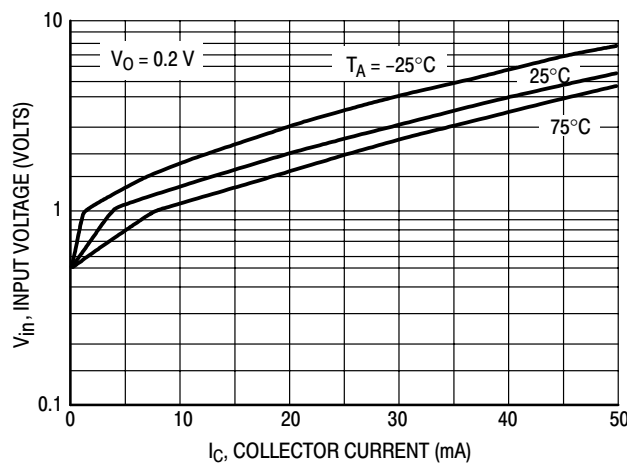


Figure 36. Input Voltage versus Output Current

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS – LMUN5314DW1T1G PNP TRANSISTOR

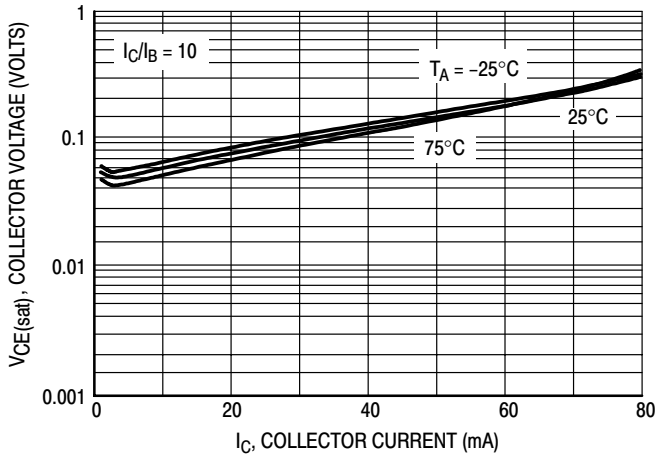


Figure 37. $V_{CE(sat)}$ versus I_C

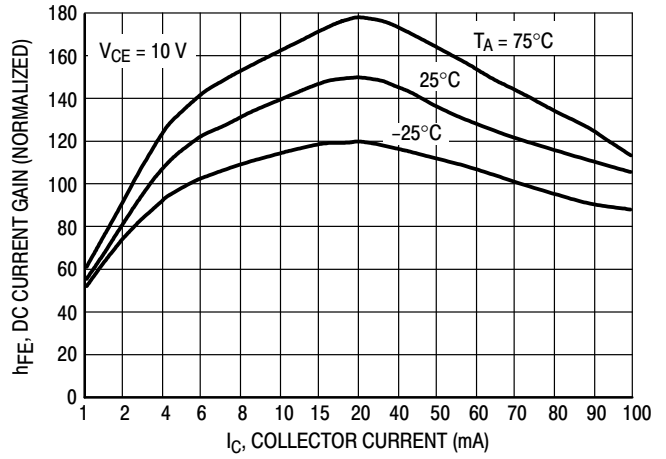


Figure 38. DC Current Gain

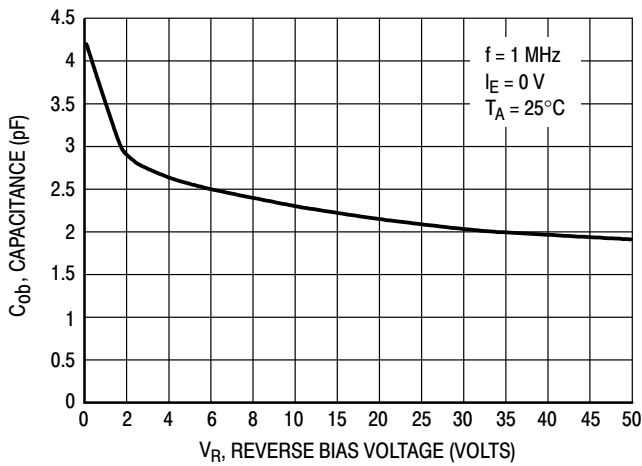


Figure 39. Output Capacitance

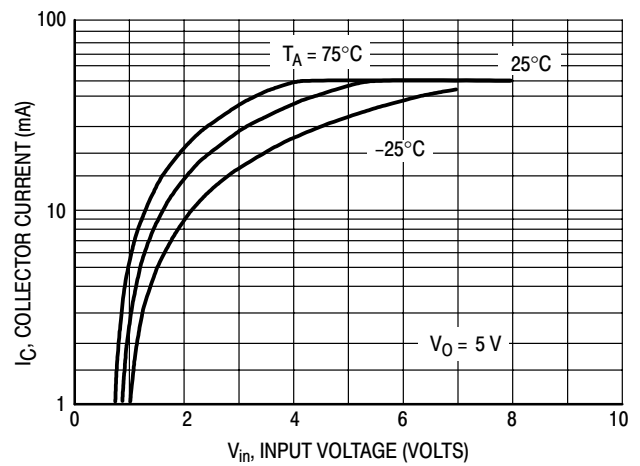


Figure 40. Output Current versus Input Voltage

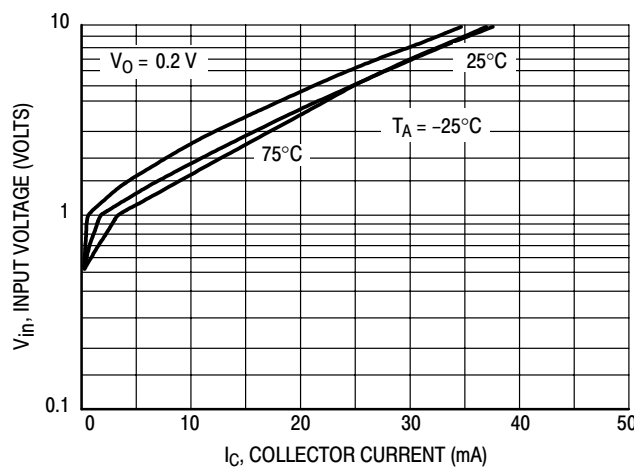


Figure 41. Input Voltage versus Output Current

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS — LMUN5315DW1T1G NPN TRANSISTOR

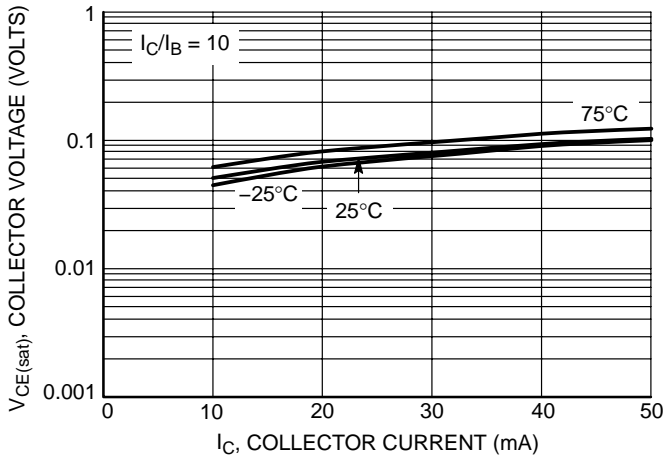


Figure 42. $V_{CE(sat)}$ versus I_C

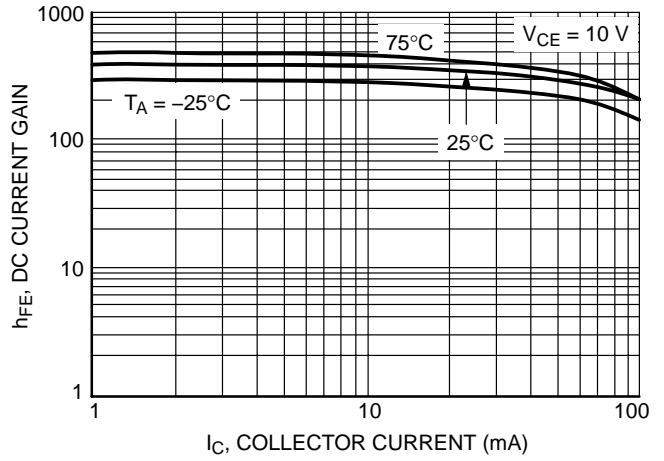


Figure 43. DC Current Gain

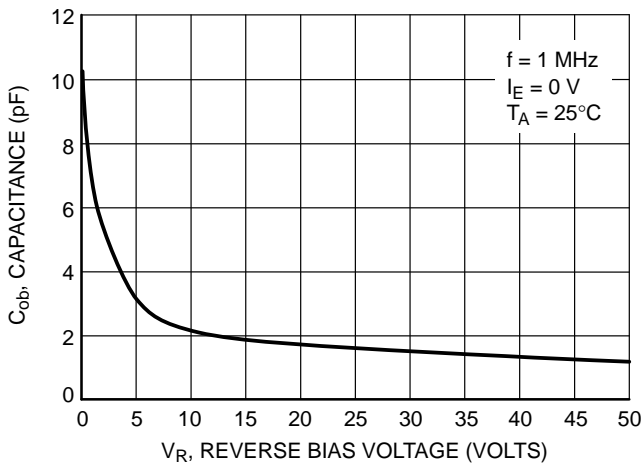


Figure 44. Output Capacitance

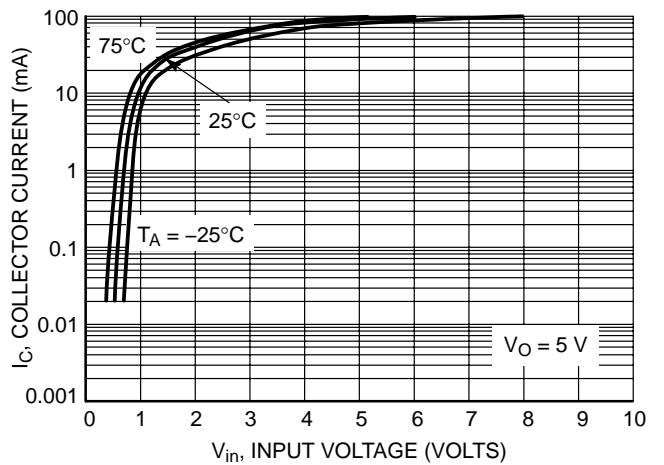


Figure 45. Output Current versus Input Voltage

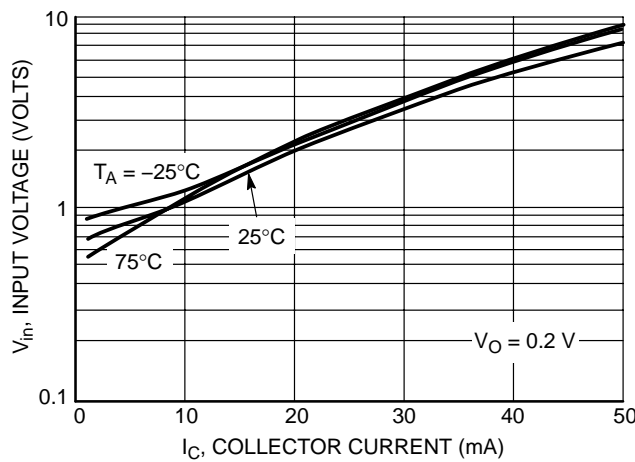


Figure 46. Input Voltage versus Output Current

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS — LMUN5315DW1T1G PNP TRANSISTOR

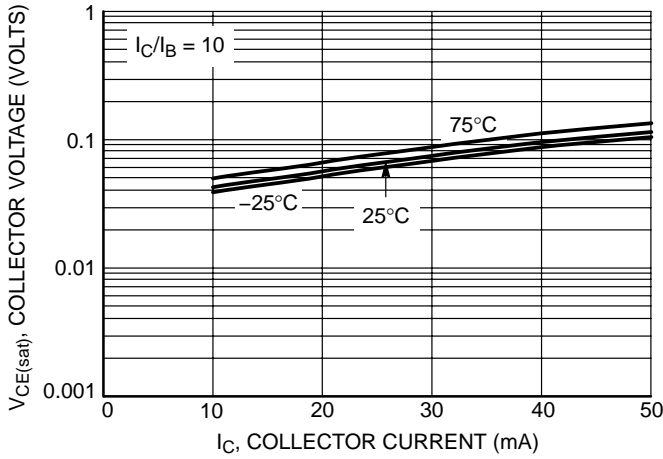


Figure 47. $V_{CE(sat)}$ versus I_C

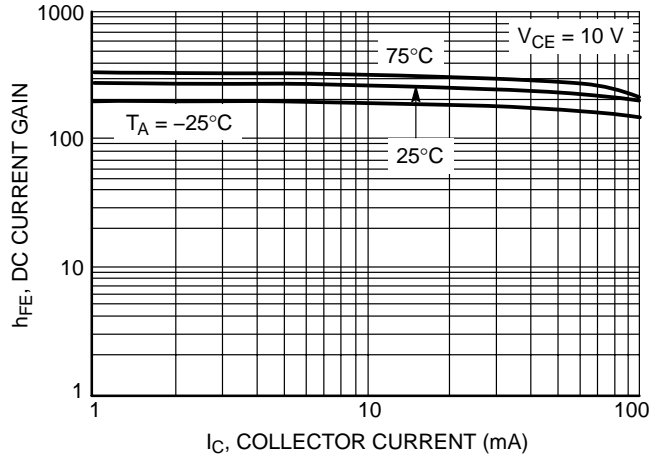


Figure 48. DC Current Gain

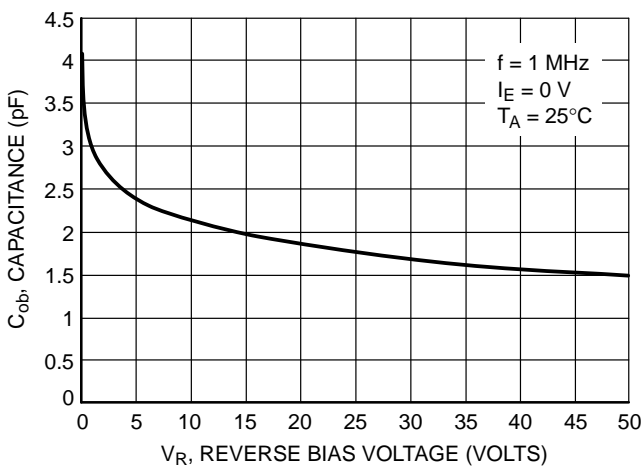


Figure 49. Output Capacitance

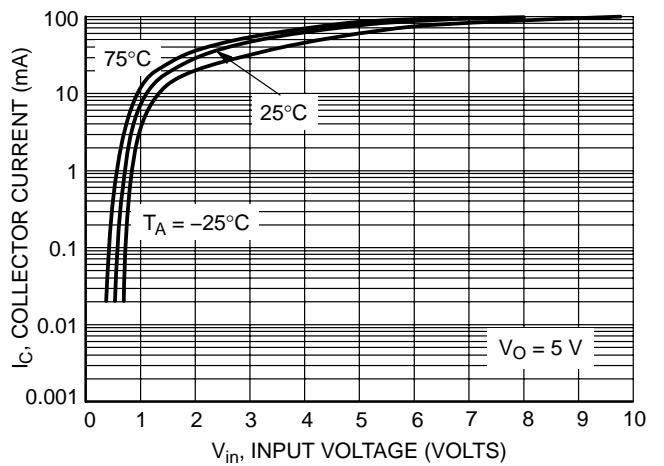


Figure 50. Output Current versus Input Voltage

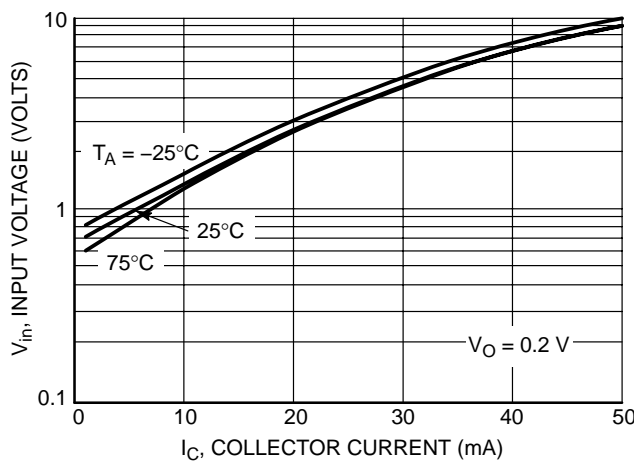


Figure 51. Input Voltage versus Output Current

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS — LMUN5316DW1T1G NPN TRANSISTOR

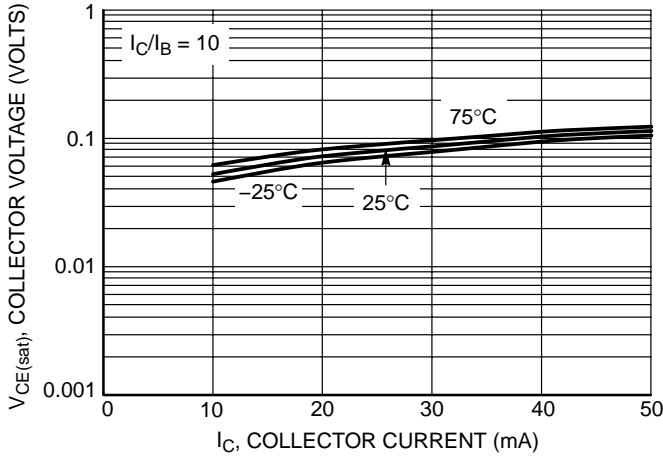


Figure 52. $V_{CE(sat)}$ versus I_C

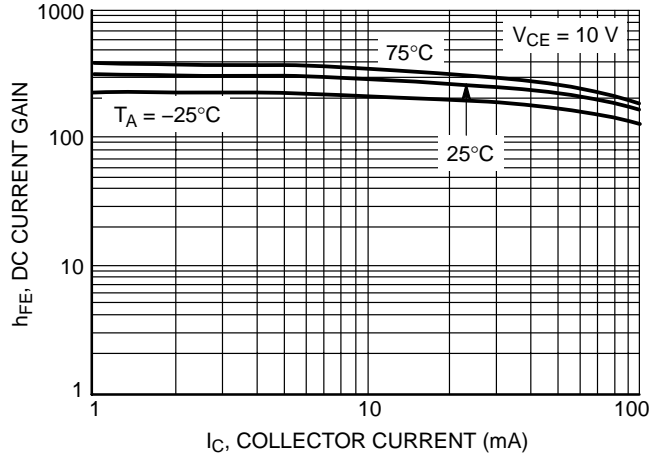


Figure 53. DC Current Gain

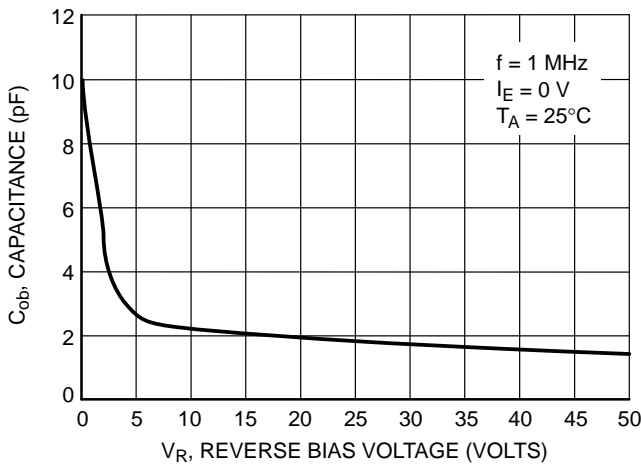


Figure 54. Output Capacitance

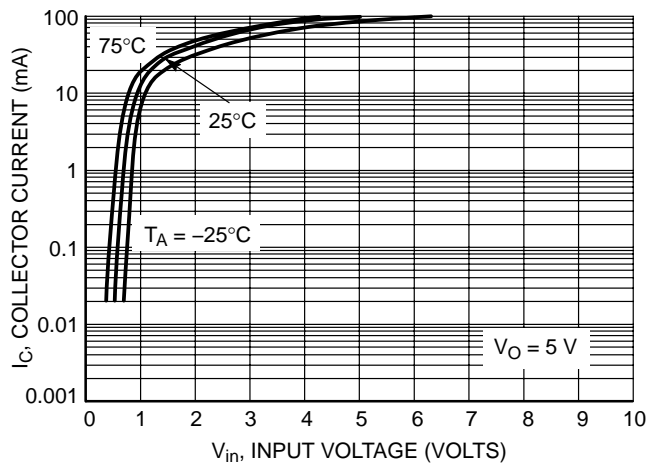


Figure 55. Output Current versus Input Voltage

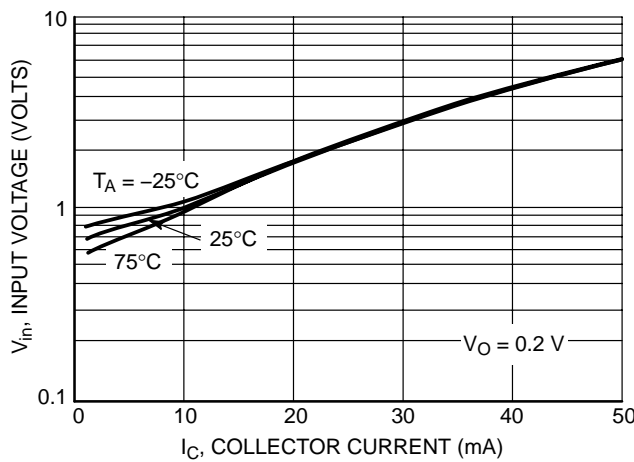


Figure 56. Input Voltage versus Output Current

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS — LMUN5316DW1T1G PNP TRANSISTOR

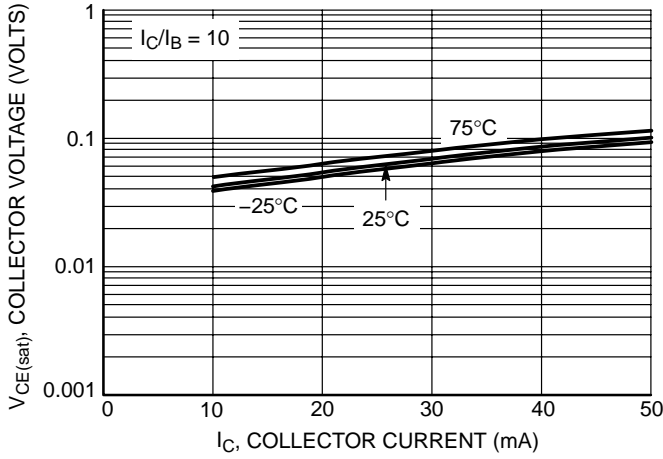


Figure 57. $V_{CE(sat)}$ versus I_C

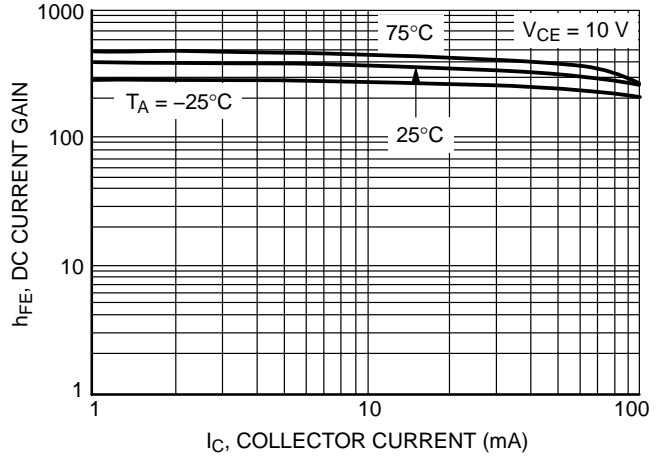


Figure 58. DC Current Gain

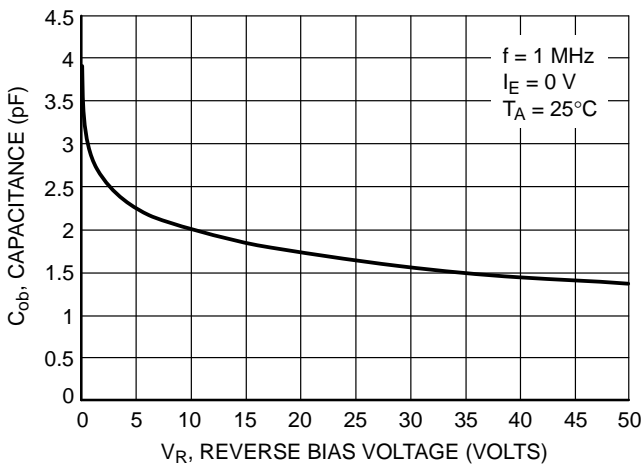


Figure 59. Output Capacitance

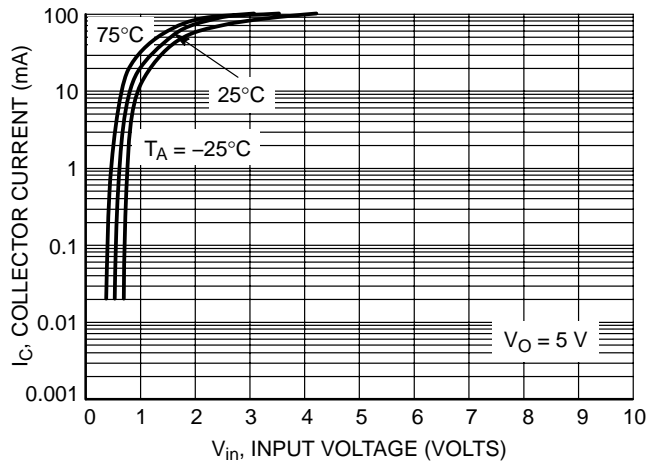


Figure 60. Output Current versus Input Voltage

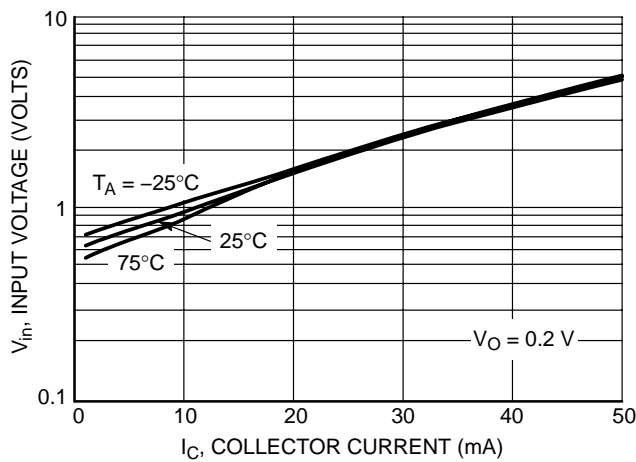


Figure 61. Input Voltage versus Output Current

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS — LMUN5330DW1T1G NPN TRANSISTOR

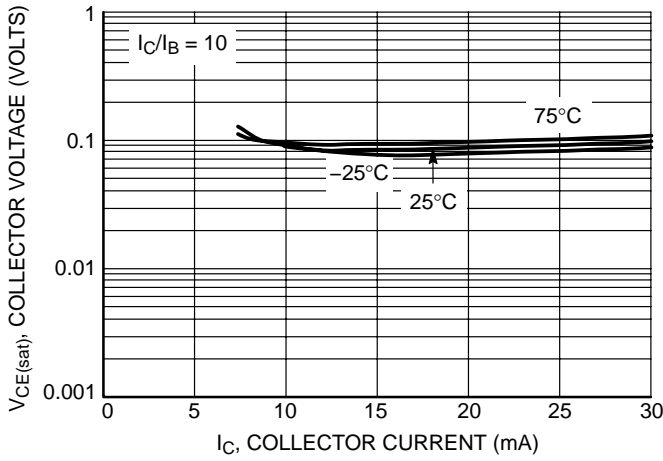


Figure 62. $V_{CE(sat)}$ versus I_C

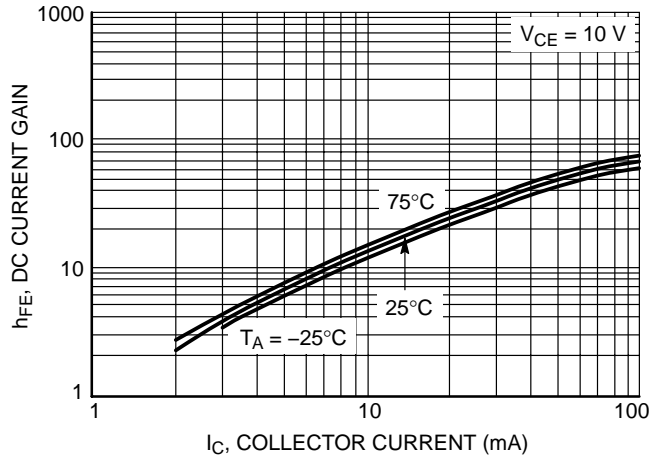


Figure 63. DC Current Gain

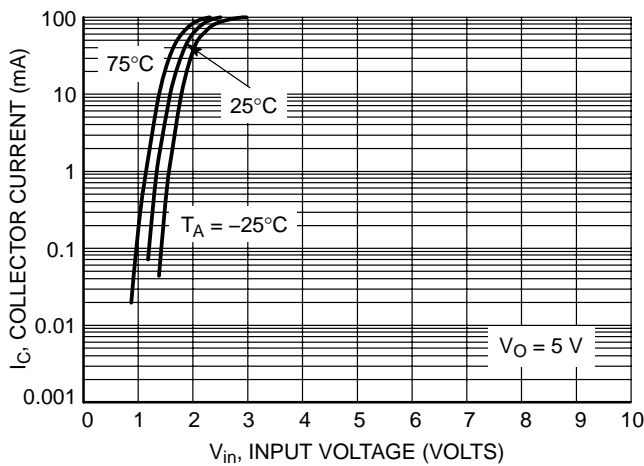


Figure 64. Output Current versus Input Voltage

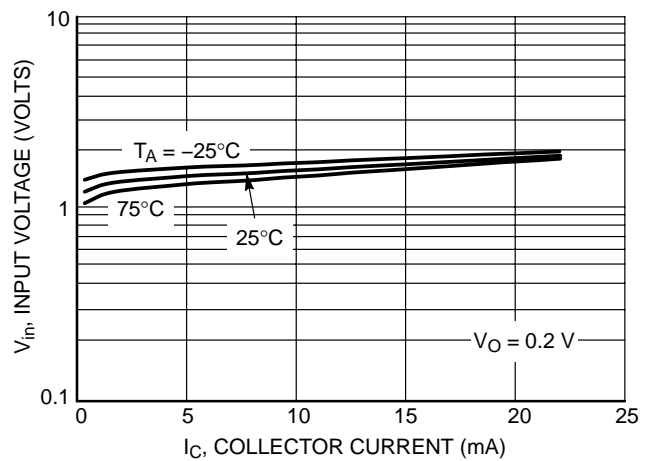


Figure 65. Input Voltage versus Output Current

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS — LMUN5330DW1T1G PNP TRANSISTOR

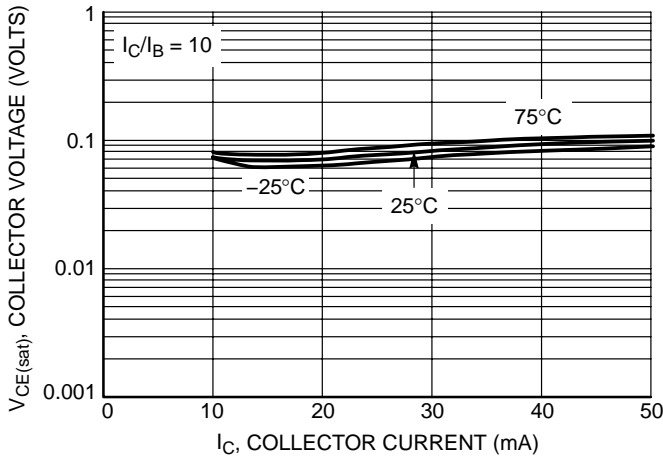


Figure 66. $V_{CE(sat)}$ versus I_C

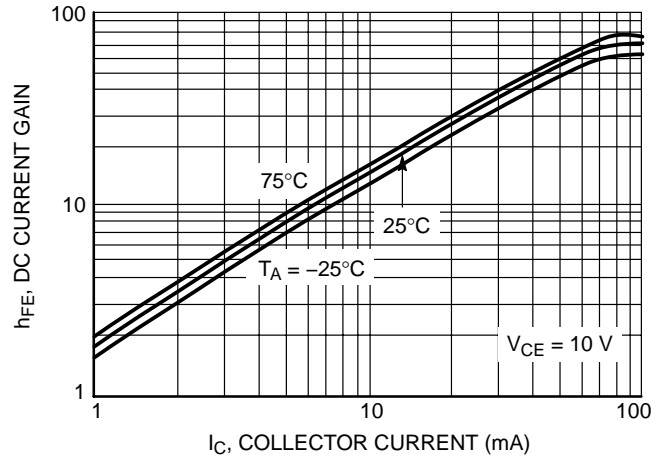


Figure 67. DC Current Gain

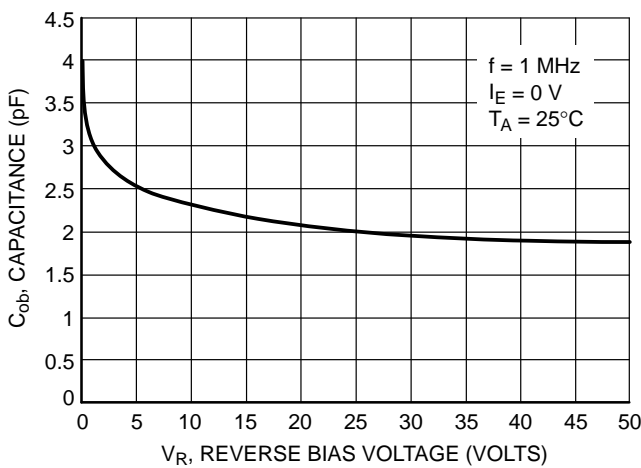


Figure 68. Output Capacitance

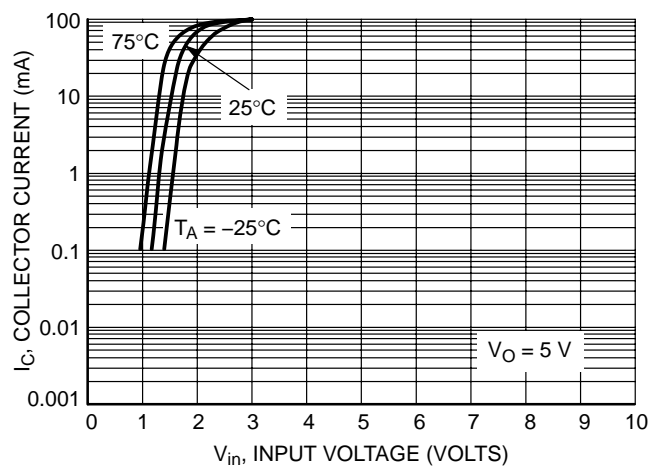


Figure 69. Output Current versus Input Voltage

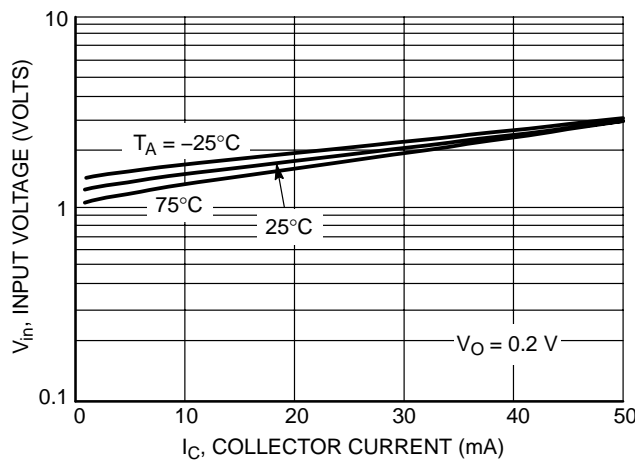


Figure 70. Input Voltage versus Output Current

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS — LMUN5311DW1T1G NPN TRANSISTOR

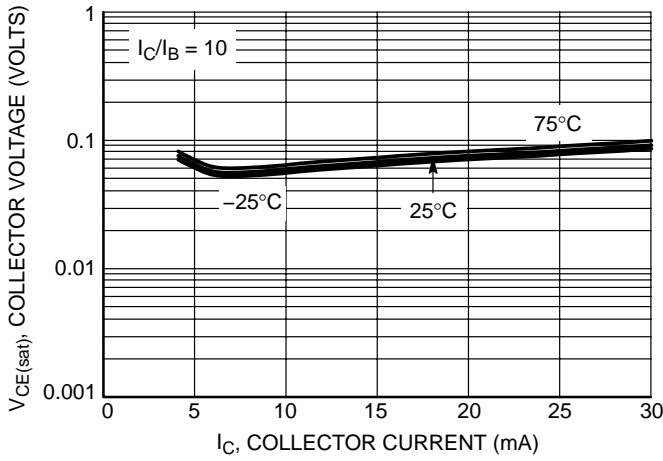


Figure 71. $V_{CE(sat)}$ versus I_C

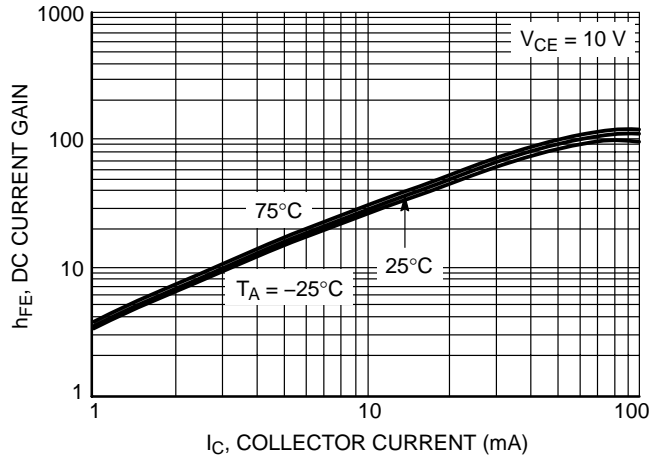


Figure 72. DC Current Gain

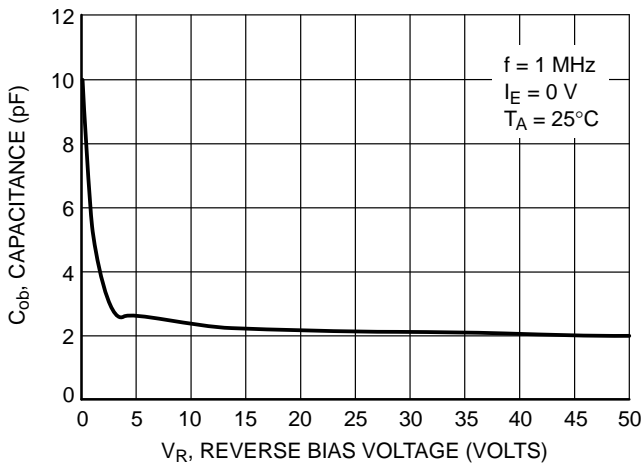


Figure 73. Output Capacitance

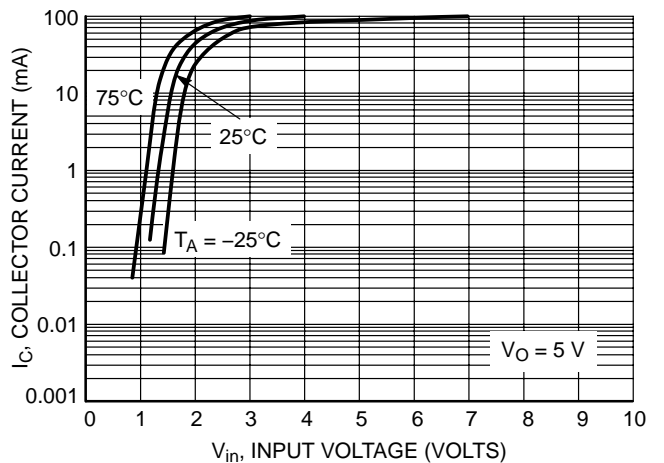


Figure 74. Output Current versus Input Voltage

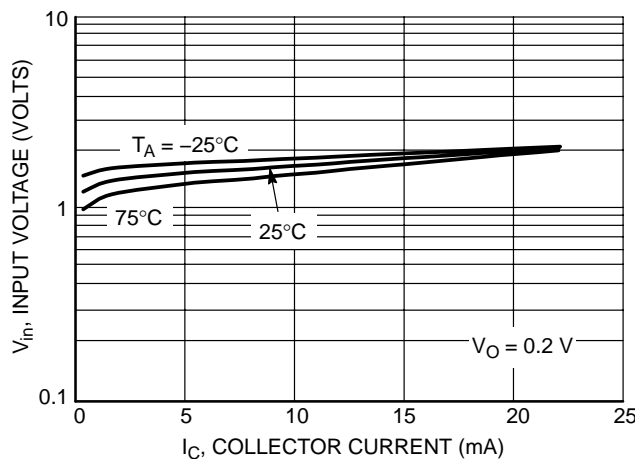


Figure 75. Input Voltage versus Output Current

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS — LMUN5331DW1T1G PNP TRANSISTOR

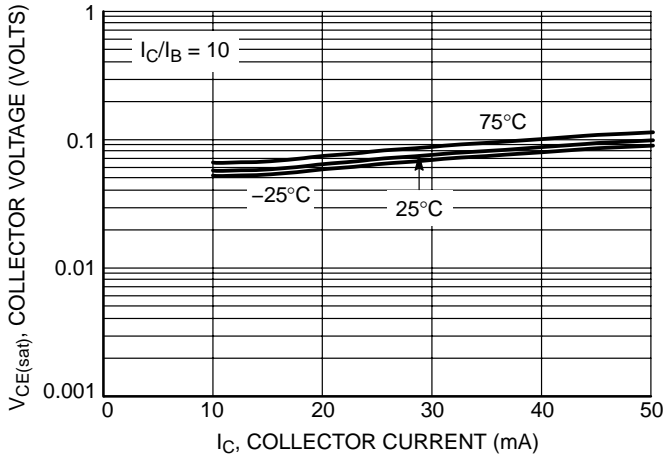


Figure 76. $V_{CE(sat)}$ versus I_C

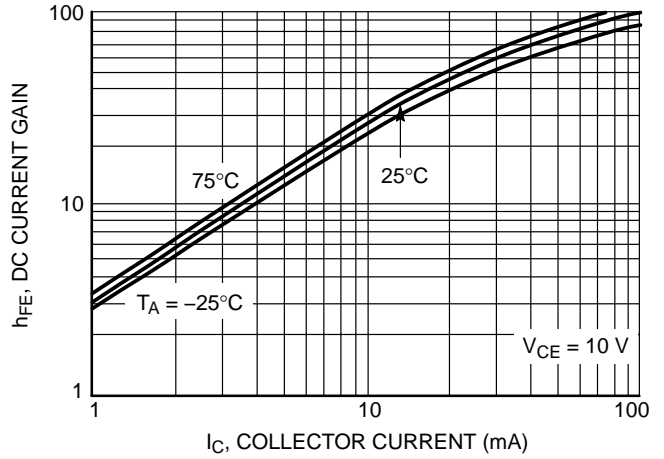


Figure 77. DC Current Gain

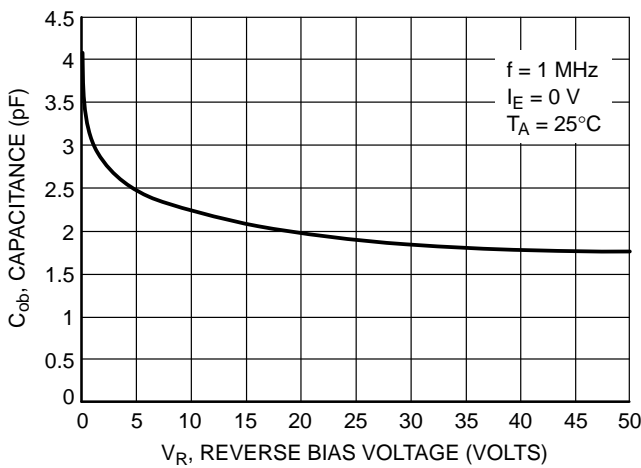


Figure 78. Output Capacitance

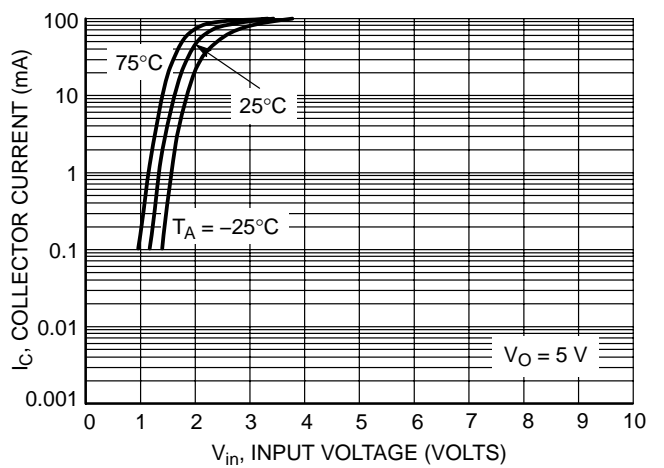


Figure 79. Output Current versus Input Voltage

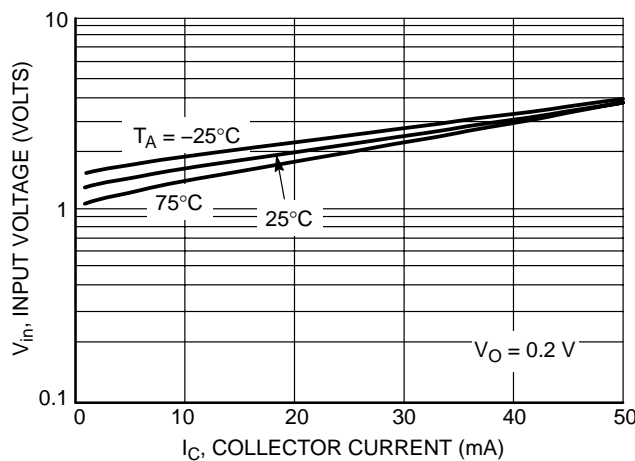


Figure 80. Input Voltage versus Output Current

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS — LMUN5332DW1T1G NPN TRANSISTOR

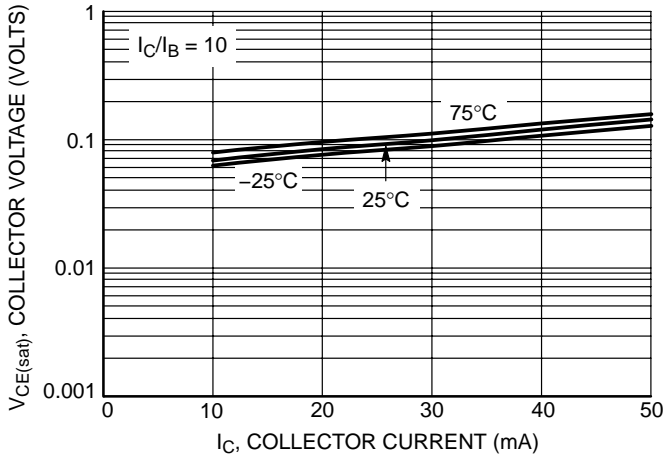


Figure 81. $V_{CE(sat)}$ versus I_C

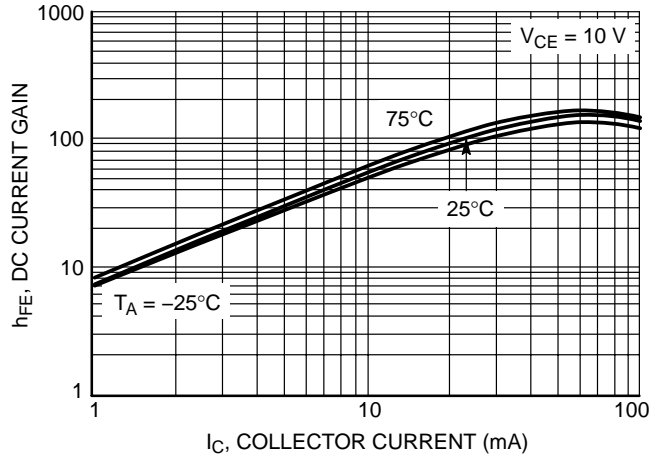


Figure 82. DC Current Gain

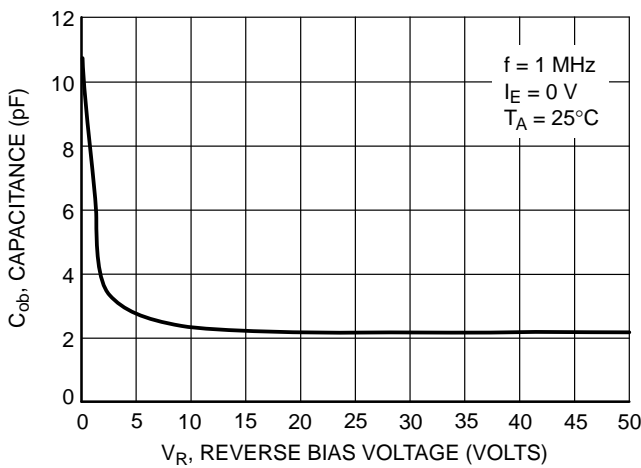


Figure 83. Output Capacitance

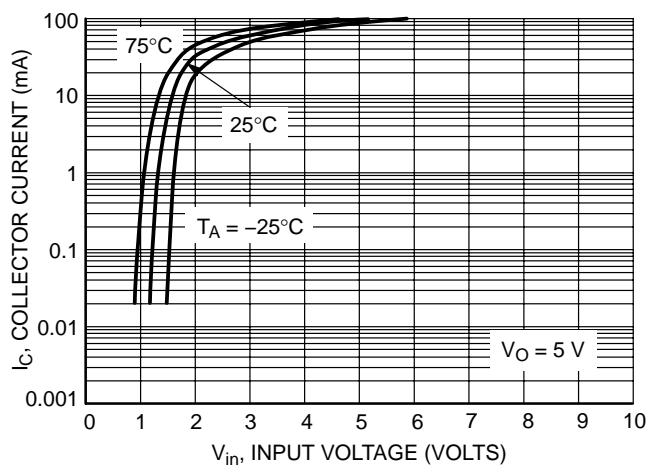


Figure 84. Output Current versus Input Voltage

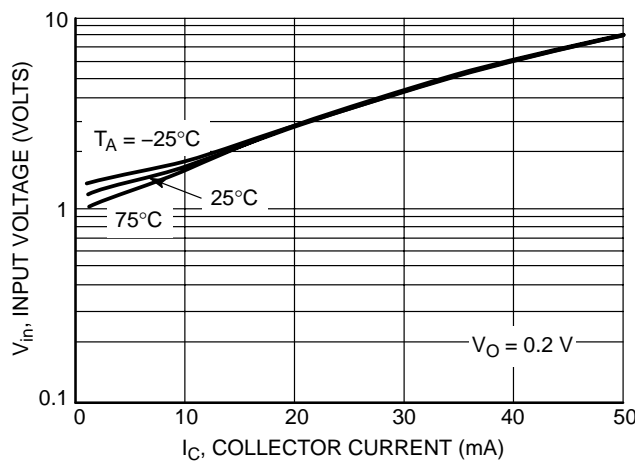


Figure 85. Input Voltage versus Output Current

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS — LMUN5332DW1T1G PNP TRANSISTOR

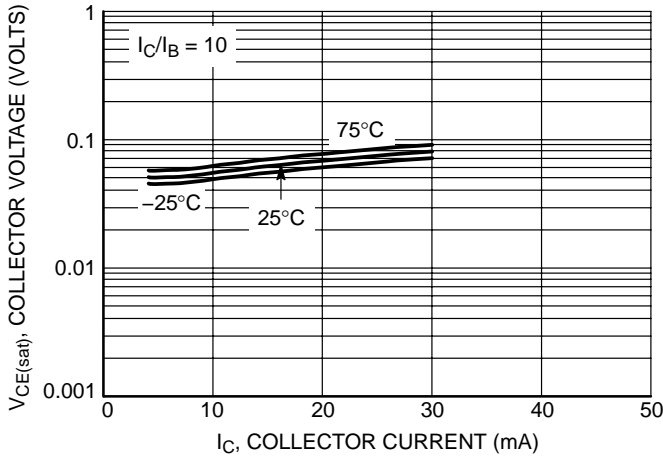


Figure 86. $V_{CE(sat)}$ versus I_C

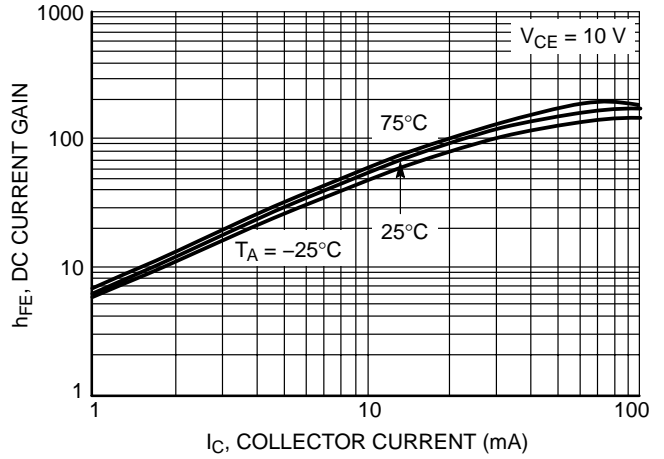


Figure 87. DC Current Gain

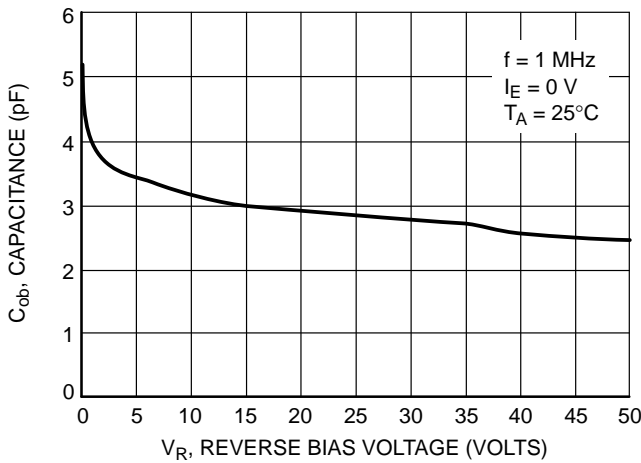


Figure 88. Output Capacitance

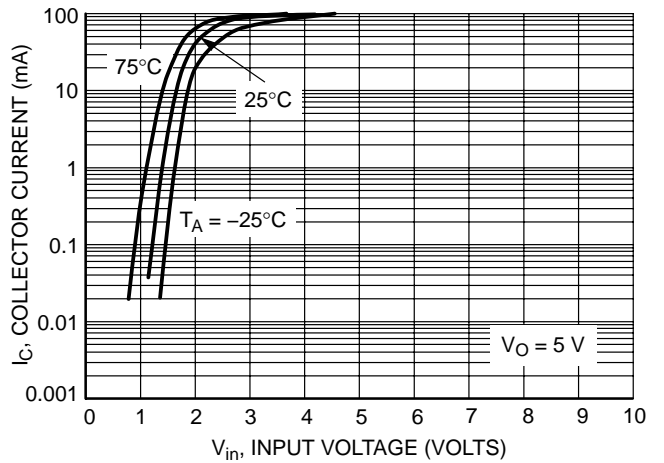


Figure 89. Output Current versus Input Voltage

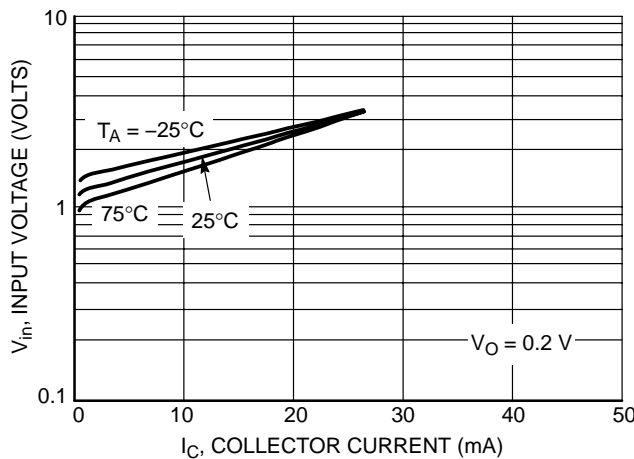


Figure 90. Input Voltage versus Output Current

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS — LMUN5333DW1T1G NPN TRANSISTOR

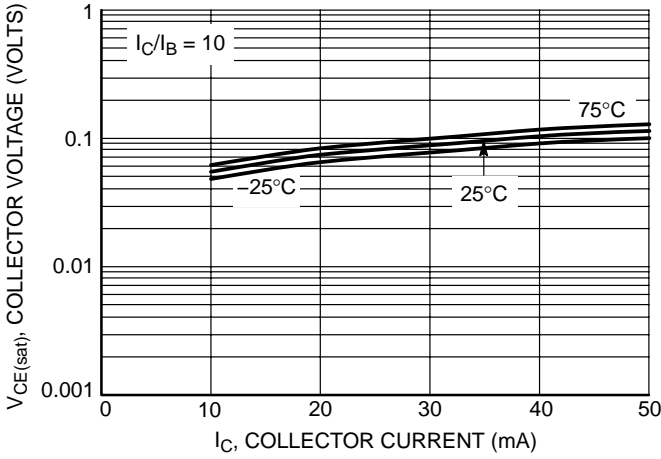


Figure 91. $V_{CE(sat)}$ versus I_C

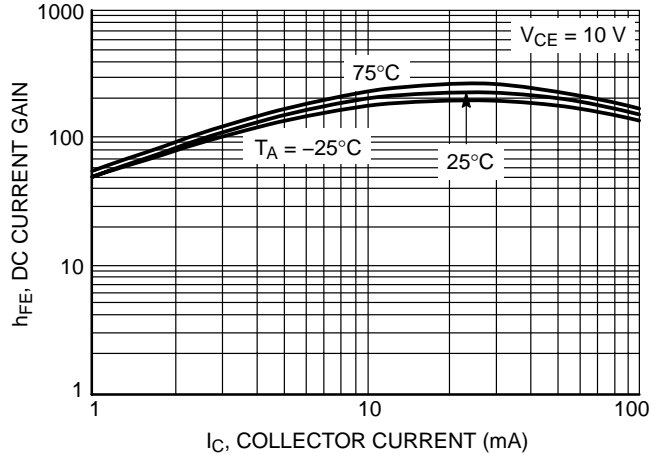


Figure 92. DC Current Gain

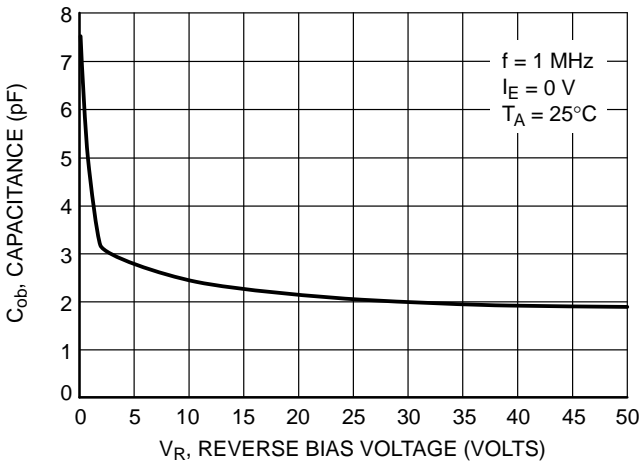


Figure 93. Output Capacitance

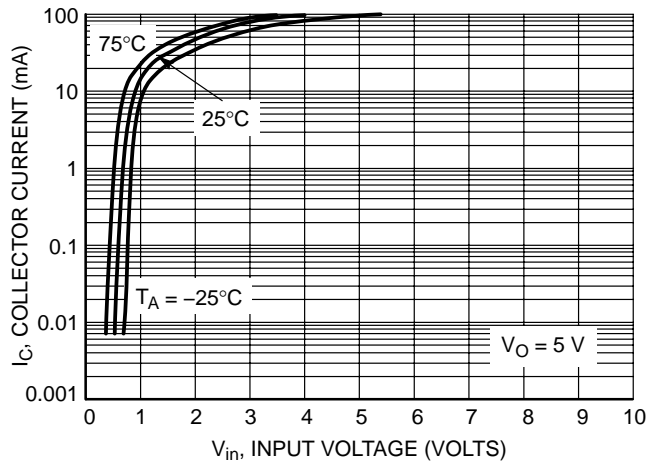


Figure 94. Output Current versus Input Voltage

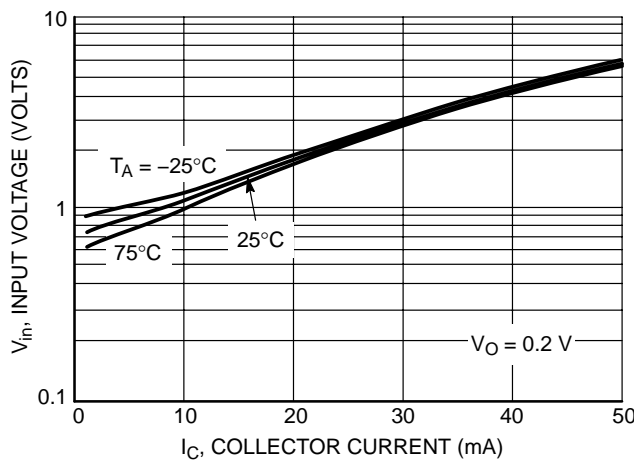


Figure 95. Input Voltage versus Output Current

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS — LMUN5333DW1T1G PNP TRANSISTOR

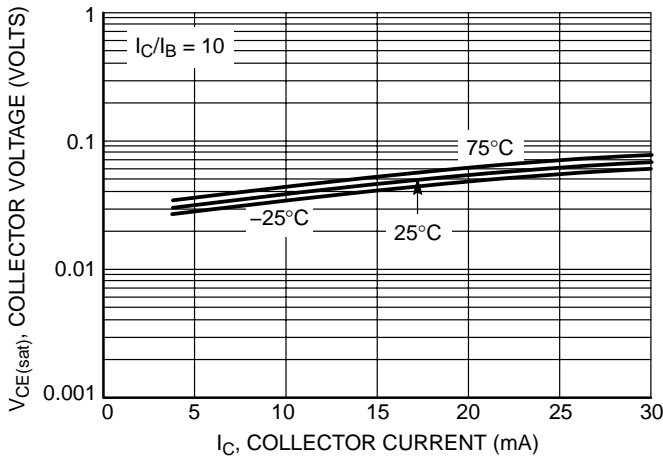


Figure 96. $V_{CE(sat)}$ versus I_C

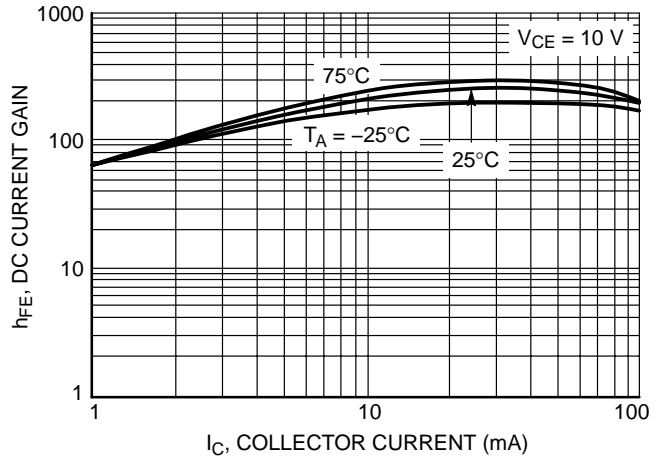


Figure 97. DC Current Gain

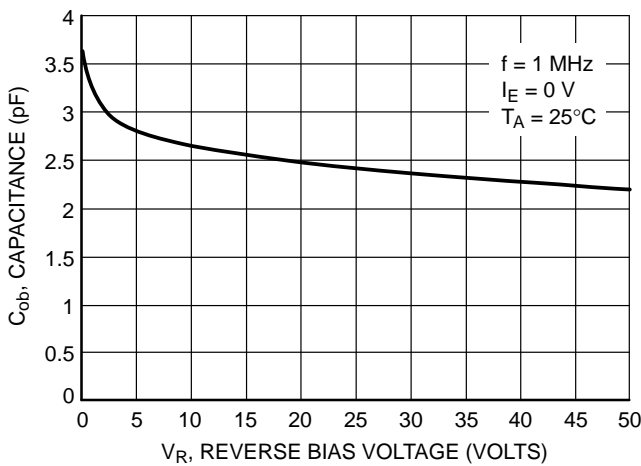


Figure 98. Output Capacitance

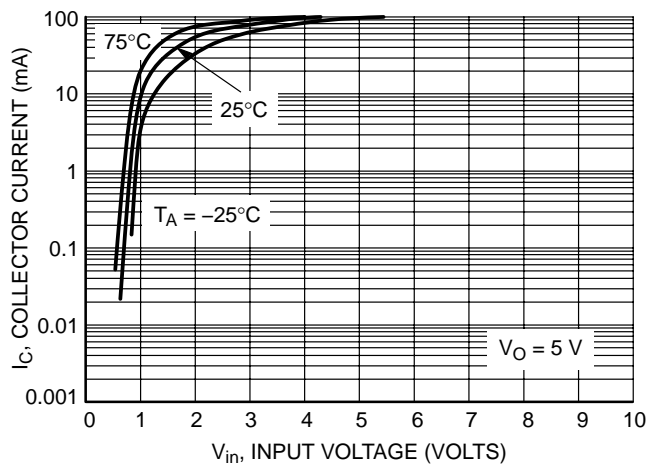


Figure 99. Output Current versus Input Voltage

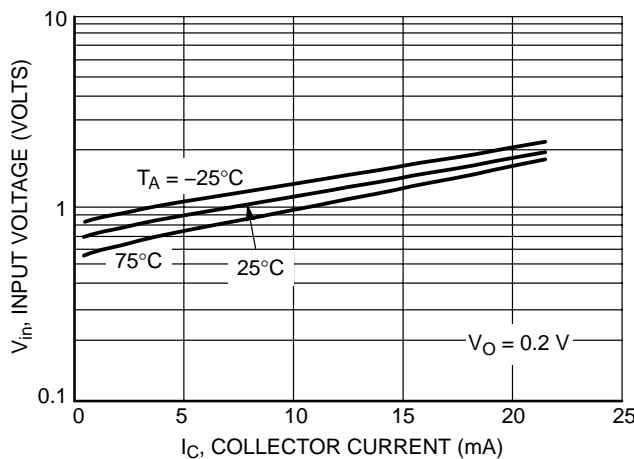


Figure 100. Input Voltage versus Output Current

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS — LMUN5334DW1T1G NPN TRANSISTOR

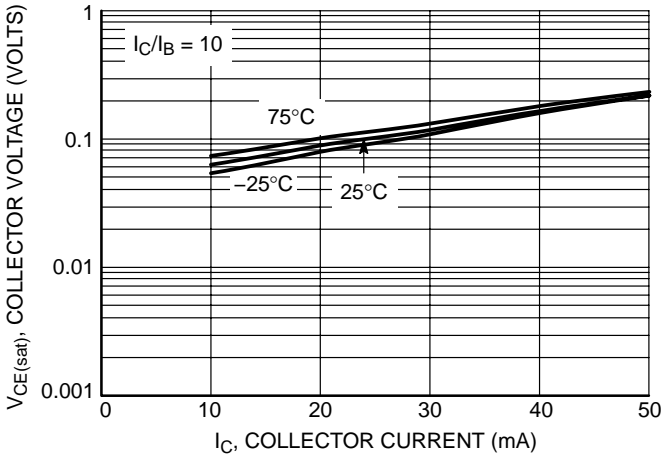


Figure 101. $V_{CE(sat)}$ versus I_C

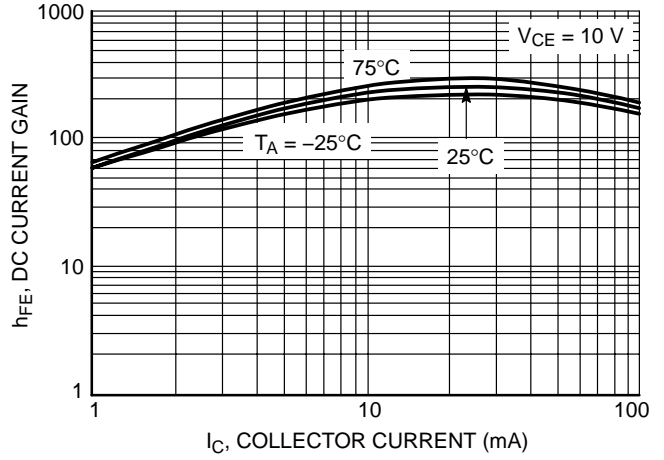


Figure 102. DC Current Gain

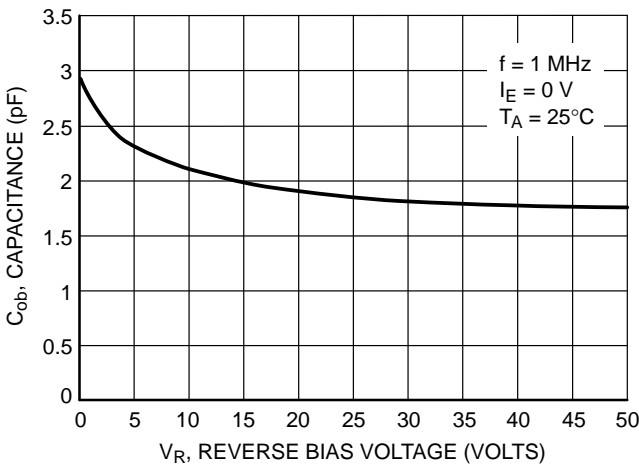


Figure 103. Output Capacitance

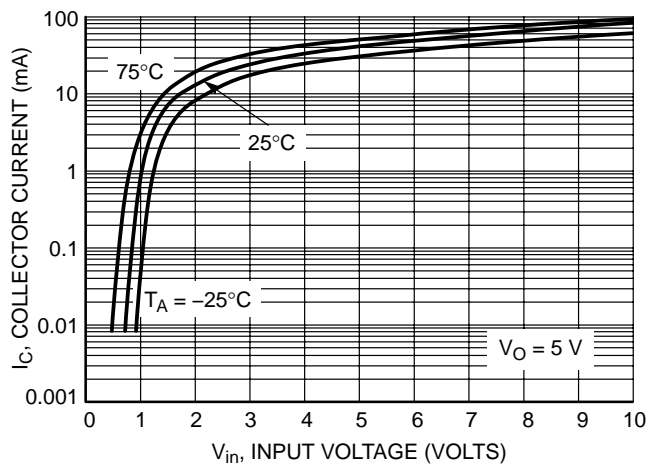


Figure 104. Output Current versus Input Voltage

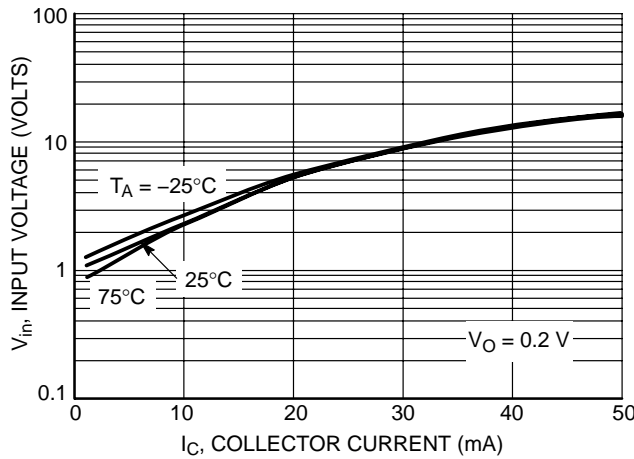
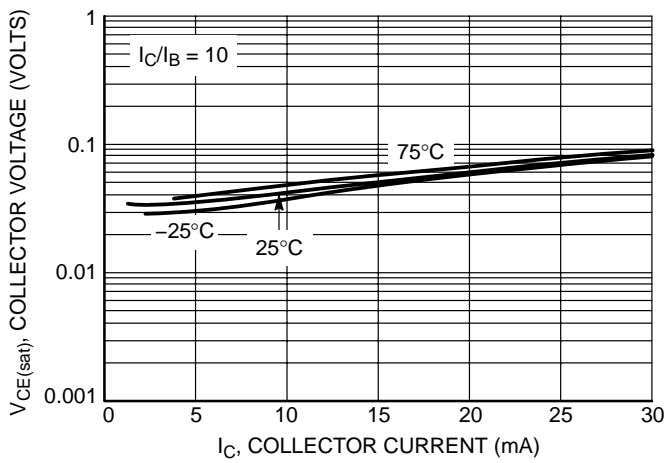
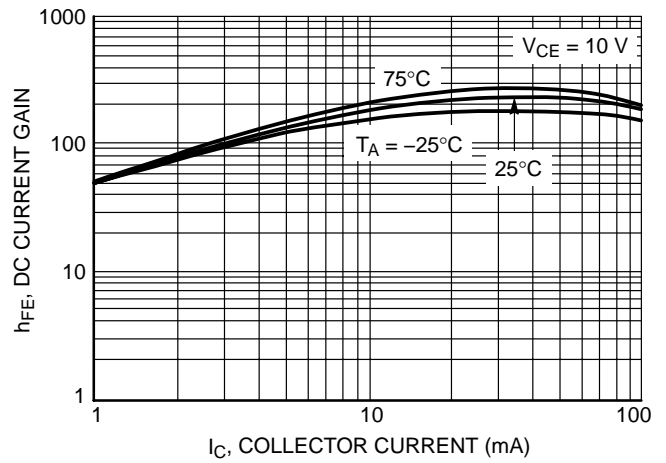


Figure 105. Input Voltage versus Output Current

LMUN5311DW1T1G Series
TYPICAL ELECTRICAL CHARACTERISTICS — LMUN5334DW1T1G PNP TRANSISTOR

Figure 106. $V_{CE(sat)}$ versus I_C

Figure 107. DC Current Gain

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS — LMUN5335DW1T1G NPN TRANSISTOR

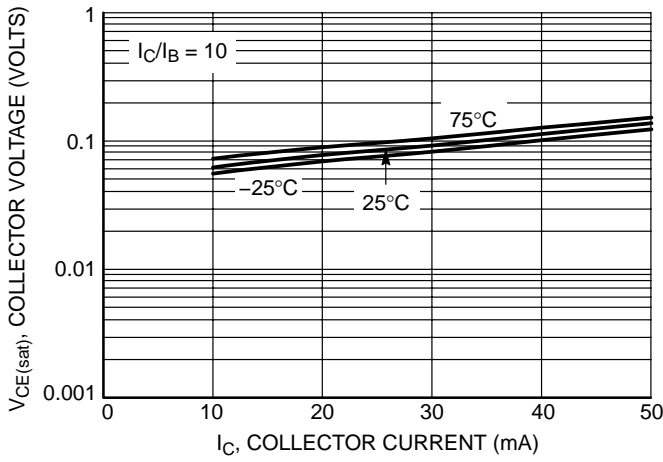


Figure 108. $V_{CE(sat)}$ versus I_C

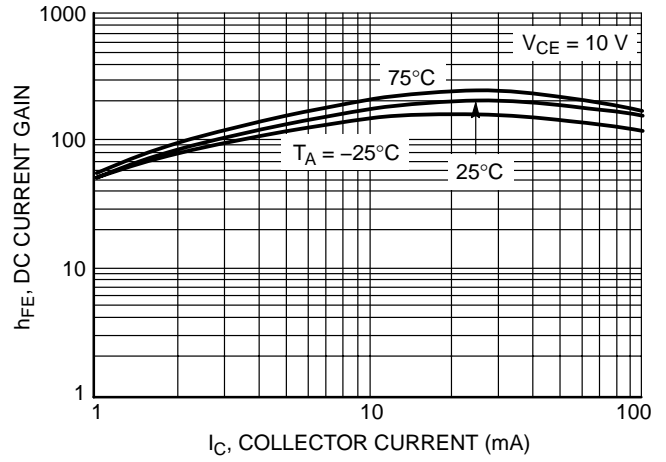


Figure 109. DC Current Gain

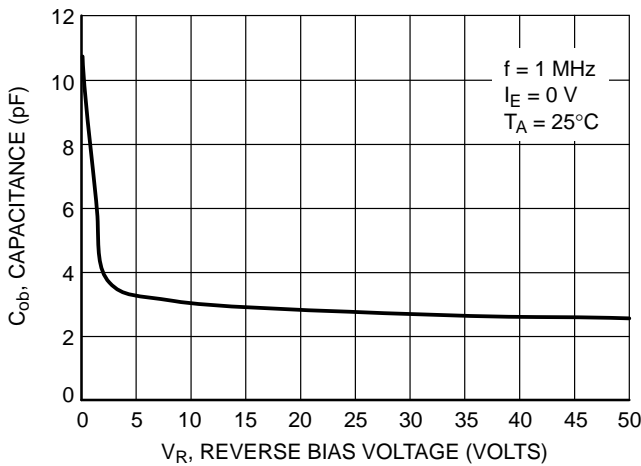


Figure 110. Output Capacitance

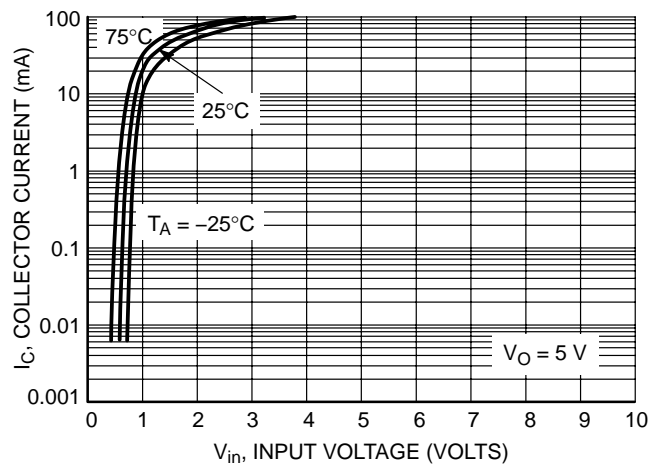


Figure 111. Output Current versus Input Voltage

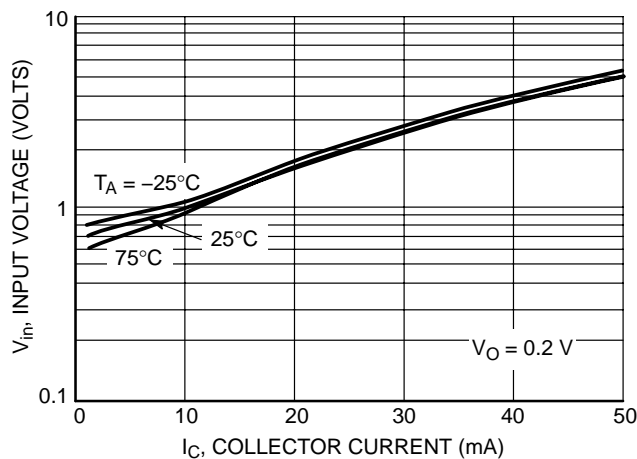


Figure 112. Input Voltage versus Output Current

LMUN5311DW1T1G Series

TYPICAL ELECTRICAL CHARACTERISTICS — LMUN5335DW1T1G PNP TRANSISTOR

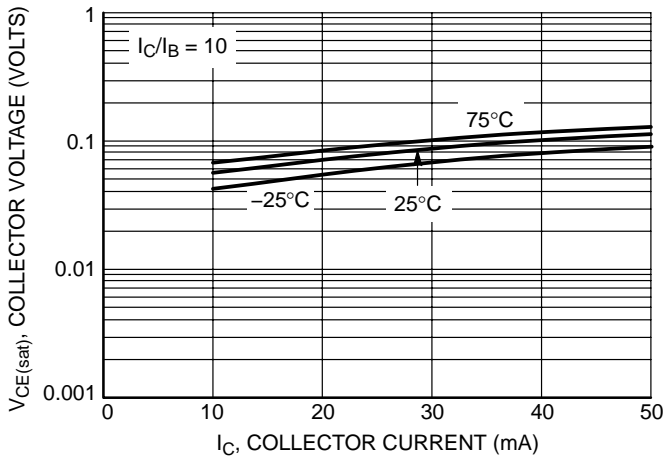


Figure 113. $V_{CE(sat)}$ versus I_C

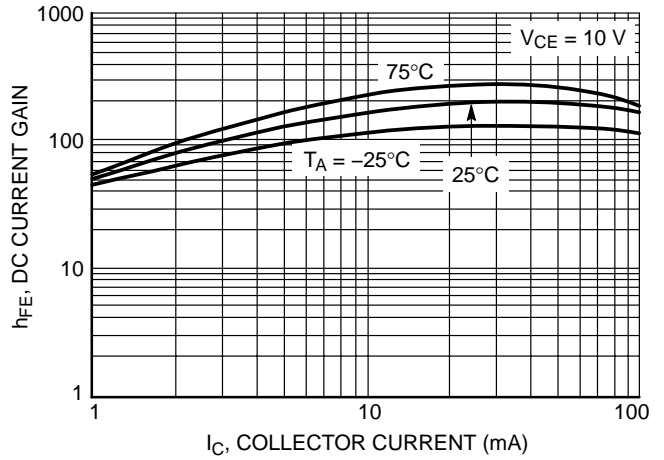


Figure 114. DC Current Gain

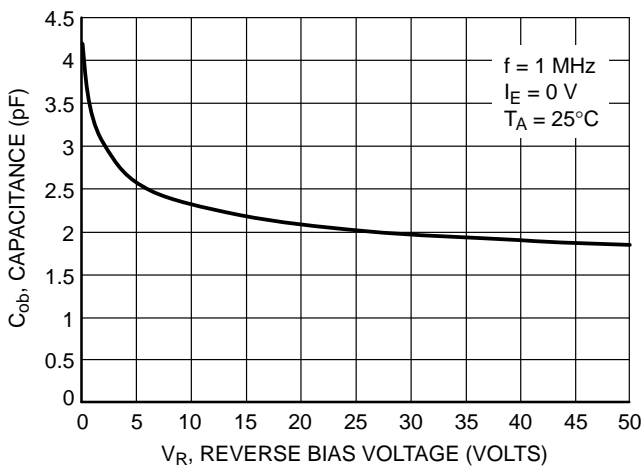


Figure 115. Output Capacitance

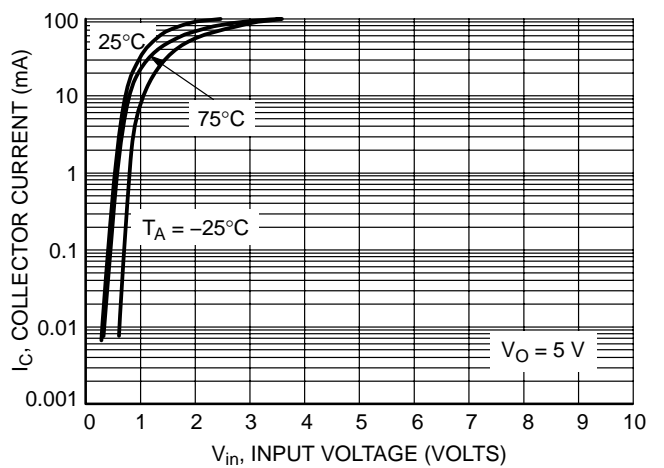


Figure 116. Output Current versus Input Voltage

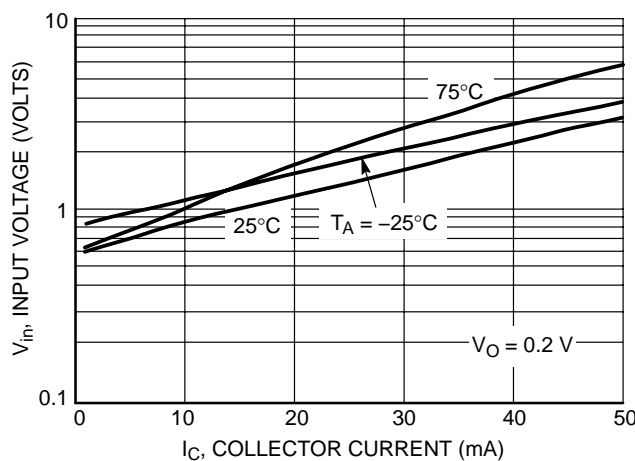
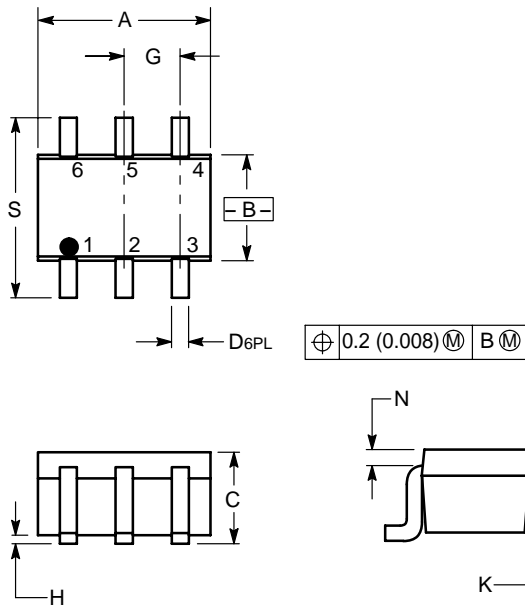


Figure 117. Input Voltage versus Output Current

LMUN5311DW1T1G SERIES

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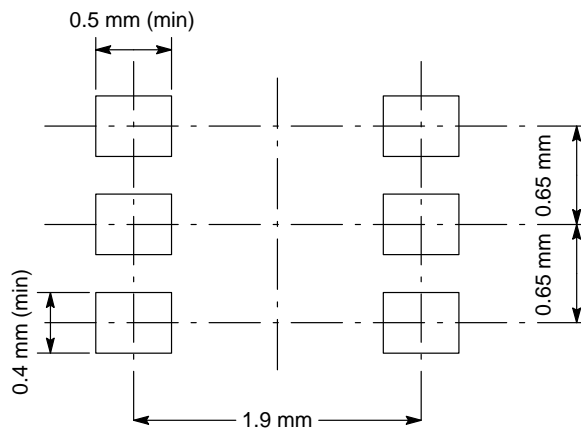


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

- PIN 1. EMITTER 2
- 2. BASE 2
- 3. COLLECTOR 1
- 4. EMITTER 1
- 5. BASE 1
- 6. COLLECTOR 2



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