20V N-Channel Enhancement-Mode MOSFET

V_{DS}= 20V

$R_{DS(ON)}$, Vgs@4.5V, Ids@5.0A = 41m

$R_{DS(ON)}$, Vgs@2.5V, Ids@4.5A = 47m

Features

Advanced trench process technology

High Density Cell Design For Ultra Low On-Resistance

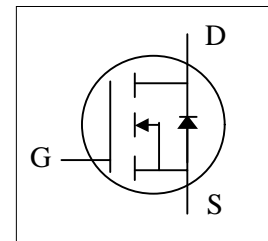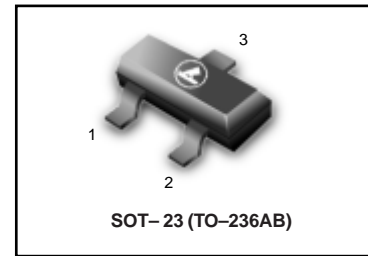we declare that the material of product

compliance with RoHS reqirements.

S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

▼ **Capable of 2.5V gate drive**

▼ **Lower on-resistance**

▼ **Surface mount package**

| LN2312LT1G |
| S-LN2312LT1G |

SOT– 23 (TO–236AB)

Ordering Information

Device	Marking	Shipping
LN2312LT1G S-LN2312LT1G	N12	3000/Tape&Reel
LN2312LT3G S-LN2312LT3G	N12	10000/Tape&Reel

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	±8	V
I_D@T_A=25℃	Continuous Drain Current[3], V_{GS} @ 4.5V	4.9	A
I_D@T_A=70℃	Continuous Drain Current[3], V_{GS} @ 4.5V	3.4	A
I_{DM}	Pulsed Drain Current[1,2]	15	A
P_D@T_A=25℃	Total Power Dissipation	0.75	W
	Linear Derating Factor	1.3	W/℃
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter		Value	Unit
Rthj-a	Thermal Resistance Junction-ambient[3]	Max.	140	℃/W

LN2312LT1G , S-LN2312LT1G

Electrical Characteristics@T$_j$=25°C(unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV$_{DSS}$	V$_{GS}$ = 0V, I$_D$ = 250uA	20	-	-	V
Drain-Source On-State Resistance	R$_{DS(on)}$	V$_{GS}$ = 1.8V, I$_D$ = 4.0A		31	57	mΩ
Drain-Source On-State Resistance	R$_{DS(on)}$	V$_{GS}$ = 2.5V, I$_D$ = 4.5A		24	47	
Drain-Source On-State Resistance	R$_{DS(on)}$	V$_{GS}$ = 4.5V, I$_D$ = 5A		21	41	
Gate Threshold Voltage	V$_{GS(th)}$	V$_{DS}$ =V$_{GS}$, I$_D$ = 250uA	0.4	0.6	1	V
Zero Gate Voltage Drain Current	I$_{DSS}$	V$_{DS}$ = 20V, V$_{GS}$ = 0V			1	uA
Gate Body Leakage	I$_{GSS}$	V$_{GS}$ = ±8V, V$_{DS}$ = 0V			± 100	nA
Gate Resistance	Rg					
Forward Transconductance	g$_{fs}$	V$_{DS}$ = 10V, I$_D$ = 5A		40		S
Dynamic						
Total Gate Charge	Q$_g$	V$_{DS}$ = 10V, I$_D$ = 5A V$_{GS}$ = 4.5V		11.2		nC
Gate-Source Charge	Q$_{gs}$			1.4		
Gate-Drain Charge	Q$_{gd}$			2.2		
Turn-On Delay Time	t$_{d(on)}$	V$_{DD}$ = 10V, I$_D$ = 1A, V$_{GEN}$ = 4.5V R$_G$ = 6Ω		15	25	ns
Turn-On Rise Time	t$_r$			40	60	
Turn-Off Delay Time	t$_{d(off)}$			48	70	
Turn-Off Fall Time	t$_f$			31	45	
Input Capacitance	C$_{iss}$	V$_{DS}$ = 8V, V$_{GS}$ = 0V f = 1.0 MHz		500		pF
Output Capacitance	C$_{oss}$			300		
Reverse Transfer Capacitance	C$_{rss}$			140		
Source-Drain Diode						
Max. Diode Forward Current	I$_S$				1.7	A
Diode Forward Voltage	V$_{SD}$	I$_S$ = 1.7A, V$_{GS}$ = 0V			1.2	V

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse width ≤300us , duty cycle ≤2%.

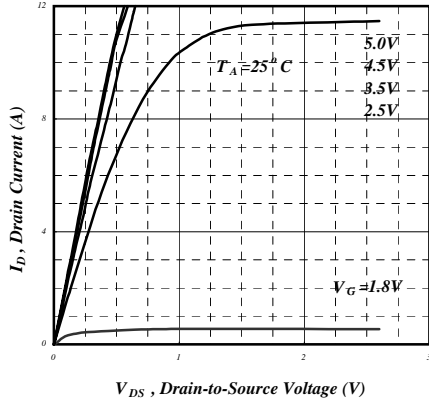3.Surface mounted on 1 in^2 copper PCB board

Fig 1. Typical Output Characteristics
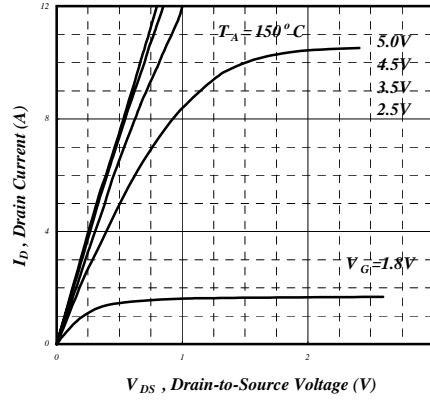

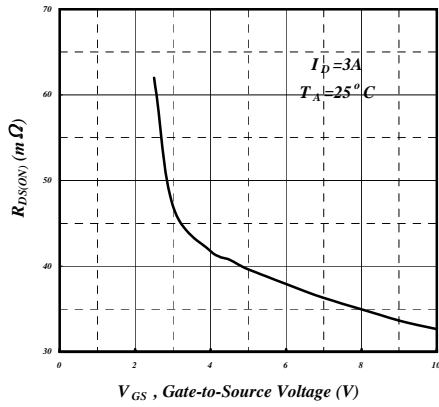**Fig 2. Typical Output Characteristics**

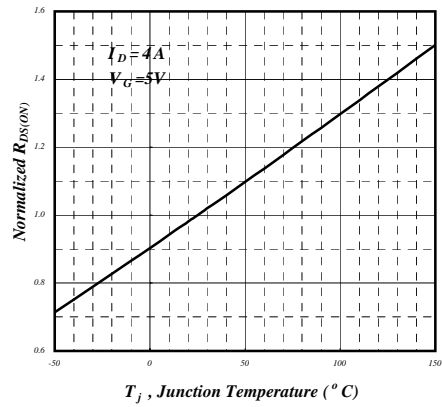**Fig 3. On-Resistance v.s. Gate Voltage**

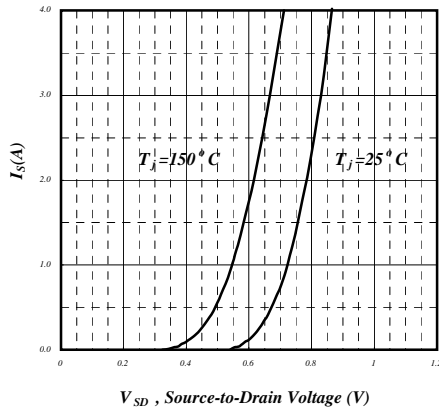**Fig 4. Normalized On-Resistance
v.s. Junction Temperature**

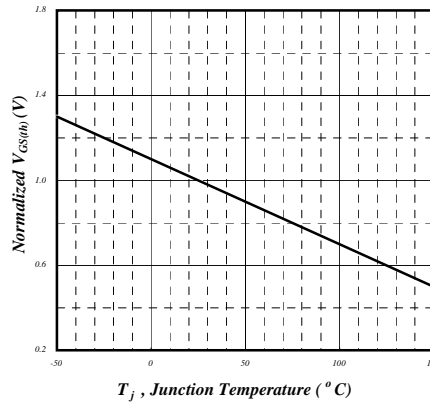
**Fig 5. Forward Characteristic of
Reverse Diode**

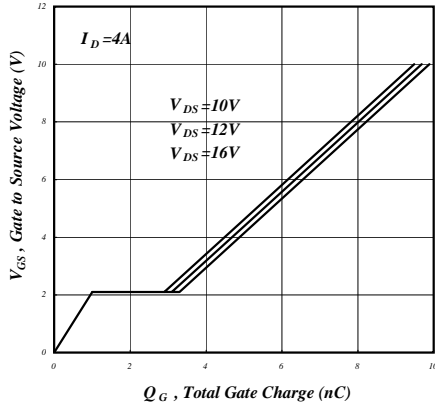**Fig 6. Gate Threshold Voltage v.s.
Junction Temperature**

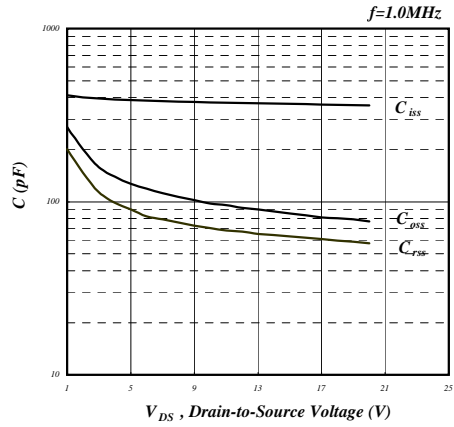Fig 7. Gate Charge Characteristics
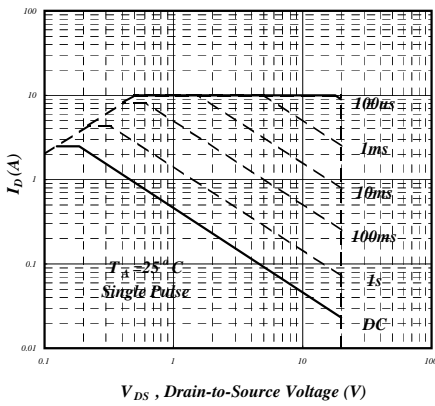

Fig 8. Typical Capacitance Characteristics
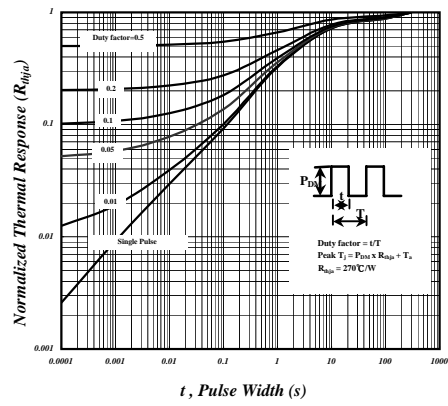

Fig 9. Maximum Safe Operating Area
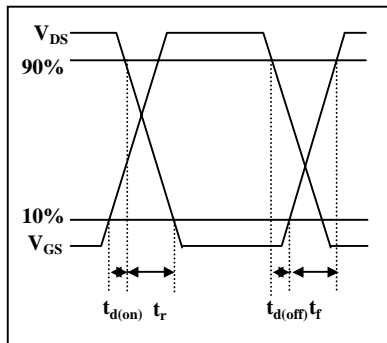

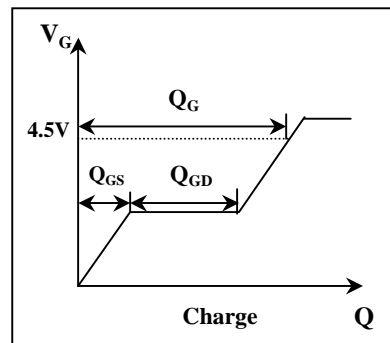Fig 10. Effective Transient Thermal Impedance
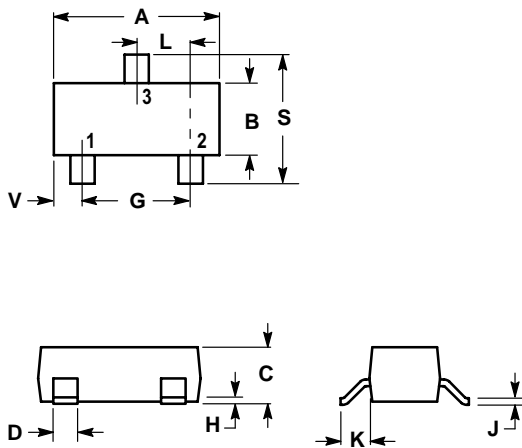

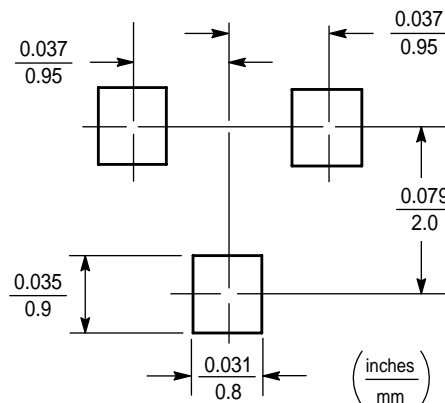
Fig 11. Switching Time Circuit

Fig 12. Gate Charge Circuit

SOT−23

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI
   Y14.5M,1982
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

$$\frac{0.037}{0.95} \quad \frac{0.037}{0.95}$$

$$\frac{0.079}{2.0}$$

$$\frac{0.035}{0.9}$$

$$\frac{0.031}{0.8} \quad \left(\frac{inches}{mm}\right)$$

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