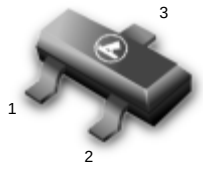
# 20V P-Channel Enhancement-Mode MOSFET

**$V_{DS}$= -20V**

**$R_{DS(ON)}$, Vgs@-4.5V, Ids@-2.8A = 100 mΩ**

**$R_{DS(ON)}$, Vgs@-2.5V, Ids@-2.0A = 150 mΩ**

LP4101LT1G
S-LP4101LT1G




SOT– 23 (TO–236AB)

## Features

**Advanced trench process technology**

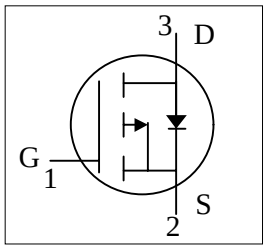
**High Density Cell Design For Ultra Low On-Resistance**

**Fully Characterized Avalanche Voltage and Current**

**Improved Shoot-Through FOM**

**we declare that the material of product compliance with RoHS reuirements.**

**S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.**




**▼ Simple Drive Requirement**

**▼ Small Package Outline**

**▼ Surface Mount Device**

### Ordering Information

| Device | Marking | Shipping |
|---|---|---|
| LP4101LT1G<br>S-LP4101LT1G | P41 | 3000/Tape & Reel |
| LP4101LT3G<br>S-LP4101LT3G | P41 | 10,000/Tape & Reel |

### Maximum Ratings and Thermal Characteristics ($T_A$ = 25°C unless otherwise noted)

| Parameter | | Symbol | Limit | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | -20 | V |
| Gate-Source Voltage | | $V_{GS}$ | ± 8 | |
| Continuous Drain Current | | $I_D$ | -2.3 | A |
| Pulsed Drain Current 1) | | $I_{DM}$ | -8 | |
| Maximum Power Dissipation | TA = 25°C | $P_D$ | 0.9 | W |
| | TA = 75°C | | 0.57 | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | -55 to 150 | °C |
| Junction-to-Case Thermal Resistance | | $R_{qJC}$ | | °C/W |
| Junction-to-Ambient Thermal Resistance (PCB mounted) 2) | | $R_{qJA}$ | 140 | |

Note: 1. Repetitive Rating: Pulse width limited by the Maximum junction temperation

2. 1-in$^2$ 2oz Cu PCB board

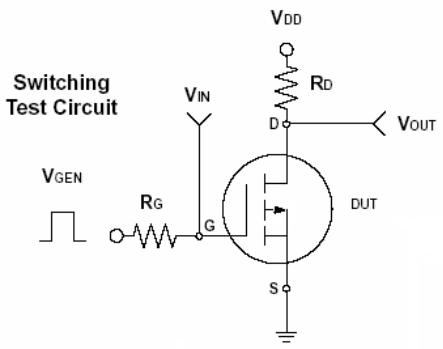
3. Guaranteed by design; not subject to production testing

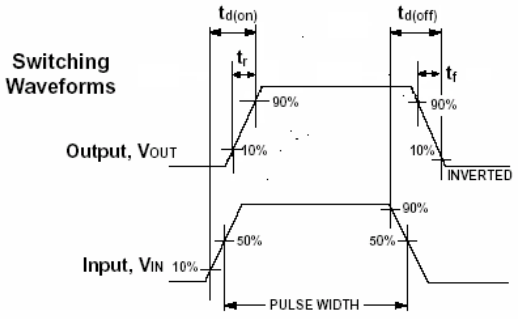
# LP4101LT1G , S-LP4101LT1G

## ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$ = 0V, $I_D$ = -250uA | -20 | - | - | V |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = -4.5V, $I_D$ = -2.8A | | 69 | 100 | mΩ |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = -2.5V, $I_D$ = -2.0A | | 83 | 150 | mΩ |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ =$V_{GS}$, $I_D$ = -250uA | -0.45 | | -0.95 | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = -9.6V, $V_{GS}$ = 0V | | | -1 | uA |
| Gate Body Leakage | $I_{GSS}$ | $V_{GS}$ = ±8V, $V_{DS}$ = 0V | | | ±100 | nA |
| Gate Resistance | Rg | | | | | Ω |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = -5V, $I_D$ = -4.0A | | 6.5 | | S |
| **Dynamic** [3)] | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = -6V, $I_D$ = -2.8A<br>$V_{GS}$ = -4.5V | | 15.23 | | nC |
| Gate-Source Charge | $Q_{gs}$ | | | 5.49 | | |
| Gate-Drain Charge | $Q_{gd}$ | | | 2.74 | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = -6V, $R_L$ = 6Ω<br>$I_D$ = −1A, $V_{GEN}$ = -4.5V<br>$R_G$ = 6Ω | | 17.28 | | ns |
| Turn-On Rise Time | $t_r$ | | | 3.73 | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 36.05 | | |
| Turn-Off Fall Time | $t_f$ | | | 6.19 | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = -6V, $V_{GS}$ = 0V<br>f = 1.0 MHz | | 882.51 | | pF |
| Output Capacitance | $C_{oss}$ | | | 145.54 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 97.26 | | |
| **Source-Drain Diode** | | | | | | |
| Max. Diode Forward Current | $I_S$ | | | | -2.4 | A |
| Diode Forward Voltage | $V_{SD}$ | $I_S$ = -0.75A, $V_{GS}$ = 0V | | -0.8 | -1.2 | V |

**Note**: Pulse test: pulse width <= 300us, duty cycle<= 2%



LP4101LT1G , S-LP4101LT1G

## TYPICAL ELECTRICAL CHARACTERISTICS

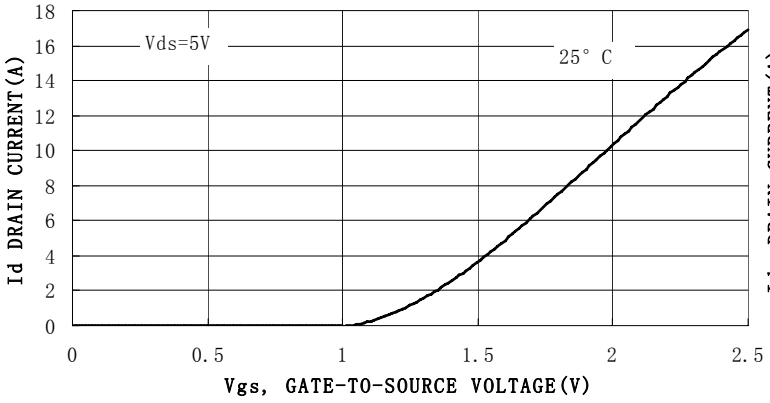



Figure 1. Transfer Characteristics

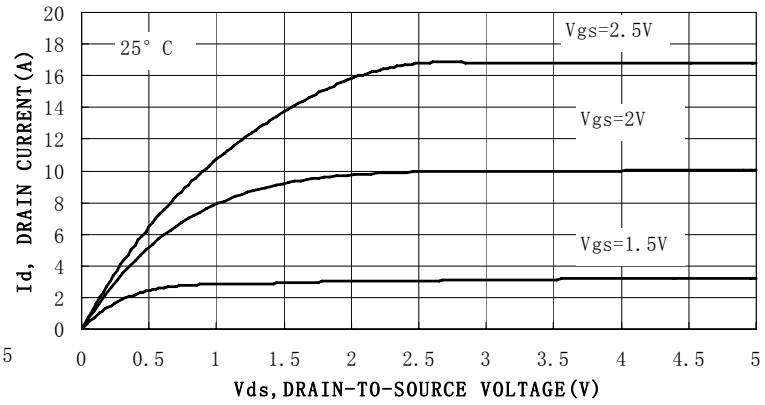



Figure 2. On–Region Characteristics

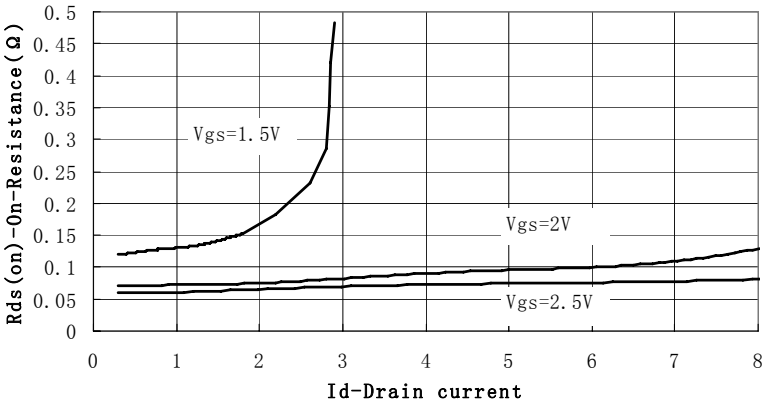



Figure 3. On–Resistance versus Drain Current

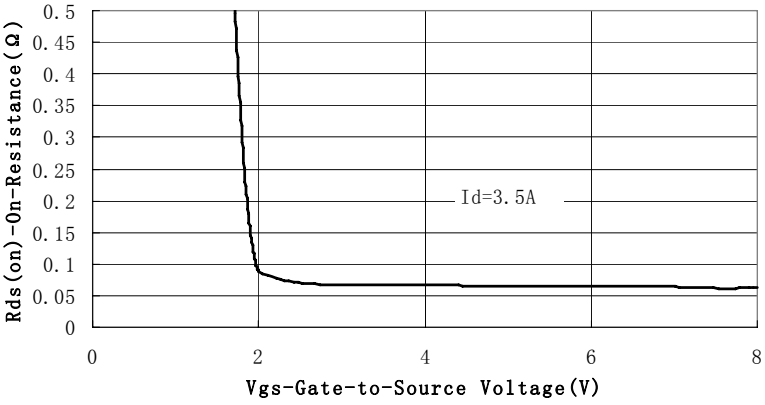



Figure 4. On-Resistance vs. Gate-to-Source Voltage

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## TYPICAL ELECTRICAL CHARACTERISTICS

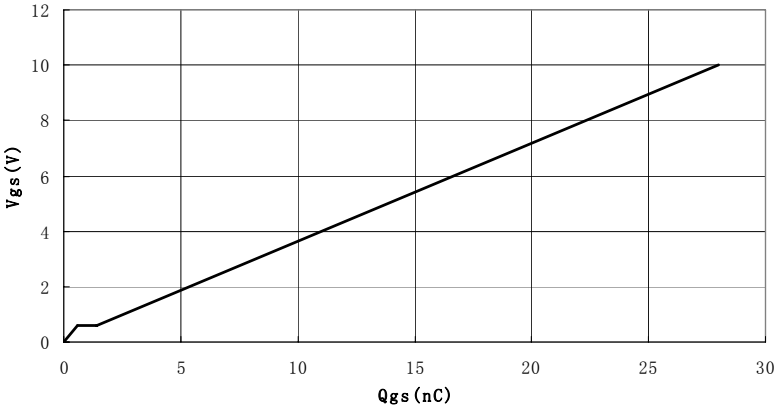


Figure 5. Gate Charge

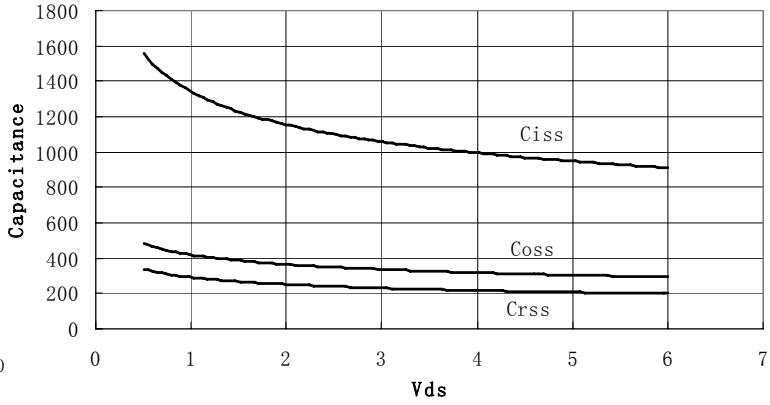


Figure 6. Capacitance

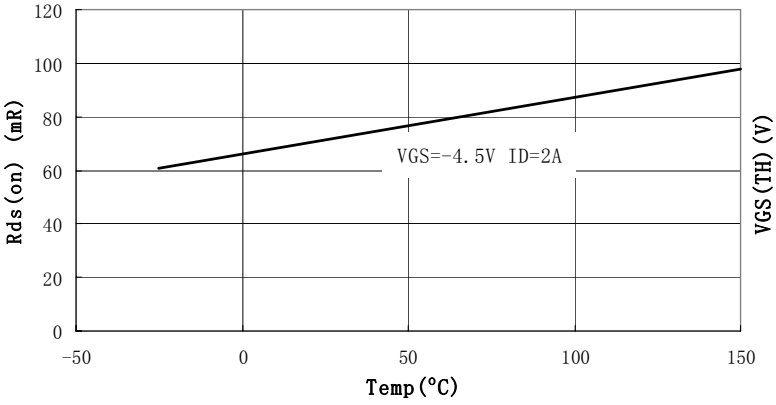


Figure 7. On-Resistance Vs.Junction Temperature

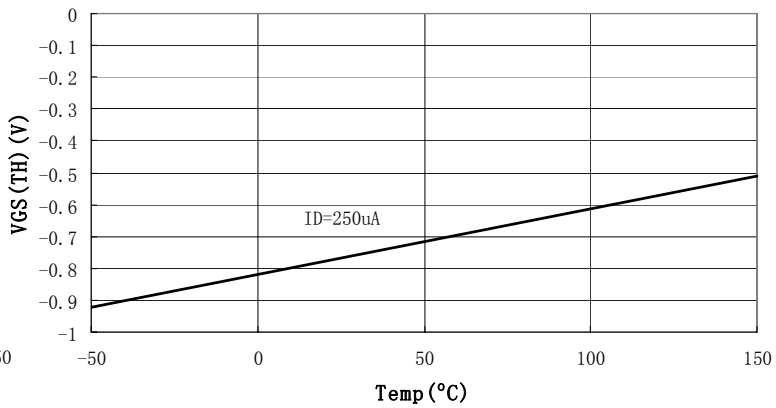


Figure 8. Vth Vs.Junction Temperature

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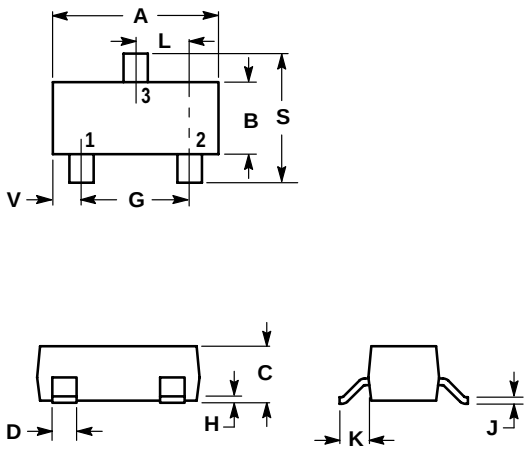
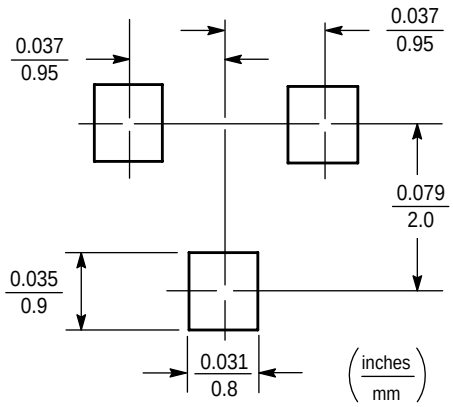
## SOT–23




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M,1982
2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.1102 | 0.1197 | 2.80 | 3.04 |
| B | 0.0472 | 0.0551 | 1.20 | 1.40 |
| C | 0.0350 | 0.0440 | 0.89 | 1.11 |
| D | 0.0150 | 0.0200 | 0.37 | 0.50 |
| G | 0.0701 | 0.0807 | 1.78 | 2.04 |
| H | 0.0005 | 0.0040 | 0.013 | 0.100 |
| J | 0.0034 | 0.0070 | 0.085 | 0.177 |
| K | 0.0140 | 0.0285 | 0.35 | 0.69 |
| L | 0.0350 | 0.0401 | 0.89 | 1.02 |
| S | 0.0830 | 0.1039 | 2.10 | 2.64 |
| V | 0.0177 | 0.0236 | 0.45 | 0.60 |



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