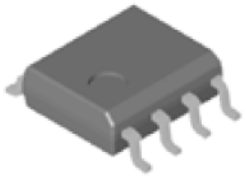
LP4565T1G

SO-8

P-Channel 60-V (D-S) MOSFET

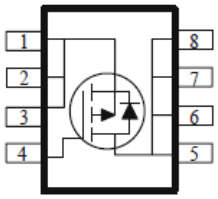


1. Key Features:

- Low $r_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed

2. Typical Applications:

- Load Switches
- DC/DC Conversion
- Motor Drives



3. ORDERING INFORMATION

Device	Marking	Shipping
LP4565T1G	LP4565	4000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25ºC unless otherwise stated)

Parameter		Symbol	Limits	Unit
Drain−to−Source Voltage		VDSS	-60	V
Gate−to−Source Voltage		VGS	± 20	V
Continuous Drain Current(Note 1)	TA =25°C	ID	-7	A
	TA =70°C		-5	
Pulsed Drain Current (Note 2)		IDM	-20	A
Continuous Source Current (Diode Conduction)(Note 1)		IS	-1.6	A
Power Dissipation(Note 1)	TA =25°C	PD	2.9	W
	TA =70°C		1.8	
Operating Junction and Storage Temperature Range		TJ , TSTG	−55 ~+150	ºC

Note: 1.Surface Mounted on 1” x 1” FR4 Board.

2.Pulse width limited by maximum junction temperature.

5. THERMAL CHARACTERISTICS

Parameter		Symbol	Max	Unit
Maximum Junction-to-Ambient (Note 1)	t≤10S	RθJA	45	ºC/W
	Steady State		95	

6. Electrical Characteristics

Characteristic	Symbol		Min.	Typ.	Max.	Unit
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 uA	-1			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±10	uA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -48 V, V_{GS} = 0 V			-1	uA
		V_{DS} = -48 V, V_{GS} = 0 V, T_J = 55°C			-10	
On-State Drain Current [a]	$I_{D(on)}$	V_{DS} = -5 V, V_{GS} = -10 V	-7.5			A
Drain-Source On-Resistance [a]	$r_{DS(on)}$	V_{GS} = -10 V, I_D = -4 A			82	mΩ
		V_{GS} = -4.5 V, I_D = -3.2 A			100	
Forward Transconductance [a]	g_{fs}	V_{DS} = -15 V, I_D = -4 A		9		S
Diode Forward Voltage [a]	V_{SD}	I_S = -2.1 A, V_{GS} = 0 V		-0.83		V
Dynamic [b]						
Total Gate Charge	Q_g	V_{DS} = -30 V, V_{GS} = -4.5 V, I_D = -4 A		10		nC
Gate-Source Charge	Q_{gs}			4.2		
Gate-Drain Charge	Q_{gd}			3.1		
Turn-On Delay Time	$t_{d(on)}$	V_{DS} = -30 V, R_L = 7.5 Ω, I_D = -4 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω		7		ns
Rise Time	t_r			5		
Turn-Off Delay Time	$t_{d(off)}$			37		
Fall Time	t_f			14		
Input Capacitance	C_{iss}	V_{DS} = -15 V, V_{GS} = 0 V, f = 1 Mhz		1146		pF
Output Capacitance	C_{oss}			84		
Reverse Transfer Capacitance	C_{rss}			60		

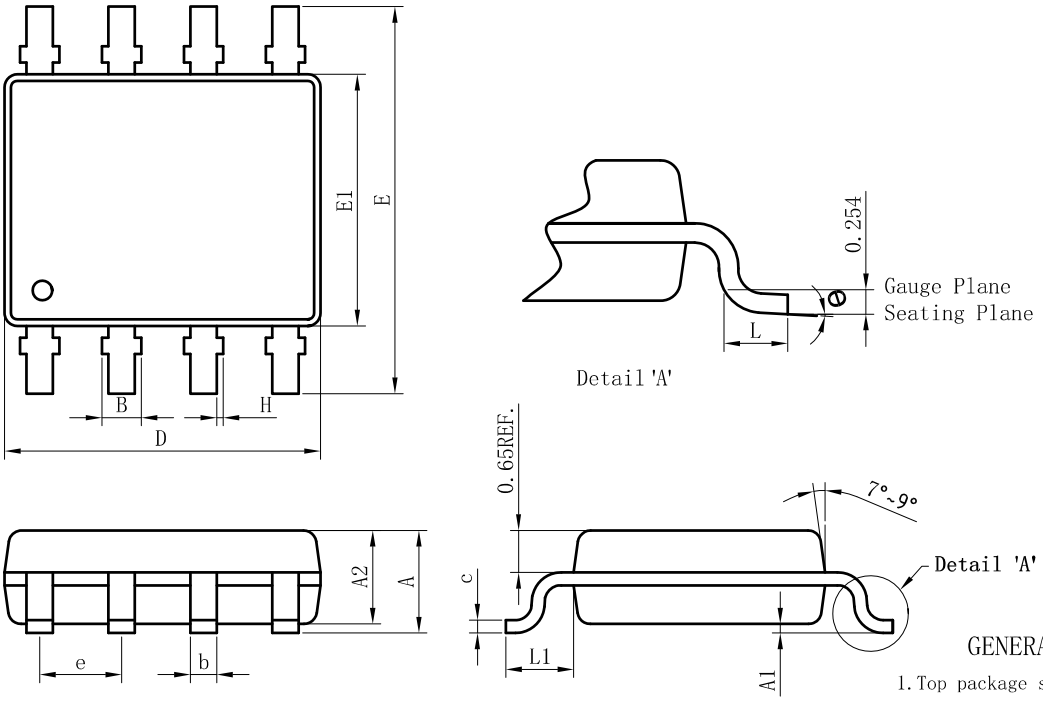
Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.

OUTLINE AND DIMENSIONS

SOP8

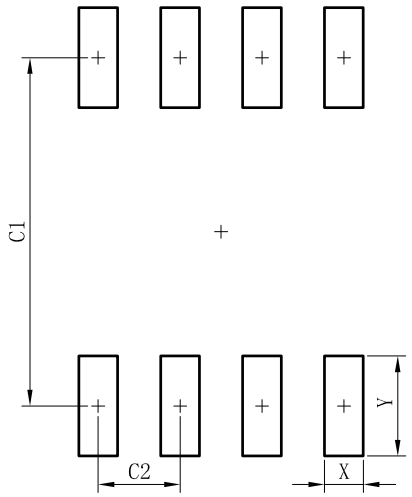


SOP8			
DIM	MIN	NOR	MAX
A	—	—	1.75
A1	0.10	0.15	0.20
A2	1.35	1.45	1.55
b	0.33	0.42	0.51
c	0.15	0.22	0.29
D	4.77	4.90	5.03
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
L	0.46	0.66	0.86
L1	0.85	1.05	1.25
θ	0°	5°	8°
B	—	—	0.55
H	0	0.05	0.10
All Dimensions in mm			

GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um
4. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
5. Dimension "b" Does Not Include Dambar Protrusion.

SOLDERING FOOTPRINT



SOP8	
DIM	(mm)
X	0.60
Y	1.55
C1	5.40
C2	1.27

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