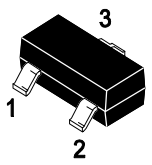
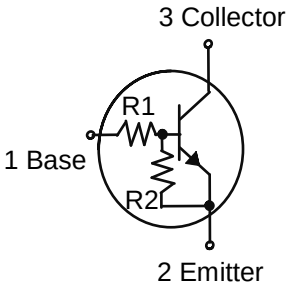
LDTD113ZLT1G
S-LDTD113ZLT1G

Bias Resistor Transistors
NPN Silicon Surface Mount Transistors
with Monolithic Bias Resistor Network



SOT23(TO-236)



1. FEATURES

- Built-in bias resistors enable the configuration of an inverter circuit without connecting exeernal input resistors.
- The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input.They also have the advantage of almost completely eliminating parasitic effects.
- Only the on/off conditions need to be set for operation,making the device design easy.
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- S- prefix for automotive and other applications requiring unique site and control change requirements; AEC-Q101 qualified and PPAP capable.

2. Applications

- Inverter ,Interface, Driver.

3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	R1(K)	R2(K)	Vin(V)	Shipping
LDTD113ZLT1G	E8	1	10	-5~+10	3000/Tape&Reel
LDTD113ZLT3G	E8	1	10	-5~+10	10000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25ºC)

Parameter	Symbol	Limits	Unit
Collector–Emitter Voltage	VCEO	50	V
Collector–Base Voltage	VCBO	50	V
Collector Current	IC	500	mA

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Total Device Dissipation, FR−5 Board (Note 1) @ TA = 25ºC Derate above 25ºC	PD	 225 1.8	 mW mW/ºC
Thermal Resistance, Junction–to–Ambient(Note 1)	RΘJA	556	ºC/W
Junction and Storage temperature	TJ,Tstg	−55~+150	º C

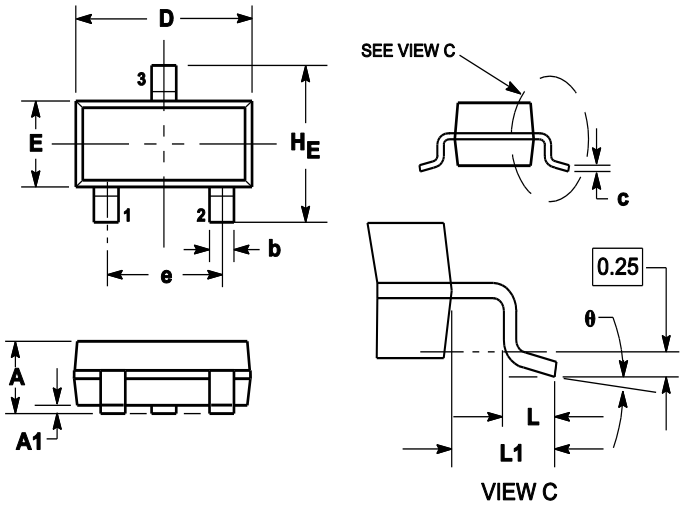
1. FR–5 = 1.0×0.75×0.062 in.

6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector–Emitter Breakdown Voltage (IC = 1 mA, IB = 0)	VBR(CEO)	50	-	-	V
Collector–Base Breakdown Voltage (IC = 100 μA, IE = 0)	VBR(CBO)	50	-	-	V
Collector-Base Cutoff Current (VCB = 50 V, IE = 0)	ICBO	-	-	500	nA
Emitter-Base Cutoff Current (VEB = 5.0 V, IC = 0)	IEBO	-	-	7.2	mA
Collector-Emitter Cutoff Current (VCE = 50 V, IB = 0)	ICEO	-	-	1	μA
DC Current Gain (IC = 50 mA, VCE = 5 V)	HFE	82	-	-	
Collector–Emitter Saturation Voltage (IC = 50 mA, IB = 2.5 mA)	VCE(sat)	-	-	0.3	V
Input Voltage (off) (VCE = 5.0 V, IC = 100 μA)	Vi(off)	-	-	0.3	V
Input Voltage (on) (VCE = 0.3 V, IC = 20 mA)	Vi(on)	1.5	-	-	V
Output Voltage (on) (VCC = 5.0 V, VB = 3 V, RL =1.0KΩ)	VOL	-	-	0.3	V
Output Voltage (off) (VCC = 5.0 V, VB = 0.3 V, RL =1.0KΩ)	VOH	3	-	-	V
Input Resistor	R1	0.7	1.0	1.3	KΩ
Resistor Ratio	R2/R1	8	10	12	

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

7.OUTLINE AND DIMENSIONS

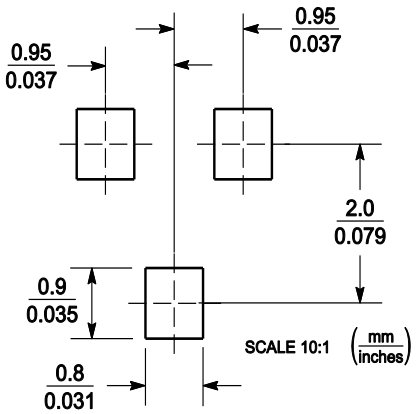


Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1	1.11	0.035	0.04	0.044
A1	0.01	0.06	0.1	0.001	0.002	0.004
b	0.37	0.44	0.5	0.015	0.018	0.02
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.9	3.04	0.11	0.114	0.12
E	1.20	1.3	1.4	0.047	0.051	0.055
e	1.78	1.9	2.04	0.07	0.075	0.081
L	0.10	0.2	0.3	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.4	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

8.SOLDERING FOOTPRINT



DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.

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