

# S-LP03N060TZHG

P-Channel 60-V (D-S) MOSFET

## 1. FEATURES

- Low RDS(on) trench technology
- Low thermal impedance
- Fast switching speed
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- S- prefix for automotive and other applications requiring unique site and control change requirements; AEC-Q101 qualified and PPAP capable.

## 2. APPLICATIONS

- Power Routing
- DC/DC Conversion
- Motor Drives

## 3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
S-LP03N060TZHG	GQ	1000/Tape&Reel

## 4. MAXIMUM RATINGS(Ta = 25°C)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	VDS	-60	V
Gate-Source Voltage	VGS	±20	
Continuous Drain Current (Note1)	ID	-2.8	A
Pulsed Drain Current (Note2)	IDM	-12	
Avalanche Current (L = 0.1mH)	IAS	8	A
Avalanche Energy (L = 0.1mH)	EAS	3.2	mJ
Power Dissipation (Note1)	PD	1.7	W
Operating Junction and Storage Temperature Range	TJ , Tstg	-55~+150	°C

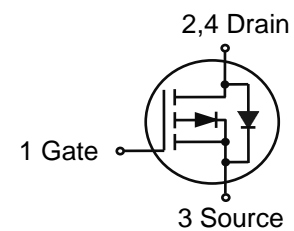
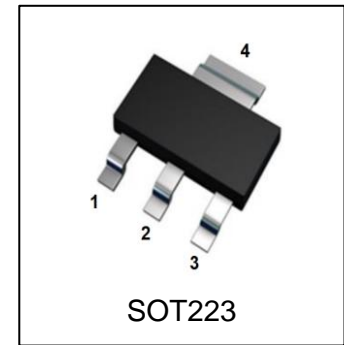
## 5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Thermal Resistance,Junction-to-Ambient(Note 1)	RθJA	70	°C/W
Thermal Resistance,Junction-to-Case (Note 3)	RθJA	160	°C/W
Thermal Resistance,Junction-to-Case (Note 3)	RθJC	20	°C/W

1."1.5 x 1.5" FR4 board using 1 sq in pad, 2 oz Cu.

2.Pulse width limited by maximum junction temperature

3.Surface-mounted on FR4 board using the minimum recommended pad size.

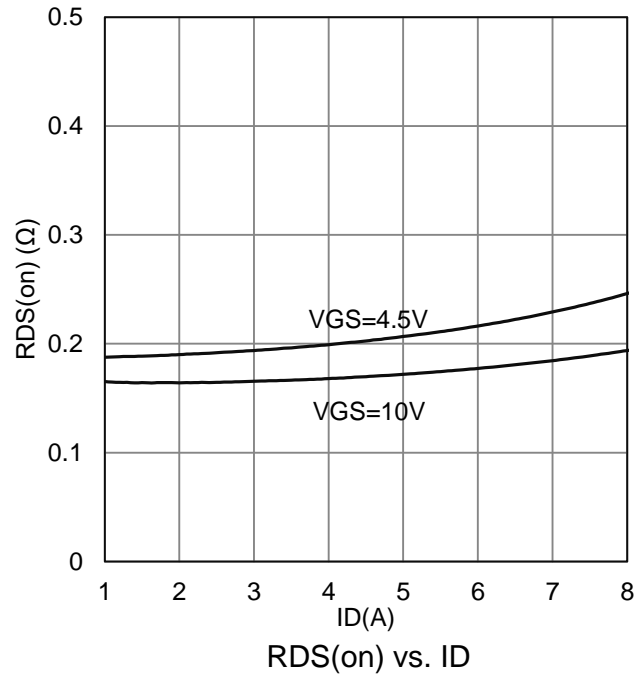
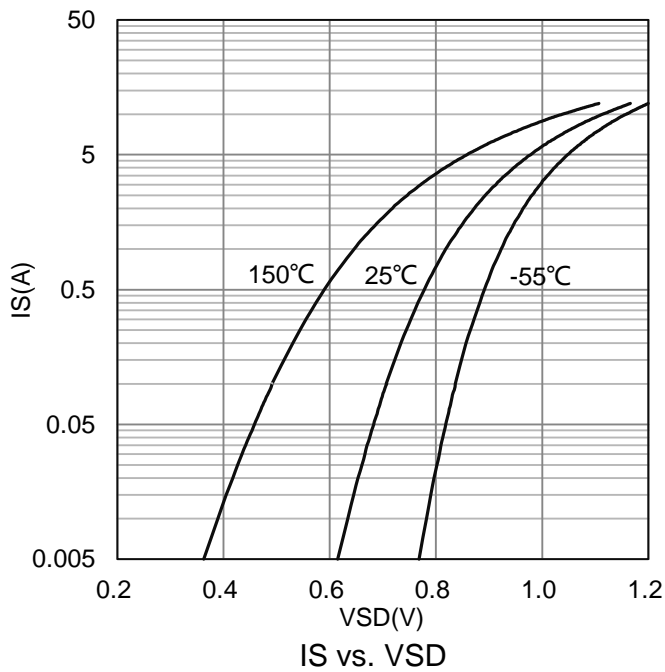
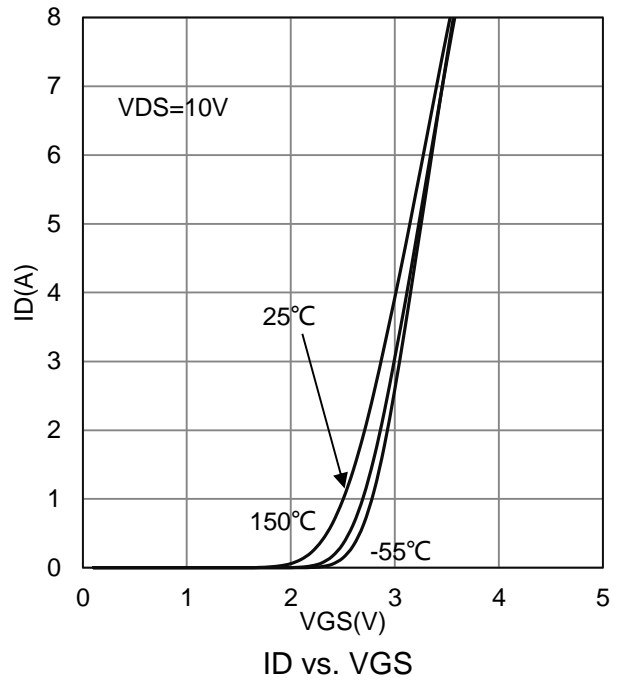
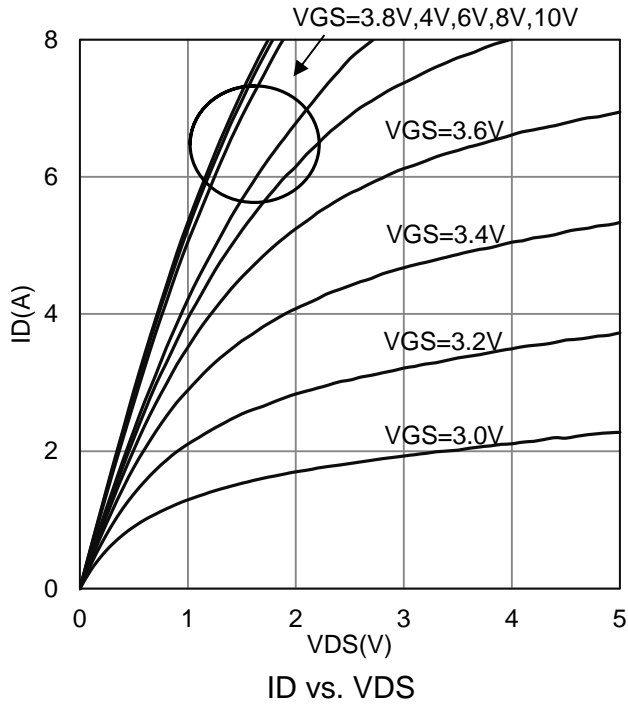


**6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)**

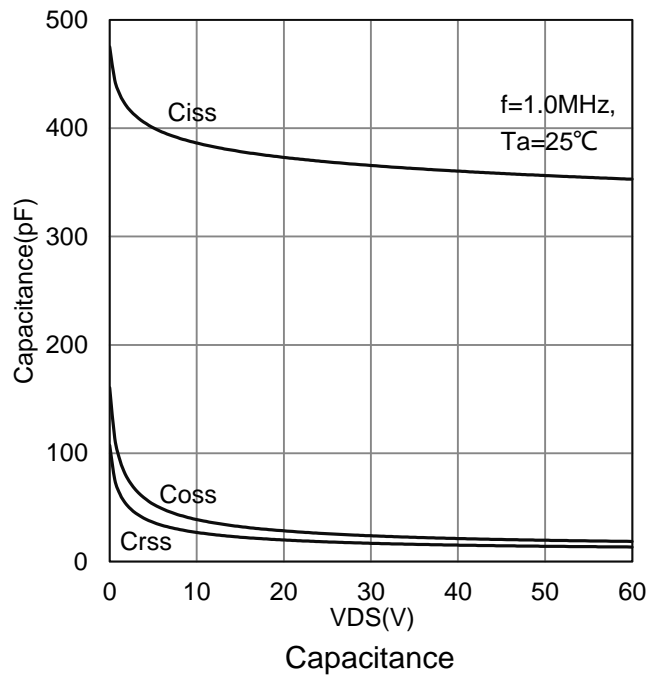
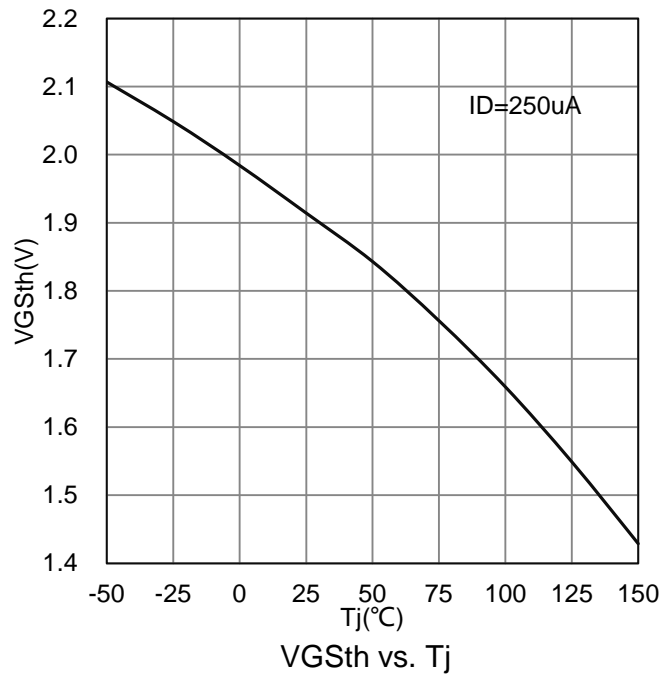
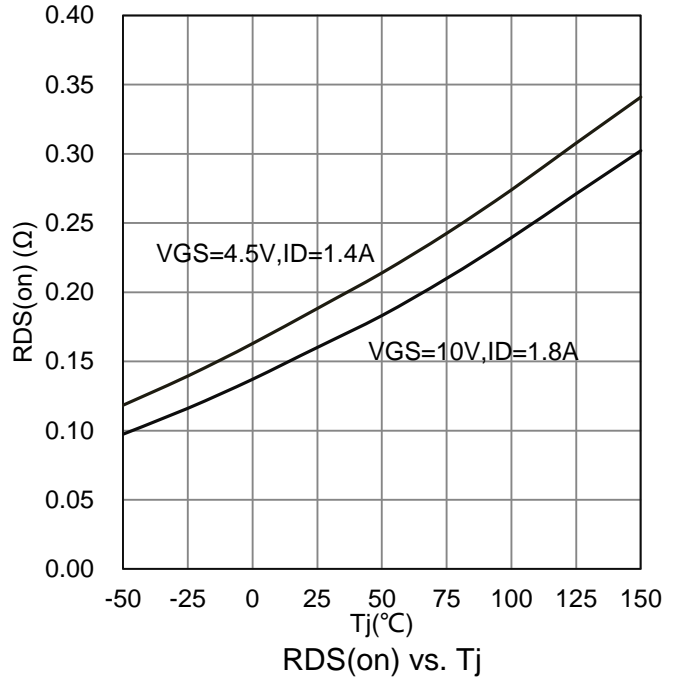
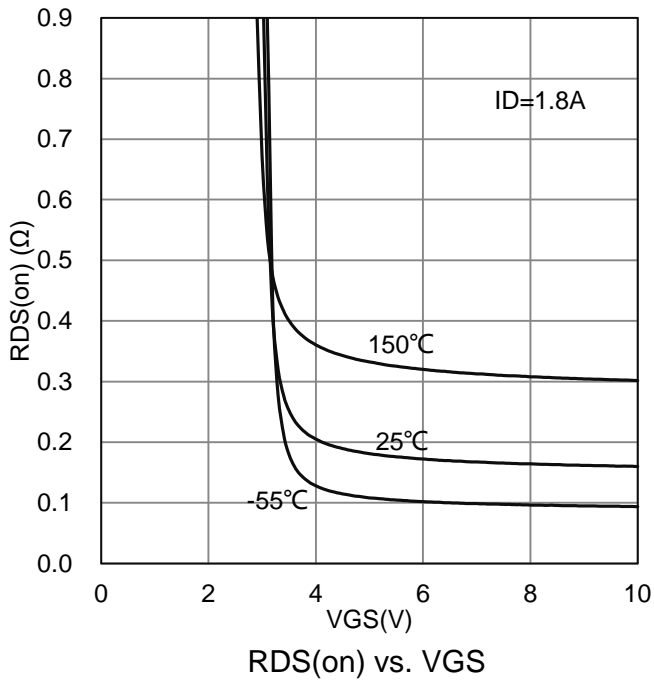
Characteristic	Symbol	Min.	Typ.	Max.	Unit	
<b>Static</b>						
Drain–Source Breakdown Voltage (VGS = 0, ID = -250μA)	VBRDSS	-60	-	-	V	
Gate Threshold Voltage (VDS =VGS , ID =-250μA)	VGS(th)	-1	-	-3	V	
Gate Leakage Current (VDS =0V, VGS =±20V)	IGSS	-	-	±100	nA	
Zero Gate Voltage Drain Current (VDS = -60 V, VGS = 0 V)	IDSS	-	-	-10	μA	
Drain-Source On-Resistance(Note 4) (VGS = -10 V, ID = -1.8 A) (VGS = -4.5 V, ID = -1.4 A)	RDS(ON)	-	170 200	215 260	mΩ	
Diode Forward Voltage (IS = -1.2 A, VGS = 0 V)	VSD	-	-	-1.2	V	
<b>Dynamic</b>						
Total Gate Charge	(VDS = -48 V, VGS = -4.5 V, ID = -1 A)	Qg	-	3.6	-	nC
Gate-Source Charge		Qgs	-	1.2	-	
Gate-Drain Charge		Qgd	-	1.7	-	
Turn-On Delay Time	(VDS = -30 V, RL = 30 Ω, ID = -1 A, VGEN = -10 V, RGEN = 3.1 Ω)	td(on)	-	3.2	-	ns
Rise Time		tr	-	23.6	-	
Turn-Off Delay Time		td(off)	-	14.5	-	
Fall Time		tf	-	17.2	-	
Input Capacitance	(VDS = -30 V, VGS = 0 V, f = 1 MHz)	Ciss	-	366	-	pF
Output Capacitance		Coss	-	24	-	
Reverse Transfer Capacitance		Crss	-	17	-	
Gate Resistance (VDS = 0 V, VGS = 0 V, f = 1 MHz)	Rg	-	5	-	Ω	

4. Pulse test: PW ≤ 300us duty cycle ≤ 2%.

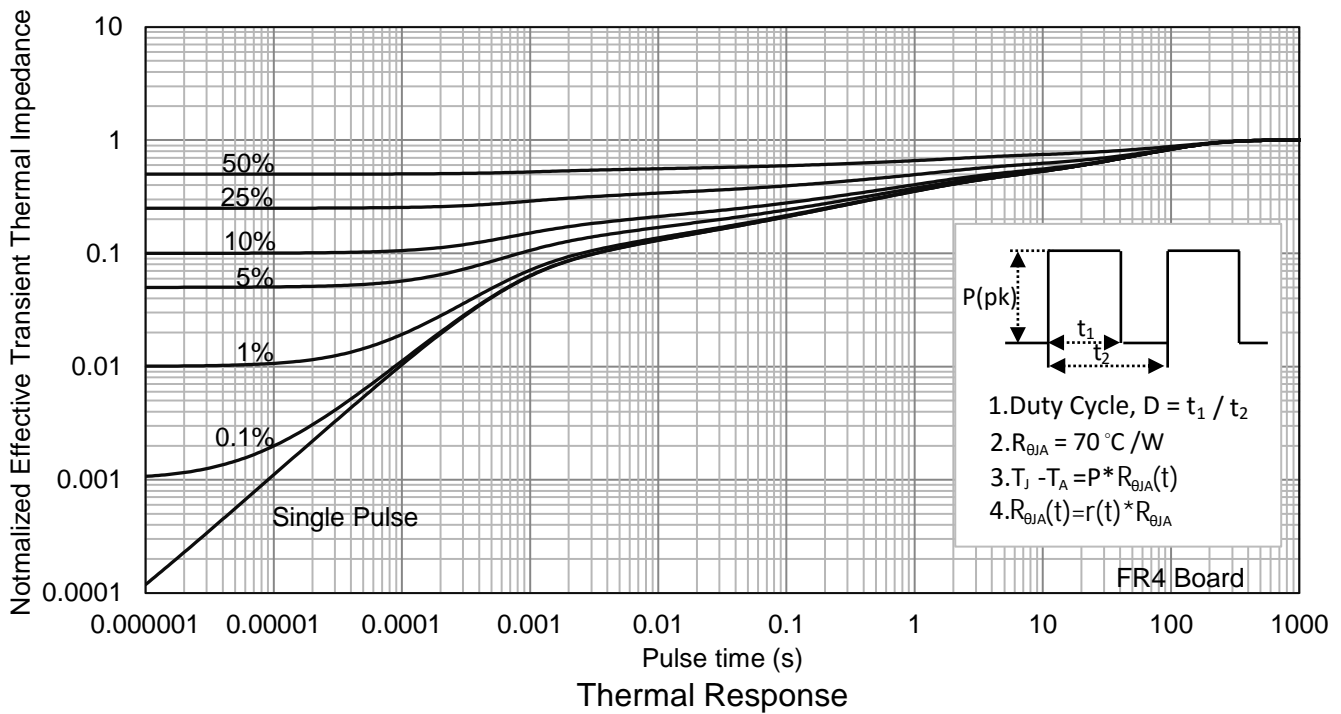
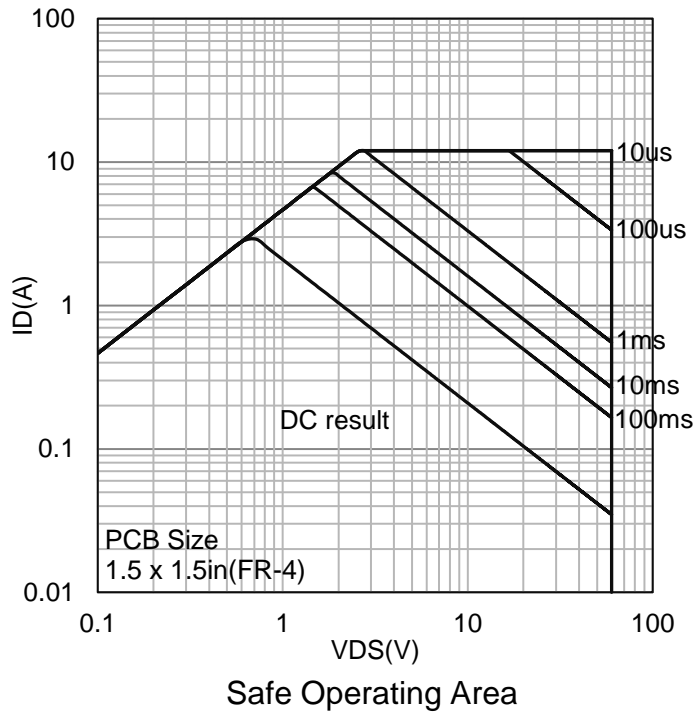
**7. ELECTRICAL CHARACTERISTICS CURVES**



**7. ELECTRICAL CHARACTERISTICS CURVES(Con.)**

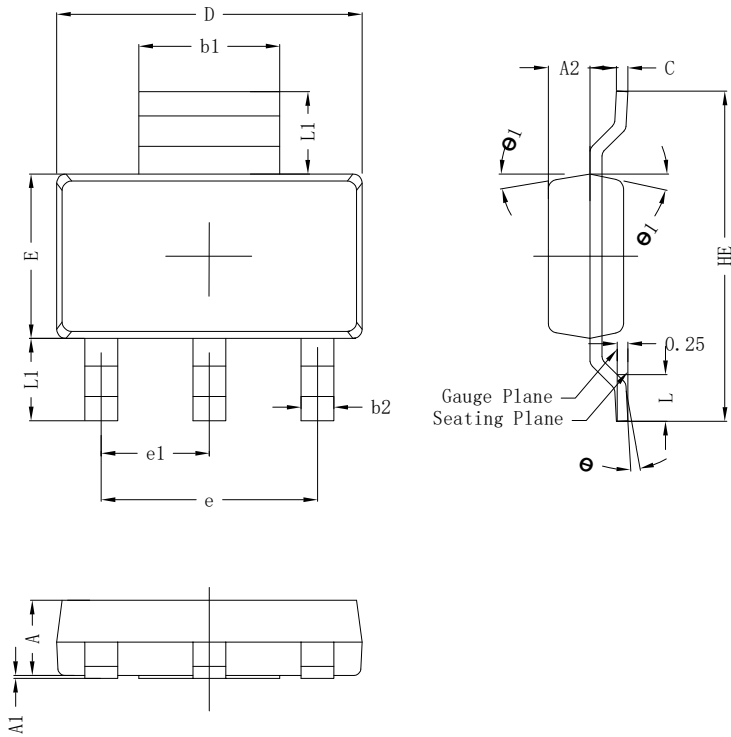


**7. ELECTRICAL CHARACTERISTICS CURVES(Con.)**



**8.OUTLINE AND DIMENSIONS**

SOT223

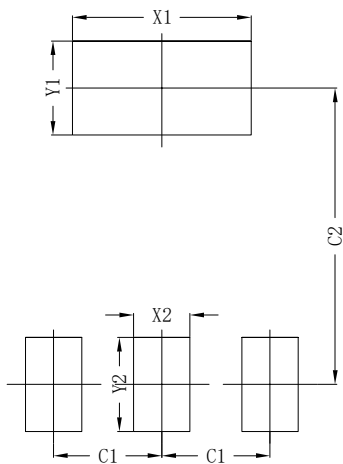


SOT223			
DIM	MIN	NOR	MAX
A	1.50	1.60	1.70
A1	0.00	0.05	0.10
A2	0.80	0.90	1.00
b1	2.90	3.02	3.10
b2	0.60	0.72	0.80
c	0.20	0.27	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	4.60BSC		
e1	2.30BSC		
HE	6.80	7.00	7.20
L	0.80	1.00	1.20
L1	1.75(REF)		
θ	0°~8°		
θ 1	8°	10°	12°
All Dimensions in mm			

**GENERAL NOTES**

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um
4. Protrusion or Gate Burrs shall not exceed 0.10mm per side.

**9.SOLDERING FOOTPRINT**



SOT223	
DIM	(mm)
X1	3.80
Y1	2.00
X2	1.20
Y2	2.00
C1	2.30
C2	6.30

## **DISCLAIMER**

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.
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