QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 1133
10/12 BIT 250, 210 AND 170 MSPS ADC
LTC2242-12/10, LTC2241-12/10 OR LTC2240-12/10

DESCRIPTION

Demonstration circuit 1133 supports a family of 10/12 BIT 250, 210 and 170 MSPS ADCs. Each assembly features one of the following devices: LTC2242-12, LTC2241-12, LTC2240-12, LTC2242-10, LTC2241-10 or LTC2240-10 high speed, high dynamic range ADCs.

The versions of the 1133A demo board that support the LTC2242 family of 10 and 12-Bit A/D converters are listed in Table 1. Depending on the required resolution and sample rate the DC1133 is supplied with the appropriate ADC. The circuitry on the analog inputs is optimized for analog input frequencies from 10 MHz to 250 MHz.

Design files for this circuit board are available. Call the LTC factory.

Table 1. DC1133A Variants

DC1133 VARIANTS	ADC PART NUMBER	RESOLUTION	MAXIMUM SAMPLE RATE	INPUT FREQUENCY
1133A-A	LTC2242-12	12-Bit	250Msps	10MHz < A_{IN} < 250MHz
1133A-B	LTC2241-12	12-Bit	210Msps	10MHz < A_{IN} < 250MHz
1133A-C	LTC2240-12	12-Bit	170Msps	10MHz < A_{IN} < 250MHz
1133A-D	LTC2242-10	10-Bit	250Msps	10MHz < A_{IN} < 250MHz
1133A-E	LTC2241-10	10-Bit	210Msps	10MHz < A_{IN} < 250MHz
1133A-F	LTC2240-10	10-Bit	170Msps	10MHz < A_{IN} < 250MHz

Table 2. Performance Summary (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Supply Voltage	Depending on sampling rate and the A/D converter provided, this supply must provide up to 500mA.	2.5V ±0.25V (10%)
Analog input range	Depending on Sense Pin Voltage (at converter inputs)	$1V_{PP}$ to $2V_{PP}$
Logic Input Voltages: OE, $\overline{SHDN}$	Minimum Logic High	1.7V
	Maximum Logic Low	0.7V
Logic Output Voltage	Minimum Logic High @ -3.4mA w/100Ω Termination	1.7V
	Maximum Logic Low @ +3.4mA w/100Ω Termination	0.7V
Sampling Frequency (Convert Clock Frequency)	See Table 1	
Encode Clock Level	50 Ω Source Impedance. (Convert Clock input is capacitor coupled on board and terminated with 50Ω.)	$0.2V_{P-P}$ ⇔$2.5V_{P-P}$ Sine Wave or Square wave
Resolution	See Table 1	
Input frequency range	See Table 1	
SFDR	See Applicable Data Sheet	
SNR	See Applicable Data Sheet	

QUICK START PROCEDURE

Demonstration circuit 1133 is easy to set up to evaluate the performance of any of the LTC2242 family of High Speed CMOS output A/D converters - LTC2242-12, LTC2241-12, LTC2240-12, LTC2242-10, LTC2241-10 or LTC2240-10. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

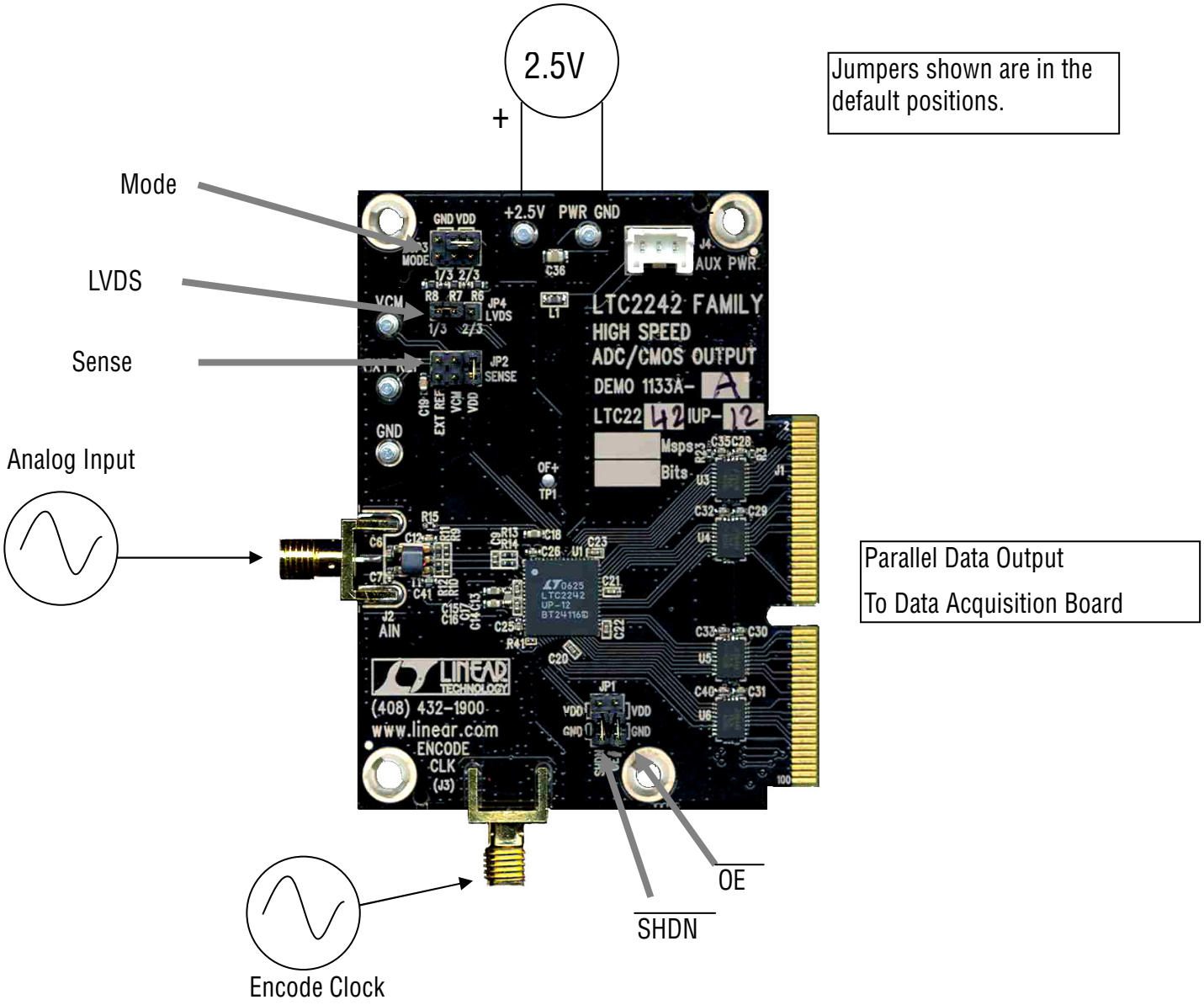


Figure 1. DC1133 Setup

JUMPERS

The DC1133 demonstration circuit board should have the following jumper settings:

JP1:

-SHDN & OE GND: Normal operation (Default)
-SHDN GND & OE Vdd: Normal operation with high output impedance
-SHDN Vdd & OE GND: Nap Mode with high output impedance
-SHDN Vdd & OE Vdd: Sleep Mode with high output impedance

JP2 - SENSE:

-Select 2.5V for the 2V_{PP} input range (Default)
-Select VCM for the 1V_{PP} input range
-Select EXT REF to use an external reference.

JP3 – MODE:

-VDD (Jumper between pins 1&3): 2's complement & disable Clock Duty Cycle Stabilizer (Default for LTC2240, 2241)

-2/3 (Jumper between pins 2&4): 2's complement & Clock Duty Cycle Stabilizer on (Default for LTC2242)

-1/3(Jumper between pins 4&6): Offset Binary & Clock Duty Cycle Stabilizer on

-GND(Jumper between pins 3&5): Offset Binary & Clock Duty Cycle Stabilizer off

JP4 - LVDS:

-1/3 (Default): Demux CMOS with simultaneous update

-2/3: Demux CMOS with interleaved update

POWER

If a DC890B is used to acquire data from the DC1133, the DC890B should be connected to a USB port and provided an external 6V, 1Amp power supply. The DC890B will not enable collection mode without externally applied power present. Apply +2.5V across the pins marked "+2.5V" and "GND" on the DC1133. The DC1133 demonstration circuit requires up to 500 mA depending on the sampling rate and the A/D converter supplied.

While the DC890B data collection board is initially powered by the USB cable, it requires an external power supply of 6V on the 2.1mm power jack or the adjacent turrets (+) and (-) before the DC890B will enable collection mode.

ENCODE CLOCK

NOTE: THIS IS NOT A LOGIC LEVEL INPUT. Apply an encode clock to the SMA connector on the DC1133 demonstration circuit board marked "ENCODE CLK". Refer to Table 2 for recommended level, impedance and coupling. For the best noise performance (SNR AND SFDR), the ENCODE CLK must be driven with a very low jitter source. When using a sinusoidal generator, the amplitude should be large, up to $2.5V_{P-P}$. Using bandpass filters on the ENCODE CLK and the Analog input [AIN] will improve the noise performance by reducing the wideband noise power of the signals. Data sheet FFT plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non-harmonically related spurs and broad band noise. The very high sampling bandwidth of the LTC2242 family of parts will fold multiple Nyquist bands of noise (if present) down to base band raising the noise floor.

[The LTC2242 family of ADCs provides a flexible Encode Clock interface capable of accommodating both single ended and differential sources from LVDS or sinusoidal inputs. See the LTC2242 data sheet for other Encode Clock drive options.]

ANALOG INPUT NETWORK

The input transformer and the RC network on the analog inputs are optimized for 10 to 250MHz. These components must be optimized for higher or lower input frequencies. Consult the LTC2242 data sheet for other frequency ranges.

Apply the analog input signal of interest to the SMA connector on the DC1133 demonstration circuit board marked "AIN". This input is capacitive coupled to the input of a MaCom ETC1-1-13. (See Schematic)

DIGITAL OUTPUTS

The LTC2242-12 can operate in several digital output modes: LVDS, CMOS running at full speed, and CMOS demultiplexed onto two buses, each of which runs at half speed. In the demultiplexed CMOS modes the two buses (referred to as bus A and bus B) can either be updated on alternate clock cycles (interleaved mode) or simultaneously (simultaneous mode). For details on the timing refer to the timing diagrams in datasheet.

Data bus A provides CMOS outputs on pins [2-36] of J1 for a 12-bit ADC, or pins [2-28] for a 10 -bit ADC. Data bus B provides CMOS outputs on pins [64-90]

of J1 for a 12-bit ADC, or pins [64-86] for a 10-bit ADC. For both data buses output signals are grouped in pairs and have one pin ground spacing between these pairs (see schematic). The clock for data bus A is located on pins [50,52]. The clock for data bus B is located on pins [56,58]. Refer to the data sheet for timing diagrams.

The data samples can be collected via a logic analyzer, cabled to a development system through a SHORT 100 pin ribbon cable (available from Samtec – HSC8 series of high speed connectors) or directly via a DC890B FastDAACS data collection system.

When using the DC890 only use the simultaneous update mode. When using other methods of data collection the interleave update is available. When not used connect Bus B to ground for full rate conversion. Refer to data sheet for timing diagrams.

SOFTWARE

The DC890B is controlled by the *PScope System Software* provided or down loaded from the Linear Technology website at http://www.linear.com/software/. If a DC890B was provided, follow the DC890 Quick Start Guide and the instructions below.

To start the data collection software if "*PScope.exe*", is installed (by default) in \Program Files\LTC\PScope\, double click the PScope Icon or bring up the run window under the star menu and browse to the PScope directory and select PScope.

If the DC1133 demonstration circuit is properly connected to the DC890, PSCOPE should automatically detect the DC1133, and configure itself accordingly. If necessary the procedure below explains how to manually configure PSCOPE. Under the device selection menu choose the following:

Selected: User configure

Bits: 12-Bit (or 10-Bit if using -10 versions)

Alignment: Left-16

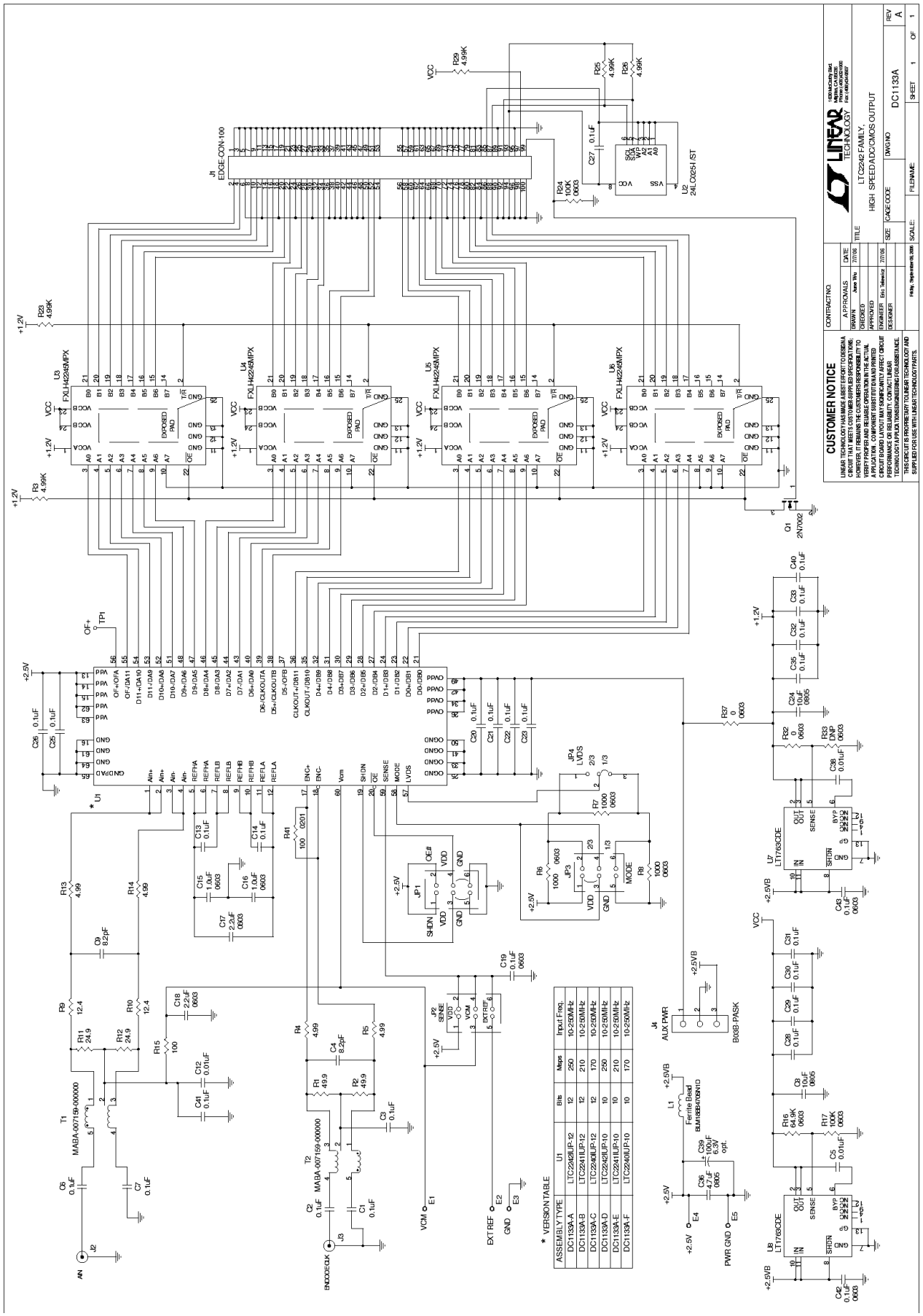
Channel: 1

Bipolar (2's complement)

Positive clock edge

FPGA: CMOS

If everything is hooked up properly, powered and a suitable convert clock is present, clicking the "Collect" button should result in time and frequency plots displayed in the PScope window. Additional information and help for *PScope* is available in the DC890B Quick Start Guide and in the online help available within the *PScope* program itself.


CUSTOMER NOTICE
LINEAR TECHNOLOGY MAKES A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS; HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.
THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.
CONTRACT NO
APPROVALS
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ENGINEER
DESIGNER
DATE
TITLE
LTC2242 FAMILY,
HIGH SPEED ADC/CMOS OUTPUT
SIZE
CAGE CODE
DWG NO
DC1133A
REV
A
SCALE:
FILENAME:
SHEET 1 OF 1
LINEAR TECHNOLOGY
ASSEMBLY TYPE
U1
Bits
Msps
Input Freq.
DC1133A-A
LTC2242IUP-12
12
250
10-250MHz
DC1133A-B
LTC2241IUP-12
12
210
10-250MHz
DC1133A-C
LTC2240IUP-12
12
170
10-250MHz
DC1133A-D
LTC2242IUP-10
10
250
10-250MHz
DC1133A-E
LTC2241IUP-10
10
210
10-250MHz
DC1133A-F
LTC2240IUP-10
10
170
10-250MHz
* VERSION TABLE
J1 EDGE-CON-100
U2 24LC02SI-IST
U3 FXLH2245MPX
U4 FXLH2245MPX
U5 FXLH2245MPX
U6 FXLH2245MPX
Q1 2N7002
U1
T1 MABA-007159-000000
T2 MABA-007159-000000
U8 LT1763CDE
U7 LT1763CDE
JP1
JP2 SENSE
JP3
JP4 LVDS
J4 AUX PWR
B03B-PASK
L1 Ferrite Bead BLM18BB470SN1D
VCM
EXT REF
GND
PWR GND
AIN
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