

FEATURES

- 2GHz -3dB Small Signal Bandwidth
- 300MHz ±0.1dB Bandwidth
- 1.8nV/√Hz Output Noise
- 46.25dBm Equivalent OIP3 at 140MHz
- 40.25dBm Equivalent OIP3 Up to 300MHz
- -81dBc/-72dBc HD2/HD3 at 140MHz, 2V_{P-P} Out
- -84.5dBc IM3 at 140MHz, 2V_{P-P} Out Composite
- -74dBc/-67.5dBc HD2/HD3 at 300MHz, 2V_{P-P} Out
- -72.5dBc IM3 at 300MHz, 2V_{P-P} Out Composite
- Programmable High Speed, Fast Recovery Output Clamping
- DC-Coupled Signal Path
- Operates on Single 2.7V to 3.9V Supply
- Low Power: 150mW on 3.6V
- 2mm × 3mm 10-Pin DFN Package

APPLICATIONS

- Differential ADC Driver
- IF Sampling Receivers
- Impedance Transformer
- SAW Filter Interface
- CCD Buffer

DESCRIPTION

The LTC®6416 is a differential unity gain buffer designed to drive 16-bit ADCs with extremely low output noise and excellent linearity beyond 300MHz. Differential input impedance is 12kΩ, allowing 1:4 and 1:8 transformers to be used at the input to achieve additional system gain.

With no external biasing or gain setting components and a flow-through pinout, the LTC6416 is very easy to use. It can be DC-coupled and has a common mode output offset of -40mV. If the input signals are AC-coupled, the LTC6416 input pins are internally biased to provide an output common mode voltage that is set by the voltage on the V_{CM} pin.

In addition the LTC6416 has high speed, fast recovery clamping circuitry to limit output signal swing. Both the high and low clamp voltages are internally biased to allow maximum output swing but are also user programmable via the CLLO and CLHI pins.

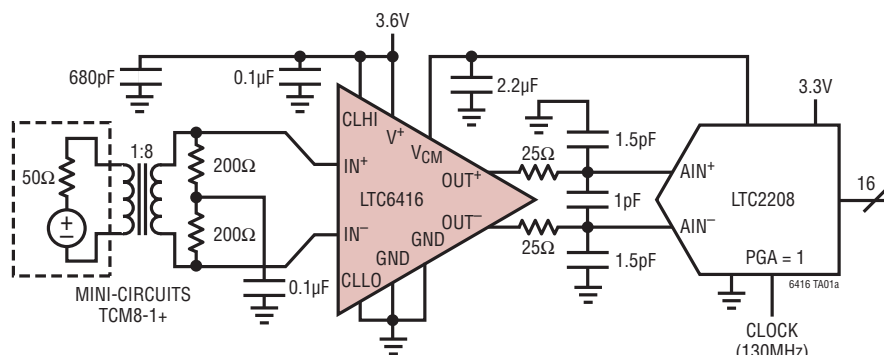
Supply current is nominally 42mA and the LTC6416 operates on supply voltages ranging from 2.7V to 3.9V.

The LTC6416 is packaged in a 10-lead 3mm × 2mm DFN package. Pinout is optimized for placement directly adjacent to Linear's high speed 12-, 14- and 16-bit ADCs.

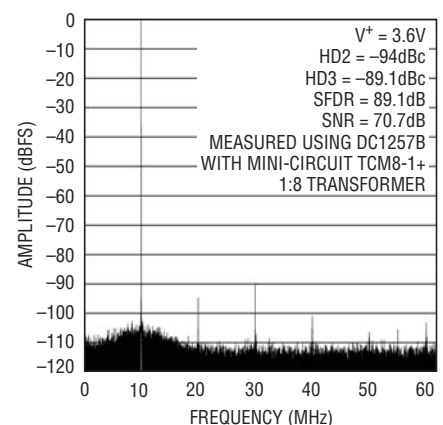
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TYPICAL APPLICATION

LTC6416 Driving LTC2208 ADC – 140MHz IF



LTC6416 Driving LTC2208 ADC
 with 1:8 Transformer $f_{IN} = 140\text{MHz}$,
 $f_S = 130\text{MHz}$, -1dBFS, PGA = 1



6416 TA01b

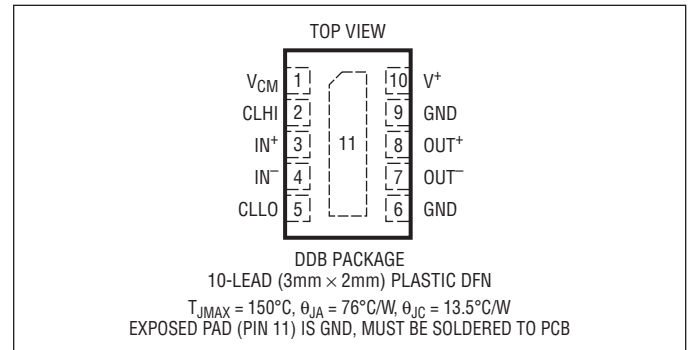
6416f

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to GND)	4V
Input Current (CLLO, CLHI, V_{CM} , IN^+ , IN^-)	± 10 mA
Output Current (OUT^+ , OUT^-)	± 22.5 mA
Operating Temperature Range (Note 2)	-40°C to 85°C
Specified Temperature Range (Note 3)	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Junction Temperature	150°C

PIN CONFIGURATION



ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6416CDDDB#TRMPBF	LTC6416CDDDB#TRPBF	LDDY	10-Lead (3mm x 2mm) Plastic DFN	0°C to 70°C
LTC6416IDDB#TRMPBF	LTC6416IDDB#TRPBF	LDDY	10-Lead (3mm x 2mm) Plastic DFN	-40°C to 85°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

3.6V ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V^+ = 3.6\text{V}$, $\text{GND} = 0\text{V}$, No R_{LOAD} , $C_{LOAD} = 6\text{pF}$. $V_{CM} = 1.25\text{V}$, $CLHI = V^+$, $CLLO = 0\text{V}$ unless otherwise noted. V_{INCM} is defined as $(IN^+ + IN^-)/2$. V_{OUTCM} is defined as $(OUT^+ + OUT^-)/2$. V_{INDIFF} is defined as $(IN^+ - IN^-)$. $V_{OUTDIFF}$ is defined as $(OUT^+ - OUT^-)$. See DC test circuit schematic.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
G_{DIFF}	Differential Gain	$V_{INDIFF} = \pm 1.2\text{V}$ Differential	●	-0.3	-0.15	0	dB
			●	-0.4		0	dB
TCG_{DIFF}	Differential Gain Temperature Coefficient		●	-0.00033		dB/ $^\circ\text{C}$	
$V_{SWINGDIFF}$	Differential Output Voltage Swing	$V_{OUTDIFF}$ $V_{INDIFF} = \pm 2.3\text{V}$	●	3.7 3.3	4.2	V_{P-P} V_{P-P}	
$V_{SWINGMIN}$	Output Voltage Swing Low	Single-Ended Measurement of OUT^+ , OUT^- . $V_{INDIFF} = \pm 2.3\text{V}$	●		0.2 0.3	V V	
$V_{SWINGMAX}$	Output Voltage Swing High	Single-Ended Measurement of OUT^+ , OUT^- . $V_{INDIFF} = \pm 2.3\text{V}$	●	2.15 2	2.3	V V	
I_{OUT}	Output Current Drive	Single-Ended Measurement of OUT^+ , OUT^-	●	± 20		mA	
V_{OS}	Differential Input Offset Voltage	$IN^+ = IN^- = 1.25\text{V}$, $V_{OS} = V_{OUTDIFF}/G_{DIFF}$	●	-5	-0.5	5	mV
			●	-10		10	mV
TCV_{OS}	Differential Input Offset Voltage Drift		●	1		$\mu\text{V}/^\circ\text{C}$	
V_{IOCM}	Common Mode Offset Voltage, Input to Output	$V_{OUTCM} - V_{INCM}$	●	-65	-47	-15	mV
			●	-75		-5	mV

3.6V ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V^+ = 3.6\text{V}$, $\text{GND} = 0\text{V}$, No R_{LOAD} , $C_{\text{LOAD}} = 6\text{pF}$. $V_{\text{CM}} = 1.25\text{V}$, $\text{CLHI} = V^+$, $\text{CLLO} = 0\text{V}$ unless otherwise noted. V_{INCM} is defined as $(\text{IN}^+ + \text{IN}^-)/2$. V_{OUTCM} is defined as $(\text{OUT}^+ + \text{OUT}^-)/2$. V_{INDIFF} is defined as $(\text{IN}^+ - \text{IN}^-)$. V_{OUTDIFF} is defined as $(\text{OUT}^+ - \text{OUT}^-)$. See DC test circuit schematic.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IVR_{MIN}	Input Voltage Range, IN^+ , IN^- (Minimum) (Single-Ended)	Defined by Output Voltage Swing Test	●			0.1	V
IVR_{MAX}	Input Voltage Range IN^+ , IN^- (Maximum) (Single-Ended)	Defined by Output Voltage Swing Test	●	2.4			V
I_B	Input Bias Current, IN^+ , IN^-	$\text{IN}^+ = \text{IN}^- = 1.25\text{V}$	●	-15	-5	15	μA
R_{INDIFF}	Differential Input Resistance	$V_{\text{INDIFF}} = \pm 1.2\text{V}$	●	9	12	15	$\text{k}\Omega$
C_{INDIFF}	Differential Input Capacitance				1		pF
R_{INCM}	Input Common Mode Resistance	$\text{IN}^+ = \text{IN}^- = 0.65\text{V}$ to 1.85V			6		$\text{k}\Omega$
CMRR	Common Mode Rejection Ratio	$\text{IN}^+ = \text{IN}^- = 0.65\text{V}$ to 1.85V , $\text{CMRR} = (V_{\text{OUTDIFF}}/G_{\text{DIFF}}/1.2\text{V})$	●	63.5 59.6	83		dB dB
e_N	Input Noise Voltage Density	$f = 100\text{kHz}$			1.8		$\text{nV}/\sqrt{\text{Hz}}$
i_N	Input Noise Current Density	$f = 100\text{kHz}$			6.5		$\text{pA}/\sqrt{\text{Hz}}$

Output Common Mode Voltage Control

G_{CM}	V_{CM} Pin Common Mode Gain	$V_{\text{CM}} = 0.65\text{V}$ to 1.85V	●	0.9	0.96	1.05	V/V
$V_{\text{INCMDEFAULT}}$	Default Input Common Mode Voltage	V_{INCM} , IN^+ , IN^- , V_{CM} Pin Floating	●	1.3	1.38	1.45	V
$V_{\text{OS}} (V_{\text{CM}} - V_{\text{INCM}})$	Offset Voltage, V_{CM} to V_{INCM}	$V_{\text{CM}} - V_{\text{INCM}}$, $V_{\text{CM}} = 1.25\text{V}$	●	-70	-28	70	mV
$V_{\text{OUTCMDEFAULT}}$	Default Output Common Mode Voltage	Inputs Floating, V_{CM} Pin Floating	●	1.25	1.34	1.45	V
$V_{\text{OS}} (V_{\text{CM}} - V_{\text{OUTCM}})$	Offset Voltage, V_{CM} to V_{OUTCM}	$V_{\text{CM}} - V_{\text{OUTCM}}$, $V_{\text{CM}} = 1.25\text{V}$	●	-60	15	60	mV
V_{OUTCMMIN}	Output Common Mode Voltage Range (Minimum)	$V_{\text{CM}} = 0.1\text{V}$	●		0.37	0.5 0.55	V V
V_{OUTCMMAX}	Output Common Mode Voltage Range (Maximum)	$V_{\text{CM}} = 2.7\text{V}$	●	2.3 2.25	2.46		V V
$V_{\text{CMDEFAULT}}$	V_{CM} Pin Default Voltage		●	1.325	1.36	1.425	V
R_{VCM}	V_{CM} Pin Input Resistance		●	2.5	3.8	5.1	$\text{k}\Omega$
C_{VCM}	V_{CM} Pin Input Capacitance				1		pF
I_{BVCM}	V_{CM} Pin Bias Current	$V_{\text{CM}} = 1.25\text{V}$	●	-50	-32	50	μA

DC Clamping Characteristics

$V_{\text{CLHIDEFAULT}}$	Default Output Clamp Voltage, High		●	2.3	2.45	2.6	V
$V_{\text{OS}} (\text{CLHI} - V_{\text{OUTCM}})$	Offset Voltage, CLHI to V_{OUTCM}		●	-55	13	55	mV
$V_{\text{CLLODEFAULT}}$	Default Output Clamp Voltage, Low		●	0.125	0.265	0.425	V
$V_{\text{OS}} (\text{CLLO} - V_{\text{OUTCM}})$	Offset Voltage, CLLO to V_{OUTCM}		●	-120	-70	0	mV
R_{CLHI}	CLHI Pin Input Resistance	$V_{\text{CLHI}} = 2.45\text{V}$	●	3	4.1	5	$\text{k}\Omega$
I_{BCLHI}	CLHI Pin Bias Current	$V_{\text{CLHI}} = 2.45\text{V}$	●	-25	-1	25	μA
R_{CLLO}	CLLO Pin Input Resistance	$V_{\text{CLLO}} = 0.275\text{V}$	●	1.5	2.3	3.2	$\text{k}\Omega$
I_{BCLLO}	CLLO Pin Bias Current	$V_{\text{CLLO}} = 0.275\text{V}$	●	-25	4.5	25	μA

Power Supply

V_S	Supply Voltage Range		●	2.7		3.9	V
I_S	Supply Current		●	33	42	51 54	mA mA
PSRR	Power Supply Rejection Ratio	$V_S = 2.7\text{V}$ to 3.6V	●	57.5	80		dB

3.3V ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V^+ = 3.3\text{V}$, $\text{GND} = 0\text{V}$, No R_{LOAD} , $C_{\text{LOAD}} = 6\text{pF}$, $V_{\text{CM}} = 1.25\text{V}$, $\text{CLHI} = V^+$, $\text{CLLO} = 0\text{V}$ unless otherwise noted. V_{INCM} is defined as $(\text{IN}^+ + \text{IN}^-)/2$. V_{OUTCM} is defined as $(\text{OUT}^+ + \text{OUT}^-)/2$. V_{INDIFF} is defined as $(\text{IN}^+ - \text{IN}^-)$. V_{OUTDIFF} is defined as $(\text{OUT}^+ - \text{OUT}^-)$. See DC test circuit schematic.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input/Output Characteristics							
G_{DIFF}	Differential Gain	$V_{\text{INDIFF}} = \pm 1.2\text{V}$	●	-0.3 -0.4	-0.15	0 0	dB dB
$\text{TC}_{G_{\text{DIFF}}}$	Differential Gain Temperature Coefficient		●		-0.00033		dB/ $^\circ\text{C}$
V_{OUTDIFF}	Differential Output Voltage Swing	$V_{\text{INDIFF}} = \pm 2.3\text{V}$	●	3.5 3.2	4		$V_{\text{P-P}}$ $V_{\text{P-P}}$
V_{OUTMIN}	Output Voltage Swing Low	Single-Ended Measurement of OUT^+ , OUT^- . $V_{\text{INDIFF}} = \pm 2.3\text{V}$	●		0.2	0.3 0.35	V V
V_{OUTMAX}	Output Voltage Swing High	Single-Ended Measurement of OUT^+ , OUT^- . $V_{\text{INDIFF}} = \pm 2.3\text{V}$	●	2.05 1.95	2.2		V V
I_{OUT}	Output Current Drive (Note 4)	Single-Ended Measurement of OUT^+ , OUT^-	●	± 20			mA
V_{OS}	Differential Input Offset Voltage	$\text{IN}^+ = \text{IN}^- = 1.25\text{V}$, $V_{\text{OS}} = V_{\text{OUTDIFF}}/G_{\text{DIFF}}$	●	-5 -10	-0.1	5 10	mV mV
$\text{TC}_{V_{\text{OS}}}$	Differential Input Offset Voltage Drift		●		1		$\mu\text{V}/^\circ\text{C}$
V_{IOCM}	Common Mode Offset Voltage, Input to Output	$V_{\text{OUTCM}} - V_{\text{INCM}}$	●	-65 -75	-40	-15 -5	mV mV
IVR_{MIN}	Input Voltage Range, IN^+ , IN^- (Minimum) (Single-Ended)	Defined by Output Voltage Swing Test	●			0.1	V
IVR_{MAX}	Input Voltage Range, IN^+ , IN^- (Maximum) (Single-Ended)	Defined by Output Voltage Swing Test	●	2.4			V
I_{B}	Input Bias Current, IN^+ , IN^-	$\text{IN}^+ = \text{IN}^- = 1.25\text{V}$	●	-15	-4	15	μA
R_{INDIFF}	Differential Input Resistance	$V_{\text{INDIFF}} = \pm 1.2\text{V}$	●	9	12	15	k Ω
C_{INDIFF}	Differential Input Capacitance				1		pF
R_{INCM}	Input Common Mode Resistance	$\text{IN}^+ = \text{IN}^- = 0.65\text{V}$ to 1.85V			6		k Ω
CMRR	Common Mode Rejection Ratio	$\text{IN}^+ = \text{IN}^- = 0.65\text{V}$ to $1.85\text{V} = \Delta V_{\text{INCM}}$, $\text{CMRR} = (V_{\text{OUTDIFF}}/G_{\text{DIFF}})/\Delta V_{\text{INCM}}$	●	63.5 59.6	83		dB dB
e_{N}	Input Noise Voltage Density	$f = 100\text{kHz}$			1.8		$\text{nV}/\sqrt{\text{Hz}}$
i_{N}	Input Noise Current Density	$f = 100\text{kHz}$			6.5		$\text{pA}/\sqrt{\text{Hz}}$
Output Common Mode Voltage Control							
G_{CM}	V_{CM} Pin Common Mode Gain	$V_{\text{CM}} = 0.65\text{V}$ to 1.85V	●	0.9	0.96	1.05	V/V
$V_{\text{INCMDEFAULT}}$	Default Input Common Mode Voltage	V_{INCM} . IN^+ , IN^- , V_{CM} Pin Floating	●	1.2	1.28	1.35	V
$V_{\text{OS}} (V_{\text{CM}} - V_{\text{INCM}})$	Offset Voltage, V_{CM} to V_{INCM}	$V_{\text{CM}} - V_{\text{INCM}}$, $V_{\text{CM}} = 1.25\text{V}$	●	-70	-26	70	mV
$V_{\text{OUTCMDEFAULT}}$	Default Output Common Mode Voltage	Inputs Floating, V_{CM} Pin Floating	●	1.15	1.24	1.35	V
$V_{\text{OS}} (V_{\text{CM}} - V_{\text{OUTCM}})$	Offset Voltage, V_{CM} to V_{OUTCM}	$V_{\text{CM}} - V_{\text{OUTCM}}$, $V_{\text{CM}} = 1.25\text{V}$	●	-60	14	60	mV
V_{OUTCMMIN}	Output Common Mode Voltage (Minimum)	$V_{\text{CM}} = 0.1\text{V}$	●		0.34	0.5 0.55	V V
V_{OUTCMMAX}	Output Common Mode Voltage (Maximum)	$V_{\text{CM}} = 2.4\text{V}$	●	2.05 2	2.16		V V
$V_{\text{CMDEFAULT}}$	V_{CM} Pin Default Voltage		●	1.2	1.25	1.3	V
R_{VCM}	V_{CM} Pin Input Resistance		●	2.5	3.8	5.1	k Ω
C_{VCM}	V_{CM} Pin Input Capacitance				1		pF
I_{BVCM}	V_{CM} Pin Bias Current	$V_{\text{CM}} = 1.25\text{V}$	●	-10	0.2	10	μA

3.3V ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V^+ = 3.3\text{V}$, $\text{GND} = 0\text{V}$, No R_{LOAD} , $C_{\text{LOAD}} = 6\text{pF}$, $V_{\text{CM}} = 1.25\text{V}$, $\text{CLHI} = V^+$, $\text{CLLO} = 0\text{V}$ unless otherwise noted. V_{INCM} is defined as $(\text{IN}^+ + \text{IN}^-)/2$. V_{OUTCM} is defined as $(\text{OUT}^+ + \text{OUT}^-)/2$. V_{INDIFF} is defined as $(\text{IN}^+ - \text{IN}^-)$. V_{OUTDIFF} is defined as $(\text{OUT}^+ - \text{OUT}^-)$. See DC test circuit schematic.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
DC Clamping Characteristics							
$V_{\text{CLHI}}^{\text{DEFAULT}}$	Default Output Clamp Voltage, High		●	2.1	2.23	2.4	V
$V_{\text{OS}}(\text{CLHI} - V_{\text{OUTCM}})$	Offset Voltage, CLHI to V_{OUTCM}		●	-55	4	55	mV
$V_{\text{CLLO}}^{\text{DEFAULT}}$	Default Output Clamp Voltage, Low		●	0.1	0.25	0.4	V
$V_{\text{OS}}(\text{CLLO} - V_{\text{OUTCM}})$	Offset Voltage, CLLO to V_{OUTCM}		●	-120	-72	0	mV
R_{CLHI}	CLHI Pin Input Resistance	$V_{\text{CLHI}} = 2.25\text{V}$	●	3	4.1	5	k Ω
I_{BCLHI}	CLHI Pin Bias Current	$V_{\text{CLHI}} = 2.25\text{V}$	●	-25	-1	25	μA
R_{CLLO}	CLLO Pin Input Resistance	$V_{\text{CLLO}} = 0.25\text{V}$	●	1.5	2.3	3.2	k Ω
I_{BCLLO}	CLLO Pin Bias Current	$V_{\text{CLLO}} = 0.25\text{V}$	●	-25	3	25	μA
Power Supply							
V_{S}	Supply Voltage Range		●	2.7		3.9	V
I_{S}	Supply Current		●	33	42	51	mA
						54	mA
PSRR	Power Supply Rejection Ratio	$V_{\text{S}} = 2.7\text{V}$ to 3.6V	●	57.5	80		dB

AC ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V^+ = 3.3\text{V}$ and 3.6V unless otherwise noted, $\text{GND} = 0\text{V}$, No R_{LOAD} , $C_{\text{LOAD}} = 6\text{pF}$, $V_{\text{CM}} = 1.25\text{V}$, $\text{CLHI} = V_{\text{CC}}$, $\text{CLLO} = 0\text{V}$ unless otherwise noted. V_{INCM} is defined as $(\text{IN}^+ + \text{IN}^-)/2$. V_{OUTCM} is defined as $(\text{OUT}^+ + \text{OUT}^-)/2$. V_{INDIFF} is defined as $(\text{IN}^+ - \text{IN}^-)$. V_{OUTDIFF} is defined as $(\text{OUT}^+ - \text{OUT}^-)$. See DC test circuit schematic.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Differential AC Characteristics						
-3dB BW	-3dB Bandwidth	200mV _{P-P,OUT} Differential		2		GHz
0.1dB BW	$\pm 0.1\text{dB}$ Bandwidth	200mV _{P-P,OUT} Differential		0.3		GHz
0.5dB BW	$\pm 0.5\text{dB}$ Bandwidth	200mV _{P-P,OUT} Differential		1.4		GHz
1/f	1/f Noise Corner			25		kHz
SR	Slew Rate	Differential		3.4		V/ns
$t_{\text{S}1\%}$	1% Settling Time	2V _{P-P,OUT}		1.8		ns
Common Mode AC Characteristics (V_{CM} Pin)						
-3dB BW _{VCM}	V_{CM} Pin Small Signal -3dB BW	$V_{\text{CM}} = 0.1\text{V}_{\text{P-P}}$, Measured Single-Ended at Output		9		MHz
SR _{CM}	Common Mode Slew Rate	Measured Single-Ended at Output		40		V/ μs
AC Clamping Characteristics						
$t_{\text{OVD R}}$	Overdrive Recovery Time	1.9V _{P-P,OUT}		5		ns
AC Linearity						
70MHz Signal						
HD2	Second Harmonic Distortion	$V^+ = 3.3\text{V}$, $V_{\text{CM}} = 1.05\text{V}$, $V_{\text{OUTDIFF}} = 2\text{V}_{\text{P-P}}$ $V^+ = 3.3\text{V}$, $V_{\text{CM}} = 1.25\text{V}$, $V_{\text{OUTDIFF}} = 2\text{V}_{\text{P-P}}$ $V^+ = 3.6\text{V}$, $V_{\text{CM}} = 1.05\text{V}$, $V_{\text{OUTDIFF}} = 2\text{V}_{\text{P-P}}$ $V^+ = 3.6\text{V}$, $V_{\text{CM}} = 1.25\text{V}$, $V_{\text{OUTDIFF}} = 2\text{V}_{\text{P-P}}$		-83.5		dBc
				-71		dBc
				-78.5		dBc
				-88.5		dBc

AC ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V^+ = 3.3\text{V}$ and 3.6V unless otherwise noted, $\text{GND} = 0\text{V}$, No R_{LOAD} , $C_{\text{LOAD}} = 6\text{pF}$, $V_{\text{CM}} = 1.25\text{V}$, $\text{CLHI} = V_{\text{CC}}$, $\text{CLLO} = 0\text{V}$ unless otherwise noted. V_{INCM} is defined as $(\text{IN}^+ + \text{IN}^-)/2$. V_{OUTCM} is defined as $(\text{OUT}^+ + \text{OUT}^-)/2$. V_{INDIFF} is defined as $(\text{IN}^+ - \text{IN}^-)$. V_{OUTDIFF} is defined as $(\text{OUT}^+ - \text{OUT}^-)$. See DC test circuit schematic.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
HD3	Third Harmonic Distortion	$V^+ = 3.3\text{V}, V_{\text{CM}} = 1.05\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-73		dBc
		$V^+ = 3.3\text{V}, V_{\text{CM}} = 1.25\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-60		dBc
		$V^+ = 3.6\text{V}, V_{\text{CM}} = 1.05\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-94.5		dBc
		$V^+ = 3.6\text{V}, V_{\text{CM}} = 1.25\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-83		dBc
IM3	Output Third Order Intermodulation Distortion	$V^+ = 3.3\text{V}, V_{\text{CM}} = 1.05\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-76.5		dBc
		$V^+ = 3.6\text{V}, V_{\text{CM}} = 1.25\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-86		dBc
OIP3	Output Third Order Intercept (Equivalent) (Note 5)	$V^+ = 3.3\text{V}, V_{\text{CM}} = 1.05\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		42.25		dBm
		$V^+ = 3.6\text{V}, V_{\text{CM}} = 1.25\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		47		dBm
P1dB	Output 1dB Compression Point (Equivalent) (Note 5)	$V^+ = 3.6\text{V}, V_{\text{CM}} = 1.25\text{V}$		14.1		dBm

140MHz Signal

HD2	Second Harmonic Distortion	$V^+ = 3.3\text{V}, V_{\text{CM}} = 1.05\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-79.5		dBc
		$V^+ = 3.3\text{V}, V_{\text{CM}} = 1.25\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-75.5		dBc
		$V^+ = 3.6\text{V}, V_{\text{CM}} = 1.05\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-73		dBc
		$V^+ = 3.6\text{V}, V_{\text{CM}} = 1.25\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-81		dBc
HD3	Third Harmonic Distortion	$V^+ = 3.3\text{V}, V_{\text{CM}} = 1.05\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-64		dBc
		$V^+ = 3.3\text{V}, V_{\text{CM}} = 1.25\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-55		dBc
		$V^+ = 3.6\text{V}, V_{\text{CM}} = 1.05\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-70		dBc
		$V^+ = 3.6\text{V}, V_{\text{CM}} = 1.25\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-72		dBc
IM3	Output Third Order Intermodulation Distortion	$V^+ = 3.3\text{V}, V_{\text{CM}} = 1.05\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-75		dBc
		$V^+ = 3.6\text{V}, V_{\text{CM}} = 1.25\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-84.5		dBc
OIP3	Output Third Order Intercept (Equivalent) (Note 5)	$V^+ = 3.3\text{V}, V_{\text{CM}} = 1.05\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		41.5		dBm
		$V^+ = 3.6\text{V}, V_{\text{CM}} = 1.25\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		46.25		dBm
P1dB	Output 1dB Compression Point (Equivalent) (Note 5)	$V^+ = 3.6\text{V}, V_{\text{CM}} = 1.25\text{V}$		14.1		dBm

300MHz Signal

HD2	Second Harmonic Distortion	$V^+ = 3.3\text{V}, V_{\text{CM}} = 1.05\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-75		dBc
		$V^+ = 3.3\text{V}, V_{\text{CM}} = 1.25\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-65		dBc
		$V^+ = 3.6\text{V}, V_{\text{CM}} = 1.05\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-69.5		dBc
		$V^+ = 3.6\text{V}, V_{\text{CM}} = 1.25\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-74		dBc
HD3	Third Harmonic Distortion	$V^+ = 3.3\text{V}, V_{\text{CM}} = 1.05\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-59		dBc
		$V^+ = 3.3\text{V}, V_{\text{CM}} = 1.25\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-51.5		dBc
		$V^+ = 3.6\text{V}, V_{\text{CM}} = 1.05\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-63		dBc
		$V^+ = 3.6\text{V}, V_{\text{CM}} = 1.25\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-67.5		dBc
IM3	Output Third Order Intermodulation Distortion	$V^+ = 3.3\text{V}, V_{\text{CM}} = 1.05\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-68.5		dBc
		$V^+ = 3.6\text{V}, V_{\text{CM}} = 1.25\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		-72.5	-64	dBc
OIP3	Output Third Order Intercept (Equivalent) (Note 5)	$V^+ = 3.3\text{V}, V_{\text{CM}} = 1.05\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$		38.25		dBm
		$V^+ = 3.6\text{V}, V_{\text{CM}} = 1.25\text{V}, V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$	36	40.25		dBm
P1dB	Output 1dB Compression Point (Equivalent) (Note 5)	$V^+ = 3.6\text{V}, V_{\text{CM}} = 1.25\text{V}$		12.9		dBm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC6416C/LTC6416I is guaranteed functional over the operating temperature range of -40°C to 85°C .

Note 3: The LTC6416C is guaranteed to meet specified performance from 0°C to 70°C . It is designed, characterized and expected to meet specified performance from -40°C and 85°C but is not tested or QA sampled

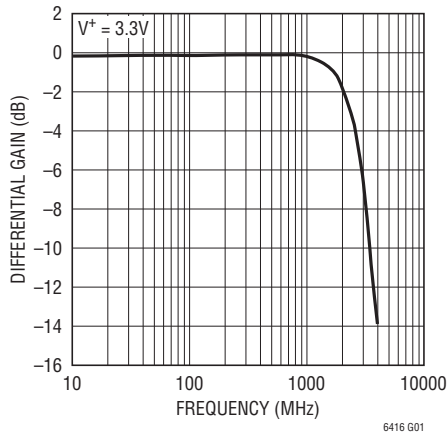
at these temperatures. The LTC6416I is guaranteed to meet specified performance from -40°C to 85°C .

Note 4: This parameter is pulse tested.

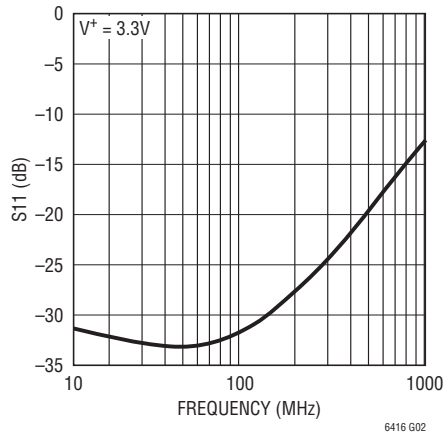
Note 5: Since the LTC6416 is a voltage-output buffer, a resistive load is not required when driving an AD converter. Therefore, typical output power is very small. In order to compare the LTC6416 with amplifiers that require a 50Ω output load, the LTC6416 output voltage swing driving a given R_L is converted to OIP3 and P1dB as if it were driving a 50Ω load. Using this modified convention, $2V_{\text{P-P}}$ is by definition equal to 10dBm, regardless of actual R_L .

TYPICAL PERFORMANCE CHARACTERISTICS

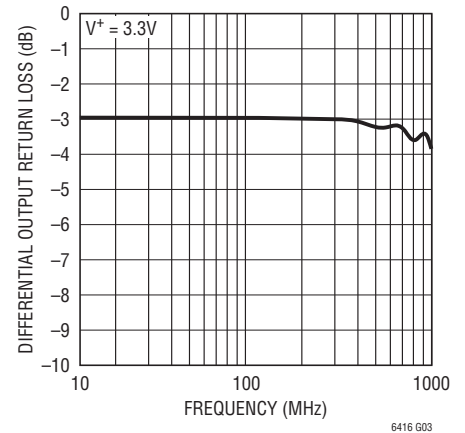
Differential Forward Gain (S21) vs Frequency



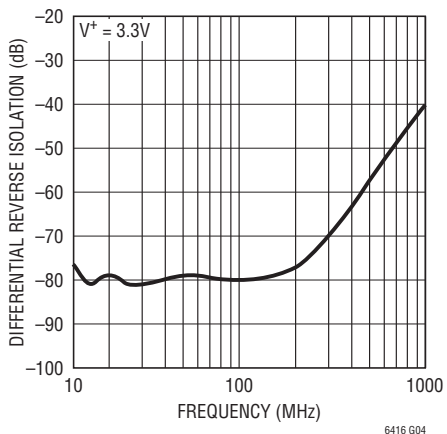
Differential Input Return Loss (S11) vs Frequency



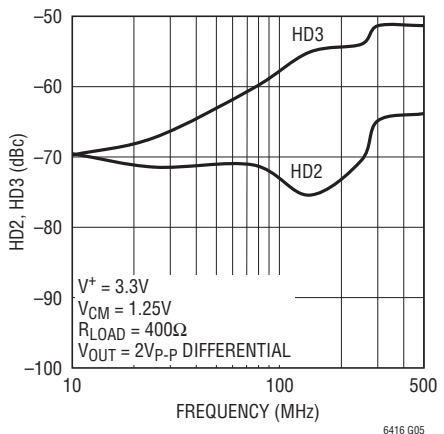
Differential Output Return Loss (S22) vs Frequency



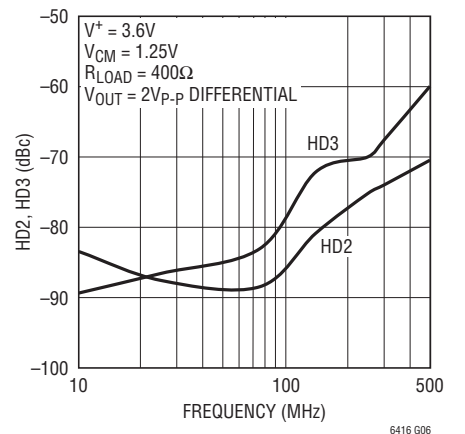
Differential Reverse Isolation (S12) vs Frequency



Second and Third Harmonic Distortion vs Frequency

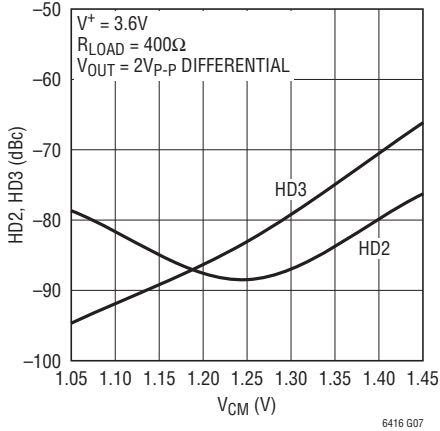


Second and Third Harmonic Distortion vs Frequency

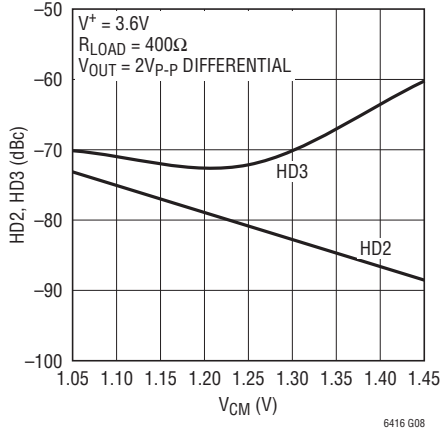


TYPICAL PERFORMANCE CHARACTERISTICS

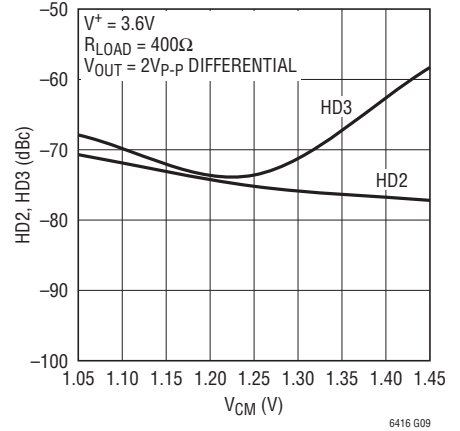
Second and Third Harmonic Distortion vs Output Common Mode Voltage (75MHz)



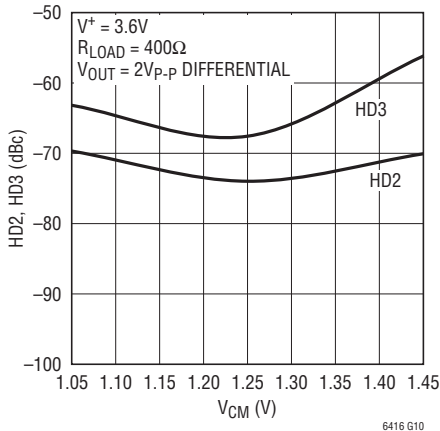
Second and Third Harmonic Distortion vs Output Common Mode Voltage (140MHz)



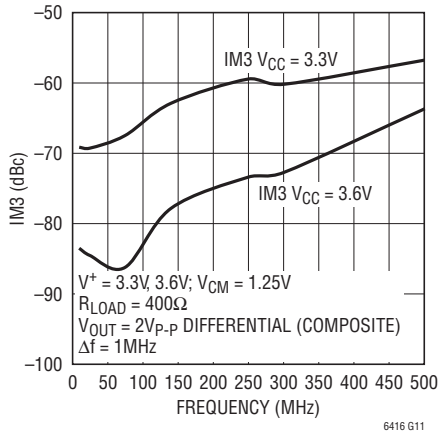
Second and Third Harmonic Distortion vs Output Common Mode Voltage (250MHz)



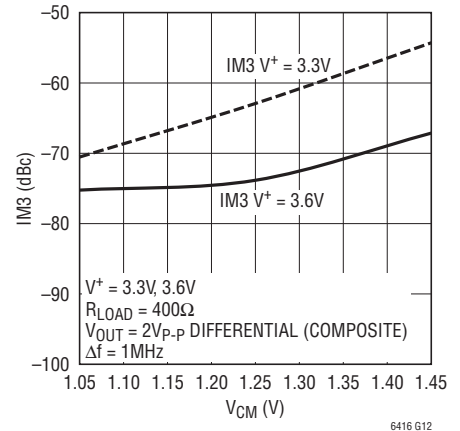
Second and Third Harmonic Distortion vs Output Common Mode Voltage (300MHz)



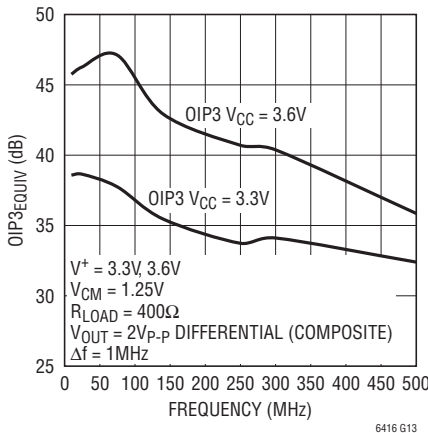
Third Order Intermodulation Distortion (IM3) vs Frequency and Supply Voltage



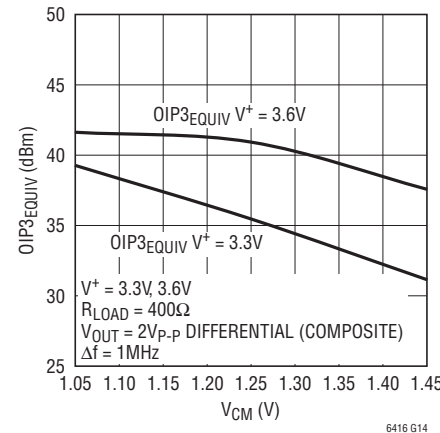
Third Order Intermodulation Distortion (IM3) vs Output Common Mode Voltage (140MHz)



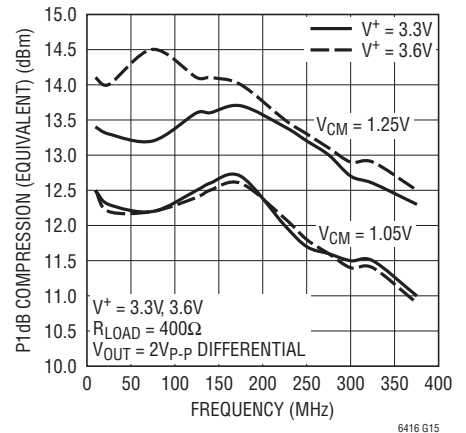
Output Third Order Intercept (OIP3_EQUIV) vs Frequency and Supply Voltage



Output Third Order Intercept (OIP3_EQUIV) vs Output Common Mode Voltage and Supply Voltage (140MHz)

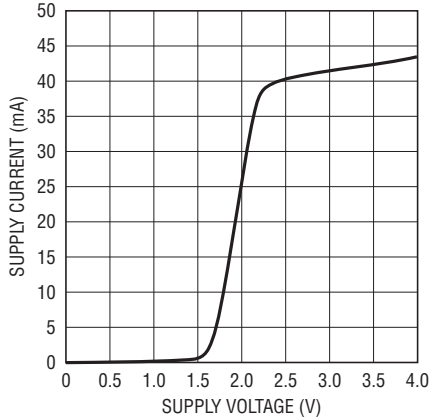


Output 1dB Compression (Equivalent) vs Frequency, V_CM and Supply Voltage

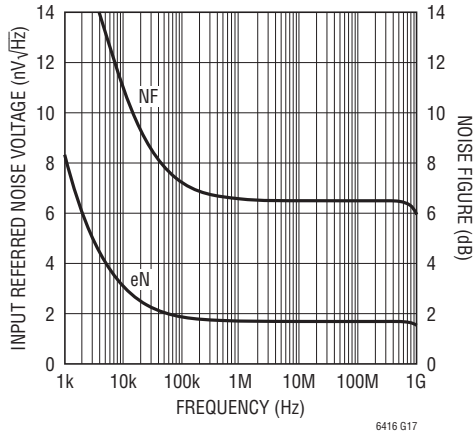


TYPICAL PERFORMANCE CHARACTERISTICS

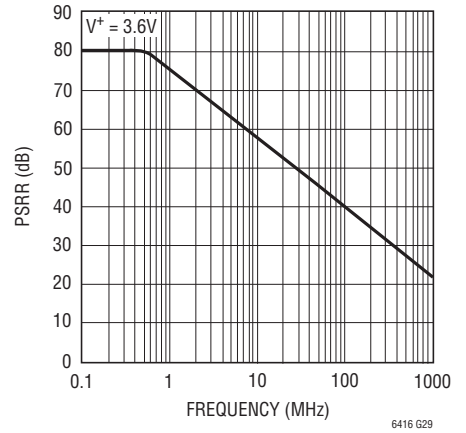
Supply Current vs Supply Voltage



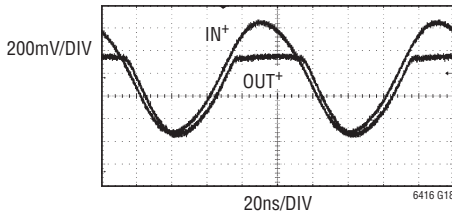
Noise Figure and Input Referred Noise Voltage vs Frequency



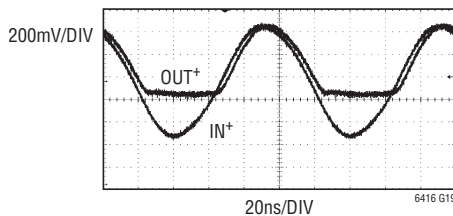
PSRR vs Frequency



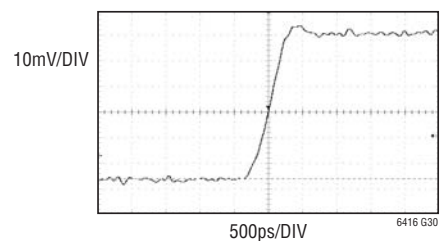
Positive Overdrive Recovery (V_{CLHI} Pin)



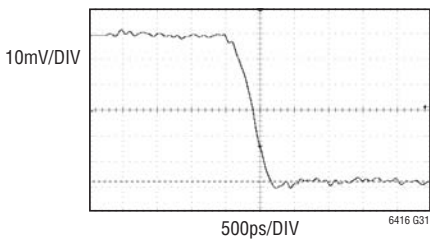
Negative Overdrive Recovery (V_{CLLO} Pin)



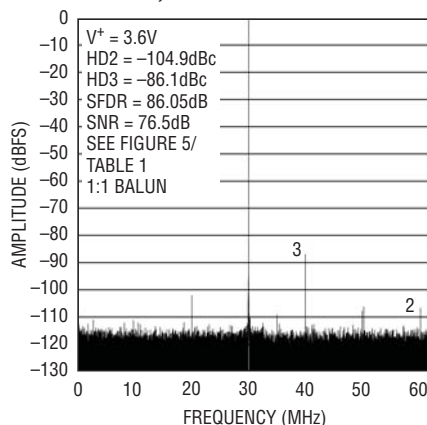
Small Signal Transient Response, Rising Edge



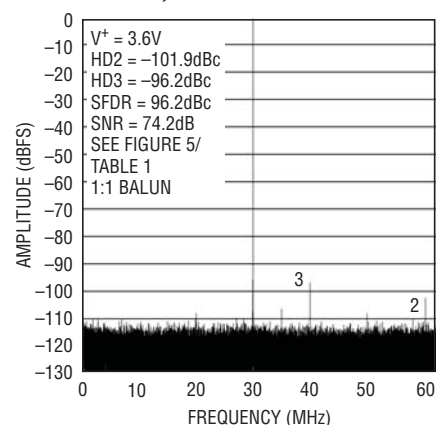
Small Signal Transient Response, Falling Edge



LTC6416 Driving LTC2208 16-Bit ADC, 64K Point FFT, $f_{IN} = 30\text{MHz}$, -1dBFS , $\text{PGA} = 0$

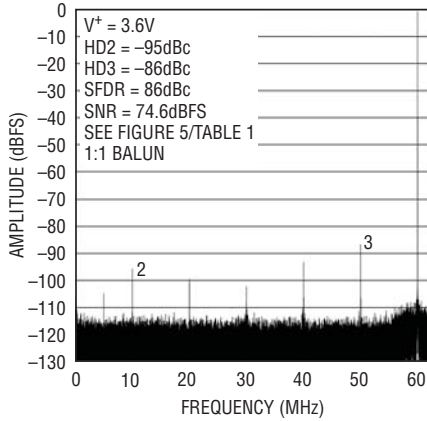


LTC6416 Driving LTC2208 16-Bit ADC, 64K Point FFT, $f_{IN} = 30\text{MHz}$, -1dBFS , $\text{PGA} = 1$



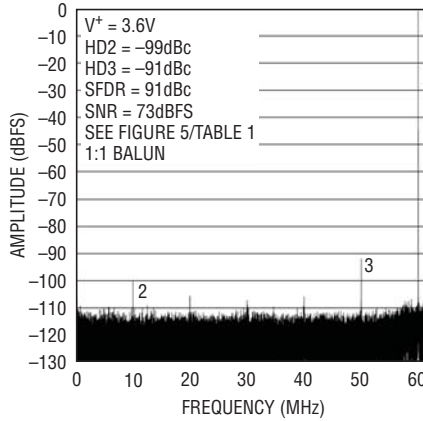
TYPICAL PERFORMANCE CHARACTERISTICS

LTC6416 Driving LTC2208 16-Bit ADC, 64K Point FFT, $f_{IN} = 70\text{MHz}$, -1dBFS, PGA = 0



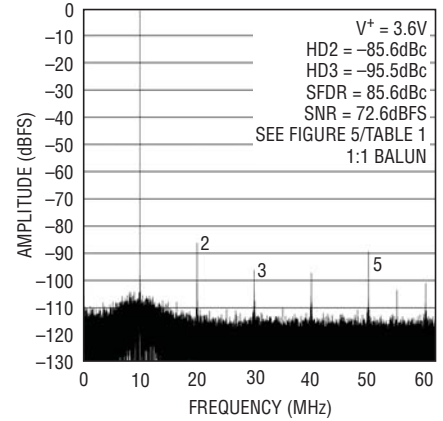
6416 G22

LTC6416 Driving LTC2208 16-Bit ADC, 64K Point FFT, $f_{IN} = 70\text{MHz}$, -1dBFS, PGA = 1



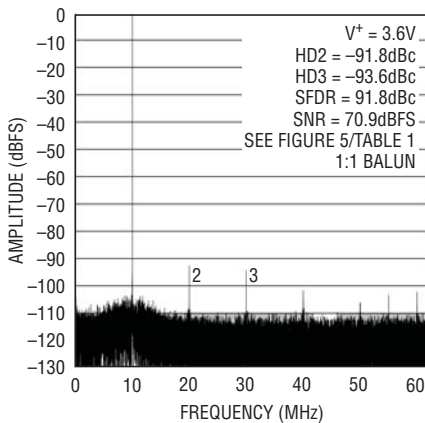
6416 G23

LTC6416 Driving LTC2208 16-Bit ADC, 64K Point FFT, $f_{IN} = 140\text{MHz}$, -1dBFS, PGA = 0



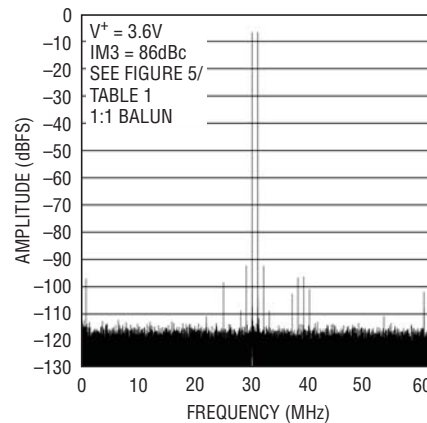
6416 G24

LTC6416 Driving LTC2208 16-Bit ADC, 64K Point FFT, $f_{IN} = 140\text{MHz}$, -1dBFS, PGA = 1



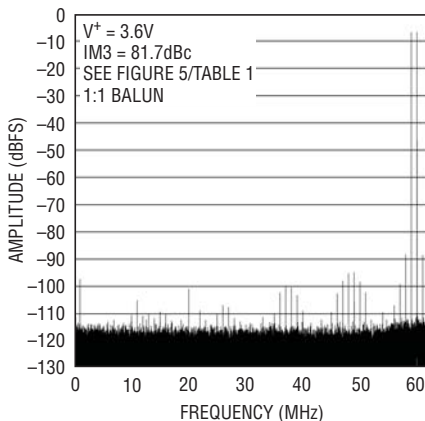
6416 G25

LTC6416 Driving LTC2208 16-Bit ADC, 64K Point FFT, $f_{IN} = 30\text{MHz}$ and 31MHz , -7dBFS/Tone, PGA = 0



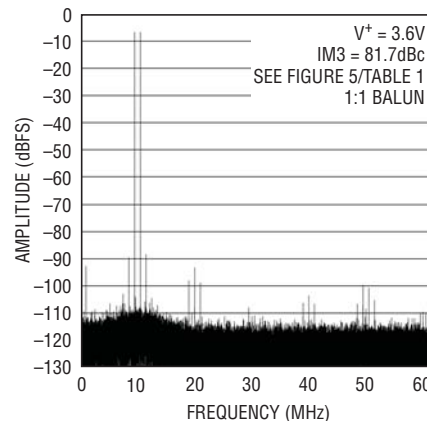
6416 G26

LTC6416 Driving LTC2208 16-Bit ADC, 64K Point FFT, $f_{IN} = 70\text{MHz}$ and 71MHz , -7dBFS/Tone, PGA = 0



6416 G27

LTC6416 Driving LTC2208 16-Bit ADC, 64K Point FFT, $f_{IN} = 139.5\text{MHz}$ and 140.5MHz , -7dBFS/Tone, PGA = 0



6416 G28

PIN FUNCTIONS

V_{CM} (Pin 1): This pin sets the output common mode voltage seen at OUT⁺ and OUT⁻ by driving IN⁺ and IN⁻ through an internal buffer with a high output resistance of 6k. The V_{CM} pin has a Thevenin equivalent resistance of approximately 3.8k and can be overdriven by an external voltage. If no voltage is applied to V_{CM}, it will float to a default voltage of approximately 1.25V on a 3.3V supply or 1.36V on a 3.6V supply. The V_{CM} pin should be bypassed with a high-quality ceramic bypass capacitor of at least 0.1μF.

CLHI (Pin 2): High Side Clamp Voltage. The voltage applied to the CLHI pin defines the upper voltage limit of the OUT⁺ and OUT⁻ pins. This voltage should be set at least 300mV above the upper voltage range of the driven ADC. On a 3.3V supply, the CLHI pin will float to a 2.23V default voltage. On a 3.6V supply, the CLHI pin will float to a 2.45V default voltage. CLHI has a Thevenin equivalent of approximately 4.1kΩ and can be overdriven by an external voltage. The CLHI pin should be bypassed with a high-quality ceramic bypass capacitor of at least 0.1μF.

IN⁺, IN⁻ (Pins 3, 4): Non-inverting and inverting input pins of the buffer, respectively. These pins are high impedance, approximately 6kΩ. If AC-coupled, these pins will self bias to the voltage present at the V_{CM} pin.

CLLO (Pin 5): Low Side Clamp Voltage. The voltage applied to the CLLO pin defines the lower voltage limit of the OUT⁺ and OUT⁻ pins. This voltage should be set at least 300mV below the lower voltage range of the driven

ADC. On a 3.3V supply, the CLLO pin will float to a 0.25V default voltage. On a 3.6V supply, the CLLO pin will float to a 0.265V default voltage. CLLO has a Thevenin equivalent resistance of approximately 2.3k and can be overdriven by an external voltage. The CLLO pin should be bypassed with a high quality ceramic bypass capacitor of at least 0.1μF.

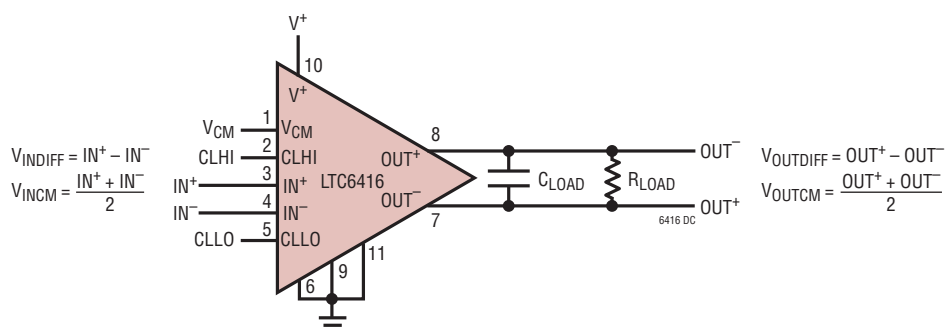
GND (Pins 6, 9, 11): Negative power supply, normally tied to ground. Both pins and the exposed paddle must be tied to the same voltage. GND may be tied to a voltage other than ground as long as the voltage between V⁺ and GND is 2.7V to 4V. If the GND pins are not tied to ground, bypass them with 680pF and 0.1μF capacitors as close to the package as possible.

OUT⁻, OUT⁺ (Pins 7, 8): Outputs. The LTC6416 outputs are low impedance. Each output has an output impedance of approximately 9Ω at DC.

V⁺ (Pin 10): Positive Power Supply. Typically 3.3V to 3.6V. Split supplies are possible as long as the voltage between V⁺ and GND is 2.7V to 4V. Bypass capacitors of 680pF and 0.1μF as close to the part as possible should be used between the supplies.

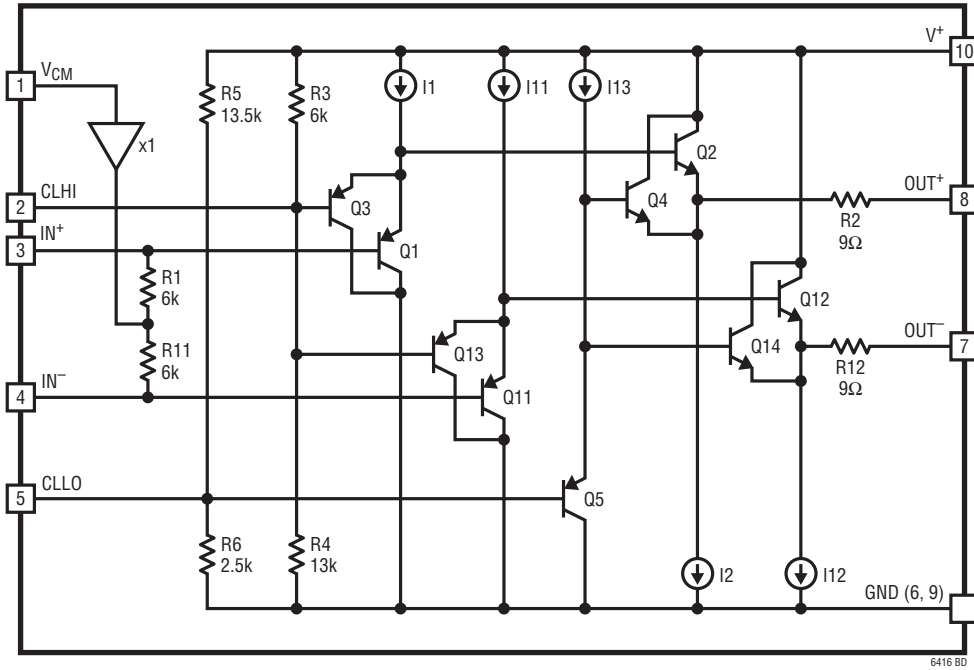
Exposed Pad (Pin 11): Ground. The exposed pad must be soldered to the printed circuit board ground plane for good heat transfer. **If GND is a voltage other than ground, the Exposed Pad must be connected to a plane with the same potential as the GND pins – Not to the system ground plane.**

DC TEST CIRCUIT SCHEMATIC



BLOCK DIAGRAM

LTC6416 Simplified Schematic



6416 BD

APPLICATIONS INFORMATION

Circuit Operation

The LTC6416 is a low noise and low distortion fully differential unity-gain ADC driver with operation from DC to 2GHz (–3dB bandwidth), a differential input impedance of 12k Ω , and a differential output impedance of 18 Ω . The LTC6416 is composed of a fully differential buffer with output common mode voltage control circuitry and high speed voltage-limiting clamps at the output. Small output resistors of 9 Ω improve the circuit stability over various load conditions. They also simplify possible external filtering options, which are often desirable when the load is an ADC. Lowpass or bandpass filters are easily implemented with just a few external components. The LTC6416 is very flexible in terms of I/O coupling. It can be AC- or DC-coupled at the inputs, the outputs or both. When using the LTC6416 with DC-coupled inputs, best performance is obtained with an input common mode voltage between 1V and 1.5V. For AC-coupled operation, the LTC6416 will take the voltage applied to the V_{CM} pin and use it to bias the inputs so that the output common mode voltage equals V_{CM} , thus no external circuitry is needed. The V_{CM} pin has been designed to directly interface with the V_{CM} pin found on Linear Technology's 16-, 14- and 12-bit high speed ADC families.

Input Impedance and Matching

The LTC6416 has a high differential input impedance of 12k Ω . The differential inputs may need to be terminated to a lower value impedance, e.g. 50 Ω , in order to provide an impedance match for the source. Figure 1 shows input

matching using a 1:1 balun, while Figure 2 shows matching using a 1:4 balun. These circuits provide a wideband impedance match. The balun and matching resistors must be placed close to the input pins in order to minimize the rejection due to input mismatch. In Figure 1, the capacitor center-tapping the two 24.9 Ω resistors improves high frequency common mode rejection. As an alternative to this wideband approach, a narrowband impedance match can be used at the inputs of the LTC6416 for frequency selection and/or noise reduction.

The noise performance of the LTC6416 also depends upon the source impedance and termination. For example, the input 1:4 balun in Figure 2 improves SNR by adding 6dB of voltage gain at the inputs. A trade-off between gain and noise is obvious when constant noise figure circle and constant gain circle are plotted within the same input Smith Chart. This technique can be used to determine the optimal source impedance for a given gain and noise requirement.

Output Match and Filter

The LTC6416 provides a source resistance of 9 Ω at each output. For testing purposes, Figure 3 and Figure 4 show the LTC6416 driving a differential 400 Ω load impedance using a 1:1 or 1:4 balun, respectively.

The LTC6416 can drive an ADC directly without external output impedance matching, but improved performance can usually be obtained with the addition of a few external components. Figure 5 shows a typical topology used for driving the LTC2208 16-bit ADC.

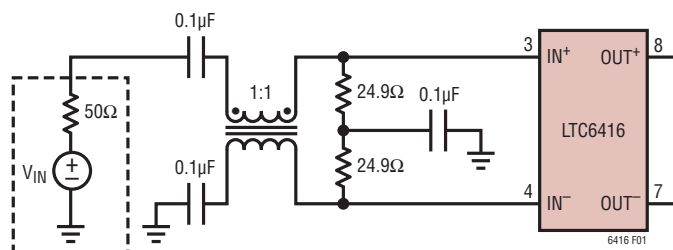


Figure 1. Input Termination for Differential 50 Ω Input Impedance Using a 1:1 Balun

APPLICATIONS INFORMATION

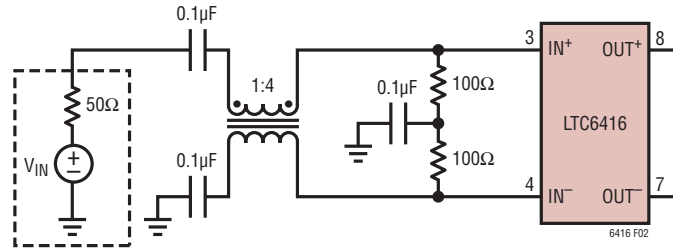


Figure 2. Input Termination for Differential 50Ω Input Impedance Using a 1:4 Balun

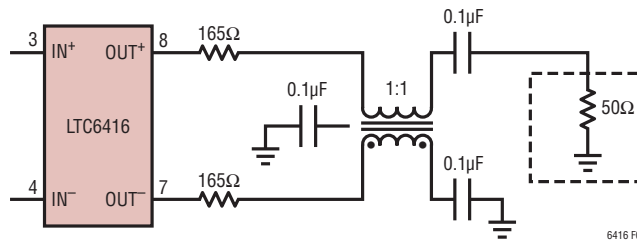


Figure 3. Output Termination for Differential 400Ω Load Impedance Using a 1:1 Balun

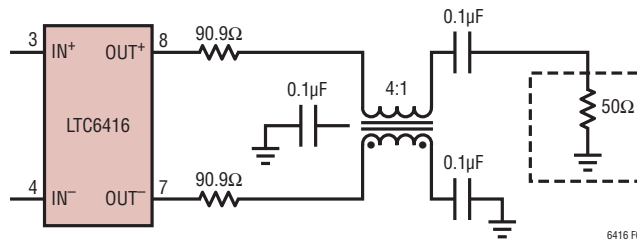


Figure 4. Output Termination for Differential 400Ω Load Impedance Using a 4:1 Balun

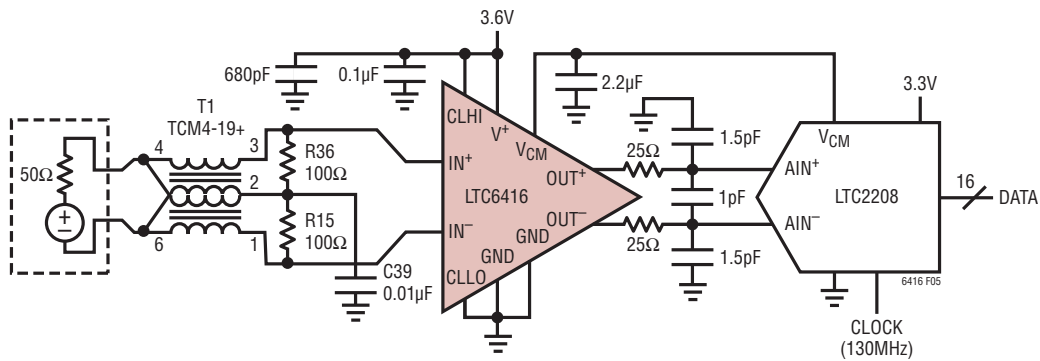


Figure 5. DC1257B Simplified Schematic with Suggested Output Termination for Driving an LTC2208 16-Bit ADC at 140MHz

APPLICATIONS INFORMATION

As seen in Table 1, suggested component values for the filter will change for differing IF frequencies.

Table 1.

INPUT FREQUENCY	LTC6416 OUTPUT RESISTORS	FILTERING CAPACITORS
30MHz	50 Ω	5.6pF/6.8pF/5.6pF
70MHz	25 Ω	5.6pF/6.8pF/5.6pF
140MHz	25 Ω	1.5pF/1pF/1.5pF
250MHz	5 Ω	-/-

Output Common Mode Adjustment

The output common mode voltage is set by the V_{CM} pin. Because the input common mode voltage is approximately the same as the output common mode voltage, both are approximately equal to V_{CM} . The V_{CM} pin has a Thevenin equivalent resistance of 3.8k and can be overdriven by an external voltage. The V_{CM} pin floats to a default voltage of 1.25V on a 3.3V supply and 1.36V on a 3.6V supply. The output common mode voltage is capable of tracking V_{CM} in a range from 0.34V to 2.16V on a 3.3V supply. The V_{CM} pin can be floated, but it should always be bypassed close to the LTC6416 with a 0.1 μ F bypass capacitor to ground. When interfacing with A/D converters such as the LTC22xx families, the V_{CM} pin can be connected to the V_{CM} output pin of the ADC, as shown in Figure 5.

CLLO and CLHI Pins

The CLLO and CLHI pins are used to set the clamping voltage for high speed internal circuitry. This circuitry limits the single-ended minimum and maximum voltage excursion seen at each of the outputs. This feature is extremely important in applications with input signals having very large peak-to-average ratios such as cellular basestation receivers. If a very large peak signal arrives at the LTC6416, the voltages applied to the CLLO and CLHI pins will determine the minimum and maximum output swing respectively. Once the input signal returns to the normal operating range, the LTC6416 returns to linear operation within 5ns. Both CLLO and CLHI are high impedance inputs. CLLO has an input impedance of 2.3k, while CLHI has an input impedance of 4.1k. On a 3.3V supply, CLLO self-biases to 0.25V while CLHI self-biases

to 2.23V. On a 3.6V supply, CLLO self-biases to 0.265V while CLHI self-biases to 2.45V. Both CLLO and CLHI pins should be bypassed with a 0.1 μ F capacitor as close to the LTC6416 as possible.

Interfacing the LTC6416 to A/D Converters

The LTC6416 has been specifically designed to interface directly with high speed A/D converters. It is possible to drive the ADC directly from the LTC6416. In practice, however, better performance may be obtained by adding a few external components at the output of the LTC6416. Figure 5 shows the LTC6416 being driven by a 1:8 transformer which provides 9dB of voltage gain while also performing a single-ended to differential conversion. The differential outputs of the LTC6416 are lowpass filtered, then drive the differential inputs of the LTC2208 ADC. In many applications, an anti-alias filter like this is desirable to limit the wideband noise of the amplifier. This is especially true in high performance 16-bit designs. The minimum recommended network between the LTC6416 and the ADC is simply two 5 Ω series resistors, which are used to help eliminate resonances associated with the stray capacitance of PCB traces and the stray inductance of the internal bond wires at the ADC input, and the driver output pins.

Single-Ended Signals

The LTC6416 has not been designed to convert single-ended signals to differential signals. A single-ended input signal can be converted to a differential signal via a balun connected to the inputs of the LTC6416.

Power Supply Considerations

For best linearity, the LTC6416 should have a positive supply of $V^+ = 3.6V$. The LTC6416 has an internal edge-triggered supply voltage clamp. The timing mechanism of the clamp enables the LTC6416 to withstand ESD events. This internal clamp is also activated by voltage overshoot and rapid slew rate on the positive supply V^+ pin. The LTC6416 should not be hot-plugged into a powered socket. Bypass capacitors of 680pF and 0.1 μ F should be placed to the V^+ pin, as close as possible to the LTC6416.

APPLICATIONS INFORMATION

Test Circuits

Due to the fully differential design of the LTC6416 and its usefulness in applications both with and without ADCs, two test circuits are used to generate the information in this data sheet. Test circuit A is Demo Board DC1287A, a two-port demonstration circuit for the LTC6416. The board layout and the schematic are shown in Figures 6 and 7. This circuit includes input and output 1:1 baluns for single-ended-to-differential conversion, allowing direct analysis using a 2-port network analyzer. In this circuit implementation, there are series resistors at the

output to present the LTC6416 with a 382Ω differential load, thereby optimizing distortion performance. Including the 1:1 input and output baluns, the -3dB bandwidth is approximately 2GHz.

Test circuit B is Demo Circuit DC1257B. It consists of an LTC6416 driving an LTC2208 ADC. It is intended for use in conjunction with demo circuit DC890B (computer interface board) and proprietary Linear Technology evaluation software to evaluate the performance of both parts together. Both the DC1257B board layout and the schematic can be seen in Figures 8 and 9.

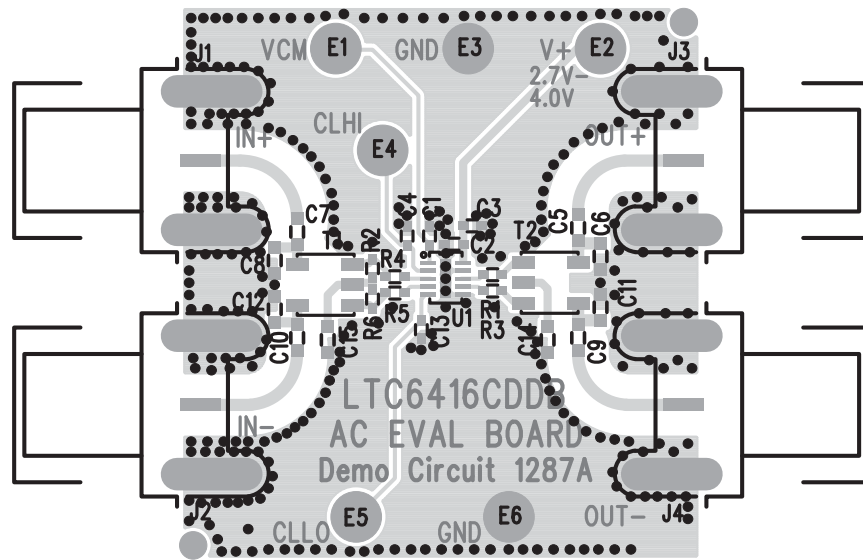


Figure 6. Demo Board DC1287A Layout

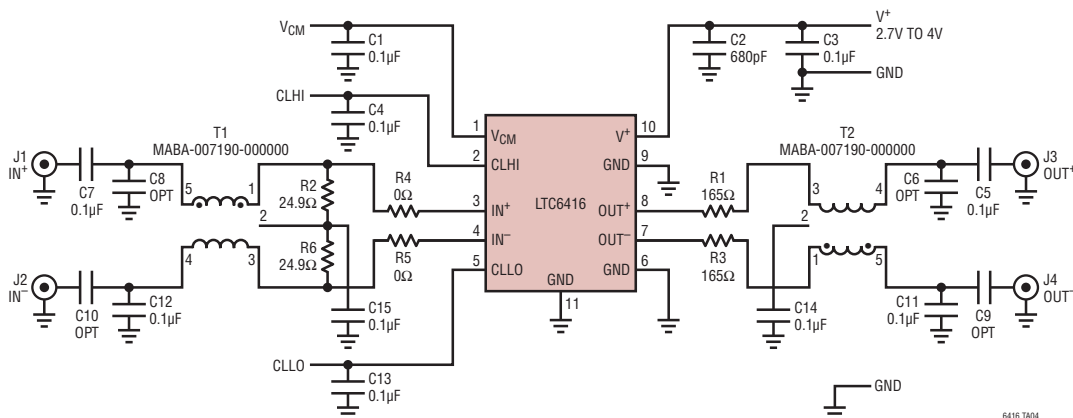


Figure 7. Demo Board DC1287A Schematic (Test Circuit A)

APPLICATIONS INFORMATION

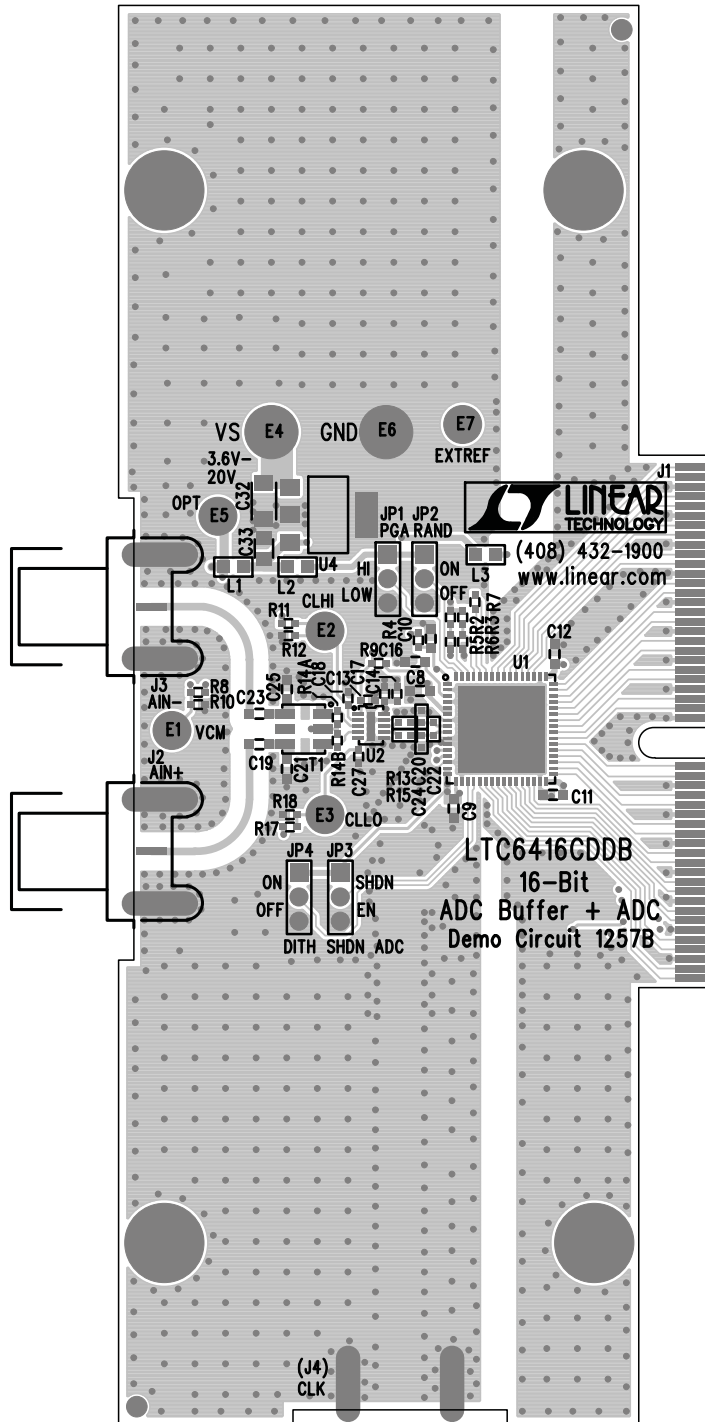


Figure 8. Demo Board DC1257B Layout

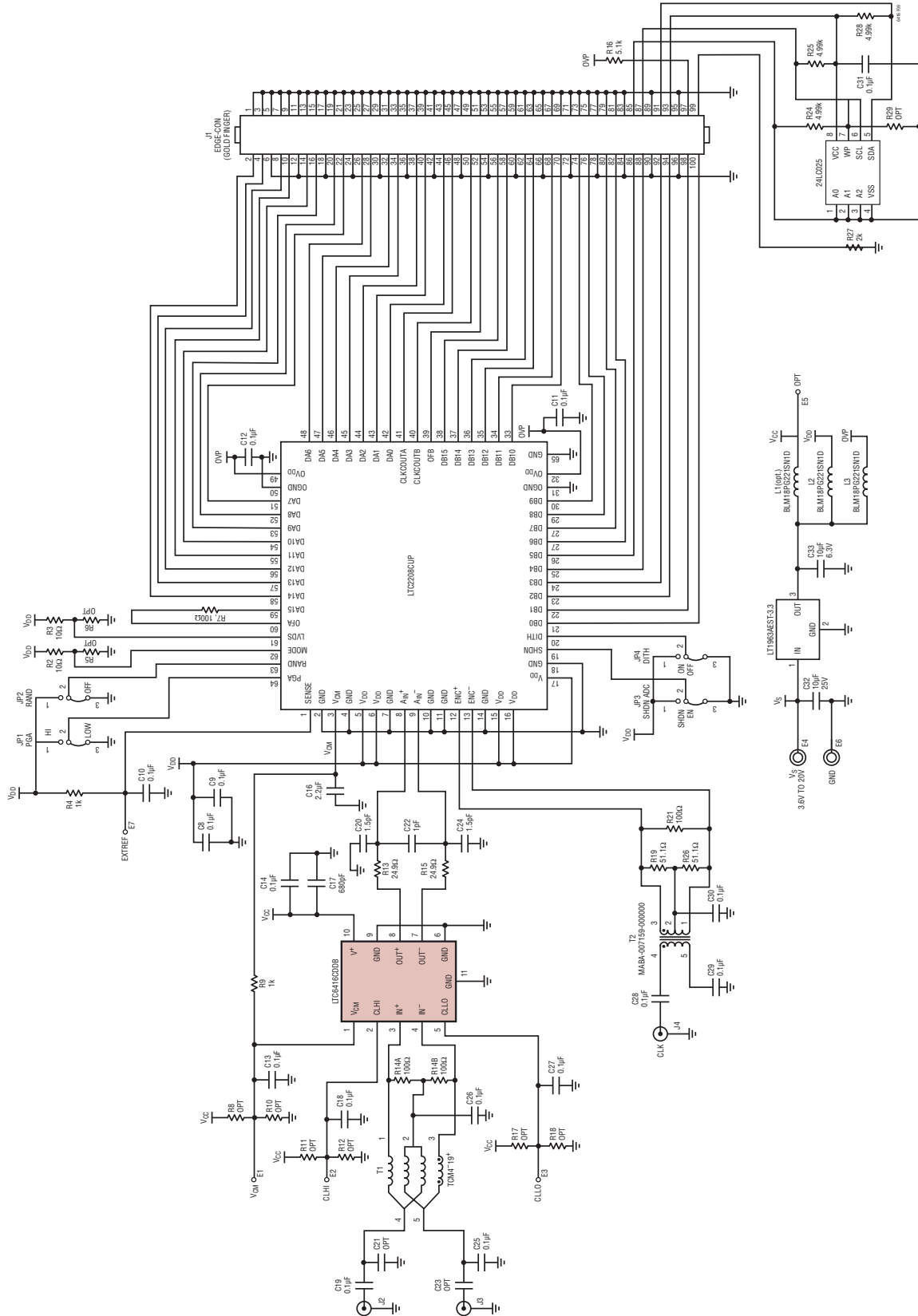
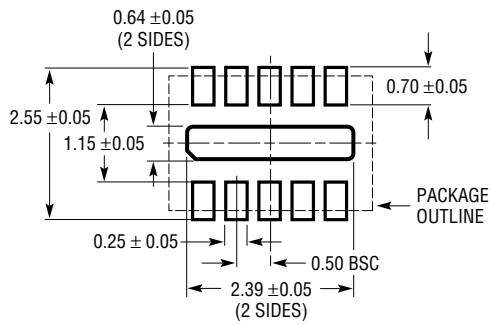


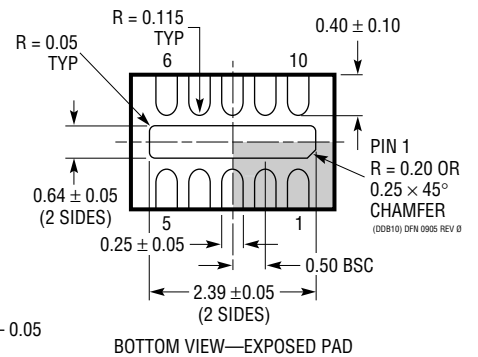
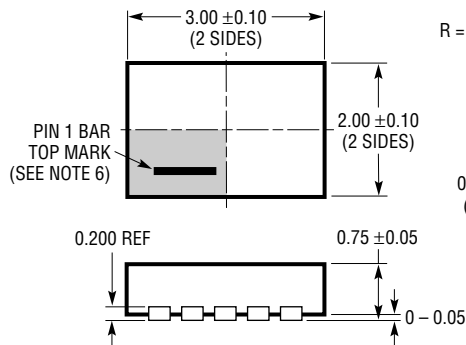
Figure 9. Demo Board DC1257B Schematic (Test Circuit B)

PACKAGE DESCRIPTION

DDB Package 10-Lead Plastic DFN (3mm × 2mm) (Reference LTC DWG # 05-08-1722 Rev 0)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

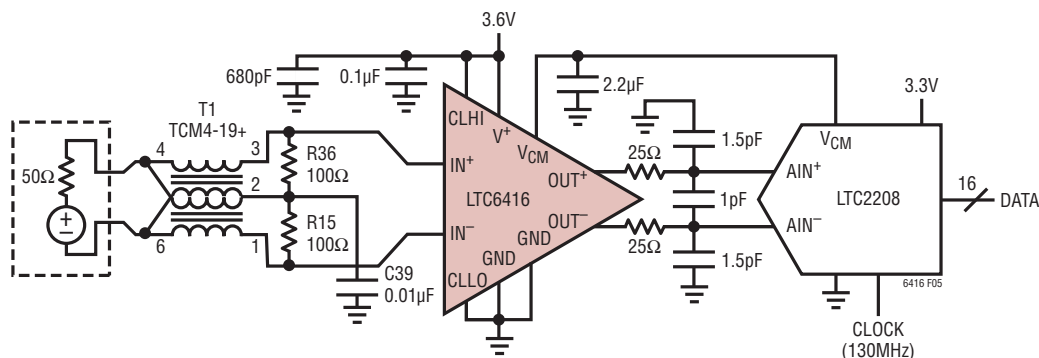


NOTE:

1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

DC1257B Simplified Schematic with Suggested Output Termination for Driving an LTC2208 16-Bit ADC at 140MHz



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Fixed Gain IF Amplifiers/ADC Drivers		
LT1993-2/LT1993-4/ LT1993-10	800MHz Differential Amplifier/ADC Drivers	-72dBc IM3 at 70MHz 2V _{p-p} Composite, A _V = 2V/V, 4V/V, 10V/V
LTC6400-8/LTC6400-14/ LTC6400-20/LTC6400-26	1.8GHz Low Noise, Low Distortion Differential ADC Drivers	-71dBc IM3 at 240MHz 2V _{p-p} Composite, I _S = 90mA, A _V = 8dB, 14dB, 20dB, 26dB
LTC6401-8/LTC6401-14/ LTC6401-20/LTC6401-26	1.3GHz Low Noise, Low Distortion Differential ADC Drivers	-74dBc IM3 at 140MHz 2V _{p-p} Composite, I _S = 50mA, A _V = 8dB, 14dB, 20dB, 26dB
LT6402-6/LT6402-12/ LT6402-20	300MHz Differential Amplifier/ADC Drivers	-71dBc IM3 at 20MHz 2V _{p-p} Composite, A _V = 6dB, 12dB, 20dB
LTC6420-XX	Dual 1.8GHz Low Noise, Low Distortion Differential ADC Drivers	Dual Version of the LTC6400-XX, A _V = 8dB, 14dB, 20dB, 26dB
LTC6421-XX	Dual 1.3GHz Low Noise, Low Distortion Differential ADC Drivers	Dual Version of the LTC6401-XX, A _V = 8dB, 14dB, 20dB, 26dB
IF Amplifiers/ADC Drivers with Digitally Controlled Gain		
LT5514	Ultra-Low Distortion IF Amplifier/ADC Driver with Digitally Controlled Gain	OIP3 = 47dBm at 100MHz, Gain Range 10.5dB to 33dB 1.5dB steps
LT5524	Low Distortion IF Amplifier/ADC Driver with Digitally Controlled Gain	OIP3 = 40dBm at 100MHz, Gain Range 4.5dB to 37dB 1.5dB steps
LT5554	High Dynamic Range 7-bit Digitally Controlled IF VGA/ADC Driver	OIP3 = 46dBm at 200MHz, Gain Range 1.725 to 17.6dB 0.125dB steps
Baseband Differential Amplifiers		
LT1994	Low Noise, Low Distortion Differential Amplifier/ADC Driver	16-Bit SNR and SFDR at 1MHz, Rail-to-Rail Outputs
LTC6403-1	Low Noise Rail-to-Rail Output Differential Amplifier/ADC Driver	16-Bit SNR and SFDR at 3MHz, Rail-to-Rail Outputs, e _N = 2.8nV/√Hz
LTC6404-1/LTC6404-2	Low Noise Rail-to-Rail Output Differential Amplifier/ADC Driver	16-Bit SNR and SFDR at 10MHz, Rail-to-Rail Outputs, e _N = 1.5nV/√Hz, LTC6404-1 is unity-gain stable, LTC6404-2 is Gain-of-2 Stable
LTC6406	3GHz Rail-to-Rail Input Differential Amplifier/ADC Driver	-65dBc IM3 at 50MHz 2V _{p-p} Composite, Rail-to-Rail Inputs, e _N = 1.6nV/√Hz, 18mA
LT6411	Low Power Differential ADC Driver/Dual Selectable Gain Amplifier	-83dBc IM3 at 70MHz 2V _{p-p} Composite, A _V = 1, -1 or 2, 16mA, Excellent for Single-Ended to Differential Conversion

6416f

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