50Ω Gain Block IF Amplifier

FEATURES

- **20MHz to 1700MHz Bandwidth**
- **15.5dB Power Gain**
- **47dBm OIP3 at 240MHz into a 50Ω Load**
- **NF = 3.33dB at 240MHz**
- **1nV/√Hz Total Input Noise**
- **S11 < –15dB Up to 1.2GHz**
- **S22 < –15dB Up to 1.2GHz**
- **>2V_{P-P} Linear Output Swing**
- **P1dB = 20.6dBm**
- **DC Power = 450mW**
- 50Ω Single-Ended Operation
- Insensitive to V_{CC} Variation
- A-Grade 100% OIP3 Tested at 240MHz
- Input/Output Internally Matched to 50Ω
- Single 5V Supply
- Unconditionally Stable

APPLICATIONS

- Single-Ended IF Amplifier
- ADC Driver
- CATV

DESCRIPTION

The LTC®6431-15 is a gain-block amplifier with excellent linearity at frequencies beyond 1000MHz and with low associated output noise.

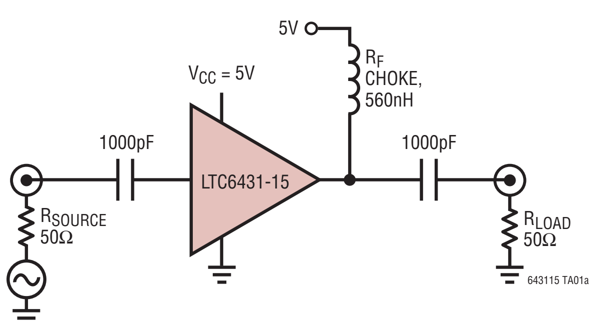
The unique combination of high linearity, low noise and low power dissipation make this an ideal candidate for many signal-chain applications. The LTC6431-15 is easy to use, requiring a minimum of external components. It is internally input/output matched to 50Ω and it draws only 90mA from a single 5V supply.

On-chip bias and temperature compensation maintain performance over environmental changes.

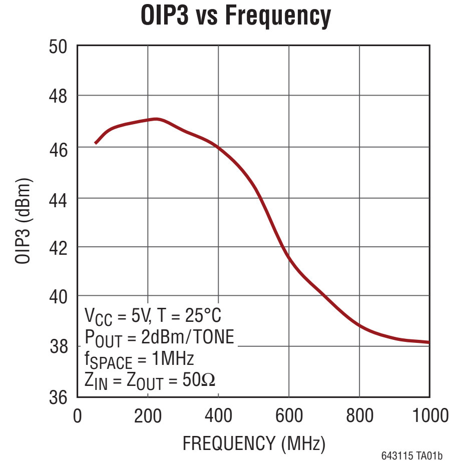
The LTC6431-15 uses a high performance SiGe BiCMOS process for excellent repeatability compared with similar GaAs amplifiers. All A-grade LTC6431-15 devices are tested and guaranteed for OIP3 at 240MHz. The LTC6431-15 is housed in a 4mm × 4mm 24-lead QFN package with an exposed pad for thermal management and low inductance.

TYPICAL APPLICATION

Single-Ended IF Amplifier



OIP3 vs Frequency

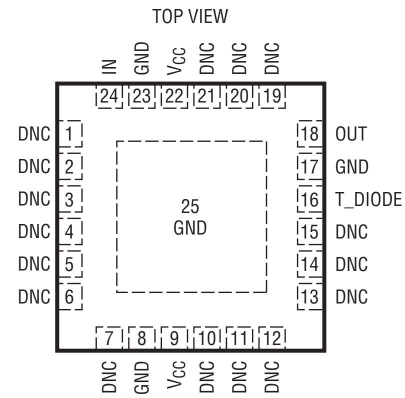


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V_{CC} to GND)...........................5.5V
Amplifier Output Current (OUT) 105mA
RF Input Power, Continuous, 50Ω (Note 2)..........15dBm
RF Input Power, 100μs Pulse, 50Ω (Note 2) 20dBm
Operating Case Temperature
Range (T_{CASE})..–40°C to 85°C
Storage Temperature Range ....–65°C to 150°C
Junction Temperature (T_J) .... 150°C

PIN CONFIGURATION



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JC} = 54°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6431AIUF-15#PBF	LTC6431AIUF-15#TRPBF	43115	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C
LTC6431BIUF-15#PBF	LTC6431BIUF-15#TRPBF	43115	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 50Ω. Typical measured DC electrical performance using Test Circuit A.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_S	Operating Supply Range			4.75	5.0	5.25	V
$I_{S,TOT}$	Total Supply Current	All V_{CC} Pins Plus OUT	 ●	75 67	85.1	100 112	mA mA
$I_{S,OUT}$	Total Supply Current to OUT Pin	Current to OUT	 ●	62 55	71	92 95	mA mA
$I_{CC,OUT}$	Current to V_{CC} Pin	Either V_{CC} Pin May Be Used	 ●	12 12.5	14	16 16.5	mA mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C (Note 3), V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 50Ω, unless otherwise noted. Measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding (Note 4).

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Small Signal								
BW	–3dB Bandwidth	De-Embedded to Package (Low Frequency Cutoff 20MHz)				2000		MHz
S11	Input Return Loss, 20MHz to 2000MHz	De-Embedded to Package				–10		dB
S21	Forward Power Gain, 50MHz to 300MHz	De-Embedded to Package				15.5		dB
S12	Reverse Isolation, 20MHz to 3000MHz	De-Embedded to Package				–19		dB
S22	Output Return Loss, 20MHz to 1700MHz	De-Embedded to Package				–10		dB
Frequency = 50MHz								
S21	Power Gain	De-Embedded to Package				15.5		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade			46.0 45.0		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade			–88.0 –86.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 6dBm				–58.0		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 6dBm				–88.0		dBc
P1dB	Output 1dB Compression Point					20.5		dBm
NF	Noise Figure	De-Embedded to Package				3.06		dB
Frequency = 140MHz								
S21	Power Gain	De-Embedded to Package				15.5		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade			47.0 46.0		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade			–90.0 –88.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 6dBm				–58.0		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 6dBm				–88.0		dBc
P1dB	Output 1dB Compression Point					20.7		dBm
NF	Noise Figure	De-Embedded to Package				3.20		dB
Frequency = 240MHz								
S21	Power Gain	De-Embedded to Package		 ●	14.5 14.2	15.6	16.5 16.7	dB dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δ_f = 8MHz	A-Grade B-Grade		44.0	47.0 45.5		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δ_f = 8MHz	A-Grade B-Grade		–84	–90.0 –87.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 6dBm				–59.0		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 6dBm				–88.0		dBc
P1dB	Output 1dB Compression Point					20.6		dBm
NF	Noise Figure	De-Embedded to Package				3.33		dB

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C (Note 3), V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 50Ω, unless otherwise noted. Measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Frequency = 300MHz							
S21	Power Gain	De-Embedded to Package			15.5		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade		46.5 45.5		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade		–89.0 –87.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 6dBm			–60.0		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 6dBm			–86.0		dBc
P1dB	Output 1dB Compression Point				20.6		dBm
NF	Noise Figure	De-Embedded to Package			3.41		dB
Frequency = 380MHz							
S21	Power Gain	De-Embedded to Package			15.4		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade		46.0 45.0		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade		–88.0 –86.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 6dBm			–57.0		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 6dBm			–87.0		dBc
P1dB	Output 1dB Compression Point				20.6		dBm
NF	Noise Figure	De-Embedded to Package			3.48		dB
Frequency = 500MHz							
S21	Power Gain	De-Embedded to Package			15.3		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade		44.5 43.5		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade		–85.0 –83.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 6dBm			–55.6		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 6dBm			–77.0		dBc
P1dB	Output 1dB Compression Point				20.6		dBm
NF	Noise Figure	De-Embedded to Package			3.60		dB
Frequency = 600MHz							
S21	Power Gain	De-Embedded to Package			15.3		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade		41.5 40.5		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade		–79.0 –77.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 6dBm			–53.6		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 6dBm			–69.0		dBc
P1dB	Output 1dB Compression Point				20.6		dBm
NF	Noise Figure	De-Embedded to Package			3.67		dB

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C (Note 3), V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 50Ω, unless otherwise noted. Measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding (Note 4).

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Frequency = 700MHz								
S21	Power Gain	De-Embedded to Package				15.2		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade			40.0 39.0		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade			–76.0 –74.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 6dBm				–51.9		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 6dBm				–69.0		dBc
P1dB	Output 1dB Compression Point					20.3		dBm
NF	Noise Figure	De-Embedded to Package				3.75		dB
Frequency = 800MHz								
S21	Power Gain	De-Embedded to Package				15.2		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade			39.0 38.0		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade			–74 –72		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 6dBm				–49.2		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 6dBm				–65.0		dBc
P1dB	Output 1dB Compression Point					20.1		dBm
NF	Noise Figure	De-Embedded to Package				3.83		dB
Frequency = 900MHz								
S21	Power Gain	De-Embedded to Package				15.1		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade			38.5 37.5		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade			–73.0 –71.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 6dBm				–46.7		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 6dBm				–63.0		dBc
P1dB	Output 1dB Compression Point					19.9		dBm
NF	Noise Figure	De-Embedded to Package				3.90		dB
Frequency = 1000MHz								
S21	Power Gain	De-Embedded to Package				15.0		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade			38.0 37.0		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δ_f = 1MHz	A-Grade B-Grade			–72.0 –70.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 6dBm				–45.0		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 6dBm				–59.0		dBc
P1dB	Output 1dB Compression Point					19.5		dBm
NF	Noise Figure	De-Embedded to Package				3.99		dB

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Guaranteed by design and characterization. This parameter is not tested.

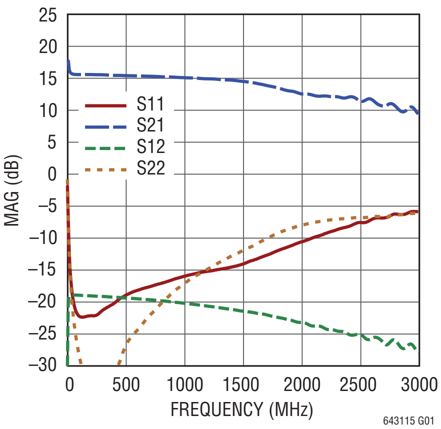
Note 3: The LTC6431-15 is guaranteed functional over the case operating temperature range of –40°C to 85°C.

Note 4: Small-signal parameters S and noise are de-embedded to the package pins, while large-signal parameters are measured directly from the circuit.

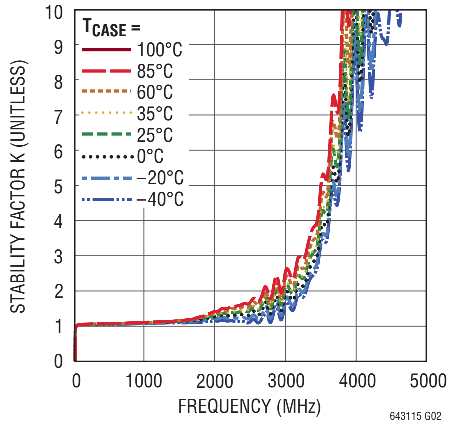
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 5V$, $Z_{SOURCE} = Z_{LOAD} = 50Ω$, unless otherwise noted. Measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding (Note 4).

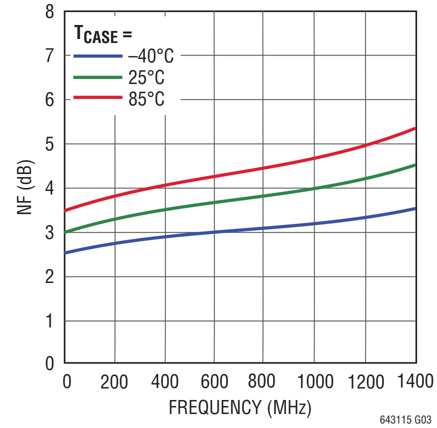
S Parameters vs Frequency



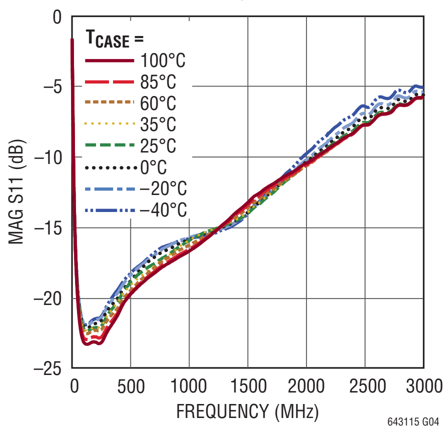
Stability Factor K vs Frequency Over Temperature



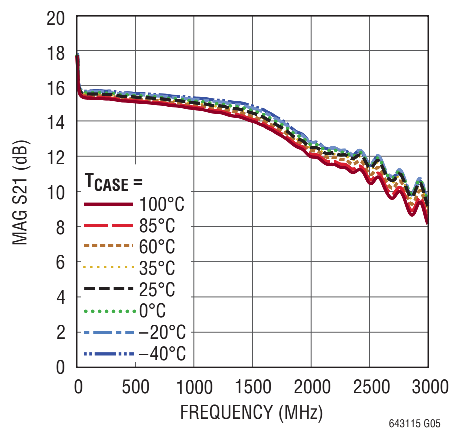
Noise Figure vs Frequency Over Temperature



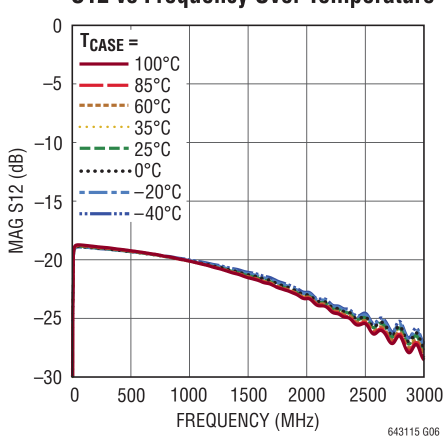
S11 vs Frequency Over Temperature



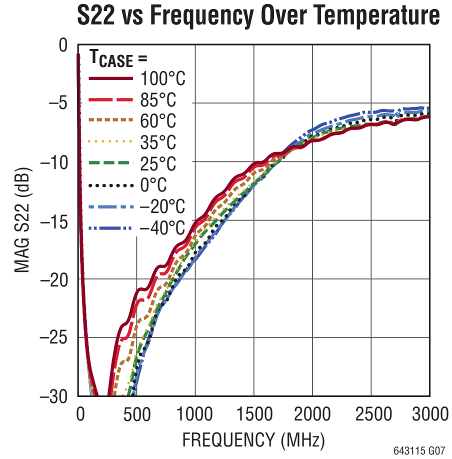
S21 vs Frequency Over Temperature



S12 vs Frequency Over Temperature



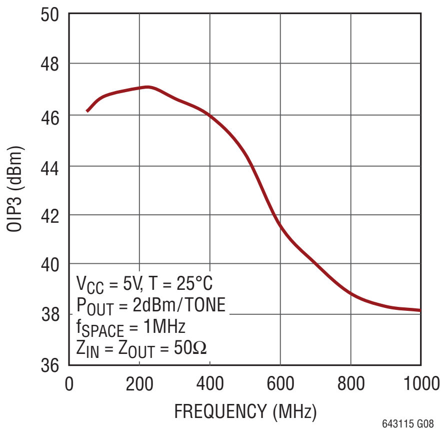
S22 vs Frequency Over Temperature



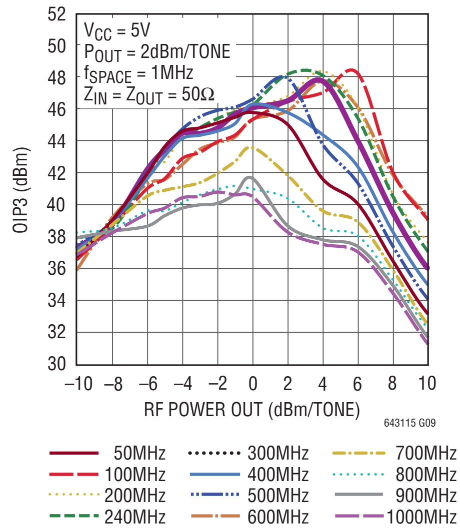
TYPICAL PERFORMANCE CHARACTERISTICS A-Grade

T_A = 25°C, V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 50Ω, unless otherwise noted. Measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding (Note 4).

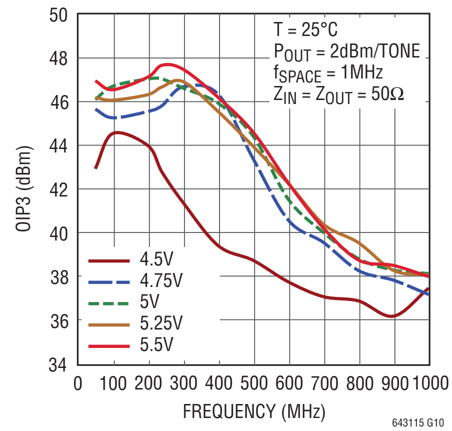
OIP3 vs Frequency



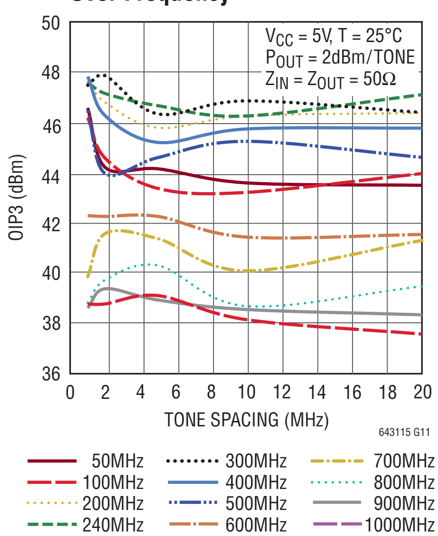
OIP3 vs Power Out Over Frequency



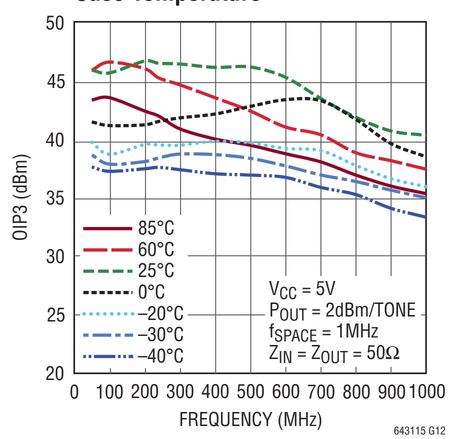
OIP3 vs Frequency Over V_{CC} Voltage



OIP3 vs Tone Spacing Over Frequency



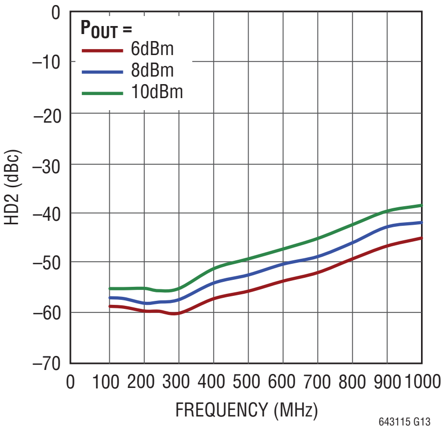
OIP3 vs Frequency Over Case Temperature



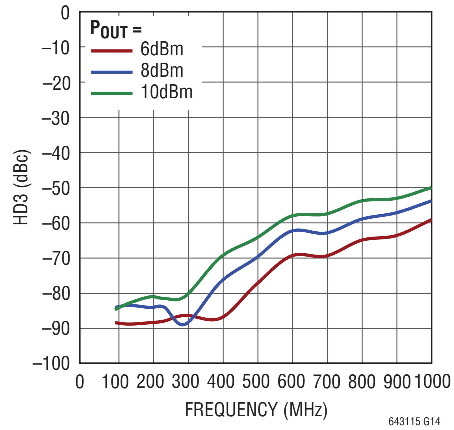
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 5V$, $Z_{SOURCE} = Z_{LOAD} = 50\Omega$, unless otherwise noted. Measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding (Note 4).

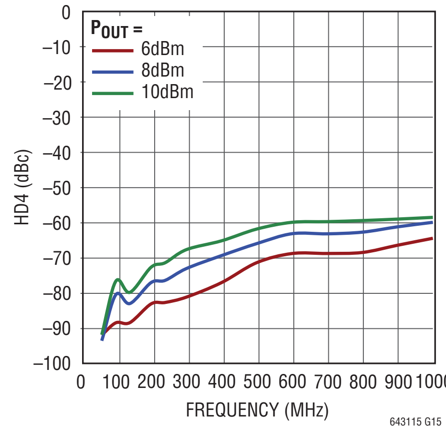
HD2 vs Frequency Over P_{OUT}



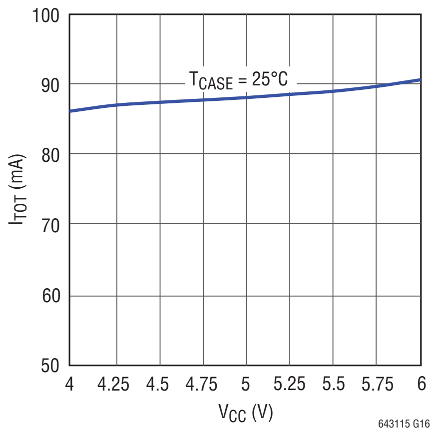
HD3 vs Frequency Over P_{OUT}



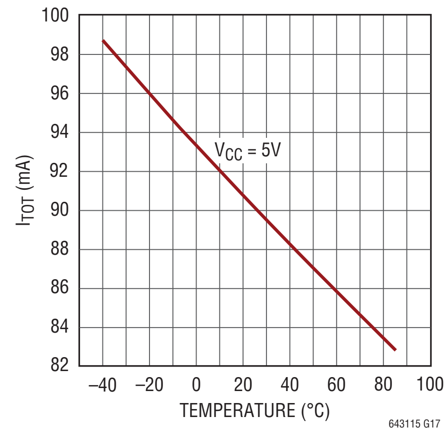
HD4 vs Frequency Over P_{OUT}



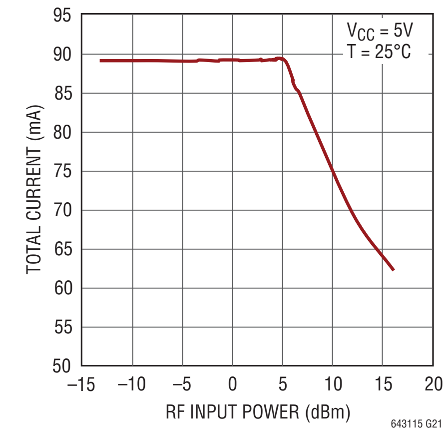
Total Current (I_{TOT}) vs V_{CC}



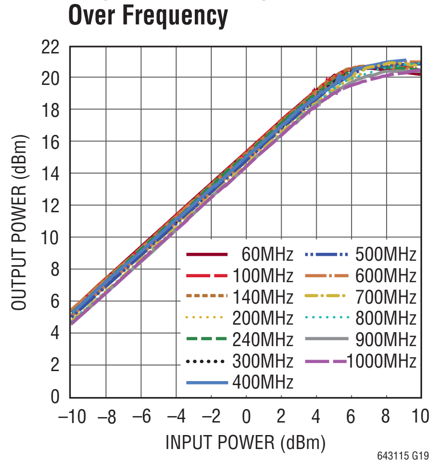
Total Current (I_{TOT}) vs Case Temperature



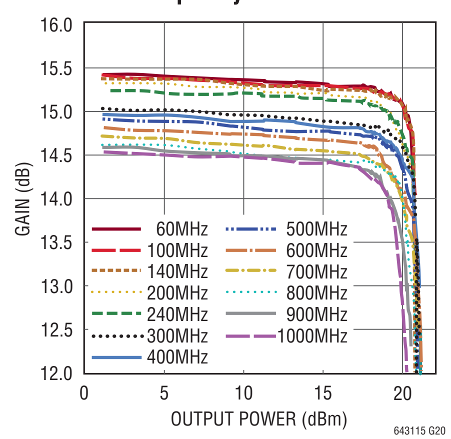
Total Current vs RF Input Power



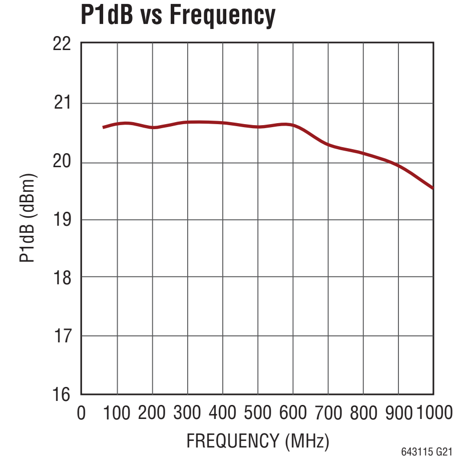
Output Power vs Input Power Over Frequency



Gain vs Output Power Over Frequency



P1dB vs Frequency



PIN FUNCTIONS

GND (Pins 8, 17, 23, Exposed Pad Pin 25): Ground. For best RF performance, all ground pins should be connected to the printed circuit board ground plane. The exposed pad should have multiple via holes to an underlying ground plane for low inductance and good thermal dissipation.

IN (Pin 24): Signal Input Pin. This pin has an internally generated 2V DC bias. A DC blocking capacitor is required. See the Applications Information section for specific recommendations.

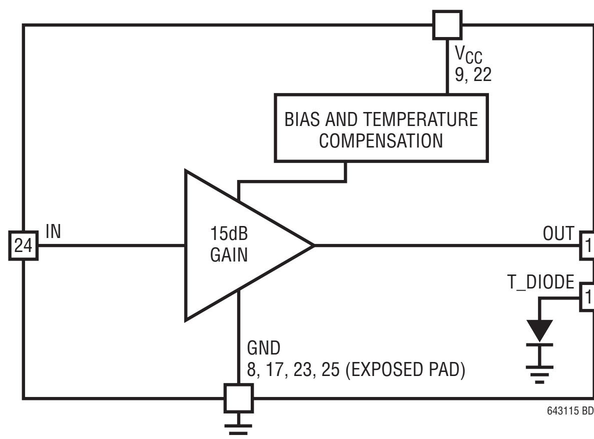
V_{CC} (Pins 9, 22): Positive Power Supply. Either V_{CC} pin should be connected to the 5V supply. Bypass the V_{CC} pin with 1000pF and 0.1µF capacitors. The 1000pF capacitor should be physically close to Pin 22.

OUT (Pin 18): Amplifier Output Pin. A choke inductor is necessary to provide power from the 5V supply and to provide RF isolation. For best performance select a choke with low loss and high self-resonant frequency (SRF). A DC blocking capacitor is also required. See the Applications Information section for specific recommendations.

DNC (Pins 1 to 7, 10 to 15, 19 to 21): Do Not Connect. Do not connect these pins; allow them to **float. Failure to float these pins may impair operation of the LTC6431-15.**

T_DIODE (Pin 16): Optional Diode. The T_DIODE can be forward-biased to ground with 1mA of current. The measured voltage will be an indicator of chip temperature.

BLOCK DIAGRAM



TEST CIRCUIT A

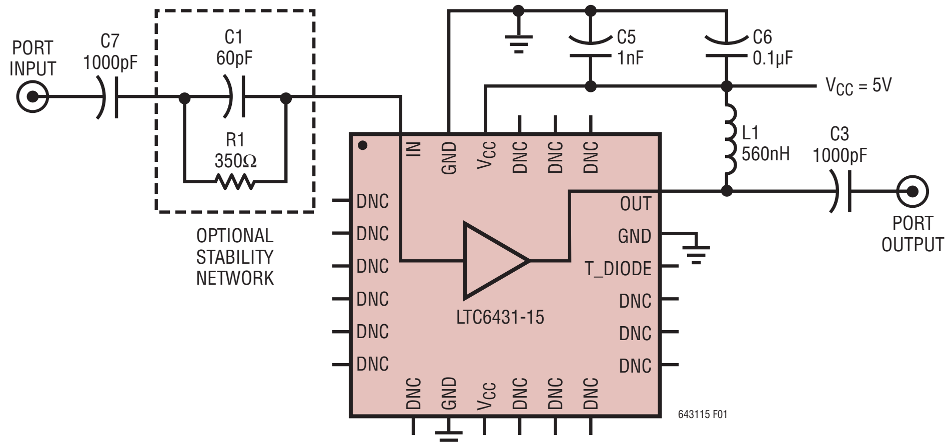


Figure 1. Application, Test Circuit A

OPERATION

The LTC6431-15 is a highly linear, fixed-gain amplifier that is configured to operate single ended. Its core signal path consists of a single amplifier stage minimizing stability issues. The input is a Darlington pair for high input impedance and high current gain. Additional circuit enhancements increase the output impedance and minimize the effects of internal Miller capacitance.

The LTC6431-15 starts with a classic RF gain-block topology but adds additional enhancements to achieve dramatically improved linearity. Shunt and series feedback are added to lower the input/output impedance and match them simultaneously to the 50Ω source and load. Meanwhile, an internal bias controller optimizes the internal operating point for peak linearity over environmental changes. This circuit architecture provides low noise, excellent RF power handling capability and wide bandwidth—characteristics that are desirable for IF signal chain applications.

APPLICATIONS INFORMATION

The LTC6431-15 is a highly linear fixed-gain amplifier which is designed for ease of use. Implementing an RF gain stage is often a multistep project. Typically an RF designer must choose a bias point and design a bias network. Next the designer needs to address impedance matching with input and output matching networks and, finally, add stability networks to ensure stable operation in and out of band. These tasks are handled internally within the LTC6431-15.

The LTC6431-15 has an internal self-biasing network which compensates for temperature variation and keeps the device biased for optimal linearity. Therefore, input and output DC blocking capacitors are required.

Both the input and output are internally impedance matched to 50Ω from 20MHz to 1700MHz. Similarly, an RF choke is required at the output to deliver DC current to the device. The RF choke acts as a high impedance (isolation) to the DC supply which is at RF ground. Thus, the internal LTC6431-15 impedance matching is unaffected by the biasing network. The open collector output topology can deliver much more power than an amplifier whose collector is biased through a resistor or active load.

Choosing the Right RF Choke

Not all choke inductors are created equal. It is always important to select an inductor with low R_{LOSS}, as this will drop the available voltage to the device. Also look for an inductor with high self-resonant frequency (SRF) as this will limit the upper frequency where the choke is useful. Above the SRF, the parasitic capacitance dominates and the choke impedance will drop. For these reasons, wire wound inductors are preferred, and multilayer ceramic chip inductors should be avoided for an RF choke. Since the LTC6431-15 is capable of such wideband operation, a single choke value will probably not result in optimized performance across its full frequency band. Table 1 lists target frequency bands and suggested corresponding inductor values.

Table 1. Target Frequency Bands and Suggested Inductor Values

FREQUENCY BAND (MHz)	INDUCTOR VALUE (nH)	MODEL NUMBER	MANUFACTURER
20 to 100	1500nH	0805LS	Coilcraft www.coilcraft.com
100 to 500	560nH	0603LS	
500 to 1000	100nH	0603LS	
1000 to 2000	51nH	0603LS	

DC Blocking Capacitor

The role of a DC blocking capacitor is straightforward: block the path of DC current and allow a low series impedance path for the AC signal. Lower frequencies require a higher value of DC blocking capacitance. Generally, 1000pF to 10000pF will suffice for operation down to 20MHz. The LTC6431-15 is relatively insensitive to the choice of blocking capacitor.

RF Bypass Capacitor

RF bypass capacitors act to shunt AC signals to ground with a low impedance path. It is best to place them as close as possible to the DC power supply pins of the device. Any extra distance translates into additional series inductance which lowers the self-resonant frequency and useful bandwidth of the bypass capacitor. The suggested bypass capacitor network consists of two capacitors: a low value 1000pF capacitor to handle high frequencies in parallel with a larger 0.1μF capacitor to handle lower frequencies. Use ceramic capacitors of an appropriate physical size for each capacitance value (e.g., 0402 for the 1000pF, 0805 for the 0.1μF) to minimize the equivalent series resistance (ESR) of the capacitor.

APPLICATIONS INFORMATION

Low Frequency Stability

Most RF gain blocks suffer from low frequency instability. To avoid any stability issues, the LTC6431-15 has an internal feedback network that lowers the gain and matches the input and output impedances at frequencies above 20MHz. This feedback network contains a series capacitor, so if at some low frequency the feedback fails, the gain increases and gross impedance mismatches occur—indeed a recipe for instability. Luckily, this situation is easily resolved with a parallel capacitor and resistor network on the input, as seen in Figure 1. This network provides resistive loss at low frequencies and is bypassed by the parallel capacitor within the desired band of operation. However, if the LTC6431-15 is preceeded by a low frequency termination, such as a choke, the input stability network is NOT required.

Test Circuit

The test circuit shown in Figure 2 is designed to allow evaluation of the LTC6431-15 with standard single-ended 50Ω test equipment. The circuit requires a minimum of external components. Since the LTC6431-15 is a wideband part, the evaluation test circuit is optimized for wideband operation. Obviously, for narrowband applications the circuit can be further optimized. As mentioned earlier, input and output DC blocking capacitors are required as this device is internally biased for optimal operation. A frequency appropriate choke and decoupling capacitors are required to provide DC bias to the RF out node. A 5V supply should also be applied to both of the V_{CC} pins on the device. A suggested parallel 60pF, 350Ω network has been added to the input to ensure low frequency stability. The 60pF capacitance can be increased to improve low frequency (<150MHz) performance. However, the designer needs to be sure that the impedance presented at low frequency will not create instability.

Please note that a number of DNC pins are connected on the demo board. These connections are not necessary for normal circuit operation.

Exposed Pad and Ground Plane Considerations

As with any RF device, minimizing ground inductance is critical. Care should be taken with board layouts using these exposed pad packages. The maximum allowable number of minimum diameter via holes should be placed underneath the exposed pad and connect to as many ground plane layers as possible. This will provide good RF ground and low thermal impedance. Maximizing the copper ground plane will also improve heat spreading and lower inductance. It is a good idea to cover the via holes with a solder mask on the backside of the PCB to prevent the solder from wicking away from the critical PCB to the exposed pad interface.

The LTC6431-15 is a wide bandwidth part, but it is not intended for operation down to DC. The lower frequency cutoff (20MHz) is limited by on-chip matching elements.

APPLICATIONS INFORMATION

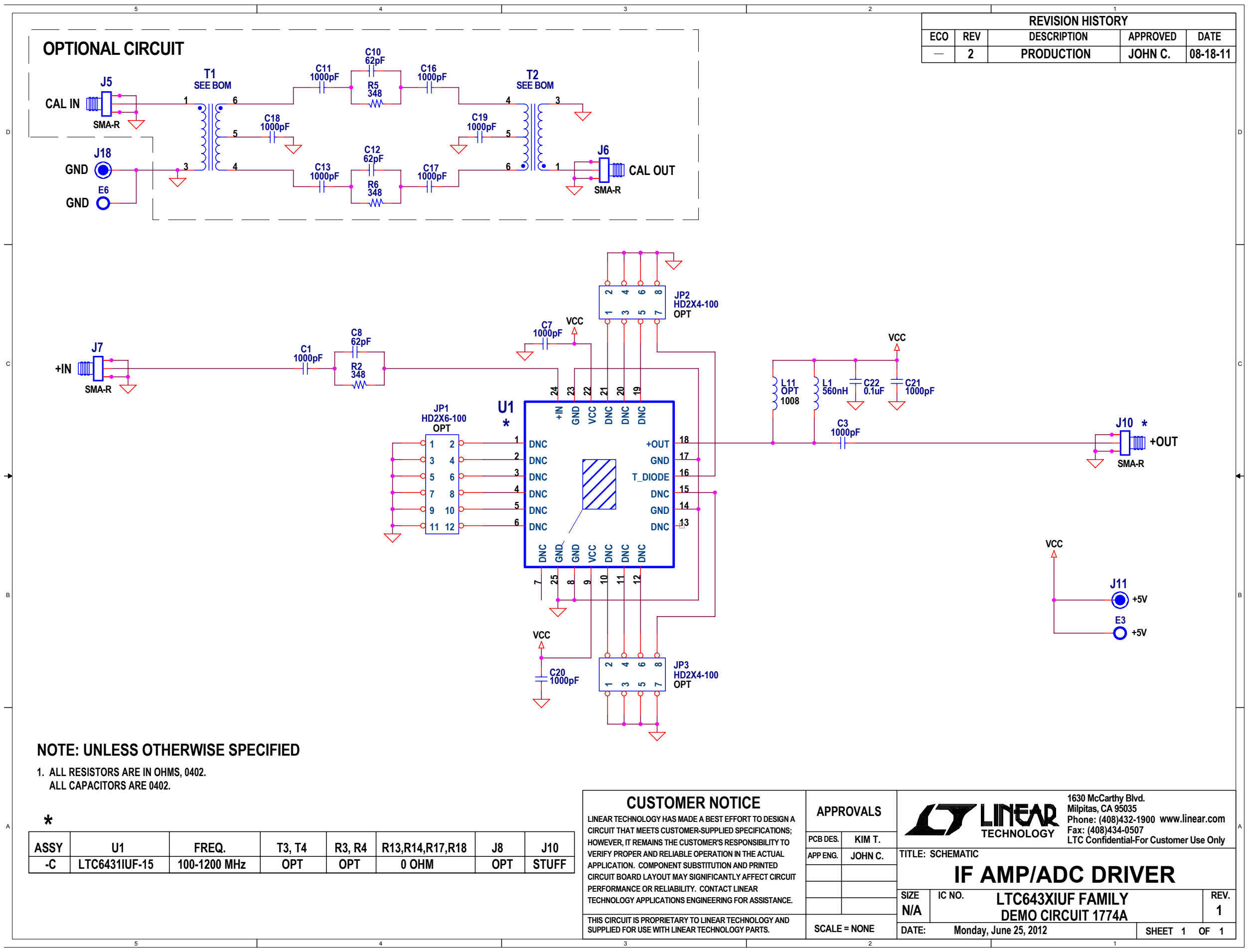


Figure 2. DC1774A-C Demo Board Schematic

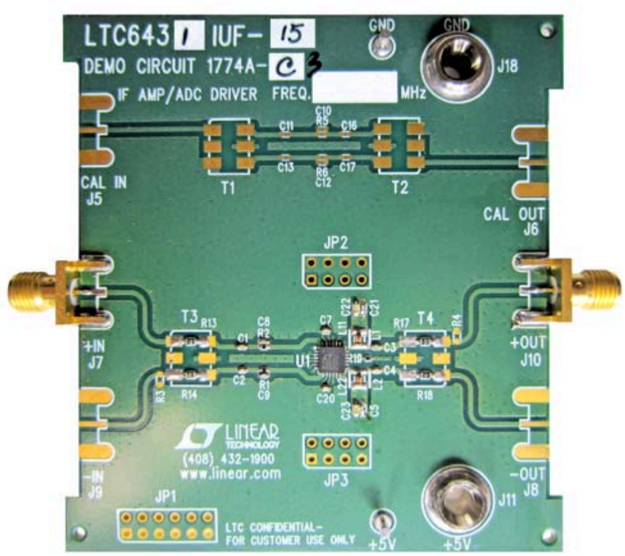


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Figure 3. Demo Board

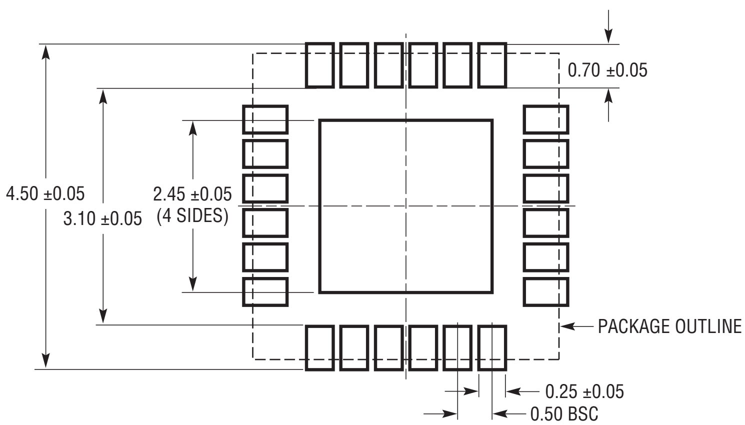
S PARAMETERS 5V, 90mA, Z = 50Ω, T = 25°C, De-Embedded to Package Pins

FREQUENCY (MHz)	S11 (Mag)	S11 (Ph)	S21 (Mag)	S21 (Ph)	S12 (Mag)	S12 (Ph)	S22 (Mag)	S22 (Ph)	GTU (Max)	Stability (K)
23.5	–14.90	–93.74	15.94	166.13	–19.01	8.83	–15.39	–77.56	16.21	0.99
83.5	–21.83	–128.88	15.54	169.51	–18.92	–3.42	–26.58	–72.76	15.58	1.07
143	–22.33	–142.38	15.54	166.10	–18.98	–8.97	–31.71	–52.44	15.57	1.07
203	–22.14	–153.70	15.54	161.63	–19.04	–13.69	–36.22	–29.74	15.57	1.08
263	–21.88	–162.35	15.52	156.90	–19.10	–18.05	–36.75	–13.45	15.55	1.08
323	–21.02	–168.55	15.49	152.16	–19.15	–22.46	–35.10	–3.73	15.52	1.08
383	–20.39	–172.14	15.42	147.41	–19.23	–26.61	–31.62	0.84	15.46	1.09
443	–19.55	–175.07	15.41	142.91	–19.29	–30.83	–29.46	–1.01	15.46	1.09
503	–18.88	–177.54	15.37	138.07	–19.37	–34.91	–26.62	–2.90	15.44	1.09
563	–18.39	179.31	15.35	133.30	–19.44	–39.04	–25.06	–7.32	15.43	1.09
623	–18.02	175.72	15.32	128.48	–19.53	–43.16	–23.84	–14.68	15.41	1.10
683	–17.70	171.89	15.29	123.64	–19.61	–47.19	–22.46	–23.42	15.39	1.10
743	–17.37	168.02	15.26	118.80	–19.71	–51.39	–21.37	–30.32	15.37	1.10
803	–17.06	164.02	15.20	113.94	–19.82	–55.31	–20.17	–37.91	15.33	1.11
863	–16.73	160.39	15.17	109.07	–19.92	–59.53	–19.13	–44.68	15.31	1.11
923	–16.35	156.50	15.12	104.20	–20.04	–63.43	–18.11	–50.82	15.29	1.11
983	–16.05	152.86	15.07	99.34	–20.16	–67.53	–17.31	–57.37	15.26	1.12
1049	–15.76	149.53	15.02	94.39	–20.29	–71.52	–16.51	–63.98	15.24	1.12
1109	–15.51	146.42	14.98	89.31	–20.42	–75.48	–15.82	–70.79	15.22	1.13
1160	–15.29	143.29	14.90	84.36	–20.55	–79.56	–15.22	–78.18	15.16	1.13
1220	–15.13	141.27	14.87	79.21	–20.70	–83.45	–14.56	–85.99	15.16	1.14
1280	–14.93	138.82	14.80	74.05	–20.84	–87.50	–13.94	–93.89	15.12	1.14
1340	–14.75	137.08	14.72	69.04	–21.01	–91.46	–13.37	–101.73	15.07	1.15
1400	–14.52	135.84	14.67	63.48	–21.14	–95.38	–12.79	–109.91	15.06	1.16
1460	–14.26	134.03	14.55	58.17	–21.34	–99.38	–12.27	–117.55	14.98	1.17
1520	–13.88	132.68	14.43	52.80	–21.47	–103.25	–11.71	–125.53	14.91	1.18
1580	–13.48	130.52	14.27	47.38	–21.63	–107.46	–11.24	–134.17	14.80	1.19
1640	–13.07	128.54	14.06	42.05	–21.83	–111.37	–10.62	–142.12	14.67	1.20
1700	–12.67	126.19	13.82	37.06	–22.01	–115.95	–10.07	–150.09	14.51	1.22
1760	–12.21	123.77	13.60	32.36	–22.30	–119.76	–9.51	–158.23	14.39	1.24
1820	–11.77	120.88	13.31	27.42	–22.49	–123.59	–9.02	–165.81	14.19	1.26
1880	–11.38	117.51	13.02	23.82	–22.74	–127.66	–8.65	–172.96	13.98	1.29
1940	–10.95	114.44	12.83	19.28	–23.04	–131.54	–8.28	179.92	13.89	1.31
2000	–10.57	110.59	12.51	15.92	–23.17	–134.66	–7.97	172.64	13.66	1.34
2060	–10.19	106.94	12.46	12.13	–23.59	–139.47	–7.71	166.43	13.71	1.36
2120	–9.78	103.11	12.20	7.92	–23.73	–141.66	–7.49	159.51	13.53	1.38
2180	–9.44	99.15	12.20	4.71	–23.99	–146.81	–7.32	153.38	13.62	1.39
2240	–9.02	95.22	12.10	–0.60	–24.32	–149.09	–7.17	146.92	13.60	1.41
2300	–8.67	91.22	12.07	–5.36	–24.53	–152.92	–7.05	140.33	13.66	1.41

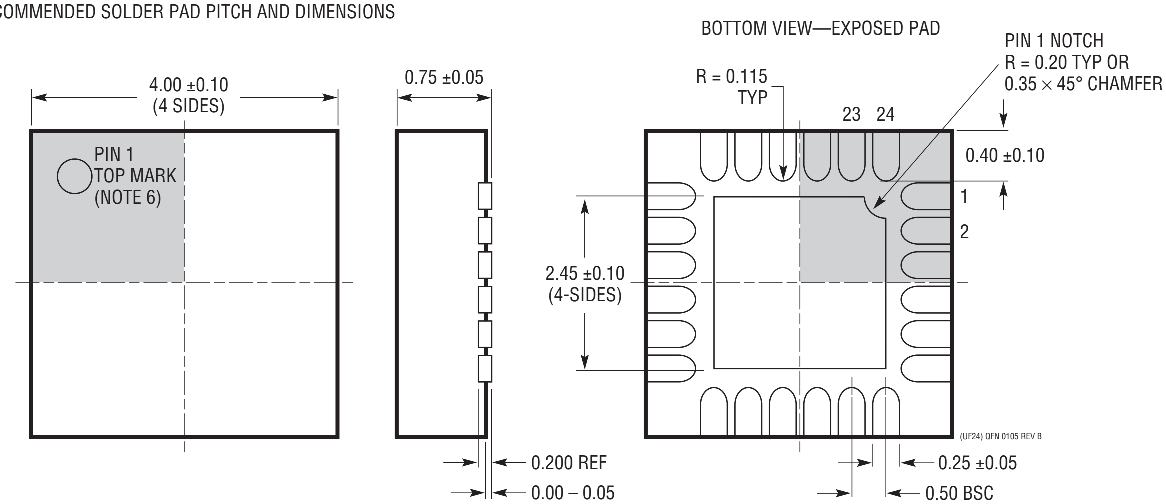
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697 Rev B)

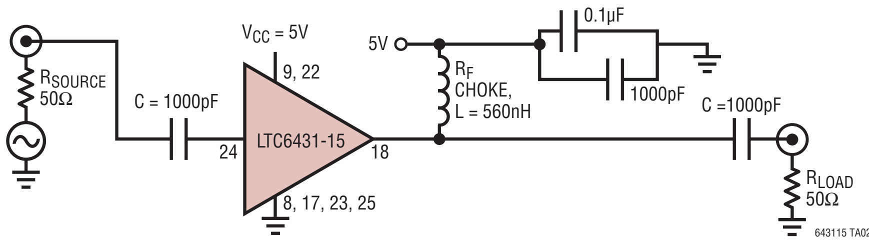


RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Fixed Gain IF Amplifiers/ADC Drivers		
LTC6417	1.6GHz Low Noise High Linearity Differential Buffer/ ADC Driver	OIP3 = 41dBm at 300MHz; Can Drive 50Ω Differential Output; High Speed Voltage Clamping Protects Subsequent Circuitry
LTC6416	2GHz, 16-Bit Differential ADC Buffer	–72dBc IM2 at 300MHz $2V_{P-P}$ Composite; I_S = 42mA; eN = 2.8nV/$\sqrt{Hz}$; A_V = 0dB; 300MHz
LTC6410-6	1.4GHz Differential IF Amplifier with Configurable Input Impedance	OIP3 = 36dBm at 70MHz; Flexible Interface to Mixer IF Port
LTC6400-8/LTC6400-14/ LTC6400-20/LTC6400-26	1.8GHz Low Noise, Low Distortion Differential ADC Drivers	–71dBc IM3 at 240MHz $2V_{P-P}$ Composite; I_S = 90mA; A_V = 8dB/14dB/20dB/26dB
LTC6420-20	Dual 1.8GHz Low Noise, Low Distortion Differential ADC Drivers	Dual Version of the LTC6400-20; A_V = 20dB
LT1993-2/LT1993-4/ LT1993-10	800MHz Differential Amplifier/ADC Drivers	–72dBc IM3 at 70MHz $2V_{P-P}$ Composite; A_V = 2V/V, 4V/V, 10V/V
Variable Gain IF Amplifiers/ADC Drivers		
LTC6412	800MHz, 31dB Range Analog-Controlled VGA	OIP3 = 35dBm at 240MHz; Continuously Adjustable Gain Control
Baseband Differential Amplifiers		
LT6411	Low Power Differential ADC Driver/Dual Selectable Gain Amplifier	–83dBc IM3 at 70MHz $2V_{P-P}$ Composite; A_V = 1, –1 or 2; 16mA; Excellent for Single-Ended to Differential Conversion
LTC6406	3GHz Rail-to-Rail Input Differential Amplifier/ ADC Driver	–65dBc IM3 at 50MHz $2V_{P-P}$ Composite; Rail-to-Rail Inputs; eN = 1.6nV/$\sqrt{Hz}$; 18mA
LTC6404-1/LTC6404-2	Low Noise Rail-to-Rail Output Differential Amplifier/ ADC Driver	16-Bit SNR, SFDR at 10MHz; Rail-to-Rail Outputs; eN = 1.5nV/$\sqrt{Hz}$; LTC6404-1 Is Unity-Gain Stable, LTC6404-2 Is Gain-of-Two Stable
LTC6403-1	Low Noise Rail-to-Rail Output Differential	16-Bit SNR, SFDR at 3MHz; Rail-to-Rail Outputs; eN = 2.8nV/$\sqrt{Hz}$
LT1994	Low Noise, Low Distortion Differential Amplifier/ADC Driver	16-Bit SNR, SFDR at 1MHz; Rail-to-Rail Outputs
High Speed ADCs		
LTC2208/LTC2209	16-Bit, 130Msps/160Msps ADCs	78dBFS/77dBFS Noise Floor, 100dB SFDR, $2.25V_{P-P}$ or $1.5V_{P-P}$ Input Range
LTC2259-16	16-Bit, 80Msps, 1.8V ADC	89mW, 73.1dB SNR, 88dB SFDR, $1V_{P-P}$ to $2V_{P-P}$ Input Range
LTC2160/LTC2161/ LTC2162/LTC2163/ LTC2164/LTC2165	16-Bit, 25Msps/40Msps/65Msps/80Msps/105Msps/ 125Msps, 1.8V ADCs	77dB SNR, 90dB SFDR, $1V_{P-P}$ to $2V_{P-P}$ Input Range
LTC2150-14/LTC2151-14/ LTC2152-14/LTC2153-14	14-Bit, 170Msps/210Msps/250Msps/310Msps, 1.8V ADCs	Single ADCs, >68dB SNR, >88dB SFDR, $1.32V_{P-P}$ Input Range
LTC2155-14/LTC2156-14/ LTC2157-14/LTC2158-14	14-Bit, 170Msps/210Msps/250Msps/310Msps, 1.8V ADCs	Dual ADCs, >68dB SNR, >88dB SFDR, $1.32V_{P-P}$ Input Range

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 ● FAX: (408) 434-0507 ● www.linear.com
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