CD40103
8-bit synchronous binary down counter

Product Specification

Specification Revision History：

Version	Date	Description
2021-11-A1	2021-11	New
2021-12-A2	2021-12	Modify Ordering Information
2023-04-B1	2023-04	Update the template

Contents

1、General Description

The CD40103 is an 8-bit synchronous down counter. It has control inputs for enabling or disabling the clock (CP), for clearing the counter to its maximum count and for presetting the counter either synchronously or asynchronously. In normal operation, the counter is decremented by one count on each positive-going transition of the clock (CP). Counting is inhibited when the terminal enable input ( ) is HIGH. The terminal count output ( ) goes LOW when the count reaches zero if is LOW, and remains LOW for one full clock period. When the synchronous preset enable input ( ) is LOW, data at the jam input (P0 to P7) is clocked into the counter on the next positive-going clock transition regardless of the state of . When the asynchronous preset enable input ( ) is LOW, data at the jam input (P0 to P7) is asynchronously forced into the counter regardless of the state of , , or CP. The jam inputs (P0 to P7) represent a single 8-bit binary word. When the master reset input ( ) is LOW, the counter is asynchronously cleared to its maximum count (decimal 255) regardless of the state of any other input. If all control inputs except are HIGH at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 256 clock pulses long. Device may be cascaded using the input and the TC output, in either a synchronous or ripple mode. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

Features:

- Cascadable
- Synchronous or asynchronous preset
- Low-power dissipation
- CMOS input levels
- Specified from -40℃ to +125℃
- Packaging information: DIP16/SOP16/TSSOP16

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
CD40103BE(LX)	DIP16	CD40103BE	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
CD40103B(LX)	SOP16	CD40103B	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
CD40103P(LX)	TSSOP16	CD40103P	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
CD40103BDR(LX)	SOP16	CD40103B	2500 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
CD40103PR(LX)	TSSOP16	CD40103P	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

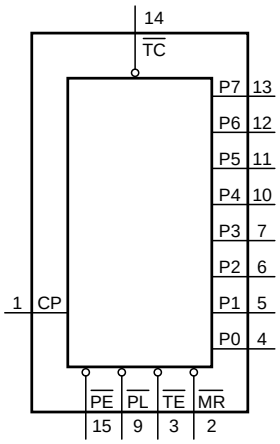


Figure 1. Functional diagram

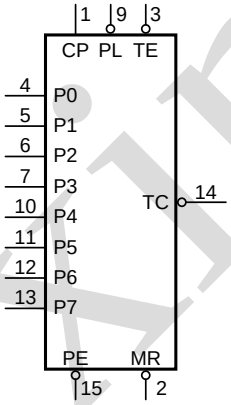


Figure 2. Logic symbol

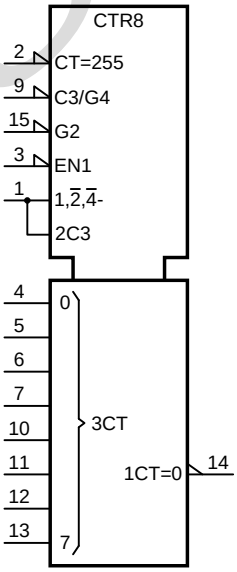


Figure 3. IEC logic symbol

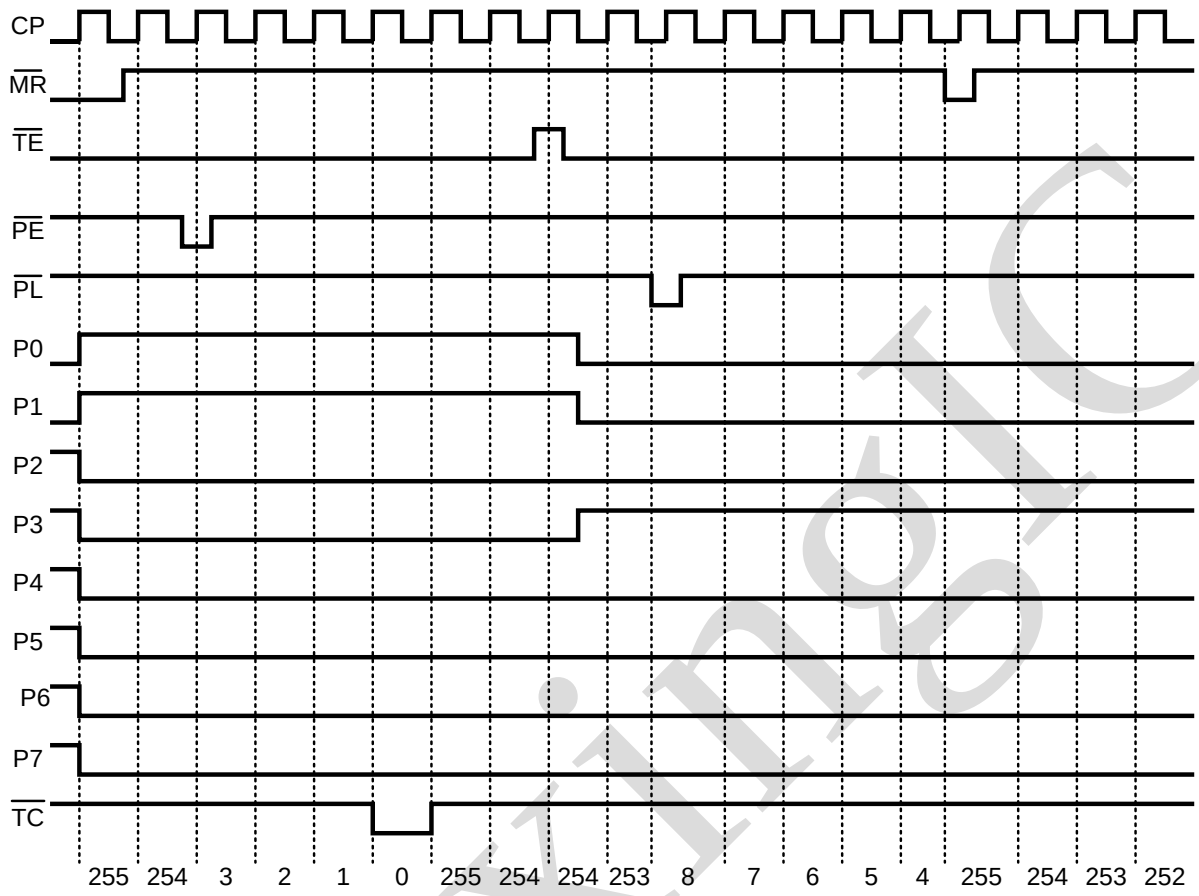


Figure 4. Timing diagram

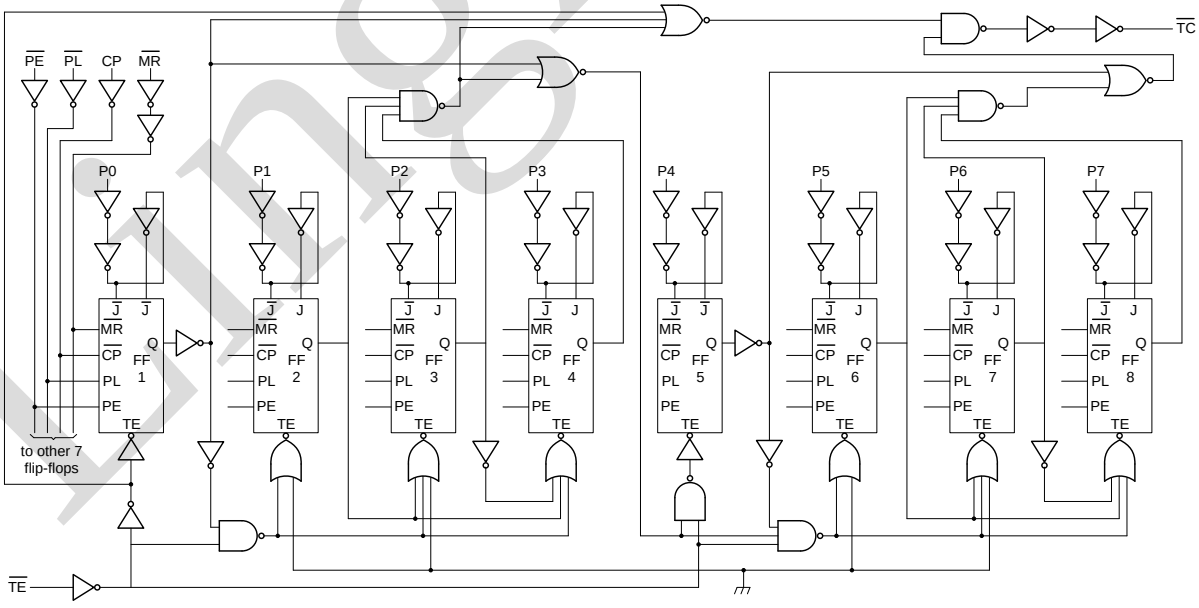
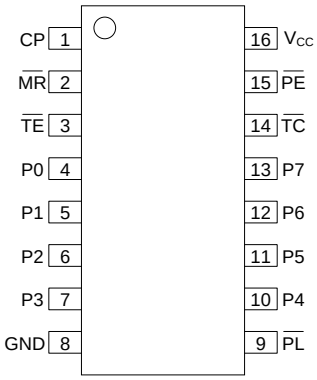


Figure 5. Logic diagram

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	CP	clock input (LOW-to-HIGH, edge-triggered)
2		asynchronous master reset input (active LOW)
3		terminal enable input (active LOW)
4	P0	jam input 0
5	P1	jam input 1
6	P2	jam input 2
7	P3	jam input 3
8	GND	ground (0 V)
9		asynchronous preset enable input (active LOW)
10	P4	jam input 4
11	P5	jam input 5
12	P6	jam input 6
13	P7	jam input 7
14		terminal count output (active LOW)
15		synchronous preset enable input (active LOW)
16	V_{CC}	positive supply voltage

2.4、Function table

Control inputs				Preset mode	Action
$\overline{MR}$	$\overline{PL}$	$\overline{PE}$	$\overline{TE}$		
L	X	X	X	asynchronous	clear to maximum count
H	L	X	X	asynchronous	preset asynchronously
	H	L	X	synchronous	preset on next LOW-to HIGH clock transition
		H	L	synchronous	count down
			H	synchronous	inhibit counter

Note:

H=HIGH voltage level; L=LOW voltage level; X=don’t care.

Clock connected to CP.

Synchronous operation: changes occur on the LOW-to-HIGH CP transition.

Jam inputs: MSD=P7, LSD=P0.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(T_{amb}=25℃, voltage are referenced to GND (ground=0V), unless otherwise specified)

Characteristic	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7.0	V
input clamping current	I_{IK}	V_I<-0.5V or V_I>V_{CC}+0.5V[1]		-	±20	mA
output clamping current	I_{OK}	V_O<-0.5V or V_O>V_{CC}+0.5V[1]		-	±20	mA
output current	I_O	V_O=-0.5V to V_{CC}+0.5V		-	±25	mA
supply current	I_{CC}	-		-	+50	mA
ground current	I_{GND}	-		-50	-	mA
storage temperature	T_{stg}	-		-65	+150	℃
total power dissipation	P_{tot}	-		-	500	mW
soldering temperature	T_L	10s	DIP	245		℃
			SOP/TSSOP	260		℃

Note:

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CD40103						
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	Δt/ΔV	V_{CC}=2.0V	-	-	625	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	83	ns/V
ambient temperature	T_{amb}	-	-40	-	+125	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
CD40103							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2.1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.26	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.26	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8.0	uA
input capacitance	C_I	-		-	3.5	-	pF

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
CD40103							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.84	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.34	-	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	-	0.33	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA

3.3.3、DC Characteristics 3

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
CD40103							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.2	-	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	-	0.4	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA

3.3.4、AC Characteristics 1

(T_{amb}=25℃, GND=0V; t_r=t_f=6 ns; C_L=50 pF, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
CD40103							
propagation delay	t_{pd}	CP to ; see Figure 6[1]	V_{CC}=2.0V	-	96	300	ns
			V_{CC}=4.5V	-	35	60	ns
			V_{CC}=5.0V; C_L=15pF	-	30	-	ns
			V_{CC}=6.0V	-	28	51	ns
		to ; see Figure 7	V_{CC}=2.0V	-	50	175	ns
			V_{CC}=4.5V	-	18	35	ns
			V_{CC}=6.0V	-	14	30	ns
		to ; see Figure 8	V_{CC}=2.0V	-	102	315	ns
			V_{CC}=4.5V	-	37	63	ns
			V_{CC}=6.0V	-	30	53	ns
HIGH to LOW propagation delay	t_{PHL}	to ; see Figure 8	V_{CC}=2.0V	-	83	275	ns
			V_{CC}=4.5V	-	30	55	ns
			V_{CC}=6.0V	-	24	47	ns
transition time	t_t	see Figure 7[2]	V_{CC}=2.0V	-	19	75	ns
			V_{CC}=4.5V	-	7	15	ns
			V_{CC}=6.0V	-	6	13	ns
pulse width	t_W	CP HIGH or LOW; see Figure 6	V_{CC}=2.0V	165	22	-	ns
			V_{CC}=4.5V	33	8	-	ns
			V_{CC}=6.0V	28	6	-	ns
		LOW; see Figure 8	V_{CC}=2.0V	125	39	-	ns
			V_{CC}=4.5V	25	14	-	ns
			V_{CC}=6.0V	21	11	-	ns
		LOW; see Figure 8	V_{CC}=2.0V	125	33	-	ns
			V_{CC}=4.5V	25	12	-	ns
			V_{CC}=6.0V	21	10	-	ns
recovery time	t_{rec}	to CP, to CP; see Figure 9	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	18	-	-	ns
set-up time	t_{su}	to CP; see Figure 10	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
		to CP; see Figure 11	V_{CC}=2.0V	150	-	-	ns
			V_{CC}=4.5V	30	-	-	ns
			V_{CC}=6.0V	26	-	-	ns
		Pn to CP; see Figure 10	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
hold time	t_h	to CP; see Figure 10	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
		to CP;	V_{CC}=2.0V	0	-	-	ns

		see Figure 11	V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
		Pn to CP; see Figure 10	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
maximum frequency	f_{max}	see Figure 6	V_{CC}=2.0V	3.0	10	-	MHz
			V_{CC}=4.5V	15	29	-	MHz
			V_{CC}=5.0V; C_L=15pF	-	32	-	MHz
			V_{CC}=6.0V	18	35	-	MHz
power dissipation capacitance	C_{PD}	V_I=GND to V_{CC}[3]		-	24	-	pF

Note:

[1] t_{pd} is the same as t_{PHL}, t_{PLH}.

[2] t_t is the same as t_{THL}, t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD}\times V_{CC}^2\times f_i\times N+\sum(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

3.3.5、AC Characteristics 2

(T_{amb}=-40℃ to +85℃, GND=0V; t_r=t_f=6 ns; C_L=50 pF, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
CD40103							
propagation delay	t_{pd}	CP to ; see Figure 6[1]	V_{CC}=2.0V	-	-	375	ns
			V_{CC}=4.5V	-	-	75	ns
			V_{CC}=6.0V	-	-	64	ns
		to ; see Figure 7	V_{CC}=2.0V	-	-	220	ns
			V_{CC}=4.5V	-	-	44	ns
			V_{CC}=6.0V	-	-	37	ns
		to ; see Figure 8	V_{CC}=2.0V	-	-	395	ns
			V_{CC}=4.5V	-	-	79	ns
			V_{CC}=6.0V	-	-	40	ns
HIGH to LOW propagation delay	t_{PHL}	to ; see Figure 8	V_{CC}=2.0V	-	-	345	ns
			V_{CC}=4.5V	-	-	69	ns
			V_{CC}=6.0V	-	-	59	ns
transition time	t_t	see Figure 7[2]	V_{CC}=2.0V	-	-	95	ns
			V_{CC}=4.5V	-	-	19	ns
			V_{CC}=6.0V	-	-	16	ns
pulse width	t_W	CP HIGH or LOW; see Figure 6	V_{CC}=2.0V	205	-	-	ns
			V_{CC}=4.5V	41	-	-	ns
			V_{CC}=6.0V	35	-	-	ns
		LOW; see Figure 8	V_{CC}=2.0V	155	-	-	ns
			V_{CC}=4.5V	31	-	-	ns
			V_{CC}=6.0V	26	-	-	ns
		LOW; see Figure 8	V_{CC}=2.0V	155	-	-	ns
			V_{CC}=4.5V	31	-	-	ns
			V_{CC}=6.0V	26	-	-	ns
recovery time	t_{rec}	to CP, to CP; see Figure 9	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	22	-	-	ns
set-up time	t_{su}	to CP; see Figure 10	V_{CC}=2.0V	95	-	-	ns
			V_{CC}=4.5V	19	-	-	ns

			V_{CC}=6.0V	16	-	-	ns
		to CP; see Figure 11	V_{CC}=2.0V	190	-	-	ns
			V_{CC}=4.5V	38	-	-	ns
			V_{CC}=6.0V	33	-	-	ns
		Pn to CP; see Figure 10	V_{CC}=2.0V	95	-	-	ns
			V_{CC}=4.5V	19	-	-	ns
			V_{CC}=6.0V	16	-	-	ns
hold time	t_h	to CP; see Figure 10	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
		to CP; see Figure 11	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
		Pn to CP; see Figure 10	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
maximum frequency	f_{max}	see Figure 6	V_{CC}=2.0V	2.4	-	-	MHz
			V_{CC}=4.5V	12	-	-	MHz
			V_{CC}=6.0V	14	-	-	MHz
		to CP; see Figure 11	V_{CC}=4.5V	0	-	-	ns
		Pn to CP; see Figure 10	V_{CC}=4.5V	0	-	-	ns
maximum frequency	f_{max}	see Figure 6;	V_{CC}=4.5V	12	-	-	MHz

Note:

[1] t_{pd} is the same as t_{PHL}, t_{PLH}.

[2] t_t is the same as t_{THL}, t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD}\times V_{CC}^2\times f_i\times N+\sum(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

3.3.6、AC Characteristics 3

(T_{amb}=-40℃ to +125℃, GND=0V; t_r=t_f=6 ns; C_L=50 pF, unless otherwise specified)

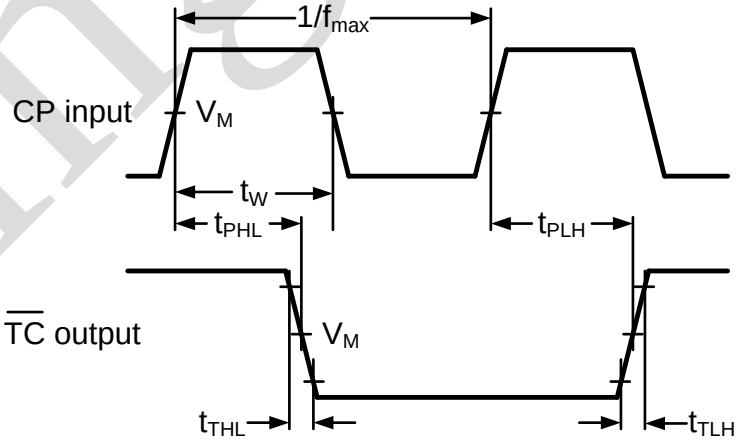
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
CD40103							
propagation delay	t_{pd}	CP to ; see Figure 6[1]	V_{CC}=2.0V	-	-	450	ns
			V_{CC}=4.5V	-	-	90	ns
			V_{CC}=6.0V	-	-	77	ns
		to ; see Figure 7	V_{CC}=2.0V	-	-	265	ns
			V_{CC}=4.5V	-	-	53	ns
			V_{CC}=6.0V	-	-	45	ns
		to ; see Figure 8	V_{CC}=2.0V	-	-	475	ns
			V_{CC}=4.5V	-	-	95	ns
			V_{CC}=6.0V	-	-	81	ns
HIGH to LOW propagation delay	t_{PHL}	to ; see Figure 8	V_{CC}=2.0V	-	-	415	ns
			V_{CC}=4.5V	-	-	83	ns
			V_{CC}=6.0V	-	-	71	ns
transition time	t_t	see Figure 7[2]	V_{CC}=2.0V	-	-	110	ns
			V_{CC}=4.5V	-	-	22	ns
			V_{CC}=6.0V	-	-	19	ns
pulse width	t_W	CP HIGH or LOW; see Figure 6	V_{CC}=2.0V	250	-	-	ns
			V_{CC}=4.5V	50	-	-	ns
			V_{CC}=6.0V	43	-	-	ns
		LOW; see Figure 8	V_{CC}=2.0V	190	-	-	ns
			V_{CC}=4.5V	38	-	-	ns
			V_{CC}=6.0V	32	-	-	ns
		LOW;	V_{CC}=2.0V	190	-	-	ns

		see Figure 8	V_{CC}=4.5V	38	-	-	ns
			V_{CC}=6.0V	32	-	-	ns
recovery time	t_{rec}	to CP, to CP; see Figure 9	V_{CC}=2.0V	132	-	-	ns
			V_{CC}=4.5V	26	-	-	ns
			V_{CC}=6.0V	24	-	-	ns
set-up time	t_{su}	to CP; see Figure 10	V_{CC}=2.0V	110	-	-	ns
			V_{CC}=4.5V	22	-	-	ns
			V_{CC}=6.0V	19	-	-	ns
		to CP; see Figure 11	V_{CC}=2.0V	225	-	-	ns
			V_{CC}=4.5V	45	-	-	ns
			V_{CC}=6.0V	38	-	-	ns
		Pn to CP; see Figure 10	V_{CC}=2.0V	110	-	-	ns
			V_{CC}=4.5V	22	-	-	ns
			V_{CC}=6.0V	19	-	-	ns
hold time	t_h	to CP; see Figure 10	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
		to CP; see Figure 11	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
		Pn to CP; see Figure 10	V_{CC}=2.0V	0	-	-	ns
			V_{CC}=4.5V	0	-	-	ns
			V_{CC}=6.0V	0	-	-	ns
maximum frequency	f_{max}	see Figure 6	V_{CC}=2.0V	2.0	-	-	MHz
			V_{CC}=4.5V	10	-	-	MHz
			V_{CC}=6.0V	12	-	-	MHz
set-up time	t_{su}	to CP; see Figure 10	V_{CC}=4.5V	30	-	-	ns
		to CP; see Figure 11	V_{CC}=4.5V	60	-	-	ns
		Pn to CP; see Figure 10	V_{CC}=4.5V	30	-	-	ns
hold time	t_h	to CP; see Figure 10	V_{CC}=4.5V	2	-	-	ns
		to CP; see Figure 11	V_{CC}=4.5V	0	-	-	ns
		Pn to CP; see Figure 10	V_{CC}=4.5V	0	-	-	ns
maximum frequency	f_{max}	see Figure 6;	V_{CC}=4.5V	10	-	-	MHz

Note:
[1] t_{pd} is the same as t_{PHL}, t_{PLH}.
[2] t_t is the same as t_{THL}, t_{TLH}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).
$P_D=C_{PD}\times V_{CC}^2\times f_i\times N+\sum(C_L\times V_{CC}^2\times f_o)$ where:
f_i=input frequency in MHz;
f_o=output frequency in MHz;
C_L=output load capacitance in pF;
V_{CC}=supply voltage in V;
N=number of inputs switching;
$\sum(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

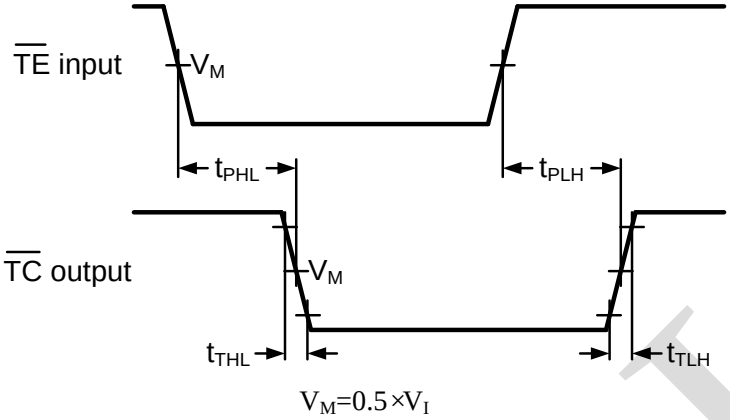
4、Testing Circuit

4.1、AC Testing Waveforms



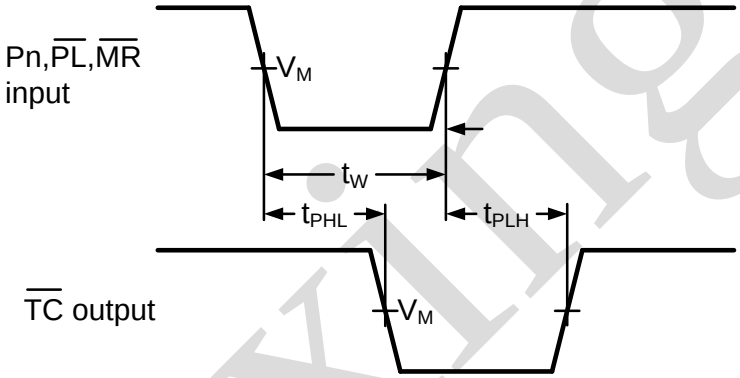
$V_M=0.5\times V_I$

Figure 6. Waveforms showing the clock input (CP) to propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency



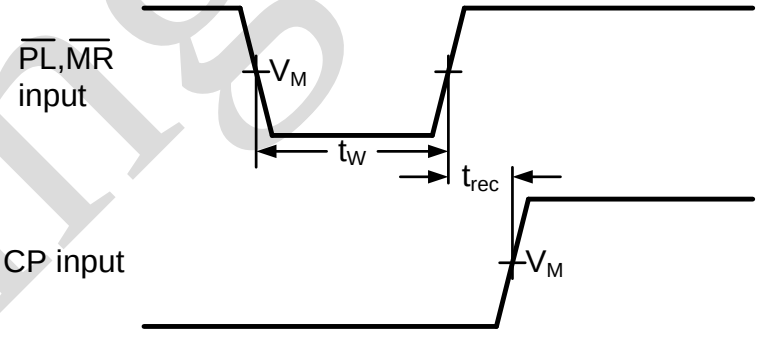
$V_M=0.5\times V_I$

Figure 7. Waveforms showing the to propagation delays



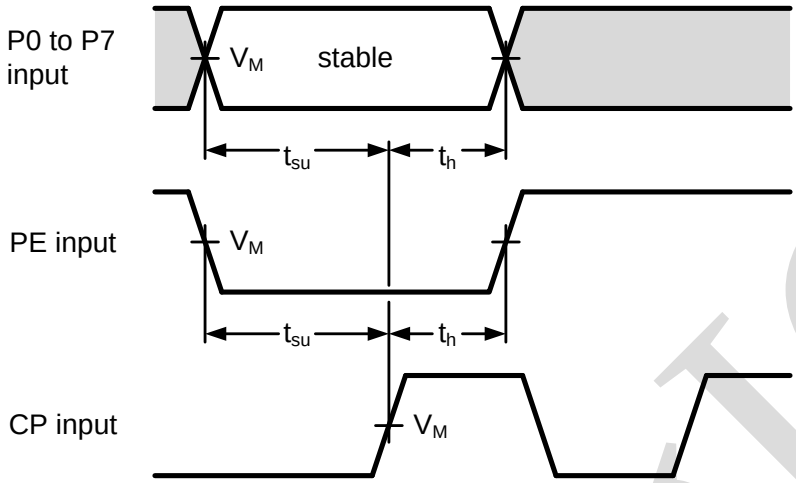
$V_M=0.5\times V_I$

Figure 8.Waveforms showing , , Pn to propagation delays



$V_M=0.5\times V_I$

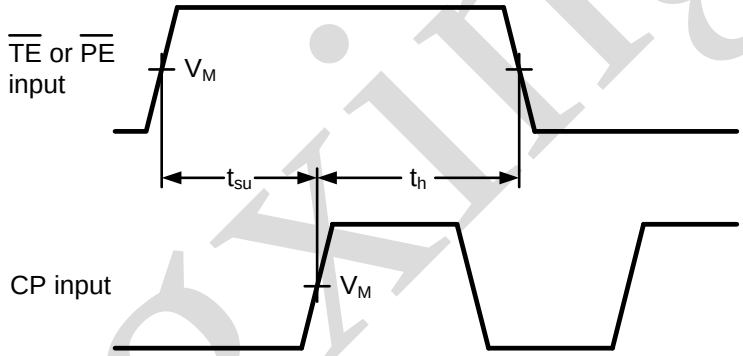
Figure 9. Waveforms showing removal time for and



The shaded areas indicate when the input is permitted to change for predictable output performance.

$V_M=0.5\times V_I$

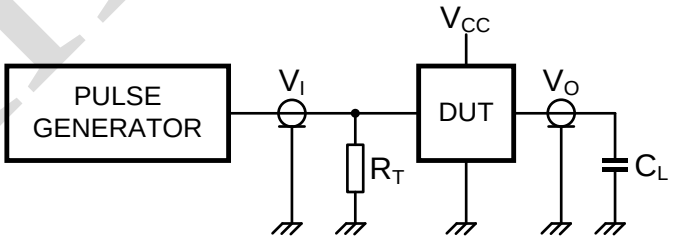
Figure 10. Waveforms showing hold and set-up times for Pn, to CP



$V_M=0.5\times V_I$

Figure 11. Waveforms showing hold and set-up times for or to CP

4.2、AC Testing Circuit



Definitions for test circuit:

R_T=Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L=Load capacitance including jig and probe capacitance.

Figure 12. Test circuit for measuring switching times

4.3、Test Data

Supply	Input		Load
V_{CC}	V_I	t_r, t_f	C_L
2.0V	V_{CC}	6ns	50pF
4.5V	V_{CC}	6ns	50pF
5.0V	V_{CC}	6ns	15pF
6.0V	V_{CC}	6ns	50pF

5、Typical Application Circuit And Application Note

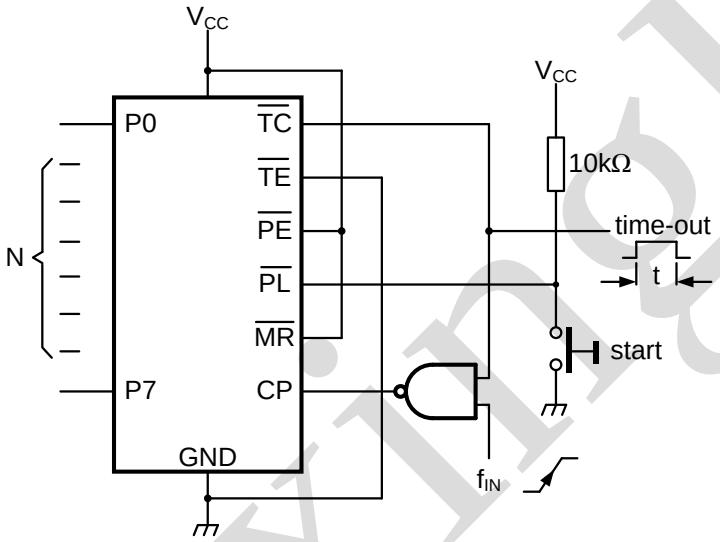


Figure 13. Programmable timer

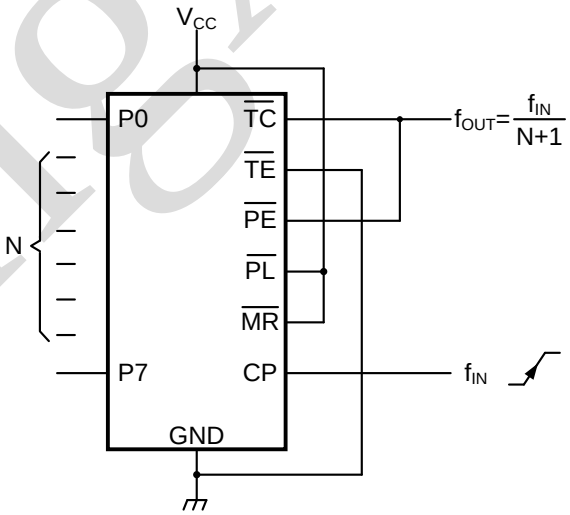
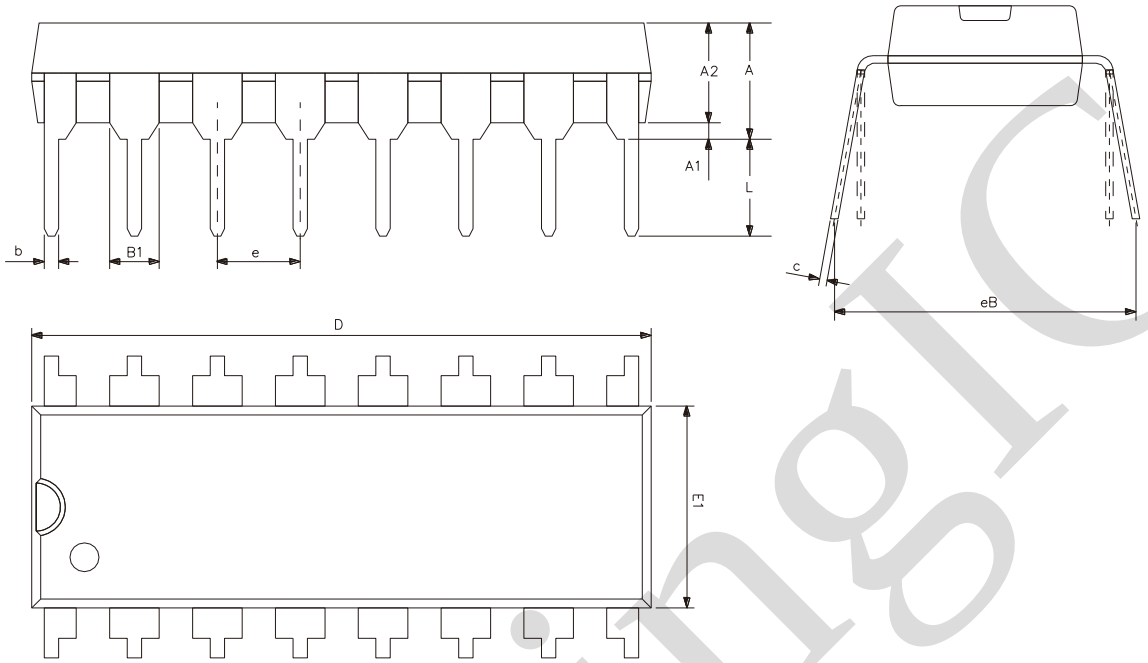


Figure 14. Divide-by-N counter

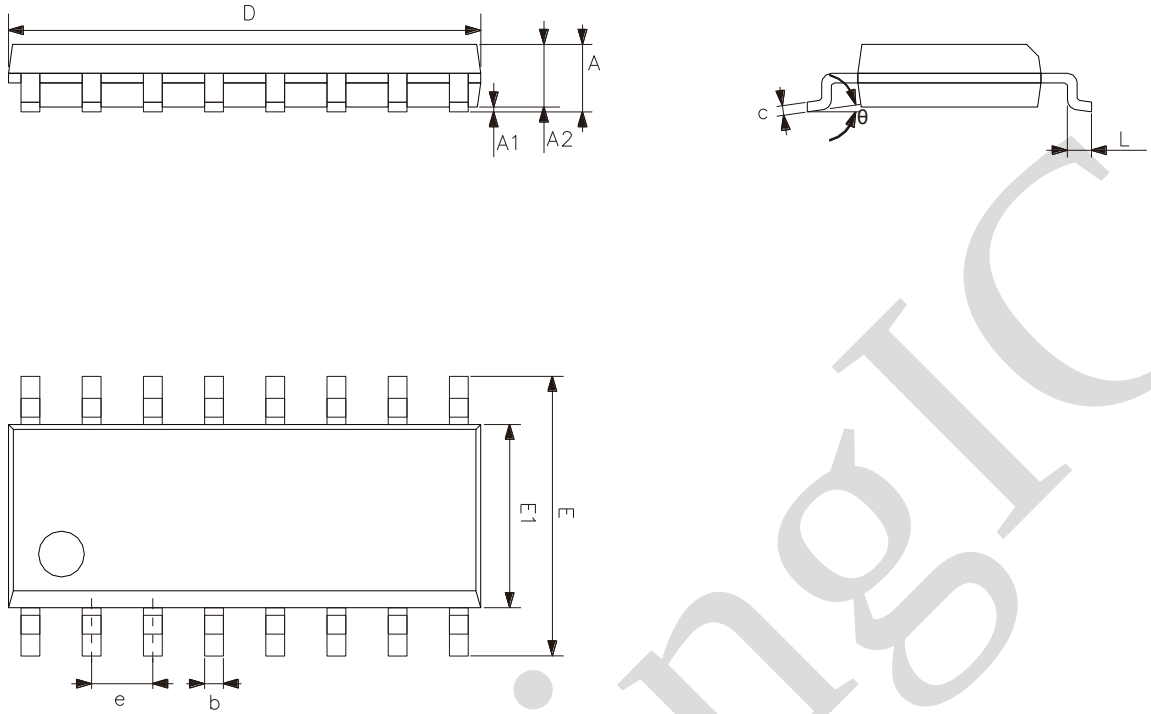
6、Package Information

6.1、DIP16



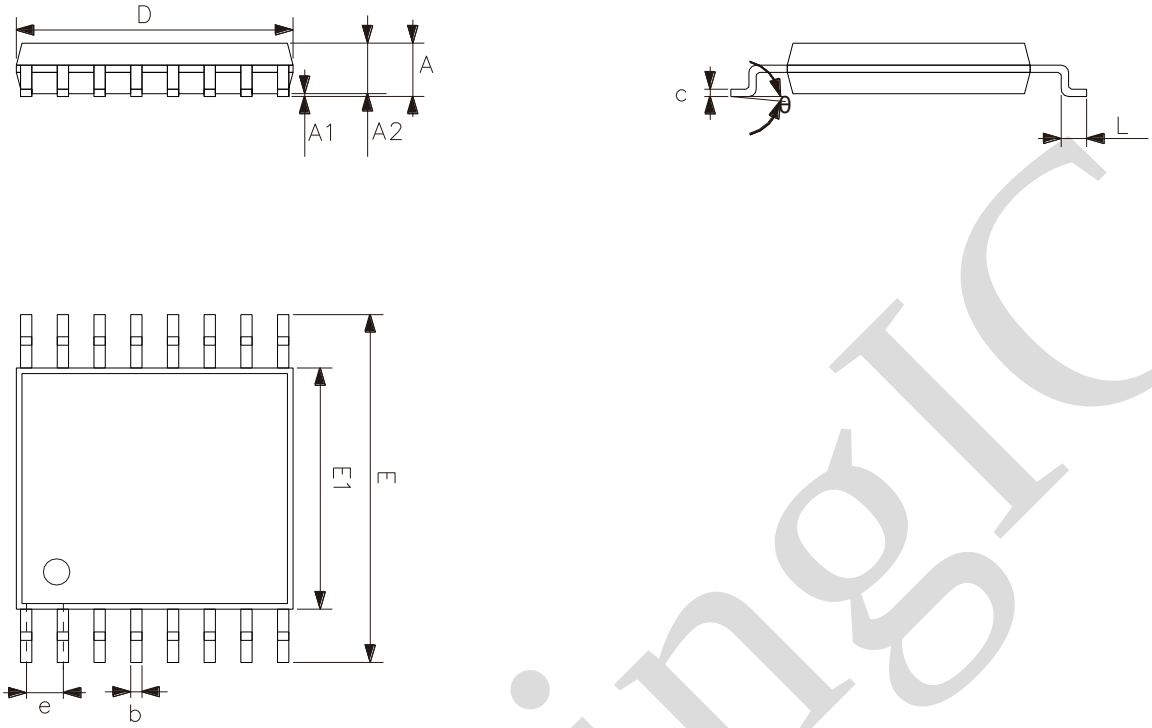
Symbol	Dimensions (mm)	
	Min.	Max.
A2	3.20	3.60
A1	0.51	-
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
c	0.20	0.36
eB	7.62	9.30

6.2、SOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°

6.3、TSSOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°

7、Statements And Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notes

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