CD4013(LX)
Dual D-type Flip-Flop

Product Specification

Specification Revision History：

Version	Date	Description
2021-12-A1	2021-12	New

1、General Description

The CD4013 is a dual D-type flip-flop that features independent set-direct input (SD), clear-direct input (CD), clock input (CP) and outputs (Q, $\overline{Q}$). Data is accepted when CP is LOW and is transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous CD and SD inputs are independent and override the D or CP inputs. The outputs are buffered for best system performance. The clock input's Schmitt-trigger action makes the circuit highly tolerant of slower clock rise and fall times.
It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

Features:

- Wide supply voltage range from 3V to 15V
- Fully static operation
- 5V, 10V, and 15V parametric ratings
- Standardized symmetrical output characteristics
- Tolerant of slow clock rise and fall times
- Specified from -40℃ to +85℃
- Packaging information: DIP14/SOP14/TSSOP14

Ordering Information:

Tube packing specifications:

Type number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Packing box number	Packing quantity	Notes
CD4013BE(LX)	DIP14	CD4013BE	25 PCS/tube	40 tube/box	1000 PCS/box	10 box/pack	10000 PCS/pack	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm

Reel packing specifications:

Type number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Packing quantity	Notes
CD4013BM(LX)	SOP14	CD4013	4000 PCS/reel	8000 PCS/box	64000 PCS/pack	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 1.27mm
CD4013BPW(LX)	TSSOP14	CD4013	5000 PCS/reel	10000 PCS/box	80000 PCS/pack	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

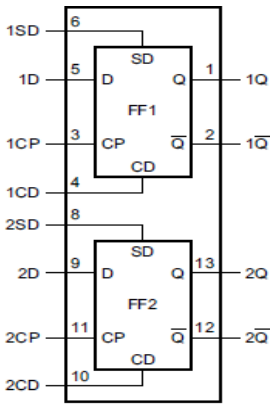


Figure 1. Functional diagram

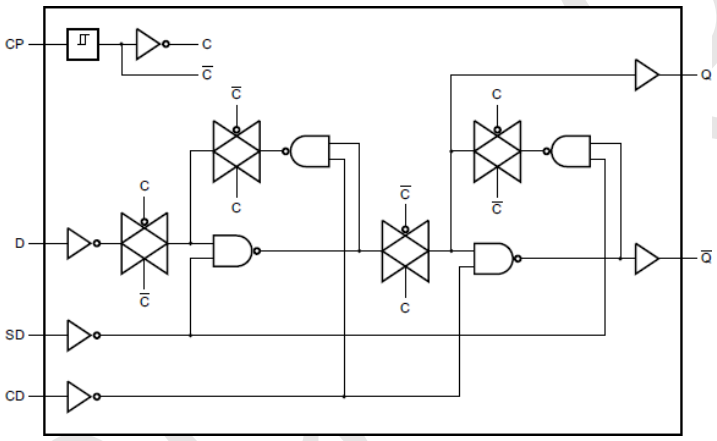
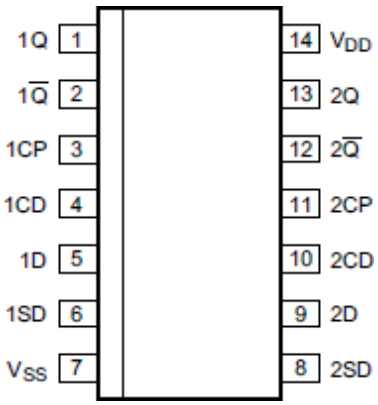


Figure 2. Logic diagram (one flip-flop)

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	1Q	true output
2	$1\bar{Q}$	complement output
3	1CP	clock input (LOW to HIGH edge-triggered)
4	1CD	asynchronous clear-direct input (active HIGH)
5	1D	data input
6	1SD	asynchronous set-direct input (active HIGH)
7	V_{SS}	ground (0V)
8	2SD	asynchronous set-direct input (active HIGH)
9	2D	data input
10	2CD	asynchronous clear-direct input (active HIGH)
11	2CP	clock input (LOW to HIGH edge-triggered)
12	$2\bar{Q}$	complement output
13	2Q	true output
14	V_{DD}	supply voltage

2.4、Function Table

Input				Output	
nSD	**nCD**	**nCP**	**nD**	**nQ**	**$n\bar{Q}$**
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	H	H
L	L	↑	L	L	H
L	L	↑	H	H	L

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care; ↑=LOW-to-HIGH clock transition.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{DD}	-		-0.5	+18	V
DC input current	I_{IK}	any one input		-	±10	mA
input voltage	V_I	all inputs		-0.5	V_{DD}+0.5	V
storage temperature	T_{stg}	-		-65	+150	℃
total power dissipation	P_{tot}	-		-	500	mW
device dissipation	P	per output transistor		-	100	mW
Soldering temperature	T_L	10s	DIP	245		℃
			SOP	250		℃

Note:

[1] For DIP14 packages: above 70℃ the value of P_{tot} derates linearly with 12mW/K.

[2] For SOP14 packages: above 70℃ the value of P_{tot} derates linearly with 8mW/K.

[3] For (T)SSOP14 packages: above 60℃ the value of P_{tot} derates linearly with 5.5mW/K.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-	3	-	15	V
ambient temperature	T_{amb}	in free air	-40	-	+85	℃
set-up time	t_{su}	V_{DD}=5V	40	-	-	ns
		V_{DD}=10V	20	-	-	ns
		V_{DD}=15V	15	-	-	ns
clock pulse width	t_{wCL}	V_{DD}=5V	140	-	-	ns
		V_{DD}=10V	60	-	-	ns
		V_{DD}=15V	40	-	-	ns
clock input frequency	f_{CL}	V_{DD}=5V	3.5	7	-	MHz
		V_{DD}=10V	8	16	-	MHz
		V_{DD}=15V	12	24	-	MHz
clock rise and fall time	t_{rCL}, t_{fCL}	V_{DD}=5V	-	-	15	us
		V_{DD}=10V	-	-	10	us
		V_{DD}=15V	-	-	5	us
Set or reset pulse width	$t_{wS/R}$	V_{DD}=5V	180	-	-	ns
		V_{DD}=10V	80	-	-	ns
		V_{DD}=15V	50	-	-	ns

Note: If more than one unit is cascaded in a parallel clocked operation, t_{rCL} must be made less than or equal to the sum of the fixed propagation delay time at 15pF and the transistion time of the output driving stage for the estimated capacitive load.

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)			T_{amb}=25℃			Unit
		V_O	V_{IN}	V_{DD}	Min.	Typ.	Max.	
supply current	I_{DD}	-	0, 5	5	-	0.02	1	uA
		-	0, 10	10	-	0.02	2	uA
		-	0, 15	15	-	0.02	4	uA
LOW-level output current	I_{OL}	0.4	0, 5	5	0.51	1	-	mA
		0.5	0, 10	10	1.3	2.6	-	mA
		1.5	0, 15	15	3.4	6.8	-	mA
HIGH-level output current	I_{OH}	4.6	0, 5	5	-0.51	-1	-	mA
		2.5	0, 5	5	-1.6	-3.2	-	mA
		9.5	0, 10	10	-1.3	-2.6	-	mA
		13.5	0, 15	15	-3.4	-6.8	-	mA

LOW-level output voltage	V_{OL}	-	0, 5	5	-	0	0.05	V
		-	0, 10	10	-	0	0.05	V
		-	0, 15	15	-	0	0.05	V
HIGH-level output voltage	V_{OH}	-	0, 5	5	4.95	5	-	V
		-	0, 10	10	9.95	10	-	V
		-	0, 15	15	14.95	15	-	V
LOW-level input voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	V
		1, 9	-	10	-	-	3	V
		1.5, 13.5	-	15	-	-	4	V
HIGH-level input voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	V
		1, 9	-	10	7	-	-	V
		1.5, 13.5	-	15	11	-	-	V
input leakage current	I_I	-	0, 15	15	-	$\pm10^{-5}$	±0.1	uA

3.3.2 、DC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)			T_{amb}=-40℃		T_{amb}=+85℃		Unit
		V_O	V_{IN}	V_{DD}	Min.	Max.	Min.	Max.	
supply current	I_{DD}	-	0, 5	5	-	1	-	30	uA
		-	0, 10	10	-	2	-	60	uA
		-	0, 15	15	-	4	-	120	uA
LOW-level output current	I_{OL}	0.4	0, 5	5	0.61	-	0.42	-	mA
		0.5	0, 10	10	1.5	-	1.1	-	mA
		1.5	0, 15	15	4	-	2.8	-	mA
HIGH-level output current	I_{OH}	4.6	0, 5	5	-0.61	-	-0.42	-	mA
		2.5	0, 5	5	-1.8	-	-1.3	-	mA
		9.5	0, 10	10	-1.5	-	-1.1	-	mA
		13.5	0, 15	15	-4	-	-2.8	-	mA
LOW-level output voltage	V_{OL}	-	0, 5	5	-	0.05	-	0.05	V
		-	0, 10	10	-	0.05	-	0.05	V
		-	0, 15	15	-	0.05	-	0.05	V
HIGH-level output voltage	V_{OH}	-	0, 5	5	4.95	-	4.95	-	V
		-	0, 10	10	9.95	-	9.95	-	V
		-	0, 15	15	14.95	-	14.95	-	V
LOW-level input voltage	V_{IL}	0.5, 4.5	-	5	-	1.5	-	1.5	V
		1, 9	-	10	-	3	-	3	V
		1.5, 13.5	-	15	-	4	-	4	V
HIGH-level input voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	V
		1.5, 13.5	-	15	11	-	11	-	V
input leakage current	I_I	-	0, 15	15	-	±0.1	-	±1	uA

3.3.3 、AC Characteristics

(T_{amb}=25℃, V_{SS}=0V, t_r, t_f=20ns, C_L=50pF, R_L=20kΩ, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH to LOW propagation delay	t_{PHL}	nCP to nQ, $\overline{nQ}$; see Figure 4	V_{DD}=5V	-	150	300	ns
			V_{DD}=10V	-	65	130	ns
			V_{DD}=15V	-	45	90	ns
		nSD to $\overline{nQ}$ or nCD to nQ	V_{DD}=5V	-	200	400	ns
			V_{DD}=10V	-	85	170	ns
			V_{DD}=15V	-	60	120	ns
LOW to HIGH propagation delay	t_{PLH}	nCP to nQ, $\overline{nQ}$; see Figure 4	V_{DD}=5V	-	150	300	ns
			V_{DD}=10V	-	65	130	ns
			V_{DD}=15V	-	45	90	ns
		nSD to nQ or nCD to $\overline{nQ}$	V_{DD}=5V	-	150	300	ns
			V_{DD}=10V	-	65	130	ns
			V_{DD}=15V	-	45	90	ns
transition time	t_t	see Figure 4	V_{DD}=5V	-	100	200	ns
			V_{DD}=10V	-	50	100	ns
			V_{DD}=15V	-	40	80	ns
maximum clock frequency	$f_{clk(max)}$	see Figure 4	V_{DD}=5V	3.5	7	-	MHz
			V_{DD}=10V	8	16	-	MHz
			V_{DD}=15V	12	24	-	MHz
pulse width	t_W	nCP input LOW; see Figure 4	V_{DD}=5V	-	70	140	ns
			V_{DD}=10V	-	30	60	ns
			V_{DD}=15V	-	20	40	ns
		nSD input HIGH or nCD input HIGH; see Figure 5	V_{DD}=5V	-	90	180	ns
			V_{DD}=10V	-	40	80	ns
			V_{DD}=15V	-	25	50	ns
set-up time	t_{su}	nD to nCP; see Figure 4	V_{DD}=5V	-	20	40	ns
			V_{DD}=10V	-	10	20	ns
			V_{DD}=15V	-	7	15	ns
hold time	t_h	nD to nCP; see Figure 4	V_{DD}=5V	-	2	5	ns
			V_{DD}=10V	-	2	5	ns
			V_{DD}=15V	-	2	5	ns
clock input rise or fall time	t_{rCL}, t_{fCL}	-	V_{DD}=5V	-	-	15	us
			V_{DD}=10V	-	-	10	us
			V_{DD}=15V	-	-	5	us
input capacitance	C_I	any input		-	5	7.5	pF

Note: t_t is the same as t_{TLH} and t_{THL}.

4、Testing Circuit

4.1、AC Testing Circuit

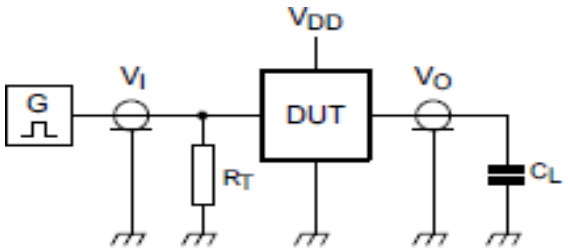


Figure 3. Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

4.2、AC Testing Waveforms

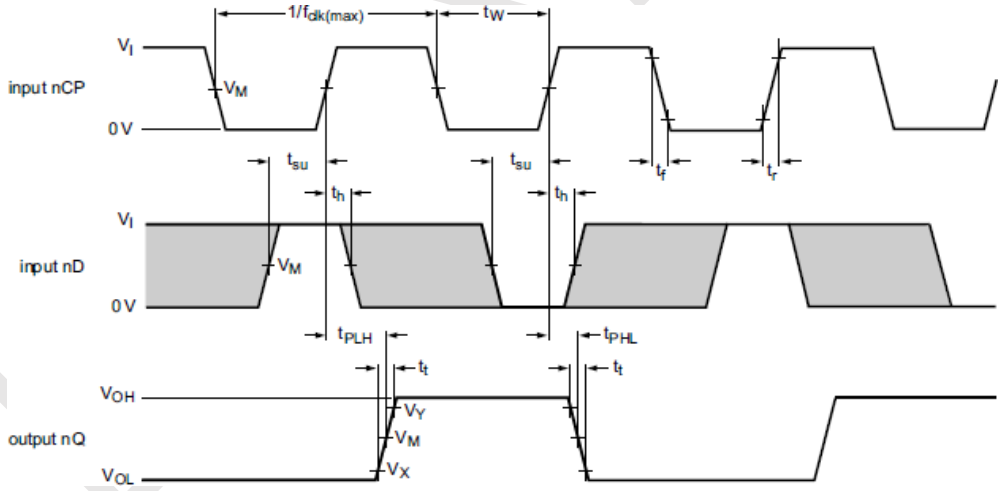


Figure 4. Set-up time, hold time, minimum clock pulse width, propagation delays and transition times

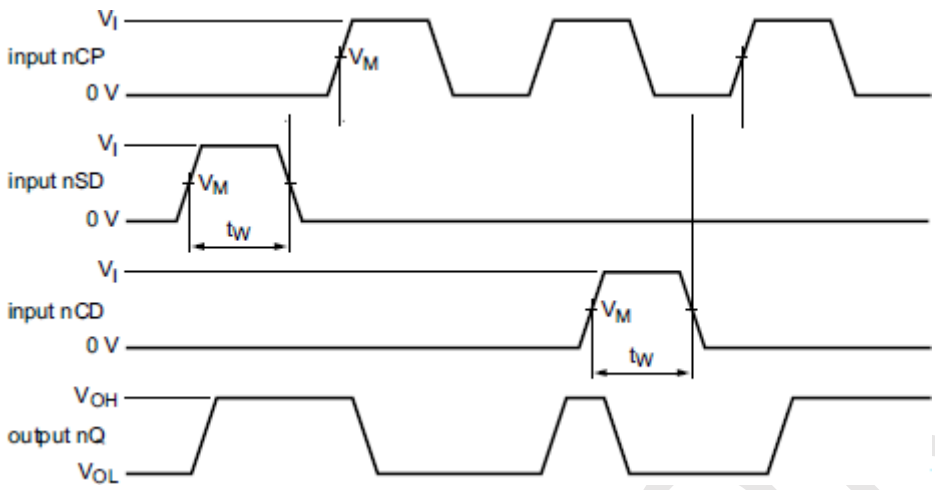


Figure 5. nSD, nCD pulse width

4.3、Measurement Points

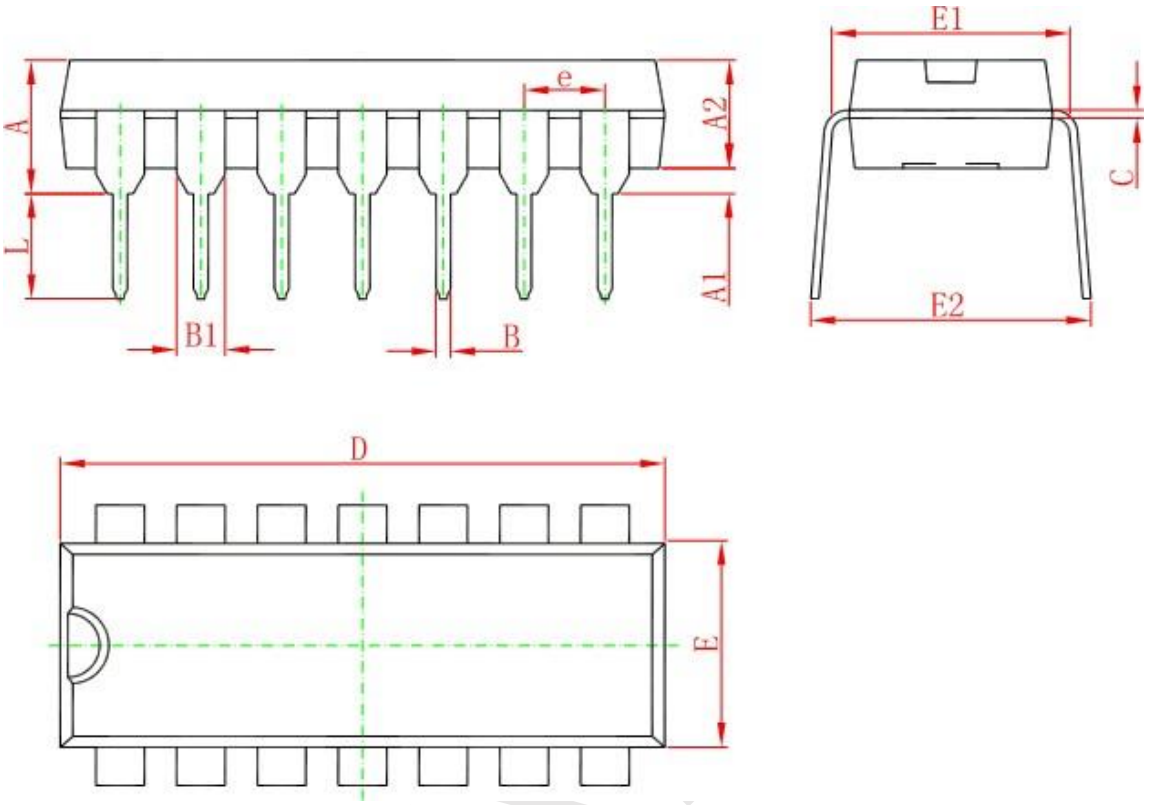
Supply voltage	Input	Output		
V_{DD}	V_M	V_M	V_X	V_Y
5V to 15V	$0.5\times V_{DD}$	$0.5\times V_{DD}$	$0.1\times V_{DD}$	$0.9\times V_{DD}$

4.4、Test Data

Supply voltage	Input		Load
V_{DD}	V_I	t_r , t_f	C_L
5V to 15V	V_{SS} or V_{DD}	≤ 20ns	50pF

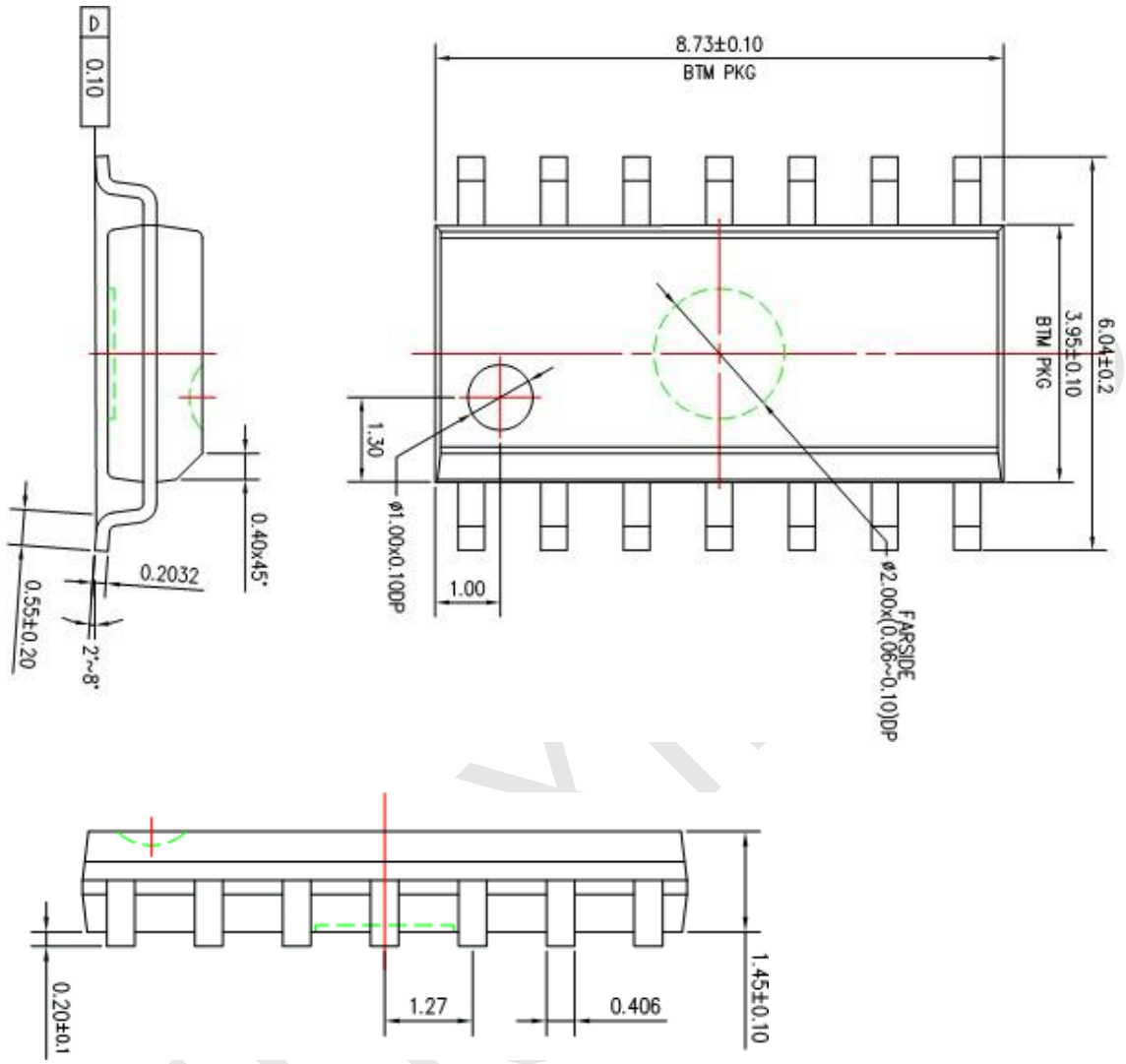
5、Package Information

5.1、DIP14

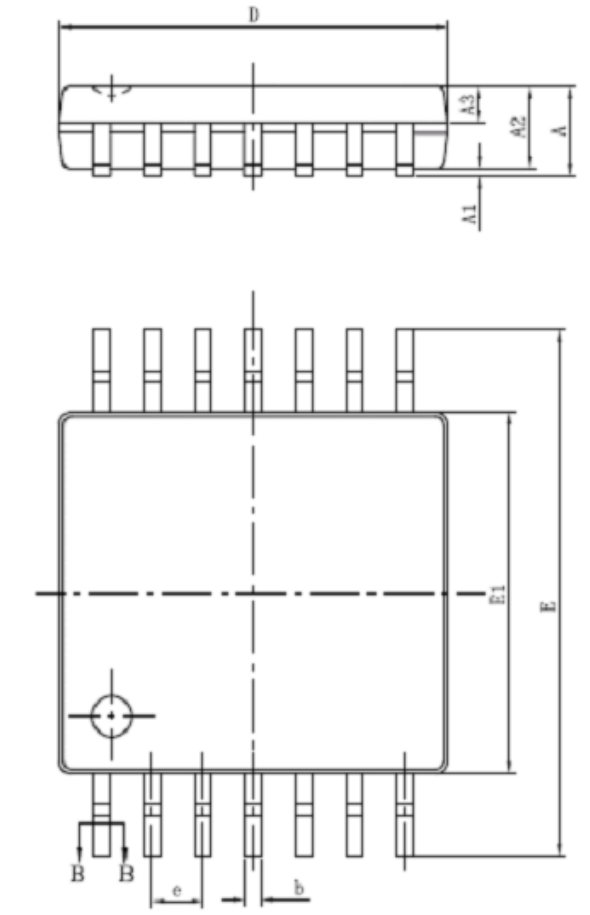


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	18.800	19.200	0.740	0.756
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

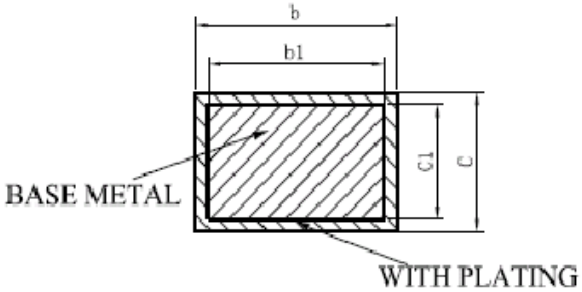
5.2、SOP14


0.10
8.73±0.10
BTM PKG
6.04±0.2
3.95±0.10
BTM PKG
1.30
ø1.00x0.10DP
1.00
ø2.00x(0.06~0.10)DP
FARSIDE
0.40x45°
0.2032
0.55±0.20
2°~8°
1.45±0.10
0.20±0.1
1.27
0.406

5.3、TSSOP14



SYMBOL	MILLIMETER	
	MIN	MAX
A	—	1.20
A1	0.05	0.15
A2	0.90	1.05
A3	0.39	0.49
b	0.20	0.30
b1	0.19	0.25
c	0.13	0.19
c1	0.12	0.14
D	4.86	5.06
E1	4.30	4.50
E	6.20	6.60
e	0.65BSC	
L	0.45	0.75
L1	1.00BSC	
θ	0	8°



SECTION B-B

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard。 ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements。									

6.2、Notion

Recommended carefully reading this information before the use of this product；

The information in this document are subject to change without notice；

This information is using to the reference only, the company is not responsible for any loss；

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Flip-Flops ***category:***

Click to view products by lingxingic ***manufacturer:***

Other Similar products are found below :

NLV74HC74ADTR2G 74F574SC NLV14013BDR2G NLV74HC74ADR2G MC10EP131MNG MC74AC74DTR2 74VHC574FT(BJ) HT4093ARZ SN74HC374ANSR CD4528BE CD4027BE RS74HC74XQ RS1G79XC5 CD40106BM-JSM 74HCT273PW-Q100J CLVC2G74QDCURG4Q1 CD4067TA24.TB CD4013SA.TR AIP74HCT14TA14.TB CD4013BPWRG AiP74LVC74TA14.TB CD4013BDRG CD4528SA16.TR AIP74HC273SA.TB SN74HCS74QDYYRQ1 CD4013TA14.TB SN74LS107N SN74LS374DWR SN74LVC2G14DC(LX) 74VHCT574AFT TC4013BF(EL,N,F) 74VHCT9541AFT 74LCX374FT(AJ) TC7WZ74FK,LXGJ(CT 74LCX374FT 74VHC174FT(TB,BJ) TC7WH74FK,LJ SN74HC374PW(LX) SN74LVC1G17DC(LX) SN74HC174DR(LX) SN74HC112N(LX) SN74HC74DR(LX) CD40174BE(LX) CD40175BE(LX) SN74LS374N SN74HC173N SN74HC107DR(LX) SN74HC107N(LX) SN74LS174DR(LX) SN74LS273N(LX)