



# CD4043 (LX) Quad R/S Latch With 3-state Outputs

## Product Specification

### Specification Revision History:

Version	Date	Description
2022-06-A1	2022-06	New
2023-04-B1	2023-04	Update the template



# Contents

<b>1、 General Description.....</b>	<b>1</b>
<b>2、 Block Diagram And Pin Description .....</b>	<b>3</b>
2.1、 Block Diagram .....	3
2.2、 Pin Configurations.....	3
2.3、 Pin Description .....	4
2.4、 Function Table.....	4
<b>3、 Electrical Parameter .....</b>	<b>4</b>
3.1、 Absolute Maximum Ratings.....	4
3.2、 Recommended Operating Conditions .....	5
3.3、 Electrical Characteristics .....	5
3.3.1、 DC Characteristics 1 .....	5
3.3.2、 DC Characteristics 2 .....	6
3.3.3、 AC Characteristics .....	7
<b>4、 Testing Circuit .....</b>	<b>8</b>
4.1、 AC Testing Circuit .....	8
4.2、 AC Testing Waveforms.....	9
4.3、 Measurement Points .....	9
4.4、 Test Data .....	9
<b>5、 Package Information .....</b>	<b>10</b>
5.1、 DIP16 .....	10
5.2、 SOP16 .....	11
5.3、 TSSOP16.....	12
<b>6、 Statements And Notes .....</b>	<b>13</b>
6.1、 The name and content of Hazardous substances or Elements in the product.....	13
6.2、 Notes .....	13



## 1、 General Description

The CD4043 is a quad R/S latch with 3-state outputs with a common output enable input (OE). Each latch has an active HIGH set input (1S to 4S), an active HIGH reset input (1R to 4R) and an active HIGH 3-state output (1Q to 4Q).

When OE is HIGH, the latch output (nQ) is determined by the nR and nS inputs as shown in function table. When OE is LOW, the latch outputs are in the high impedance OFF-state. OE does not affect the state of the latch. The high impedance off-state feature allows common bussing of the outputs.

It operates over a recommended  $V_{DD}$  power supply range of 3V to 15V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input.

### Features:

- 5V, 10V, and 15V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to +125°C
- Packaging information: DIP16/SOP16/TSSOP16



**Ordering Information:**

**Tube packing specifications:**

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
CD4043BE(LX)	DIP16	CD4043BE	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing:2.54mm
CD4043BDR(LX)	SOP16	CD4043BDR	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
CD4043BPWR(LX)	TSSOP16	CD4043BPWR	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm

**Reel packing specifications:**

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
CD4043BDR(LX)	SOP16	CD4043BDR	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
CD4043BPWR(LX)	TSSOP16	CD4043BPWR	5000PCS/reel	10000PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.



## 2、Block Diagram And Pin Description

### 2.1、Block Diagram

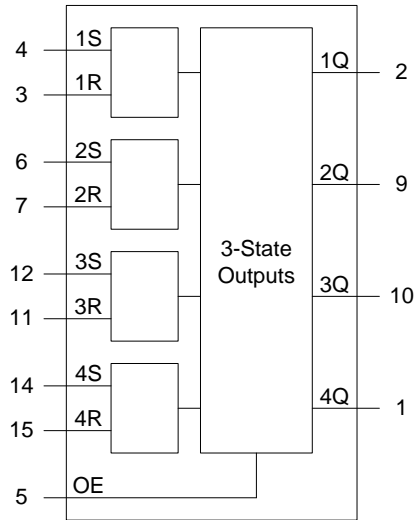


Figure 1. Functional diagram

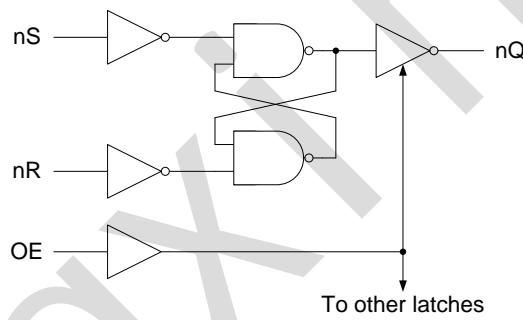
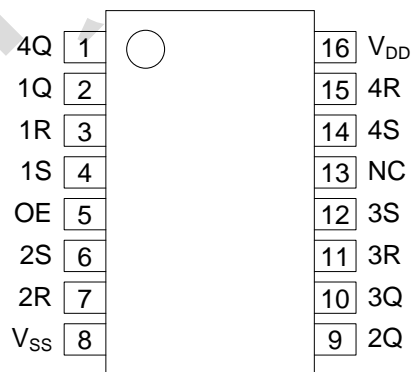


Figure 2. Logic diagram for one latch

### 2.2、Pin Configurations





### 2.3、Pin Description

Pin No.	Pin Name	Description
1	4Q	3-state buffered latch output
2	1Q	3-state buffered latch output
3	1R	reset input (active HIGH)
4	1S	set input (active HIGH)
5	OE	common output enable input
6	2S	set input (active HIGH)
7	2R	reset input (active HIGH)
8	V <sub>SS</sub>	ground supply voltage
9	2Q	3-state buffered latch output
10	3Q	3-state buffered latch output
11	3R	reset input (active HIGH)
12	3S	set input (active HIGH)
13	NC	not connected
14	4S	set input (active HIGH)
15	4R	reset input (active HIGH)
16	V <sub>DD</sub>	supply voltage

### 2.4、Function Table

Inputs			Output
OE	nS	nR	nQ
L	X	X	Z
H	L	H	L
H	H	X	H
H	L	L	latched

Note: [1] H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high impedance state.

## 3、Electrical Parameter

### 3.1、Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V <sub>DD</sub>	-	-0.5	+18	V
input clamping current	I <sub>IK</sub>	V <sub>I</sub> <-0.5V or V <sub>I</sub> >V <sub>DD</sub> +0.5V	-	±10	mA
input voltage	V <sub>I</sub>	-	-0.5	V <sub>DD</sub> +0.5	V
output clamping current	I <sub>OK</sub>	V <sub>O</sub> <-0.5V or V <sub>O</sub> >V <sub>DD</sub> +0.5V	-	±10	mA
output current	I <sub>O</sub>	V <sub>O</sub> =0V to V <sub>CC</sub>	-	±10	mA
supply current	I <sub>DD</sub>	-	-	50	mA
total power dissipation	P <sub>tot</sub>	-	-	500	mW
power dissipation	P <sub>D</sub>	per output	-	100	mW
storage temperature	T <sub>stg</sub>	-	-65	+150	°C
soldering temperature	T <sub>L</sub>	10s	DIP	245	°C
			SOP/TSSOP	260	°C



### 3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	$V_{DD}$	-	3	-	15	V
input voltage	$V_I$	-	0	-	$V_{DD}$	V
ambient temperature	$T_{amb}$	-	-40	-	+125	°C

### 3.3、Electrical Characteristics

#### 3.3.1、DC Characteristics 1

( $T_{amb}=25^{\circ}\text{C}$ , voltages are referenced to  $V_{SS}$  (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions (V)			$T_{amb}=25^{\circ}\text{C}$			Unit
		$V_O$	$V_{IN}$	$V_{DD}$	Min.	Typ.	Max.	
supply current	$I_{DD}$	-	0, 5	5	-	-	20	uA
		-	0, 10	10	-	-	40	uA
		-	0, 15	15	-	-	80	uA
LOW-level output current	$I_{OL}$	0.4	0, 5	5	0.44	-	-	mA
		0.5	0, 10	10	1.1	-	-	mA
		1.5	0, 15	15	3.0	-	-	mA
HIGH-level output current	$I_{OH}$	4.6	0, 5	5	-	-	-0.44	mA
		2.5	0, 5	5	-	-	-1.4	mA
		9.5	0, 10	10	-	-	-1.1	mA
		13.5	0, 15	15	-	-	-3.0	mA
LOW-level output voltage	$V_{OL}$	-	0, 5	5	-	-	0.05	V
		-	0, 10	10	-	-	0.05	V
		-	0, 15	15	-	-	0.05	V
HIGH-level output voltage	$V_{OH}$	-	0, 5	5	4.95	-	-	V
		-	0, 10	10	9.95	-	-	V
		-	0, 15	15	14.95	-	-	V
LOW-level input voltage	$V_{IL}$	0.5, 4.5	-	5	-	-	1.5	V
		1, 9	-	10	-	-	3	V
		1.5, 13.5	-	15	-	-	4	V
HIGH-level input voltage	$V_{IH}$	0.5, 4.5	-	5	3.5	-	-	V
		1, 9	-	10	7	-	-	V
		1.5, 13.5	-	15	11	-	-	V
input leakage current	$I_I$	-	0, 15	15	-	-	±1.0	uA
OFF-state output current	$I_{OZ}$	nQ output HIGH; returned to $V_{DD}$		15	-	-	1.6	uA
		nQ output LOW; returned to $V_{SS}$		15	-	-	1.6	uA
input capacitance	$C_I$	-		-	-	-	7.5	pF



### 3.3.2、DC Characteristics 2

( $T_{amb}=-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , voltages are referenced to  $V_{SS}$  (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions (V)			$T_{amb}=-40^{\circ}\text{C}$		$T_{amb}=+85^{\circ}\text{C}$		$T_{amb}=+125^{\circ}\text{C}$		Unit
		$V_O$	$V_{IN}$	$V_{DD}$	Min.	Max.	Min.	Max.	Min.	Max.	
supply current	$I_{DD}$	-	0, 5	5	-	20	-	150	-	150	uA
		-	0, 10	10	-	40	-	300	-	300	uA
		-	0, 15	15	-	80	-	600	-	600	uA
LOW-level output current	$I_{OL}$	0.4	0, 5	5	0.52	-	0.36	-	0.36	-	mA
		0.5	0, 10	10	1.3	-	0.9	-	0.9	-	mA
		1.5	0, 15	15	3.6	-	2.4	-	2.4	-	mA
HIGH-level output current	$I_{OH}$	4.6	0, 5	5	-	-0.52	-	-0.36	-	-0.36	mA
		2.5	0, 5	5	-	-1.7	-	-1.1	-	-1.1	mA
		9.5	0, 10	10	-	-1.3	-	-0.9	-	-0.9	mA
		13.5	0, 15	15	-	-3.6	-	-2.4	-	-2.4	mA
LOW-level output voltage	$V_{OL}$	-	0, 5	5	-	0.05	-	0.05	-	0.05	V
		-	0, 10	10	-	0.05	-	0.05	-	0.05	V
		-	0, 15	15	-	0.05	-	0.05	-	0.05	V
HIGH-level output voltage	$V_{OH}$	-	0, 5	5	4.95	-	4.95	-	4.95	-	V
		-	0, 10	10	9.95	-	9.95	-	9.95	-	V
		-	0, 15	15	14.95	-	14.95	-	14.95	-	V
LOW-level input voltage	$V_{IL}$	0.5, 4.5	-	5	-	1.5	-	1.5	-	1.5	V
		1, 9	-	10	-	3	-	3	-	3	V
		1.5, 13.5	-	15	-	4	-	4	-	4	V
HIGH-level input voltage	$V_{IH}$	0.5, 4.5	-	5	3.5	-	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	7	-	V
		1.5, 13.5	-	15	11	-	11	-	11	-	V
input leakage current	$I_I$	-	0, 15	15	-	$\pm 1.0$	-	$\pm 1.0$	-	$\pm 1.0$	uA
OFF-state output current	$I_{OZ}$	nQ output HIGH; returned to $V_{DD}$		15	-	1.6	-	12	-	12	uA
		nQ output LOW; returned to $V_{SS}$		15	-	1.6	-	12	-	12	uA





### 3.3.3、AC Characteristics

( $T_{amb}=25^{\circ}\text{C}$ ,  $V_{SS}=0\text{V}$ , unless otherwise specified)

Parameter	Symbol	Conditions	$V_{DD}$	Min.	Typ.	Max.	Unit
HIGH to LOW propagation delay	$t_{PHL}$	nR→nQ; see Figure 4	5 <sup>[1]</sup>	-	90	180	ns
			10	-	35	70	ns
			15	-	25	50	ns
LOW to HIGH propagation delay	$t_{PLH}$	nS→nQ; see Figure 4	5 <sup>[1]</sup>	-	65	135	ns
			10	-	25	50	ns
			15	-	15	35	ns
transition time	$t_{THL}$ , $t_{TLH}$	nQ output; see Figure 4	5 <sup>[1][2]</sup>	-	60	120	ns
			10	-	30	60	ns
			15	-	30	60	ns
HIGH to OFF-state propagation delay	$t_{PHZ}$	OE→nQ; see Figure 5	5	-	45	90	ns
			10	-	25	50	ns
			15	-	20	40	ns
LOW to OFF-state propagation delay	$t_{PLZ}$	OE→nQ; see Figure 5	5	-	50	100	ns
			10	-	20	40	ns
			15	-	15	30	ns
OFF-state to HIGH propagation delay	$t_{PZH}$	OE→nQ; see Figure 5	5	-	40	80	ns
			10	-	26	60	ns
			15	-	25	50	ns
OFF-state to LOW propagation delay	$t_{PZL}$	OE→nQ; see Figure 5	5	-	45	90	ns
			10	-	30	60	ns
			15	-	30	60	ns
pulse width	$t_w$	nS input HIGH; minimum width; see Figure 4	5	30	15	-	ns
			10	20	10	-	ns
			15	16	8	-	ns
		nR input HIGH; minimum width; see Figure 4	5	30	15	-	ns
			10	20	10	-	ns
			15	16	8	-	ns

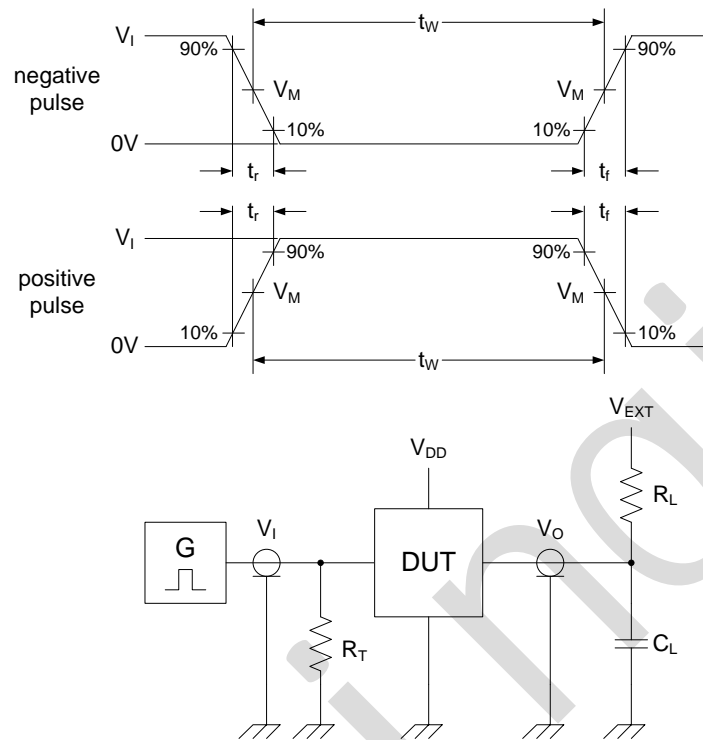
Note:

The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown ( $C_L$  in pF).



## 4、Testing Circuit

### 4.1、AC Testing Circuit



Definitions test circuit:

DUT=Device Under Test.

$R_L$ =Load resistance;

$C_L$ =Load capacitance including jig and probe capacitance.

$R_T$ =Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$ =External voltage for measuring switching times.

Figure 3. Test circuit for measuring switching times



### 4.2、AC Testing Waveforms

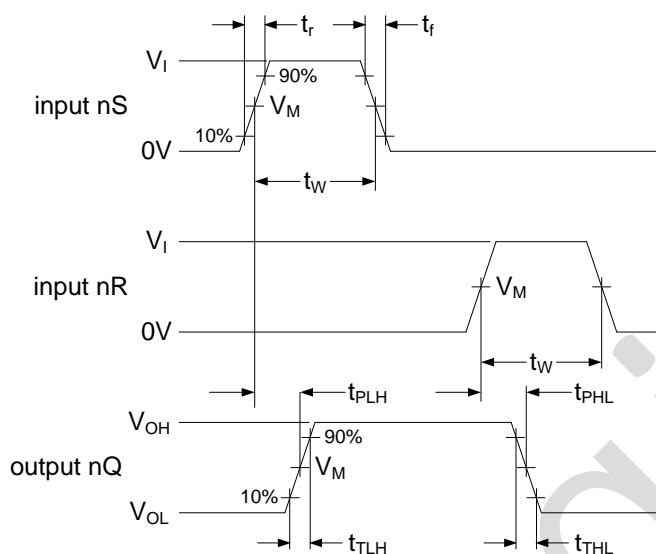


Figure 4. Input minimum set (nS) and reset (nR) pulse widths, inputs nS or nR to latch output (nQ) propagation delay and nQ transition time

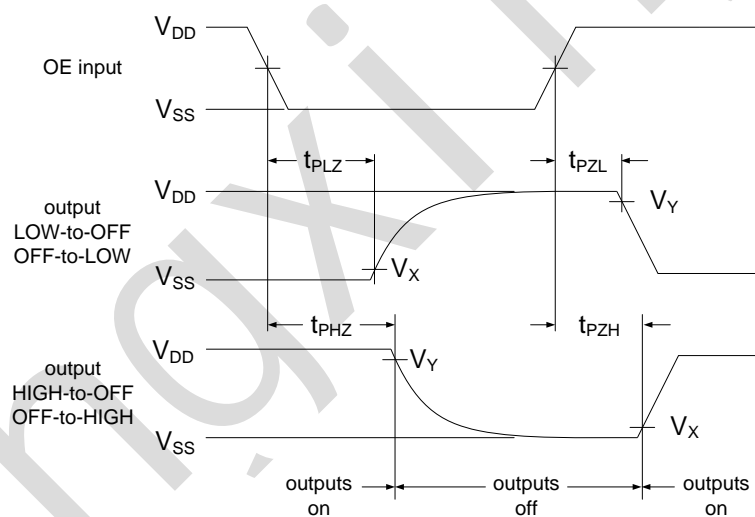


Figure 5. Output enable (OE) to latch output (nQ) enable time ( $t_{PZL}$  and  $t_{PZH}$ ) and disable time ( $t_{PLZ}$  and  $t_{PHZ}$ )

### 4.3、Measurement Points

Supply voltage	Input		Output		
$V_{DD}$	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
5V to 15V	$V_{DD}$ or 0V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$	$0.1 \times V_{DD}$	$0.9 \times V_{DD}$

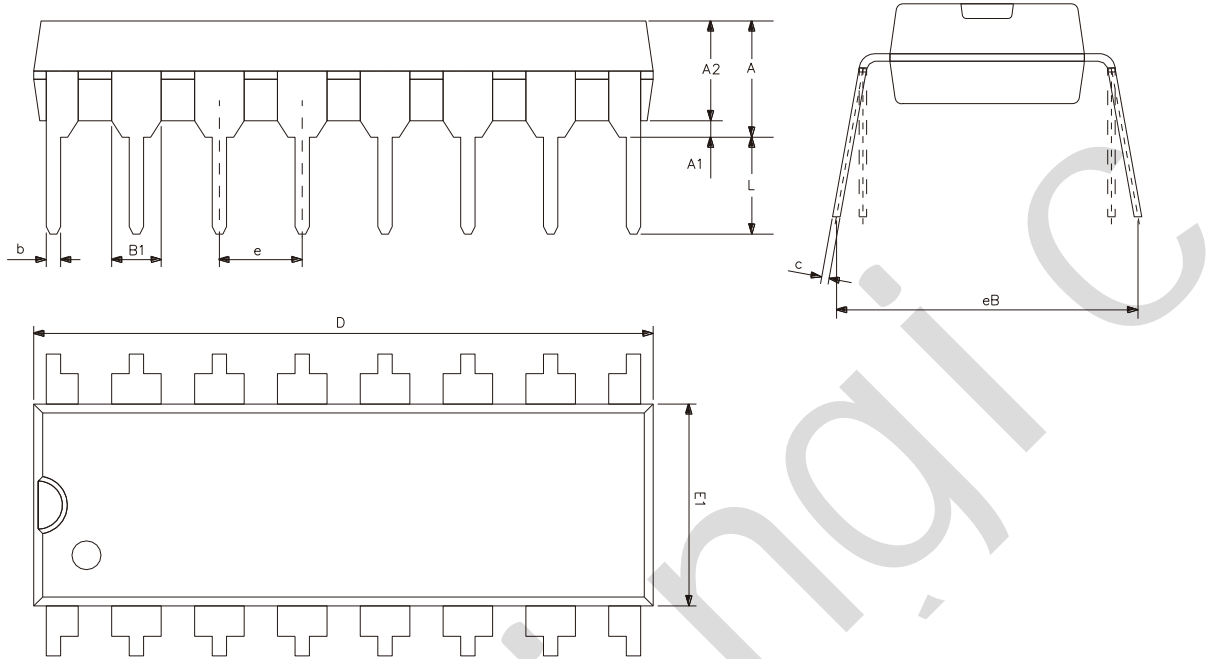
### 4.4、Test Data

Supply voltage	Input		Load		$V_{EXT}$		
$V_{DD}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
5V to 15V	$V_{DD}$	$\leq 20\text{ns}$	50pF	1k $\Omega$	open	$V_{DD}$	GND



## 5、Package Information

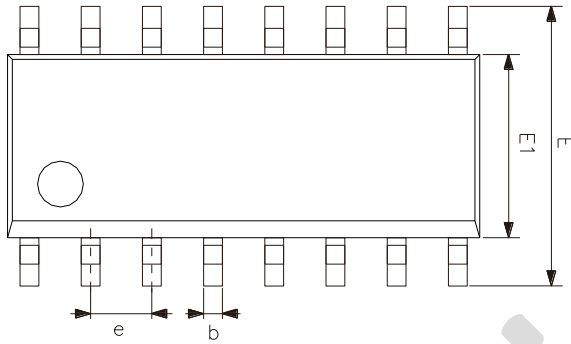
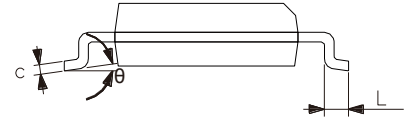
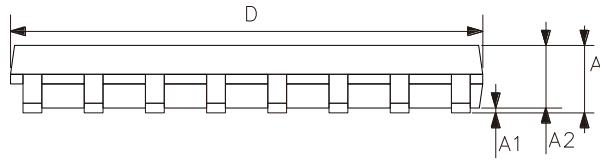
### 5.1、DIP16



Symbol	Dimensions (mm)	
	Min.	Max.
A2	3.20	3.60
A1	0.51	-
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
c	0.20	0.36
eB	7.62	9.30



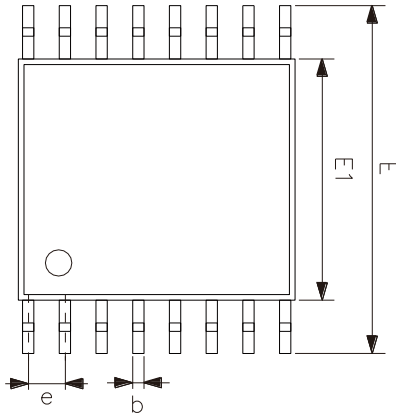
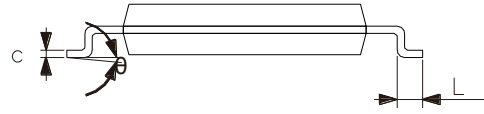
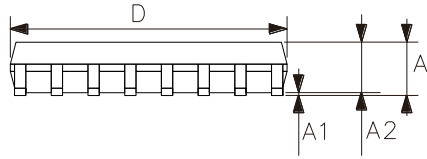
## 5.2、SOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°



### 5.3、TSSOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
$\theta$	0°	8°



## 6、 Statements And Notes

### 6.1、 The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

### 6.2、 Notes

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