CD4049 (LX)
Hex Inverting Buffer

Product Specification

Specification Revision History:

Version	Date	Description
2021-11-A1	2021-11	New
2023-04-B1	2023-04	Update the template

Contents

1、General Description

The CD4049 provides six inverting buffers with high current output capability suitable for driving TTL or high capacitive loads. Since input voltages in excess of the buffers' supply voltage are permitted, the buffers may also be used to convert logic levels of up to 15V to standard TTL levels.

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

Features:

- Wide supply voltage range from 3V to 15V
- Accepts input voltages in excess of the supply voltage
- 5V, 10V, and 15V parametric ratings
- Specified from -40℃ to +125℃
- Packaging information: DIP16/SOP16/TSSOP16

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
CD4049BE(LX)	DIP16	CD4049BE	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
CD4049BM(LX)	SOP16	CD4049BM	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
CD4049BPW(LX)	TSSOP16	CD4049	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
CD4049BM(LX)	SOP16	CD4049BM	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
CD4049BPW(LX)	TSSOP16	CD4049	5000PCS/reel	10000PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

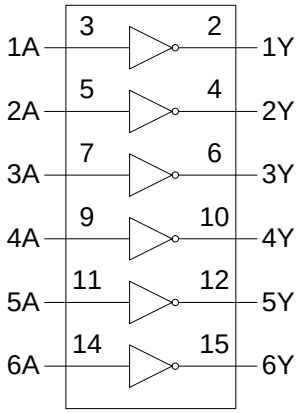


Figure 1. Logic symbol

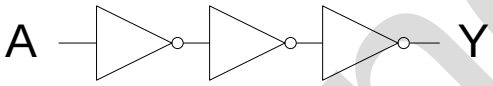


Figure 2. Logic diagram for one gate

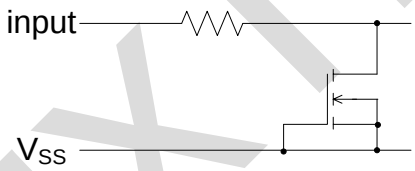


Figure 3. Input protection circuit

2.2、Pin Configurations

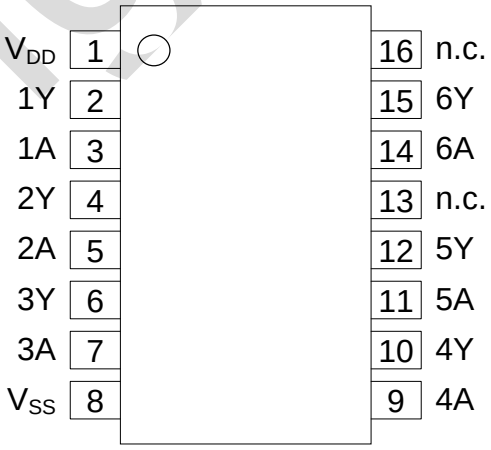


Figure 4. Pin configuration

2.3、Pin Description

Pin No.	Pin Name	Description
1	V_{DD}	supply voltage
2	1Y	data output
3	1A	data input
4	2Y	data output
5	2A	data input
6	3Y	data output
7	3A	data input
8	V_{SS}	ground supply voltage
9	4A	data input
10	4Y	data output
11	5A	data input
12	5Y	data output
13	n.c.	not connected
14	6A	data input
15	6Y	data output
16	n.c.	not connected

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(T_{amb}=25℃, All voltage referenced to Vss, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{DD}	-		-0.5	+18	V
DC input current	I_{IK}	V_I<-0.5V		-10	-	mA
input voltage	V_I	-		-0.5	+18	V
output clamping current	I_{OK}	V_O<-0.5V or V_O>V_{DD}+0.5V		-	±10	mA
input/output current	$I_{I/O}$	-		-	±10	mA
supply current	I_{DD}	-		-	50	mA
storage temperature	T_{stg}	-		-65	+150	℃
soldering temperature	T_L	10s	DIP	245		℃
			SOP/TSSOP	260		

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-	3	-	15	V
input voltage	V_I	-	0	-	15	V
ambient temperature	T_{amb}	in free air	-40	-	+125	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions (V)			T_{amb}=25℃			Unit
		V_O	V_{IN}	V_{DD}	Min.	Typ.	Max.	
supply current	I_{DD}	-	0, 5	5	-	-	4	uA
		-	0, 10	10	-	-	8	uA
		-	0, 15	15	-	-	16	uA
LOW-level output current	I_{OL}	0.4	0, 5	5	2.9	-	-	mA
		0.5	0, 10	10	10	-	-	mA
		1.5	0, 15	15	20	-	-	mA
HIGH-level output current	I_{OH}	4.6	0, 5	5	-	-	-0.44	mA
		2.5	0, 5	5	-	-	-1.4	mA
		9.5	0, 10	10	-	-	-1.1	mA
		13.5	0, 15	15	-	-	-3	mA
LOW-level output voltage	V_{OL}	-	0, 5	5	-	-	0.05	V
		-	0, 10	10	-	-	0.05	V
		-	0, 15	15	-	-	0.05	V
HIGH-level output voltage	V_{OH}	-	0, 5	5	4.95	-	-	V
		-	0, 10	10	9.95	-	-	V
		-	0, 15	15	14.95	-	-	V
LOW-level input voltage	V_{IL}	-	0, 5	5	-	-	1.5	V
		-	0, 10	10	-	-	3	V
		-	0, 15	15	-	-	4	V
HIGH-level input voltage	V_{IH}	-	0, 5	5	3.5	-	-	V
		-	0, 10	10	7	-	-	V
		-	0, 15	15	11	-	-	V
input leakage current	I_I	-	0, 15	15	-	-	±1.0	uA

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions (V)			T_{amb}=-40℃		T_{amb}=125℃		Unit
		V_O	V_{IN}	V_{DD}	Min.	Max.	Min.	Max.	
supply current	I_{DD}	-	0, 5	5	-	4	-	30	uA
		-	0, 10	10	-	8	-	60	uA
		-	0, 15	15	-	16	-	120	uA
LOW-level output current	I_{OL}	0.4	0, 5	5	3.5	-	2.3		mA
		0.5	0, 10	10	12	-	8		mA
		1.5	0, 15	15	24	-	16		mA
HIGH-level output current	I_{OH}	4.6	0, 5	5	-	-0.52	-	-0.36	mA
		2.5	0, 5	5	-	-1.7	-	-1.1	mA
		9.5	0, 10	10	-	-1.3		-0.9	mA
		13.5	0, 15	15	-	-3.6		-2.4	mA
LOW-level output voltage	V_{OL}	-	0, 5	5	-	0.05	-	0.05	V
		-	0, 10	10	-	0.05	-	0.05	V
		-	0, 15	15	-	0.05	-	0.05	V
HIGH-level output voltage	V_{OH}	-	0, 5	5	4.95	-	4.95	-	V
		-	0, 10	10	9.95	-	9.95	-	V
		-	0, 15	15	14.95	-	14.95	-	V
LOW-level input voltage	V_{IL}	-	0, 5	5	-	1.5	-	1.5	V
		-	0, 10	10	-	3	-	3	V
		-	0, 15	15	-	4	-	4	V
HIGH-level input voltage	V_{IH}	-	0, 5	5	3.5	-	3.5	-	V
		-	0, 10	10	7	-	7	-	V
		-	0, 15	15	11	-	11	-	V
input leakage current	I_I	-	0, 15	15	-	±1.0	-	±1.0	uA

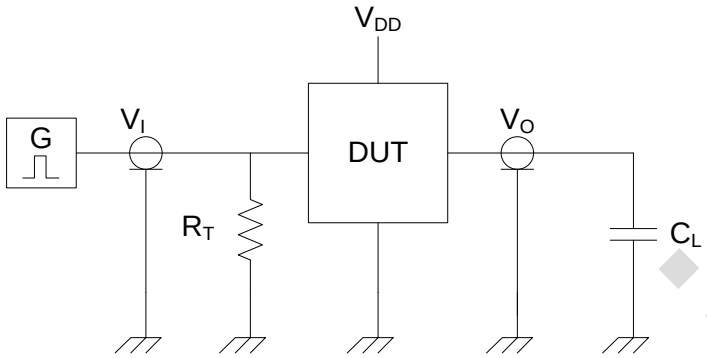
3.3.3、AC Characteristics

(T_{amb}=25℃, V_{SS}=0V; C_L=50pF; t_r=t_f≤20ns, unless otherwise specified)

Parameter	Symbol	Conditions	V_{DD}	Min.	Typ.	Max.	Unit
HIGH to LOW propagation delay	t_{PHL}	nA to nY; see Figure 6	5	-	35	70	ns
			10	-	15	30	ns
			15	-	12	25	ns
LOW to HIGH propagation delay	t_{PLH}	nA to nY; see Figure 6	5	-	50	100	ns
			10	-	25	50	ns
			15	-	20	40	ns
HIGH to LOW output transition time	t_{THL}	see Figure 6	5	-	20	40	ns
			10	-	10	20	ns
			15	-	7	14	ns
LOW to HIGH output transition time	t_{TLH}	see Figure 6	5	-	60	120	ns
			10	-	30	60	ns
			15	-	20	40	ns

4、Testing Circuit

4.1、AC Testing Circuit



Definitions for test circuit:

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to output impedance Z_o of the pulse generator.

Figure 5. Test circuit for measuring switching times

4.2、AC Testing Waveforms

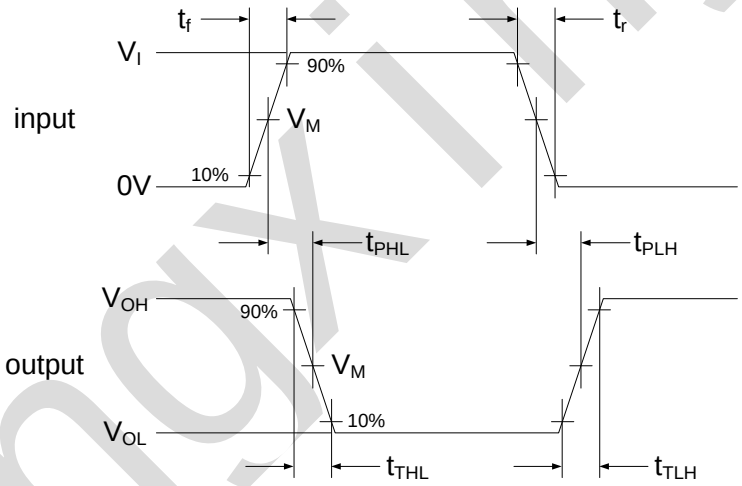


Figure 6. Input (nA) to output (nY) propagation delays and transition times

4.3、Measurement Points

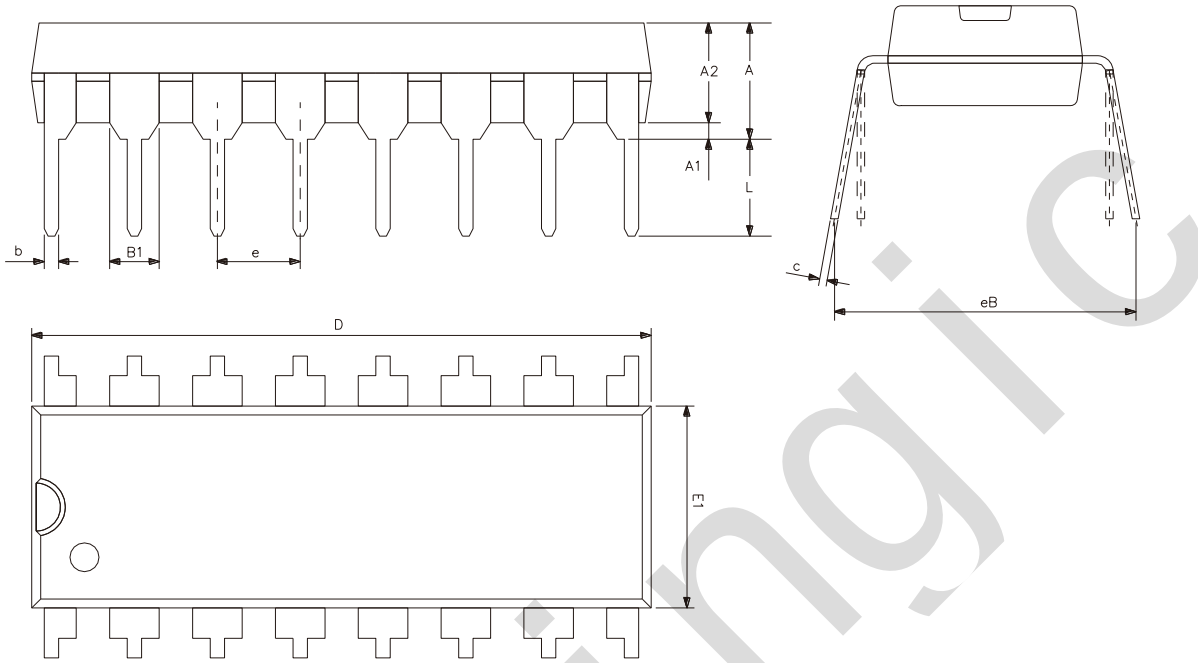
Input		Output		
V_M	**V_I**	**V_M**	**V_X**	**V_Y**
$0.5\times V_{DD}$	0V to V_{DD}	$0.5\times V_{DD}$	$0.1\times V_{DD}$	$0.9\times V_{DD}$

4.4、Test Data

Supply voltage	Input			Load
V_{DD}	**V_I**	**V_M**	**t_r , t_f**	**C_L**
5V to 15V	V_{DD}	$0.5\times V_I$	≤ 20ns	50pF

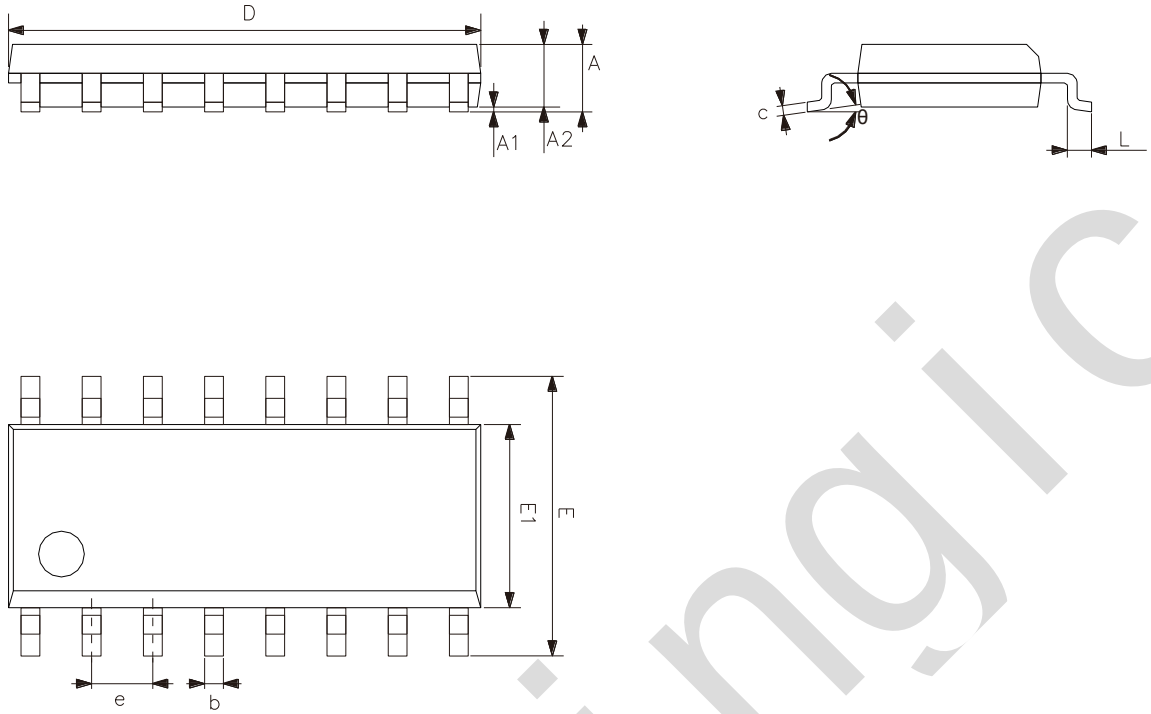
5、Package Information

5.1、DIP16



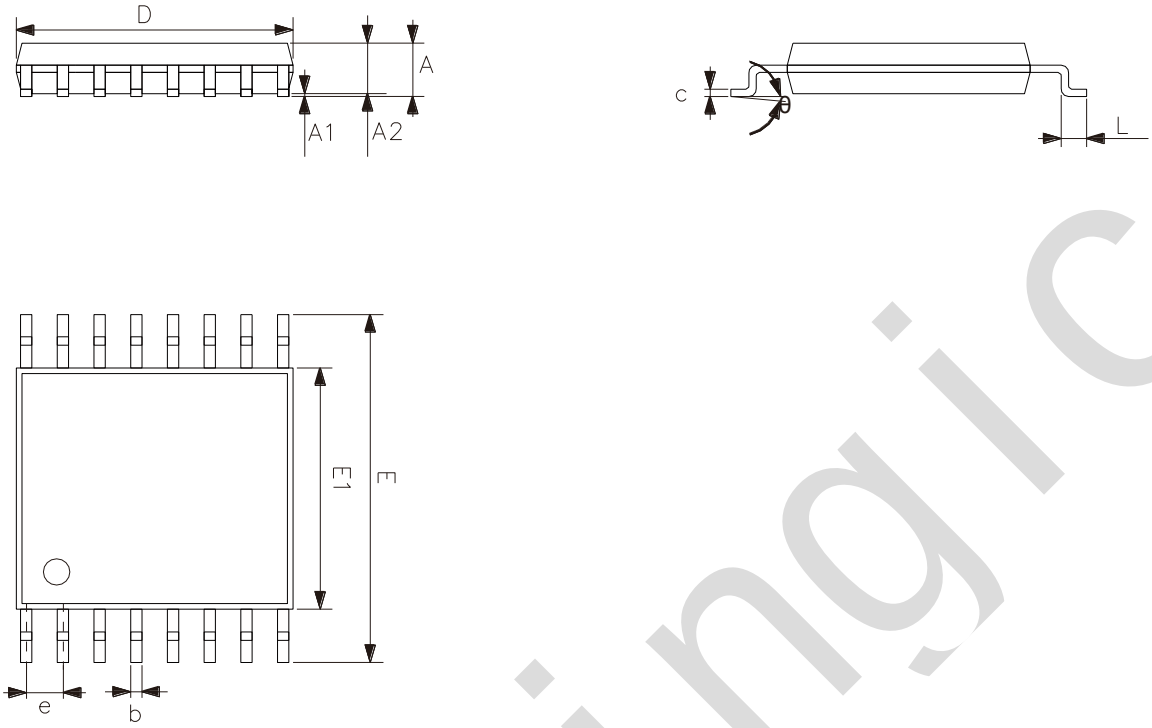
Symbol	Dimensions (mm)	
	Min.	Max.
A2	3.20	3.60
A1	0.51	-
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
c	0.20	0.36
eB	7.62	9.30

5.2、SOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°

5.3、TSSOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

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