CD74HC73/HCT73 (LX)
Dual JK Flip-Flop with Reset; Negative-EdgeTrigger

Product Specification

Specification Revision History:

Version	Date	Description
2023-12-A0	2023-12	New
2024-03-A1	2024-03	Modify the parameters

Contents

1、General Description

The CD74HC/HCT73 is dual negative-edge triggered JK-type flip-flops featuring individual J, K, clock (n$\overline{CP}$) and reset (n$\overline{R}$) inputs; also complementary Q and $\overline{Q}$ outputs.

Features:

- Supply voltage range:
  CD74HC73: 2V to 6V
  CD74HCT73: 4.5V to 5.5V
- Input levels:
  CD74HC73: CMOS level
  CD74HCT73: TTL level
- Temperature range:-40℃ to +125℃
- Packaging information: DIP14/SOP14

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
CD74HC73E(LX)	DIP14	CD74HC73E	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
CD74HCT73E(LX)	DIP14	CD74HCT73E	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
CD74HC73M(LX)	SOP14	HC73M	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 1.27mm
CD74HCT73M(LX)	SOP14	HCT73M	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 1.27mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
CD74HC73M(LX)	SOP14	HC73M	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 1.27mm
CD74HCT73M(LX)	SOP14	HCT73M	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 1.27mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

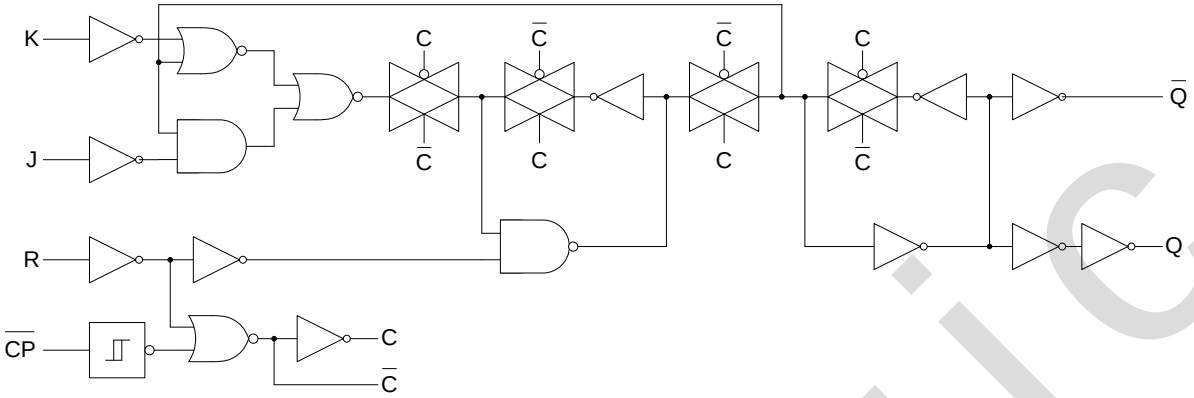


Figure 1. Logic symbol

2.2、Pin Configurations

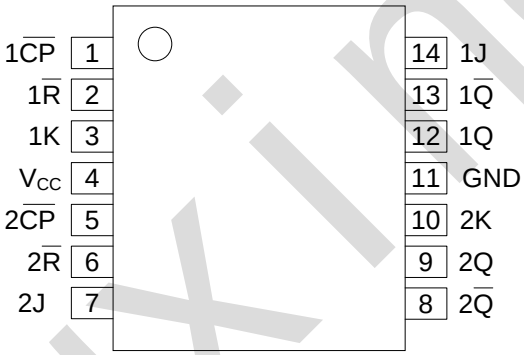


Figure 2. Pin Configurations

2.3、Pin Description

Pin No.	Pin Name	Description
1	$1\overline{CP}$	clock input (HIGH-to-LOW edge-triggered)
2	$1\overline{R}$	asynchronous reset input (active LOW)
3	1K	synchronous K input
4	V_{CC}	supply voltage
5	$2\overline{CP}$	clock input (HIGH-to-LOW edge-triggered)
6	$2\overline{R}$	asynchronous reset input (active LOW)
7	2J	synchronous J input
8	$2\overline{Q}$	complement output
9	2Q	true output
10	2K	synchronous K input
11	GND	ground (0V)
12	1Q	true output
13	$1\overline{Q}$	complement output
14	1J	synchronous J input

2.4、Function Table

Input				Output		Operating mode
$\overline{nR}$	$\overline{nCP}$	nJ	nK	nQ	$\overline{nQ}$	
L	X	X	X	L	H	asynchronous reset
H	↓	h	h	$\overline{q}$	q	toggle
H	↓	l	h	L	H	load 0 (reset)
H	↓	h	l	H	L	load 1 (set)
H	↓	l	l	q	$\overline{q}$	hold (no change)

Notes:
H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW clock transition;
L = LOW voltage level;
I = LOW voltage level one set-up time prior to the HIGH-to-LOW clock transition;
q = state of referenced output one set-up time prior to the HIGH-to-LOW clock transition;
X = don't care;
↓= HIGH-to-LOW clock transition.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7	V
supply current	I_{CC}	-		-	50	mA
ground current	I_{GND}	-		-50	-	mA
input clamping current	I_{IK}	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$		-	±20	mA
output clamping current	I_{OK}	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$		-	±20	mA
output current	I_O	$-0.5V < V_O < V_{CC}+0.5V$		-	±25	mA
storage temperature	T_{stg}	-		-65	+150	℃
soldering temperature	T_L	10s	DIP	245		℃
			SOP/TSSOP	260		

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CD74HC73						
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
ambient temperature	T_{amb}	-	-40	-	+125	℃
CD74HCT73						
supply voltage	V_{CC}	-	4.5	5.0	5.5	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
ambient temperature	T_{amb}	-	-40	-	+125	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	V_{CC}	Conditions	Min.	Typ.	Max.	Unit
CD74HC73							
HIGH-level input voltage	V_{IH}	2.0V	-	1.5	1.2	-	V
		4.5V	-	3.15	2.4	-	V
		6.0V	-	4.2	3.2	-	V
LOW-level input voltage	V_{IL}	2.0V	-	-	0.8	0.5	V
		4.5V	-	-	2.1	1.35	V
		6.0V	-	-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	2.0V	I_O=-20uA	1.9	2.0	-	V
		4.5V	I_O=-20uA	4.4	4.5	-	V
		6.0V	I_O=-20uA	5.9	6.0	-	V
		4.5V	I_O=-4.0mA	3.84	4.32	-	V
		6.0V	I_O=-5.2mA	5.34	5.81	-	V
LOW-level output voltage	V_{OL}	2.0V	I_O=20uA	-	0	0.1	V
		4.5V	I_O=20uA	-	0	0.1	V
		6.0V	I_O=20uA	-	0	0.1	V
		4.5V	I_O=4.0mA	-	0.15	0.33	V
		6.0V	I_O=5.2mA	-	0.16	0.33	V
input leakage current	I_I	6.0V	V_I=V_{CC} or GND	-	-	±1	uA
supply current	I_{CC}	6.0V	V_I=V_{CC} or GND;I_O=0A	-	-	80	uA
CD74HCT73							
HIGH-level input voltage	V_{IH}	4.5~5.5V	-	2.0	1.6	-	V
LOW-level input voltage	V_{IL}	4.5~5.5V	-	-	1.2	0.8	V
HIGH-level output voltage	V_{OH}	4.5V	I_O=-20uA	4.4	4.5	-	V
			I_O=-4.0mA	3.84	4.32	-	V
LOW-level output voltage	V_{OL}	4.5V	I_O=20uA	-	0	0.1	V
			I_O=4.0mA	-	0.15	0.33	V
input leakage current	I_I	5.5V	V_I=V_{CC} or GND	-	-	±1	uA
supply current	I_{CC}	5.5V	V_I=V_{CC} or GND;I_O=0A	-	-	80	uA
additional supply current	ΔI_{CC}	4.5~5.5V	One input at V_I=V_{CC}-2.1V; Other inputs at V_{CC} or GND; I_O=0A	-	-	135	uA

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	V_{CC}	Conditions	Min.	Typ.	Max.	Unit
CD74HC73							
HIGH-level input voltage	V_{IH}	2.0V	-	1.5	-	-	V
		4.5V	-	3.15	-	-	V
		6.0V	-	4.2	-	-	V
LOW-level input voltage	V_{IL}	2.0V	-	-	-	0.5	V
		4.5V	-	-	-	1.35	V
		6.0V	-	-	-	1.8	V
HIGH-level output voltage	V_{OH}	2.0V	I_O=-20uA	1.9	-	-	V
		4.5V	I_O=-20uA	4.4	-	-	V
		6.0V	I_O=-20uA	5.9	-	-	V
		4.5V	I_O=-4.0mA	3.7	-	-	V
		6.0V	I_O=-5.2mA	5.2	-	-	V
LOW-level output voltage	V_{OL}	2.0V	I_O=20uA	-	-	0.1	V
		4.5V	I_O=20uA	-	-	0.1	V
		6.0V	I_O=20uA	-	-	0.1	V
		4.5V	I_O=4.0mA	-	-	0.4	V
		6.0V	I_O=5.2mA	-	-	0.4	V
input leakage current	I_I	6.0V	V_I=V_{CC} or GND	-	-	±1	uA
supply current	I_{CC}	6.0V	V_I=V_{CC} or GND;I_O=0A	-	-	160	uA
CD74HCT73							
HIGH-level input voltage	V_{IH}	4.5~5.5V	-	2.0	-	-	V
LOW-level input voltage	V_{IL}	4.5~5.5V	-	-	-	0.8	V
HIGH-level output voltage	V_{OH}	4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-4.0mA	3.7	-	-	V
LOW-level output voltage	V_{OL}	4.5V	I_O=20uA	-	-	0.1	V
			I_O=4.0mA	-	-	0.4	V
input leakage current	I_I	5.5V	V_I=V_{CC} or GND	-	-	±1	uA
supply current	I_{CC}	5.5V	V_I=V_{CC} or GND;I_O=0A	-	-	160	uA
additional supply current	ΔI_{CC}	4.5~5.5V	One input at V_I=V_{CC}-2.1V; Other inputs at V_{CC} or GND; I_O=0A	-	-	147	uA

3.3.3、AC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	V_{CC}	Conditions		Min.	Typ.	Max.	Unit
CD74HC73								
$n\overline{CP}$ to nQ propagation delay	t_{PLH}, t_{PHL}	2.0V	C_L=50pF	see Figure 4	-	52	160	ns
		4.5V	C_L=50pF		-	19	32	ns
		5.0V	C_L=15pF		-	16	-	ns
		6.0V	C_L=50pF			15	27	ns
$n\overline{CP}$ to $n\overline{Q}$ propagation delay		2.0V	C_L=50pF		-	52	200	ns
		4.5V	C_L=50pF		-	19	40	ns
		5.0V	C_L=15pF		-	16	-	ns
		6.0V	C_L=50pF			15	34	ns
$n\overline{R}$ to nQ/$n\overline{Q}$ propagation delay		2.0V	C_L=50pF	see Figure 5	-	52	195	ns
		4.5V	C_L=50pF		-	19	39	ns
		5.0V	C_L=15pF		-	16	-	ns
		6.0V	C_L=50pF			15	26	ns
nQ/$n\overline{Q}$ transition time	t_{THL}, t_{TLH}	2.0V	C_L=50pF	see Figure 4	-	19	95	ns
		4.5V	C_L=50pF		-	7	19	ns
		6.0V	C_L=50pF		-	6	16	ns
$n\overline{CP}$ input HIGH or LOW pulse width	tw	2.0V	C_L=50pF	see Figure 4	100	22	-	ns
		4.5V	C_L=50pF		20	8	-	ns
		6.0V	C_L=50pF		17	6	-	ns
$n\overline{R}$ input, HIGH pulse width		2.0V	C_L=50pF	see Figure 5	100	22	-	ns
		4.5V	C_L=50pF		20	8	-	ns
		6.0V	C_L=50pF		17	6	-	ns
$n\overline{R}$ to $n\overline{CP}$ recovery time	trec	2.0V	C_L=50pF	see Figure 5	75	19	-	ns
		4.5V	C_L=50pF		15	7	-	ns
		6.0V	C_L=50pF		13	6	-	ns
nJ,nK to $n\overline{CP}$ set-up time	tsu	2.0V	C_L=50pF	see Figure 4	125	22	-	ns
		4.5V	C_L=50pF		25	8	-	ns
		6.0V	C_L=50pF		21	6	-	ns
nJ,nK to $n\overline{CP}$ hold time	th	2.0V	C_L=50pF	see Figure 4	3	-6	-	ns
		4.5V	C_L=50pF		3	-2	-	ns
		6.0V	C_L=50pF		3	-2	-	ns
maximum clock frequency	fmax	2.0V	C_L=50pF	see Figure 4	4.8	30	-	MHz
		4.5V	C_L=50pF		24	91	-	MHz
		6.0V	C_L=50pF		28	108	-	MHz
CD74HCT73								
$n\overline{CP}$ to nQ propagation delay	t_{PLH}, t_{PHL}	4.5V	C_L=50pF	see Figure 4	-	19	45	ns
		5.0V	C_L=15pF			16	-	ns
$n\overline{CP}$ to $n\overline{Q}$ propagation delay		4.5V	C_L=50pF		-	21	45	ns
		5.0V	C_L=15pF		-	18	-	ns
$n\overline{R}$ to nQ/$n\overline{Q}$		4.5V	C_L=50pF	see Figure 5	-	20	48	ns

propagation delay		5.0V	C_L=15pF			17	-	ns
transition time	t_{THL}, t_{TLH}	4.5V	C_L=50pF	see Figure 4	-	7	15	ns
$n\overline{CP}$ HIGH or LOW pulse width	tw	4.5V	C_L=50pF	see Figure 4	20	9	-	ns
$n\overline{R}$ HIGH pulse width		4.5V	C_L=50pF	see Figure 5	25	11	-	ns
$n\overline{R}$ to $n\overline{CP}$ recovery time	trec	4.5V	C_L=50pF	see Figure 5	18	8	-	ns
nJ/nQ to $n\overline{CP}$ set-up time	tsu	4.5V	C_L=50pF	see Figure 4	25	7	-	ns
nJ/nQ to $n\overline{CP}$ hold time	th	4.5V	C_L=50pF	see Figure 4	5	-2	-	ns
maximum clock frequency	fmax	4.5V	C_L=50pF	see Figure 4	24	66	-	MHz

3.3.4、AC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	V_{CC}	Conditions		Min.	Typ.	Max.	Unit
CD74HC73								
$n\overline{CP}$ to nQ propagation delay	t_{PLH}, t_{PHL}	2.0V	C_L=50pF	see Figure 4	-	-	240	ns
		4.5V	C_L=50pF		-	-	48	ns
		6.0V	C_L=50pF				41	ns
$n\overline{CP}$ to $n\overline{Q}$ propagation delay		2.0V	C_L=50pF		-	-	240	ns
		4.5V	C_L=50pF		-	-	48	ns
		6.0V	C_L=50pF		-	-	41	ns
$n\overline{R}$ to nQ/$n\overline{Q}$ propagation delay		2.0V	C_L=50pF	see Figure 5	-	-	235	ns
		4.5V	C_L=50pF		-	-	47	ns
		6.0V	C_L=50pF				40	ns
nQ/$n\overline{Q}$ transition time	t_{THL}, t_{TLH}	2.0V	C_L=50pF	see Figure 4	-	-	110	ns
		4.5V	C_L=50pF		-	-	22	ns
		6.0V	C_L=50pF		-	-	19	ns
$n\overline{CP}$ input HIGH or LOW pulse width	tw	2.0V	C_L=50pF	see Figure 4	120	-	-	ns
		4.5V	C_L=50pF		24	-	-	ns
		6.0V	C_L=50pF		20	-	-	ns
$n\overline{R}$ input, HIGH pulse width		2.0V	C_L=50pF	see Figure 5	120	-	-	ns
		4.5V	C_L=50pF		24	-	-	ns
		6.0V	C_L=50pF		20	-	-	ns
$n\overline{R}$ to $n\overline{CP}$ recovery time	trec	2.0V	C_L=50pF	see Figure 5	90	-	-	ns
		4.5V	C_L=50pF		18	-	-	ns
		6.0V	C_L=50pF		15	-	-	ns
nJ,nK to $n\overline{CP}$ set-up time	tsu	2.0V	C_L=50pF	see Figure 4	150	-	-	ns
		4.5V	C_L=50pF		30	-	-	ns

		6.0V	C_L=50pF		26	-	-	ns
nJ,nK to n$\overline{CP}$ hold time	th	2.0V	C_L=50pF	see Figure 4	3	-	-	ns
		4.5V	C_L=50pF		3	-	-	ns
		6.0V	C_L=50pF		3	-	-	ns
maximum clock frequency	fmax	2.0V	C_L=50pF	see Figure 4	4.0	-	-	MHz
		4.5V	C_L=50pF		20	-	-	MHz
		6.0V	C_L=50pF		24	-	-	MHz
CD74HCT73								
n$\overline{CP}$ to nQ propagation delay	t_{PLH}, t_{PHL}	4.5V	C_L=50pF	see Figure 4	-	-	54	ns
n$\overline{CP}$ to n$\overline{Q}$ propagation delay		4.5V	C_L=50pF		-	-	54	ns
n$\overline{R}$ to nQ/n$\overline{Q}$ propagation delay		4.5V	C_L=50pF	see Figure 5	-	-	57	ns
transition time	t_{THL}, t_{TLH}	4.5V	C_L=50pF	see Figure 4	-	-	22	ns
n$\overline{CP}$ HIGH or LOW pulse width	tw	4.5V	C_L=50pF	see Figure 4	24	-	-	ns
n$\overline{R}$ HIGH pulse width		4.5V	C_L=50pF	see Figure 5	30	-	-	ns
n$\overline{R}$ to n$\overline{CP}$ recovery time	trec	4.5V	C_L=50pF	see Figure 5	21	-	-	ns
nJ/nQ to n$\overline{CP}$ set-up time	tsu	4.5V	C_L=50pF	see Figure 4	30	-	-	ns
nJ/nQ to n$\overline{CP}$ hold time	th	4.5V	C_L=50pF	see Figure 4	5	-	-	ns
maximum clock frequency	fmax	4.5V	C_L=50pF	see Figure 4	20	-	-	MHz

4、Testing Circuit

4.1、AC Testing Circuit

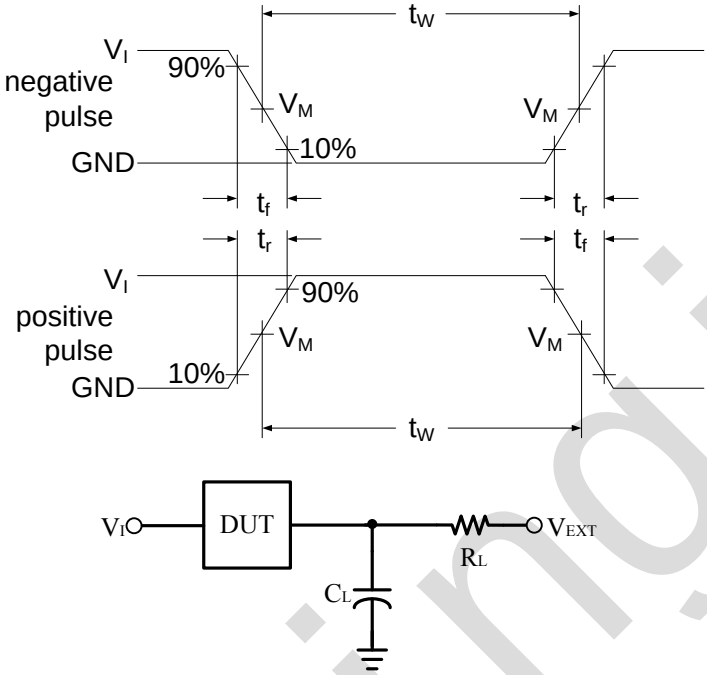


Figure 3. Test circuit for measuring switching times

C_L includes probe and jig capacitance.

4.2、Test Data

Type	Input		Load		V_{EXT}		
	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}/t_{PHL}	t_{PLZ}/t_{PZL}	t_{PHZ}/t_{PZH}
CD74HC73	V_{CC}	3.0ns	15pF, 50pF	1KΩ	Open	V_{CC}	GND
CD74HCT73	3.0V	3.0ns	15pF, 50pF	1KΩ	Open	V_{CC}	GND

4.3、AC Testing Waveforms

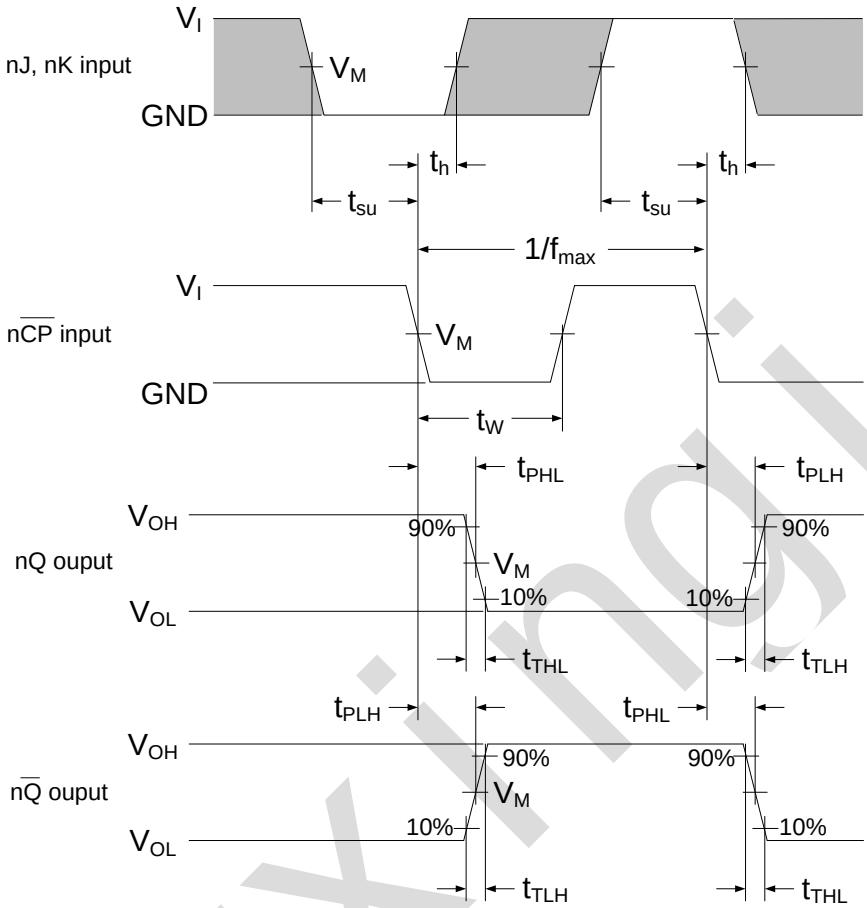


Figure 4. Clock propagation delays, pulse width, set-up and hold times, output transition times and the maximum frequency

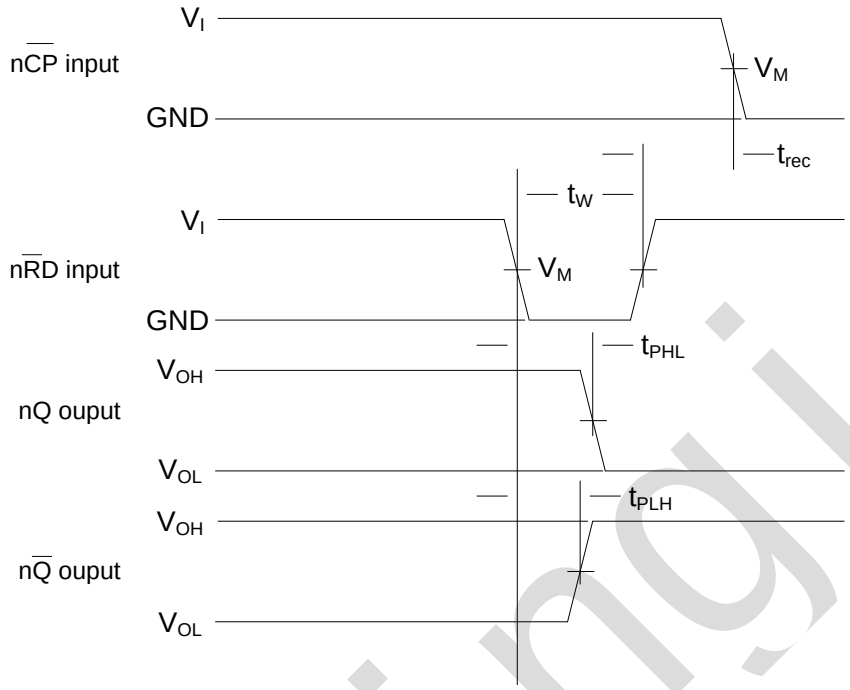


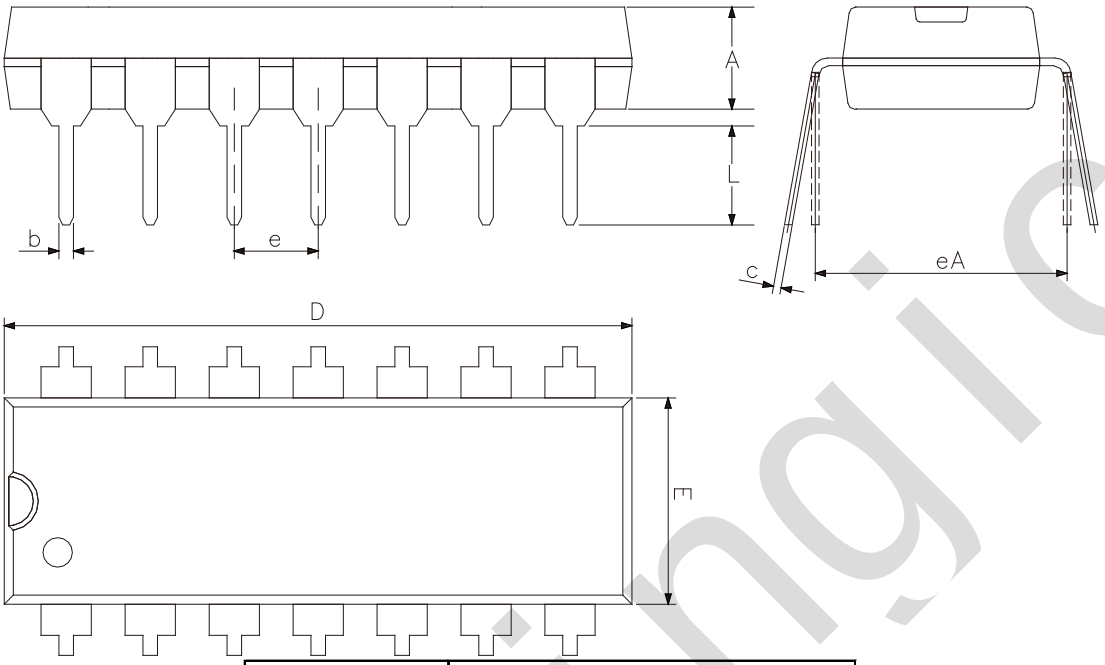
Figure 5. Reset propagation delays, pulse width and recovery time

4.4、Measurement Points

Type	Input	Output
	V_M	V_M
CD74HC73	$0.5\times V_{CC}$	$0.5\times V_{CC}$
CD74HCT73	1.3V	1.3V

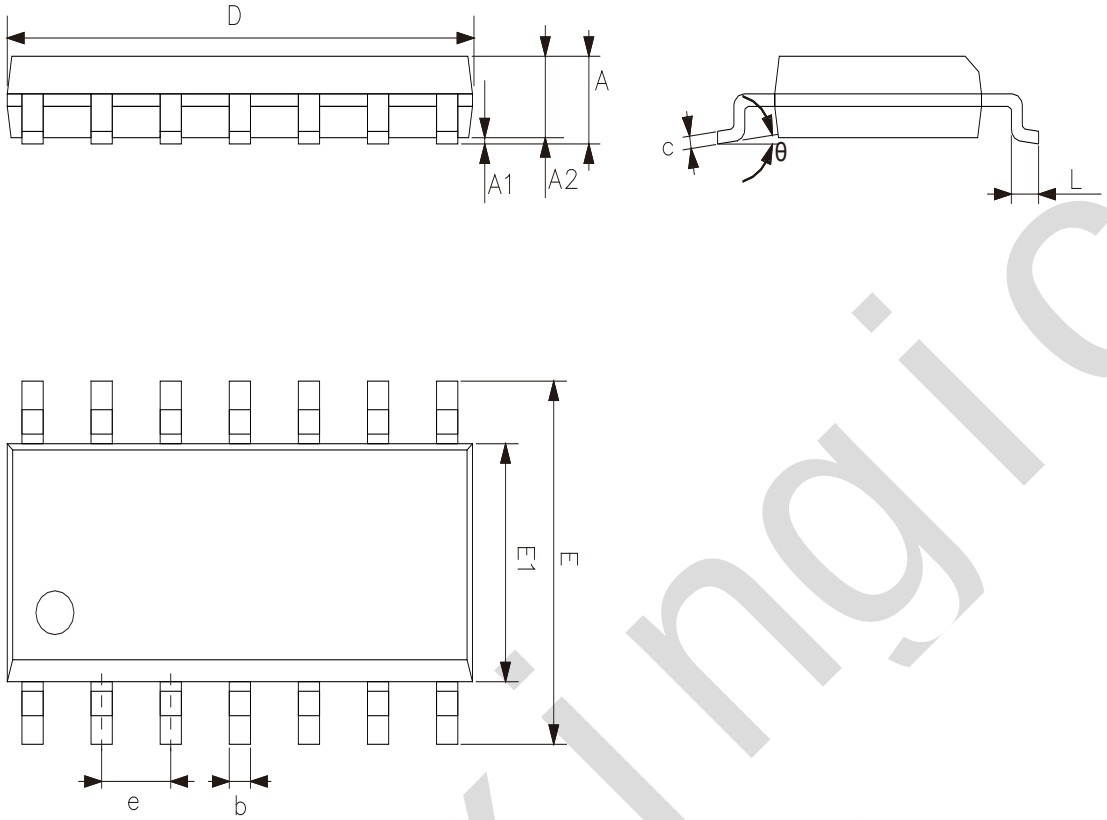
5、Package Information

5.1、DIP14



2023/12/A	Dimensions In Millimeters	
Symbol	**Min**	**Max**
A	3.05	3.60
b	0.33	0.56
c	0.20	0.36
D	18.80	19.40
E	6.20	6.60
e	2.54	
eA	7.62	10.90
L	2.92	—

5.2、SOP14



2023/12/A	Dimensions In Millimeters	
Symbol	**Min.**	**Max.**
A	1.50	1.75
A1	0.05	0.25
A2	1.30	—
b	0.33	0.50
c	0.19	0.25
D	8.43	8.76
E	5.80	6.25
E1	3.75	4.00
e	1.27	
L	0.40	0.89
θ	0°	8°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

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