



SN74LS174 (LX)

Hex D-type Flip-flop with Reset; Positive-edge Trigger

Product Specification

Specification Revision History:

Version	Date	Description
2023-05-A1	2023-05	New



灵星芯微 精密经营

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1、General Description

The SN74LS174 is a hex positive edge-triggered D-type flip-flop with individual data inputs (D_n) and outputs (Q_n).

Features:

- Temperature range: -40°C to +125°C
- Packaging information: DIP16/SOP16/TSSOP16

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
SN74LS174N (LX)	DIP16	SN74LS174N	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
SN74LS174D(LX)	SOP16	LS174	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
SN74LS174PW(LX)	TSSOP16	LS174	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm



Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
SN74LS174DR (LX)	SOP16	LS174	2500 PCS/reel	5000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
SN74LS174PW(LX)	TSSOP16	LS174	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.



2、Block Diagram And Pin Description

2.1、Block Diagram

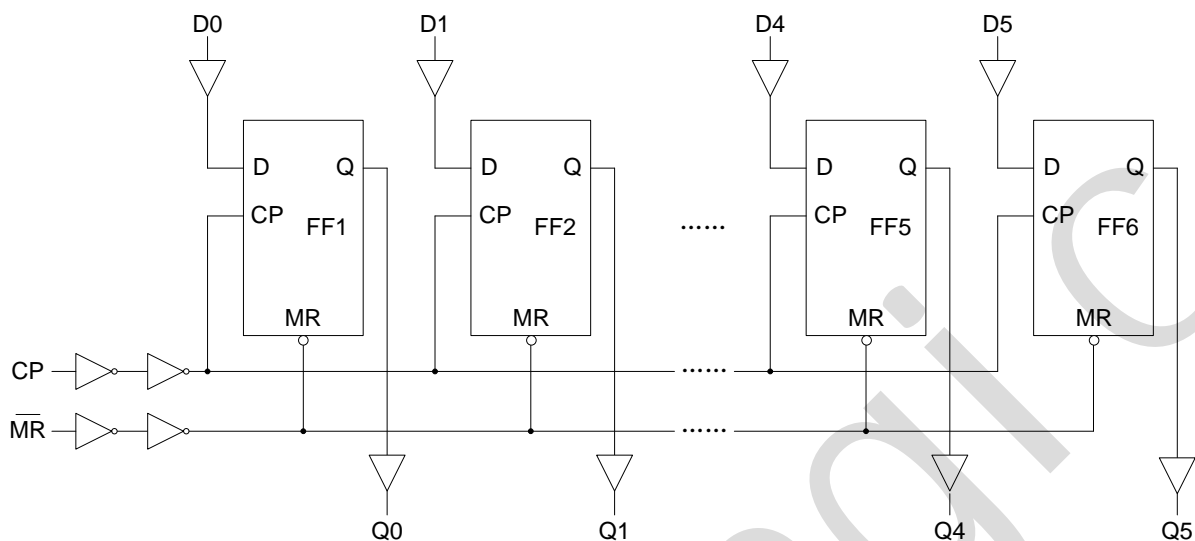


Figure 1. Logic diagram

2.2、Pin Configurations

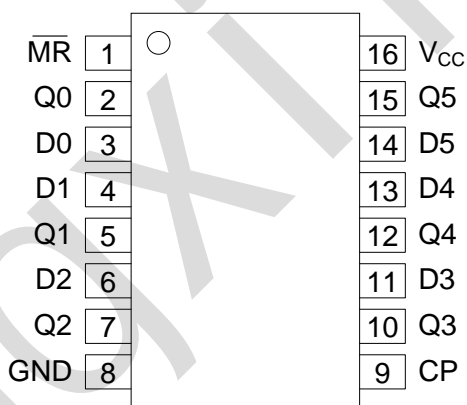


Figure 2. Pin configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	$\overline{\text{MR}}$	asynchronous master reset input (active LOW)
2	Q0	data output
3	D0	data input
4	D1	data input
5	Q1	data output
6	D2	data input
7	Q2	data output
8	GND	ground (0V)
9	CP	clock input (LOW-to-HIGH edge-triggered)
10	Q3	data output
11	D3	data input
12	Q4	data output
13	D4	data input
14	D5	data input
15	Q5	data output
16	V _{CC}	supply voltage

2.4、Function Table

Input			Output
$\overline{\text{MR}}$	CP	Dn	Qn
L	X	X	L
H	↑	h	H
H	↑	l	L

Note:

H=HIGH voltage level;

h=HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;

L=LOW voltage level;

l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;

X=don't care;

↑=LOW-to-HIGH clock transition.



3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	-	-0.5	+7	V
supply current	I_{CC}	-	-	50	mA
ground current	I_{GND}	-	-50	-	mA
input clamping current	I_{IK}	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$	-	± 20	mA
output clamping current	I_{OK}	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$	-	± 20	mA
output current	I_O	$-0.5V < V_O < V_{CC}+0.5V$	-	± 25	mA
storage temperature	T_{stg}	-	-65	+150	$^{\circ}C$
soldering temperature	T_L	10s	DIP	245	$^{\circ}C$
			SOP/TSSOP	260	

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
ambient temperature	T_{amb}	-	-40	-	+125	$^{\circ}C$

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

($T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	V_{CC}	Conditions	Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	2.0V	-	1.5	1.2	-	V
		4.5V	-	3.15	2.4	-	V
		6.0V	-	4.2	3.2	-	V
LOW-level input voltage	V_{IL}	2.0V	-	-	0.8	0.5	V
		4.5V	-	-	2.1	1.35	V
		6.0V	-	-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	2.0V	$I_O = -20\mu A$	1.9	2.0	-	V
		4.5V	$I_O = -20\mu A$	4.4	4.5	-	V
		6.0V	$I_O = -20\mu A$	5.9	6.0	-	V
		4.5V	$I_O = -4.0mA$	3.84	4.32	-	V
		6.0V	$I_O = -5.2mA$	5.34	5.81	-	V
LOW-level	V_{OL}	2.0V	$I_O = 20\mu A$	-	0	0.1	V



output voltage		4.5V	$I_O=20\mu A$	-	0	0.1	V
		6.0V	$I_O=20\mu A$	-	0	0.1	V
		4.5V	$I_O=4.0mA$	-	0.15	0.33	V
		6.0V	$I_O=5.2mA$	-	0.16	0.33	V
input leakage current	I_I	6.0V	$V_I=V_{CC}$ or GND	-	-	± 1	μA
supply current	I_{CC}	6.0V	$V_I=V_{CC}$ or GND; $I_O=0A$	-	-	80	μA

3.3.2、DC Characteristics 2

($T_{amb}=-40^{\circ}C$ to $+125^{\circ}C$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	V_{CC}	Conditions	Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	2.0V	-	1.5	-	-	V
		4.5V	-	3.15	-	-	V
		6.0V	-	4.2	-	-	V
LOW-level input voltage	V_{IL}	2.0V	-	-	-	0.5	V
		4.5V	-	-	-	1.35	V
		6.0V	-	-	-	1.8	V
HIGH-level output voltage	V_{OH}	2.0V	$I_O=-20\mu A$	1.9	-	-	V
		4.5V	$I_O=-20\mu A$	4.4	-	-	V
		6.0V	$I_O=-20\mu A$	5.9	-	-	V
		4.5V	$I_O=-4.0mA$	3.7	-	-	V
		6.0V	$I_O=-5.2mA$	5.2	-	-	V
LOW-level output voltage	V_{OL}	2.0V	$I_O=20\mu A$	-	-	0.1	V
		4.5V	$I_O=20\mu A$	-	-	0.1	V
		6.0V	$I_O=20\mu A$	-	-	0.1	V
		4.5V	$I_O=4.0mA$	-	-	0.4	V
		6.0V	$I_O=5.2mA$	-	-	0.4	V
input leakage current	I_I	6.0V	$V_I=V_{CC}$ or GND	-	-	± 1	μA
supply current	I_{CC}	6.0V	$V_I=V_{CC}$ or GND; $I_O=0A$	-	-	160	μA



3.3.3、AC Characteristics 1

($T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	V _{CC}	Conditions	Min.	Typ.	Max.	Unit	
CP to Qn propagation delay	t _{PLH} , t _{PHL}	2.0V	C _L =50pF	see Figure 4	-	55	205	ns
		4.5V	C _L =50pF		-	20	41	ns
		5.0V	C _L =15pF		-	17	-	ns
		6.0V	C _L =50pF		-	16	35	ns
MR to Qn HIGH to LOW propagation delay	t _{PHL}	2.0V	C _L =50pF	see Figure 5	-	44	190	ns
		4.5V	C _L =50pF		-	16	38	ns
		5V	C _L =15pF		-	13	-	ns
		6.0V	C _L =50pF		-	13	33	ns
transition time	t _{THL} , t _{TLH}	2.0V	C _L =50pF	see Figure 4	-	19	95	ns
		4.5V	C _L =50pF		-	7	19	ns
		6.0V	C _L =50pF		-	6	16	ns
CP input HIGH or LOW pulse width	t _w	2.0V	C _L =50pF	see Figure 4	100	17	-	ns
		4.5V	C _L =50pF		20	6	-	ns
		6.0V	C _L =50pF		17	5	-	ns
MR input LOW pulse width	t _w	2.0V	C _L =50pF	see Figure 5	100	12	-	ns
		4.5V	C _L =50pF		20	4	-	ns
		6.0V	C _L =50pF		17	3	-	ns
MR to CP Recovery time	t _{rec}	2.0V	C _L =50pF	see Figure 5	5	-11	-	ns
		4.5V	C _L =50pF		5	-4	-	ns
		6.0V	C _L =50pF		5	-3	-	ns
Dn to CP set-up time	t _{su}	2.0V	C _L =50pF	see Figure 4	75	6	-	ns
		4.5V	C _L =50pF		15	2	-	ns
		6.0V	C _L =50pF		13	2	-	ns
Dn to CP hold time	t _h	2.0V	C _L =50pF	see Figure 4	3	-6	-	ns
		4.5V	C _L =50pF		3	-2	-	ns
		6.0V	C _L =50pF		3	-2	-	ns
maximum frequency	f _{max}	2.0V	C _L =50pF	see Figure 4	5	-	-	MHZ
		4.5V	C _L =50pF		24	-	-	MHZ
		6.0V	C _L =50pF		28	-	-	MHZ



3.3.4、AC Characteristics 2

($T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	V _{CC}	Conditions	Min.	Typ.	Max.	Unit	
SN74LS174								
CP to Qn propagation delay	t _{PLH} , t _{PHL}	2.0V	C _L =50pF	see Figure 4	-	-	250	ns
		4.5V	C _L =50pF		-	-	50	ns
		6.0V	C _L =50pF		-	-	43	ns
MR to Qn HIGH to LOW propagation delay	t _{PHL}	2.0V	C _L =50pF	see Figure 5	-	-	225	ns
		4.5V	C _L =50pF		-	-	45	ns
		6.0V	C _L =50pF		-	-	38	ns
transition time	t _{THL} , t _{TLH}	2.0V	C _L =50pF	see Figure 4	-	-	110	ns
		4.5V	C _L =50pF		-	-	22	ns
		6.0V	C _L =50pF		-	-	19	ns
CP input HIGH or LOW pulse width	t _w	2.0V	C _L =50pF	see Figure 4	120	-	-	ns
		4.5V	C _L =50pF		24	-	-	ns
		6.0V	C _L =50pF		20	-	-	ns
MR input LOW pulse width	t _w	2.0V	C _L =50pF	see Figure 5	120	-	-	ns
		4.5V	C _L =50pF		24	-	-	ns
		6.0V	C _L =50pF		20	-	-	ns
MR to CP Recovery time	t _{rec}	2.0V	C _L =50pF	see Figure 5	5	-	-	ns
		4.5V	C _L =50pF		5	-	-	ns
		6.0V	C _L =50pF		5	-	-	ns
Dn to CP set-up time	t _{su}	2.0V	C _L =50pF	see Figure 4	90	-	-	ns
		4.5V	C _L =50pF		18	-	-	ns
		6.0V	C _L =50pF		15	-	-	ns
Dn to CP hold time	t _h	2.0V	C _L =50pF	see Figure 4	3	-	-	ns
		4.5V	C _L =50pF		3	-	-	ns
		6.0V	C _L =50pF		3	-	-	ns
maximum frequency	f _{max}	2.0V	C _L =50pF	see Figure 4	4	-	-	MHZ
		4.5V	C _L =50pF		20	-	-	MHZ
		6.0V	C _L =50pF		24	-	-	MHZ



4、Testing Circuit

4.1、AC Testing Circuit

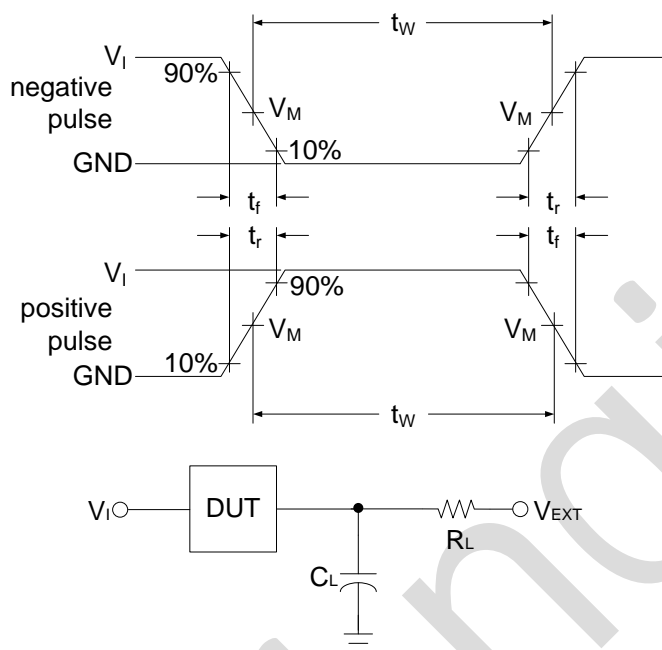


Figure 3. Test circuit for measuring switching times

C_L includes probe and jig capacitance.

4.2、Test Data

Input		Load		V_{EXT}		
V_I	$t_r = t_f$	C_L	R_L	t_{PLH}/t_{PHL}	t_{PLZ}/t_{PZL}	t_{PHZ}/t_{PZH}
V_{CC}	6.0ns	15pF, 50pF	1K Ω	Open	V_{CC}	GND



4.3、AC Testing Waveforms

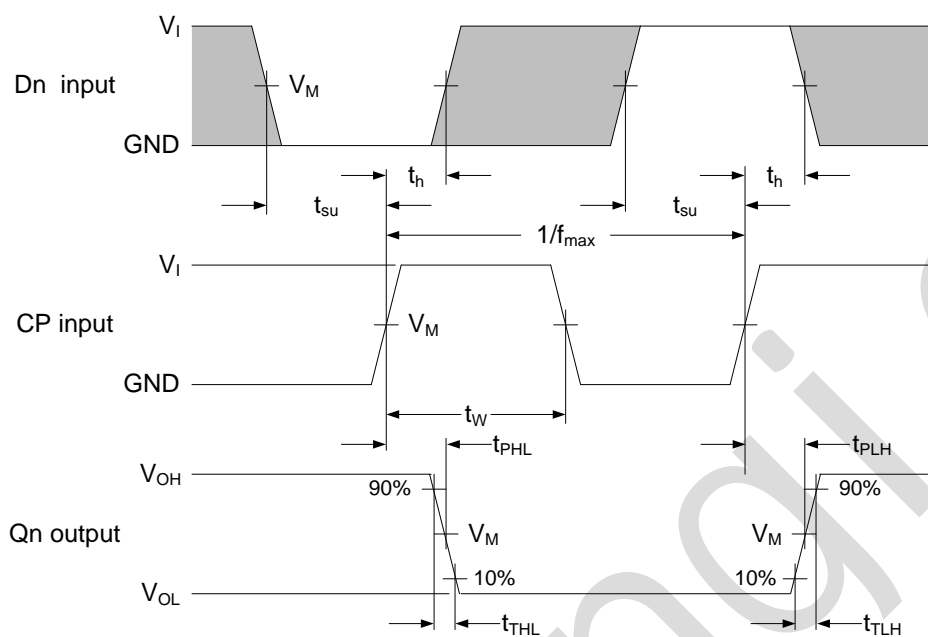


Figure 4. Input to output propagation delay, output transition time, clock input pulse width, set-up and hold times for data input and maximum frequency

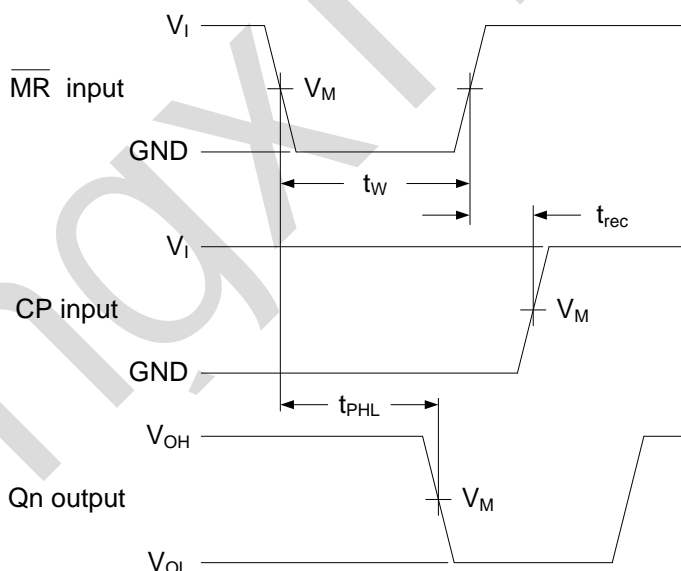


Figure 5. Master reset to output propagation delays, master reset pulse width and master reset to recovery time

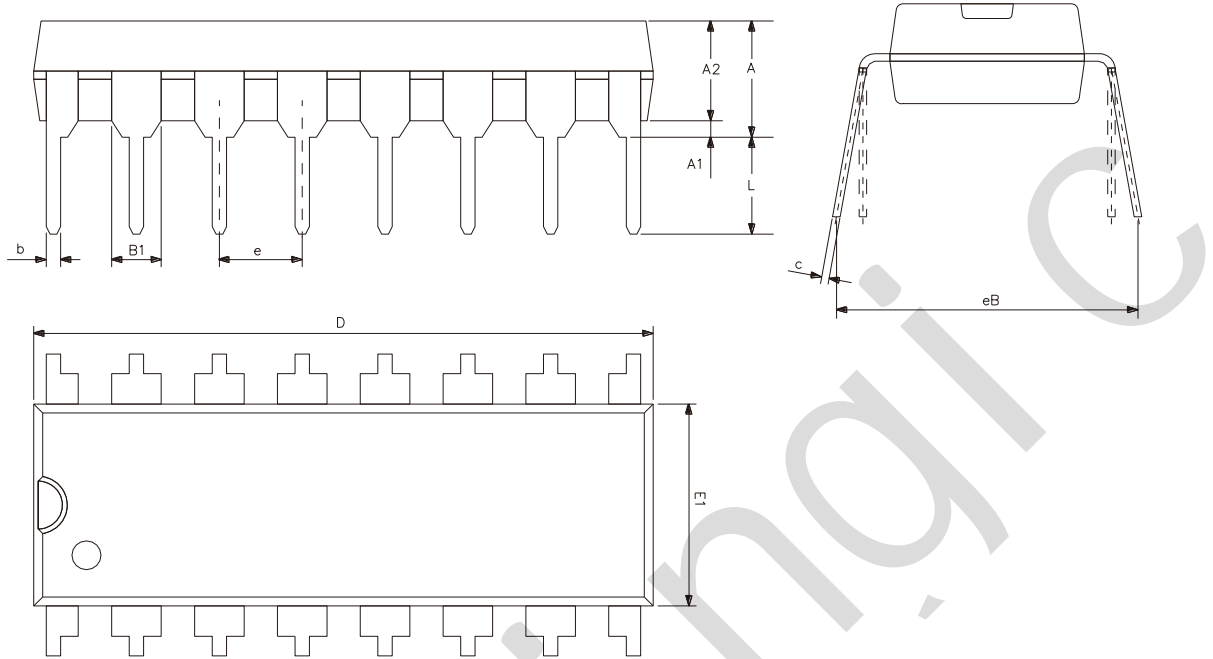
4.4、Measurement Points

Input	Output		
V_M	V_M	V_X	V_Y
$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$



5、Package Information

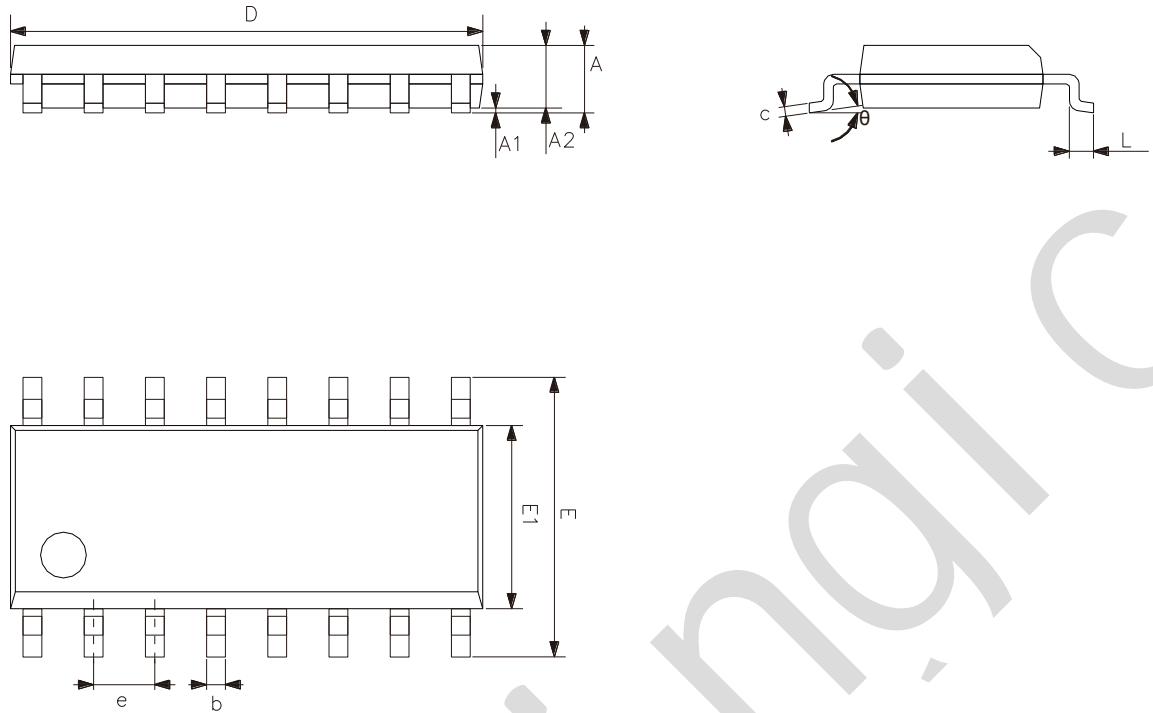
5.1、DIP16



Symbol	Dimensions (mm)	
	Min.	Max.
A2	3.20	3.60
A1	0.51	-
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
c	0.20	0.36
eB	7.62	9.30



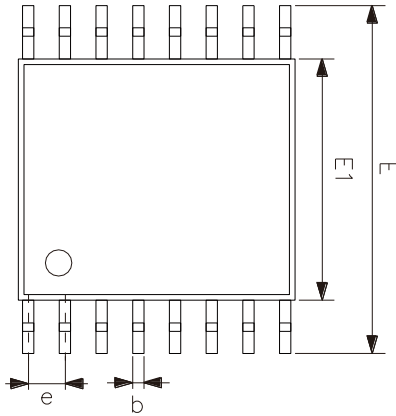
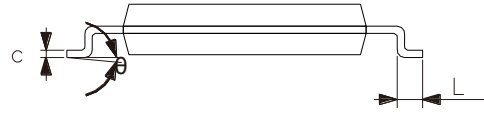
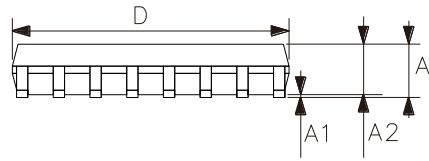
5.2、SOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°



5.3、TSSOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°



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6、 Statements And Notes

6.1、 The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、 Notes

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[SN74HC174DR\(LX\)](#) [SN74HC112N\(LX\)](#) [SN74HC74DR\(LX\)](#) [CD40174BE\(LX\)](#) [CD40175BE\(LX\)](#) [SN74LS374N](#) [SN74HC173N](#)
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