



SN74LS192 (LX)

Presettable Synchronous BCD Decade up/down Counter; Asynchronous Reset

Product Specification

Specification Revision History:

Version	Date	Description
2021-06-A1	2021-06	New
2023-04-B1	2023-04	Update the template



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1、General Description

The SN74LS192 is a synchronous BCD up/down counter. Separate up/down clocks, CPU and CPD respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the CPU clock is pulsed while CPD is held HIGH, the device will count up. If the CPD clock is pulsed while CPU is held HIGH, the device will count down. Only one clock input can be held HIGH at any time to guarantee predictable behavior. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input (\overline{PL}).

The terminal count up (\overline{TCU}) and terminal count down (\overline{TCD}) outputs are normally HIGH. When the circuit has reached the maximum count state of 15, the next HIGH-to-LOW transition of CPU will cause \overline{TCU} to go LOW. \overline{TCU} will stay LOW until CPU goes HIGH again, duplicating the count up clock. Likewise, the \overline{TCD} output will go LOW when the circuit is in the zero state and the CPD goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a slight delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (D0 to D3) is loaded into the counter and appears on the outputs (Q0 to Q3) regardless of the conditions of the clock inputs when the parallel load (\overline{PL}) input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates, override both clock inputs and set all outputs (Q0 to Q3) LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

Features:

- Synchronous reversible counting
- Asynchronous parallel load
- Asynchronous reset
- Expandable without external logic
- Specified from -40°C to $+125^{\circ}\text{C}$
- Packaging information: DIP16/SOP16/TSSOP16



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Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
SN74LS192N (LX)	DIP16	SN74LS192N	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
SN74LS192DR (LX)	SOP16	LS192	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
SN74LS192PW(LX)	TSSOP16	LS192	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm



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深圳市灵星芯微电子科技有限公司

Shenzhen Lingxing Microelectronics Technology Co., Ltd.

Tab: 835-12-B4

Number:SN74LS192-AX-LJ-A065EN

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
SN74LS192DR(LX)	SOP16	LS192	2500 PCS/reel	5000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
SN74LS192PW(LX)	TSSOP16	LS192	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.



2、Block Diagram And Pin Description

2.1、Block Diagram

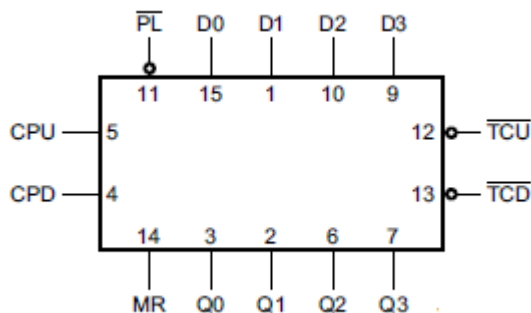


Figure 1. Logic symbol

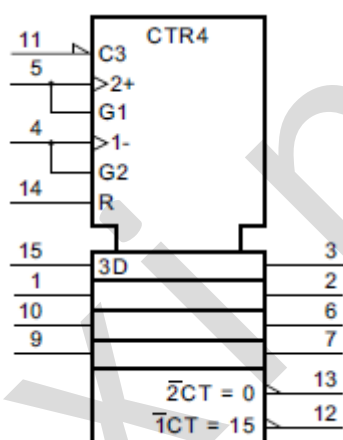


Figure 2. IEC logic symbol

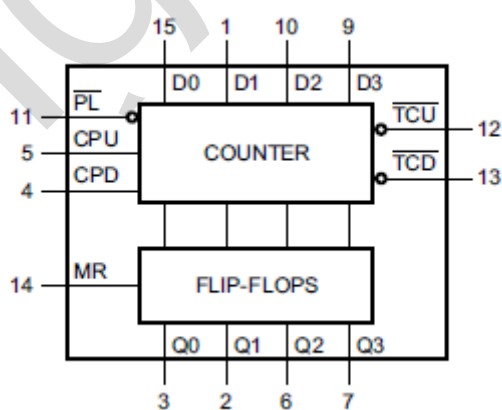


Figure 3. Functional diagram

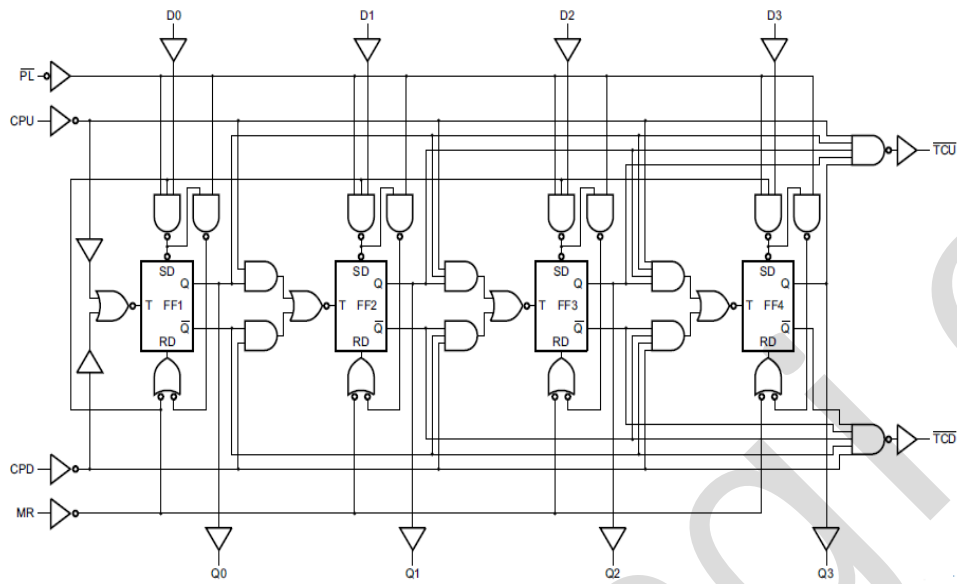


Figure 4. Logic diagram

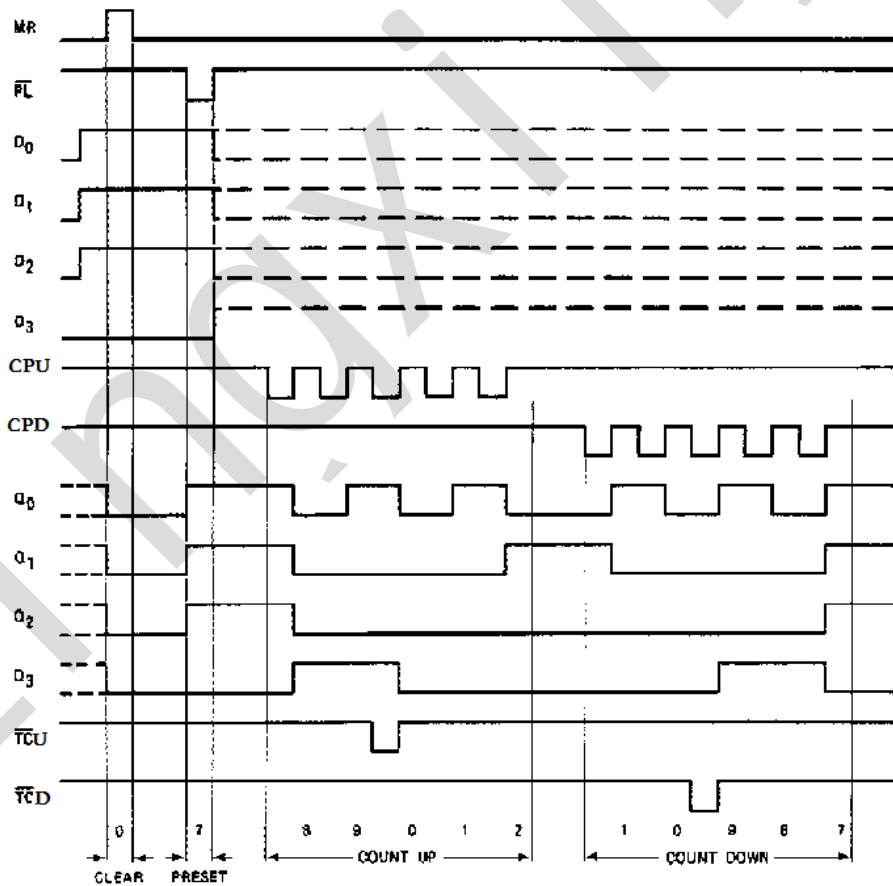
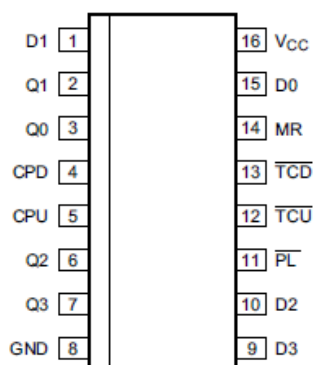


Figure 5. Typical clear, load and count sequence



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2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	D1	data input 1
2	Q1	flip-flop output 1
3	Q0	flip-flop output 0
4	CPD	count down clock input
5	CPU	count up clock input
6	Q2	flip-flop output 2
7	Q3	flip-flop output 3
8	GND	ground (0V)
9	D3	data input 3
10	D2	data input 2
11	\overline{PL}	asynchronous parallel load input (active LOW)
12	\overline{TCU}	terminal count up (carry) output (active LOW)
13	\overline{TCD}	terminal count down (borrow) output (active LOW)
14	MR	asynchronous master reset input (active HIGH)
15	D0	data input 0
16	V _{CC}	supply voltage

Note: CPD, CPU is LOW-to-HIGH, edge triggered.



2.4、Function Table

Operating mode	Input								Output					
	MR	$\bar{P}L$	CPU	CPD	D0	D1	D2	D3	Q0	Q1	Q2	Q3	$\bar{T}CU$	$\bar{T}CD$
reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	X	X	H	Qn=Dn			L	H	
	L	L	H	X	H	X	X	H	Qn=Dn			H	H	
count up	L	H	↑	H	X	X	X	X	count up			H	H	
count down	L	H	H	↑	X	X	X	X	count down			H	H	

Note:

[1] H=HIGH voltage level; L=LOW voltage level; X=don't care; ↑=LOW-to-HIGH transition.

[2] $\bar{T}CU$ =CPU at terminal count up (HLLH).

[3] $\bar{T}CD$ =CPD at terminal count down (LLLL).

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	-	-0.5	+7.0	V
input clamping current	I_{IK}	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$	-	±20	mA
output clamping current	I_{OK}	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$	-	±20	mA
output current	I_O	$V_O = -0.5V$ to $(V_{CC}+0.5V)$	-	±25	mA
supply current	I_{CC}	-	-	50	mA
ground current	I_{GND}	-	-	-50	mA
storage temperature	T_{stg}	-	-65	+150	°C
total power dissipation	P_{tot}	-	-	500	mW
Soldering temperature	T_L	10s	DIP		°C
			SOP/TSSOP		



3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	$\Delta t/\Delta V$	$V_{CC}=2.0V$	-	-	625	ns/V
		$V_{CC}=4.5V$	-	1.67	139	ns/V
		$V_{CC}=6.0V$	-	-	83	ns/V
ambient temperature	T_{amb}	-	-40	-	+125	°C

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

($T_{amb}=25^{\circ}C$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
HIGH-level input voltage	V_{IH}	$V_{CC}=2.0V$	1.5	1.2	-	V	
		$V_{CC}=4.5V$	3.15	2.4	-	V	
		$V_{CC}=6.0V$	4.2	3.2	-	V	
LOW-level input voltage	V_{IL}	$V_{CC}=2.0V$	-	0.8	0.5	V	
		$V_{CC}=4.5V$	-	2.1	1.35	V	
		$V_{CC}=6.0V$	-	2.8	1.8	V	
HIGH-level output voltage	V_{OH}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O=-20\mu A; V_{CC}=2.0V$	1.9	2.0	-	V
			$I_O=-20\mu A; V_{CC}=4.5V$	4.4	4.5	-	V
			$I_O=-20\mu A; V_{CC}=6.0V$	5.9	6.0	-	V
			$I_O=-4mA; V_{CC}=4.5V$	3.98	4.32	-	V
			$I_O=-5.2mA; V_{CC}=6.0V$	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O=20\mu A; V_{CC}=2.0V$	-	0	0.1	V
			$I_O=20\mu A; V_{CC}=4.5V$	-	0	0.1	V
			$I_O=20\mu A; V_{CC}=6.0V$	-	0	0.1	V
			$I_O=4mA; V_{CC}=4.5V$	-	0.15	0.26	V
			$I_O=5.2mA; V_{CC}=6.0V$	-	0.16	0.26	V
input leakage current	I_I	$V_I=V_{CC} \text{ or } GND;$ $V_{CC}=6.0V$	-	-	± 1.0	μA	
supply current	I_{CC}	$V_I=V_{CC} \text{ or } GND; I_O=0A; V_{CC}=6.0V$	-	-	8.0	μA	
input capacitance	C_I	-	-	3.5	-	pF	



3.3.2、DC Characteristics 2

($T_{amb}=-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
HIGH-level input voltage	V_{IH}	$V_{CC}=2.0\text{V}$	1.5	-	-	V	
		$V_{CC}=4.5\text{V}$	3.15	-	-	V	
		$V_{CC}=6.0\text{V}$	4.2	-	-	V	
LOW-level input voltage	V_{IL}	$V_{CC}=2.0\text{V}$	-	-	0.5	V	
		$V_{CC}=4.5\text{V}$	-	-	1.35	V	
		$V_{CC}=6.0\text{V}$	-	-	1.8	V	
HIGH-level output voltage	V_{OH}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O=-20\mu\text{A}; V_{CC}=2.0\text{V}$	1.9	-	-	V
			$I_O=-20\mu\text{A}; V_{CC}=4.5\text{V}$	4.4	-	-	V
			$I_O=-20\mu\text{A}; V_{CC}=6.0\text{V}$	5.9	-	-	V
			$I_O=-4\text{mA}; V_{CC}=4.5\text{V}$	3.84	-	-	V
			$I_O=-5.2\text{mA}; V_{CC}=6.0\text{V}$	5.34	-	-	V
LOW-level output voltage	V_{OL}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O=20\mu\text{A}; V_{CC}=2.0\text{V}$	-	-	0.1	V
			$I_O=20\mu\text{A}; V_{CC}=4.5\text{V}$	-	-	0.1	V
			$I_O=20\mu\text{A}; V_{CC}=6.0\text{V}$	-	-	0.1	V
			$I_O=4\text{mA}; V_{CC}=4.5\text{V}$	-	-	0.33	V
			$I_O=5.2\text{mA}; V_{CC}=6.0\text{V}$	-	-	0.33	V
input leakage current	I_I	$V_I=V_{CC} \text{ or } \text{GND}; V_{CC}=6.0\text{V}$	-	-	± 1.0	μA	
supply current	I_{CC}	$V_I=V_{CC} \text{ or } \text{GND}; I_O=0\text{A}; V_{CC}=6.0\text{V}$	-	-	80	μA	



3.3.3、DC Characteristics 3

($T_{amb}=-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
HIGH-level input voltage	V_{IH}	$V_{CC}=2.0\text{V}$	1.5	-	-	V	
		$V_{CC}=4.5\text{V}$	3.15	-	-	V	
		$V_{CC}=6.0\text{V}$	4.2	-	-	V	
LOW-level input voltage	V_{IL}	$V_{CC}=2.0\text{V}$	-	-	0.5	V	
		$V_{CC}=4.5\text{V}$	-	-	1.35	V	
		$V_{CC}=6.0\text{V}$	-	-	1.8	V	
HIGH-level output voltage	V_{OH}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O=-20\mu\text{A}; V_{CC}=2.0\text{V}$	1.9	-	-	V
			$I_O=-20\mu\text{A}; V_{CC}=4.5\text{V}$	4.4	-	-	V
			$I_O=-20\mu\text{A}; V_{CC}=6.0\text{V}$	5.9	-	-	V
			$I_O=-4\text{mA}; V_{CC}=4.5\text{V}$	3.7	-	-	V
			$I_O=-5.2\text{mA}; V_{CC}=6.0\text{V}$	5.2	-	-	V
LOW-level output voltage	V_{OL}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O=20\mu\text{A}; V_{CC}=2.0\text{V}$	-	-	0.1	V
			$I_O=20\mu\text{A}; V_{CC}=4.5\text{V}$	-	-	0.1	V
			$I_O=20\mu\text{A}; V_{CC}=6.0\text{V}$	-	-	0.1	V
			$I_O=4\text{mA}; V_{CC}=4.5\text{V}$	-	-	0.4	V
			$I_O=5.2\text{mA}; V_{CC}=6.0\text{V}$	-	-	0.4	V
input leakage current	I_I	$V_I=V_{CC} \text{ or } \text{GND}; V_{CC}=6.0\text{V}$	-	-	± 1.0	μA	
supply current	I_{CC}	$V_I=V_{CC} \text{ or } \text{GND}; I_O=0\text{A}; V_{CC}=6.0\text{V}$	-	-	160	μA	



3.3.4、AC Characteristics 1

($T_{amb}=25^{\circ}\text{C}$, $\text{GND}=0\text{V}$, $t_r=t_f=6\text{ns}$, $C_L=50\text{pF}$, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
propagation delay	t_{pd}	CPU, CPD to Qn; see Figure 7	$V_{CC}=2.0\text{V}$	-	66	215	ns
			$V_{CC}=4.5\text{V}$	-	23	43	ns
			$V_{CC}=5.0\text{V}; C_L=15\text{pF}$	-	24	-	ns
			$V_{CC}=6.0\text{V}$	-	19	37	ns
		CPU to $\overline{\text{TCU}}$; see Figure 8	$V_{CC}=2.0\text{V}$	-	33	125	ns
			$V_{CC}=4.5\text{V}$	-	12	25	ns
			$V_{CC}=6.0\text{V}$	-	10	21	ns
		CPD to $\overline{\text{TCD}}$; see Figure 8	$V_{CC}=2.0\text{V}$	-	39	125	ns
			$V_{CC}=4.5\text{V}$	-	14	25	ns
			$V_{CC}=6.0\text{V}$	-	11	21	ns
		$\overline{\text{PL}}$ to Qn; see Figure 9	$V_{CC}=2.0\text{V}$	-	69	215	ns
			$V_{CC}=4.5\text{V}$	-	25	43	ns
			$V_{CC}=6.0\text{V}$	-	20	37	ns
		MR to Qn; see Figure 10	$V_{CC}=2.0\text{V}$	-	63	200	ns
			$V_{CC}=4.5\text{V}$	-	23	40	ns
			$V_{CC}=6.0\text{V}$	-	18	34	ns
		Dn to Qn; see Figure 9	$V_{CC}=2.0\text{V}$	-	91	275	ns
			$V_{CC}=4.5\text{V}$	-	33	55	ns
			$V_{CC}=6.0\text{V}$	-	26	47	ns
		$\overline{\text{PL}}$ to $\overline{\text{TCU}}$, $\overline{\text{PL}}$ to $\overline{\text{TCD}}$; see Figure 12	$V_{CC}=2.0\text{V}$	-	102	315	ns
			$V_{CC}=4.5\text{V}$	-	37	63	ns
			$V_{CC}=6.0\text{V}$	-	30	54	ns
		MR to $\overline{\text{TCU}}$, MR to $\overline{\text{TCD}}$; see Figure 12	$V_{CC}=2.0\text{V}$	-	96	285	ns
			$V_{CC}=4.5\text{V}$	-	35	57	ns
$V_{CC}=6.0\text{V}$	-		28	48	ns		
Dn to $\overline{\text{TCU}}$, Dn to $\overline{\text{TCD}}$; see Figure 12	$V_{CC}=2.0\text{V}$	-	83	290	ns		
	$V_{CC}=4.5\text{V}$	-	30	58	ns		
	$V_{CC}=6.0\text{V}$	-	24	49	ns		
transition time	t_t	see Figure 10	$V_{CC}=2.0\text{V}$	-	19	75	ns
			$V_{CC}=4.5\text{V}$	-	7	15	ns
			$V_{CC}=6.0\text{V}$	-	6	13	ns
pulse width	t_w	up clock pulse width HIGH or LOW;	$V_{CC}=2.0\text{V}$	120	39	-	ns
			$V_{CC}=4.5\text{V}$	24	14	-	ns



		see Figure 7	$V_{CC}=6.0V$	20	11	-	ns		
		down clock pulse width HIGH or LOW; see Figure 7	$V_{CC}=2.0V$	140	50	-	ns		
			$V_{CC}=4.5V$	28	18	-	ns		
			$V_{CC}=6.0V$	24	14	-	ns		
		master reset pulse width HIGH; see Figure 10	$V_{CC}=2.0V$	80	22	-	ns		
			$V_{CC}=4.5V$	16	8	-	ns		
			$V_{CC}=6.0V$	14	6	-	ns		
		parallel load pulse width LOW; see Figure 9	$V_{CC}=2.0V$	80	22	-	ns		
			$V_{CC}=4.5V$	16	8	-	ns		
			$V_{CC}=6.0V$	14	6	-	ns		
		recovery time	t_{rec}	\bar{PL} to CPU, CPD; see Figure 9	$V_{CC}=2.0V$	50	3	-	ns
					$V_{CC}=4.5V$	10	1	-	ns
$V_{CC}=6.0V$	9				1	-	ns		
MR to CPU, CPD; see Figure 10	$V_{CC}=2.0V$			50	0	-	ns		
	$V_{CC}=4.5V$			10	0	-	ns		
	$V_{CC}=6.0V$			9	0	-	ns		
set-up time	t_{su}	Dn to \bar{PL} ; see Figure 11; note: CPU=CPD=HIGH	$V_{CC}=2.0V$	80	22	-	ns		
			$V_{CC}=4.5V$	16	8	-	ns		
			$V_{CC}=6.0V$	14	6	-	ns		
hold time	t_h	Dn to \bar{PL} ; see Figure 11	$V_{CC}=2.0V$	0	-14	-	ns		
			$V_{CC}=4.5V$	0	-5	-	ns		
			$V_{CC}=6.0V$	0	-4	-	ns		
		CPU to CPD, CPD to CPU; see Figure 13	$V_{CC}=2.0V$	80	19	-	ns		
			$V_{CC}=4.5V$	16	7	-	ns		
			$V_{CC}=6.0V$	14	6	-	ns		
maximum frequency	f_{max}	CPU, CPD; see Figure 7	$V_{CC}=2.0V$	4.0	12	-	MHz		
			$V_{CC}=4.5V$	20	36	-	MHz		
			$V_{CC}=5.0V$; $C_L=15pF$	-	40	-	MHz		
			$V_{CC}=6.0V$	24	43	-	MHz		
power dissipation capacitance	C_{PD}	$V_I=GND$ to V_{CC}	-	24	-	pF			

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] t_i is the same as t_{THL} and t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i =input frequency in MHz;

f_o =output frequency in MHz;

C_L =output load capacitance in pF;

V_{CC} =supply voltage in V;

$\sum (C_L \times V_{CC}^2 \times f_o)$ =sum of outputs.



3.3.5、AC Characteristics 2

($T_{amb}=-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $\text{GND}=0\text{V}$, $t_r=t_f=6\text{ns}$, $C_L=50\text{pF}$, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
propagation delay	t_{pd}	CPU, CPD to Qn; see Figure 7	$V_{CC}=2.0\text{V}$	-	-	270	ns
			$V_{CC}=4.5\text{V}$	-	-	54	ns
			$V_{CC}=6.0\text{V}$	-	-	46	ns
		CPU to $\overline{\text{TCU}}$; see Figure 8	$V_{CC}=2.0\text{V}$	-	-	155	ns
			$V_{CC}=4.5\text{V}$	-	-	31	ns
			$V_{CC}=6.0\text{V}$	-	-	26	ns
		CPD to $\overline{\text{TCD}}$; see Figure 8	$V_{CC}=2.0\text{V}$	-	-	155	ns
			$V_{CC}=4.5\text{V}$	-	-	31	ns
			$V_{CC}=6.0\text{V}$	-	-	26	ns
		$\overline{\text{PL}}$ to Qn; see Figure 9	$V_{CC}=2.0\text{V}$	-	-	270	ns
			$V_{CC}=4.5\text{V}$	-	-	54	ns
			$V_{CC}=6.0\text{V}$	-	-	46	ns
		MR to Qn; see Figure 10	$V_{CC}=2.0\text{V}$	-	-	250	ns
			$V_{CC}=4.5\text{V}$	-	-	50	ns
			$V_{CC}=6.0\text{V}$	-	-	43	ns
		Dn to Qn; see Figure 9	$V_{CC}=2.0\text{V}$	-	-	345	ns
			$V_{CC}=4.5\text{V}$	-	-	69	ns
			$V_{CC}=6.0\text{V}$	-	-	59	ns
		$\overline{\text{PL}}$ to $\overline{\text{TCU}}$, $\overline{\text{PL}}$ to $\overline{\text{TCD}}$; see Figure 12	$V_{CC}=2.0\text{V}$	-	-	395	ns
			$V_{CC}=4.5\text{V}$	-	-	79	ns
			$V_{CC}=6.0\text{V}$	-	-	67	ns
		MR to $\overline{\text{TCU}}$, MR to $\overline{\text{TCD}}$; see Figure 12	$V_{CC}=2.0\text{V}$	-	-	355	ns
			$V_{CC}=4.5\text{V}$	-	-	71	ns
			$V_{CC}=6.0\text{V}$	-	-	60	ns
Dn to $\overline{\text{TCU}}$, Dn to $\overline{\text{TCD}}$; see Figure 12	$V_{CC}=2.0\text{V}$	-	-	365	ns		
	$V_{CC}=4.5\text{V}$	-	-	73	ns		
	$V_{CC}=6.0\text{V}$	-	-	62	ns		
transition time	t_t	see Figure 10	$V_{CC}=2.0\text{V}$	-	-	95	ns
			$V_{CC}=4.5\text{V}$	-	-	19	ns
			$V_{CC}=6.0\text{V}$	-	-	16	ns
pulse width	t_w	up clock pulse width HIGH or LOW; see Figure 7	$V_{CC}=2.0\text{V}$	150	-	-	ns
			$V_{CC}=4.5\text{V}$	30	-	-	ns
			$V_{CC}=6.0\text{V}$	26	-	-	ns
		down clock pulse width HIGH or LOW; see Figure 7	$V_{CC}=2.0\text{V}$	175	-	-	ns
			$V_{CC}=4.5\text{V}$	35	-	-	ns
			$V_{CC}=6.0\text{V}$	30	-	-	ns
		master reset pulse width HIGH; see Figure 10	$V_{CC}=2.0\text{V}$	100	-	-	ns
			$V_{CC}=4.5\text{V}$	20	-	-	ns
			$V_{CC}=6.0\text{V}$	17	-	-	ns
		parallel load pulse	$V_{CC}=2.0\text{V}$	100	-	-	ns



		width LOW; see Figure 9	$V_{CC}=4.5V$	20	-	-	ns
			$V_{CC}=6.0V$	17	-	-	ns
recovery time	t_{rec}	$\bar{P}L$ to CPU, CPD; see Figure 9	$V_{CC}=2.0V$	65	-	-	ns
			$V_{CC}=4.5V$	13	-	-	ns
			$V_{CC}=6.0V$	11	-	-	ns
		MR to CPU, CPD; see Figure 10	$V_{CC}=2.0V$	65	-	-	ns
			$V_{CC}=4.5V$	13	-	-	ns
			$V_{CC}=6.0V$	11	-	-	ns
set-up time	t_{su}	Dn to $\bar{P}L$; see Figure 11; note: CPU=CPD=HIGH	$V_{CC}=2.0V$	100	-	-	ns
			$V_{CC}=4.5V$	20	-	-	ns
			$V_{CC}=6.0V$	17	-	-	ns
hold time	t_h	Dn to $\bar{P}L$; see Figure 11	$V_{CC}=2.0V$	0	-	-	ns
			$V_{CC}=4.5V$	0	-	-	ns
			$V_{CC}=6.0V$	0	-	-	ns
		CPU to CPD, CPD to CPU; see Figure 13	$V_{CC}=2.0V$	100	-	-	ns
			$V_{CC}=4.5V$	20	-	-	ns
			$V_{CC}=6.0V$	17	-	-	ns
maximum frequency	f_{max}	CPU, CPD; see Figure 7	$V_{CC}=2.0V$	3.2	-	-	MHz
			$V_{CC}=4.5V$	16	-	-	MHz
			$V_{CC}=6.0V$	19	-	-	MHz

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] t_i is the same as t_{THL} and t_{TLH} .



3.3.6、AC Characteristics 3

($T_{amb}=-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $GND=0\text{V}$, $t_r=t_f=6\text{ns}$, $C_L=50\text{pF}$, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
propagation delay	t_{pd}	CPU, CPD to Qn; see Figure 7	$V_{CC}=2.0\text{V}$	-	-	324	ns
			$V_{CC}=4.5\text{V}$	-	-	65	ns
			$V_{CC}=6.0\text{V}$	-	-	55	ns
		CPU to $\overline{\text{TCU}}$; see Figure 8	$V_{CC}=2.0\text{V}$	-	-	186	ns
			$V_{CC}=4.5\text{V}$	-	-	37	ns
			$V_{CC}=6.0\text{V}$	-	-	31	ns
		CPD to $\overline{\text{TCD}}$; see Figure 8	$V_{CC}=2.0\text{V}$	-	-	186	ns
			$V_{CC}=4.5\text{V}$	-	-	37	ns
			$V_{CC}=6.0\text{V}$	-	-	31	ns
		$\overline{\text{PL}}$ to Qn; see Figure 9	$V_{CC}=2.0\text{V}$	-	-	324	ns
			$V_{CC}=4.5\text{V}$	-	-	65	ns
			$V_{CC}=6.0\text{V}$	-	-	55	ns
		MR to Qn; see Figure 10	$V_{CC}=2.0\text{V}$	-	-	300	ns
			$V_{CC}=4.5\text{V}$	-	-	60	ns
			$V_{CC}=6.0\text{V}$	-	-	52	ns
		Dn to Qn; see Figure 9	$V_{CC}=2.0\text{V}$	-	-	414	ns
			$V_{CC}=4.5\text{V}$	-	-	83	ns
			$V_{CC}=6.0\text{V}$	-	-	71	ns
		$\overline{\text{PL}}$ to $\overline{\text{TCU}}$, $\overline{\text{PL}}$ to $\overline{\text{TCD}}$; see Figure 12	$V_{CC}=2.0\text{V}$	-	-	474	ns
			$V_{CC}=4.5\text{V}$	-	-	95	ns
			$V_{CC}=6.0\text{V}$	-	-	80	ns
MR to $\overline{\text{TCU}}$, MR to $\overline{\text{TCD}}$; see Figure 12	$V_{CC}=2.0\text{V}$	-	-	426	ns		
	$V_{CC}=4.5\text{V}$	-	-	85	ns		
	$V_{CC}=6.0\text{V}$	-	-	72	ns		
Dn to $\overline{\text{TCU}}$, Dn to $\overline{\text{TCD}}$; see Figure 12	$V_{CC}=2.0\text{V}$	-	-	438	ns		
	$V_{CC}=4.5\text{V}$	-	-	88	ns		
	$V_{CC}=6.0\text{V}$	-	-	74	ns		
transition time	t_t	see Figure 10	$V_{CC}=2.0\text{V}$	-	-	114	ns
			$V_{CC}=4.5\text{V}$	-	-	23	ns
			$V_{CC}=6.0\text{V}$	-	-	19	ns



pulse width	t_w	up clock pulse width HIGH or LOW; see Figure 7	$V_{CC}=2.0V$	180	-	-	ns
			$V_{CC}=4.5V$	36	-	-	ns
			$V_{CC}=6.0V$	31	-	-	ns
		down clock pulse width HIGH or LOW; see Figure 7	$V_{CC}=2.0V$	210	-	-	ns
			$V_{CC}=4.5V$	42	-	-	ns
			$V_{CC}=6.0V$	36	-	-	ns
		master reset pulse width HIGH; see Figure 10	$V_{CC}=2.0V$	120	-	-	ns
			$V_{CC}=4.5V$	24	-	-	ns
			$V_{CC}=6.0V$	20	-	-	ns
parallel load pulse width LOW; see Figure 9	$V_{CC}=2.0V$	120	-	-	ns		
	$V_{CC}=4.5V$	24	-	-	ns		
	$V_{CC}=6.0V$	20	-	-	ns		
recovery time	t_{rec}	\bar{PL} to CPU, CPD; see Figure 9	$V_{CC}=2.0V$	78	-	-	ns
			$V_{CC}=4.5V$	16	-	-	ns
			$V_{CC}=6.0V$	13	-	-	ns
		MR to CPU, CPD; see Figure 10	$V_{CC}=2.0V$	78	-	-	ns
			$V_{CC}=6.0V$	13	-	-	ns
set-up time	t_{su}	Dn to \bar{PL} ; see Figure 11; note: CPU=CPD=HIGH	$V_{CC}=2.0V$	120	-	-	ns
			$V_{CC}=4.5V$	24	-	-	ns
			$V_{CC}=6.0V$	20	-	-	ns
hold time	t_h	Dn to \bar{PL} ; see Figure 11	$V_{CC}=2.0V$	0	-	-	ns
			$V_{CC}=4.5V$	0	-	-	ns
			$V_{CC}=6.0V$	0	-	-	ns
		CPU to CPD, CPD to CPU; see Figure 13	$V_{CC}=2.0V$	120	-	-	ns
			$V_{CC}=4.5V$	24	-	-	ns
			$V_{CC}=6.0V$	20	-	-	ns
maximum frequency	f_{max}	CPU, CPD; see Figure 7	$V_{CC}=2.0V$	3	-	-	MHz
			$V_{CC}=4.5V$	13	-	-	MHz
			$V_{CC}=6.0V$	16	-	-	MHz

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] t_t is the same as t_{THL} and t_{TLH} .



4、Testing Circuit

4.1、AC Testing Circuit

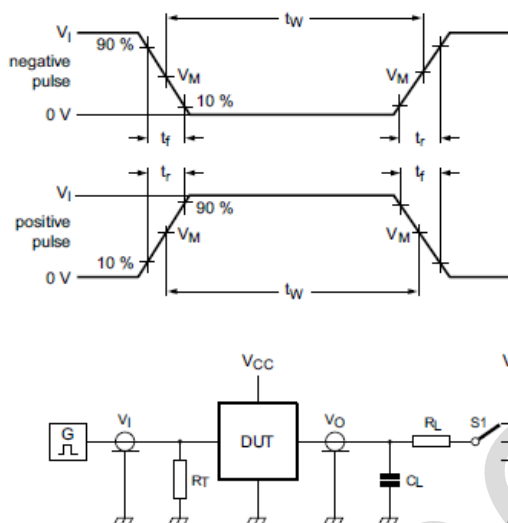


Figure 6. Test circuit for measuring switching times

Definitions for test circuit:

R_L =Load resistance.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

S1=Test selection switch.

4.2、AC Testing Waveforms

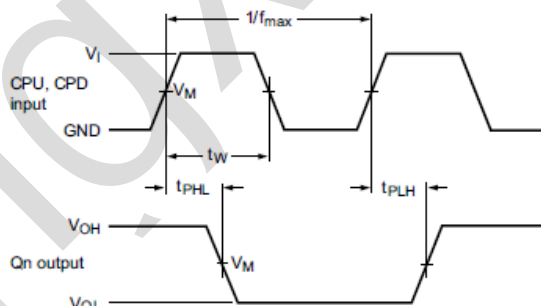


Figure 7. The clock (CPU, CPD) to output (Qn) propagation delays, the clock pulse width, and the maximum clock pulse frequency

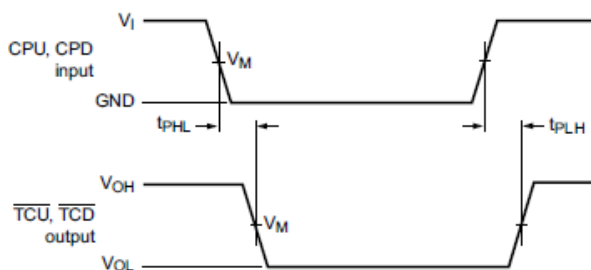


Figure 8. The clock (CPU, CPD) to terminal count output (TCU, TCD) propagation delays

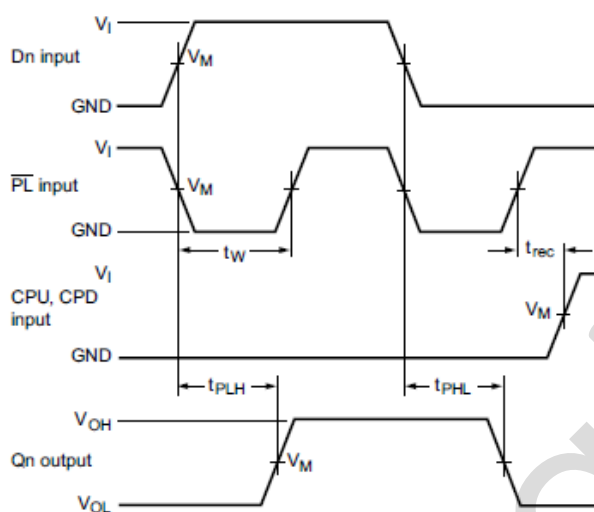


Figure 9. The parallel load input (\overline{PL}) and data (Dn) to Qn output propagation delays and \overline{PL} removal time to clock input (CPU, CPD)

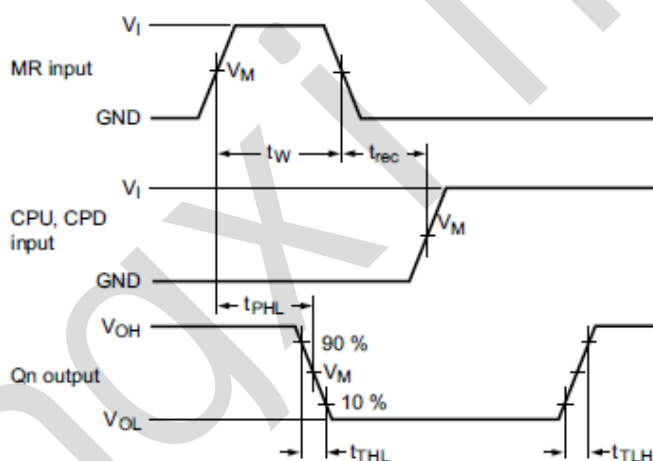


Figure 10. The master reset input (MR) pulse width, MR to Qn propagation delays, MR to CPU, CPD removal time and output transition times

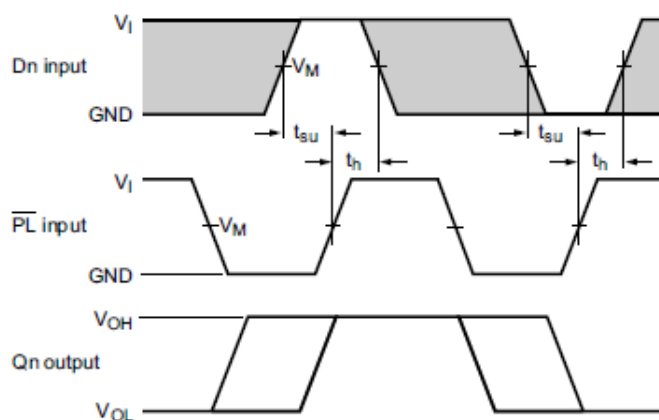


Figure 11. The data input (Dn) to parallel load input (\overline{PL}) set-up and hold times

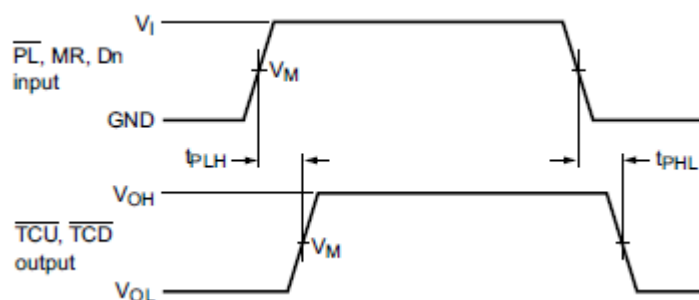


Figure 12. The data input (Dn), parallel load input (PL) and the master reset input (MR) to the terminal count outputs (TCU, TCD) propagation delays

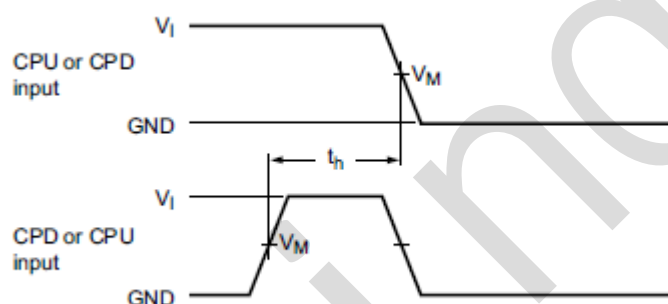


Figure 13. The CPU to CPD or CPD to CPU hold times

4.3. Measurement Points

Input		Output
V_I	V_M	V_M
GND to V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

4.4. Test Data

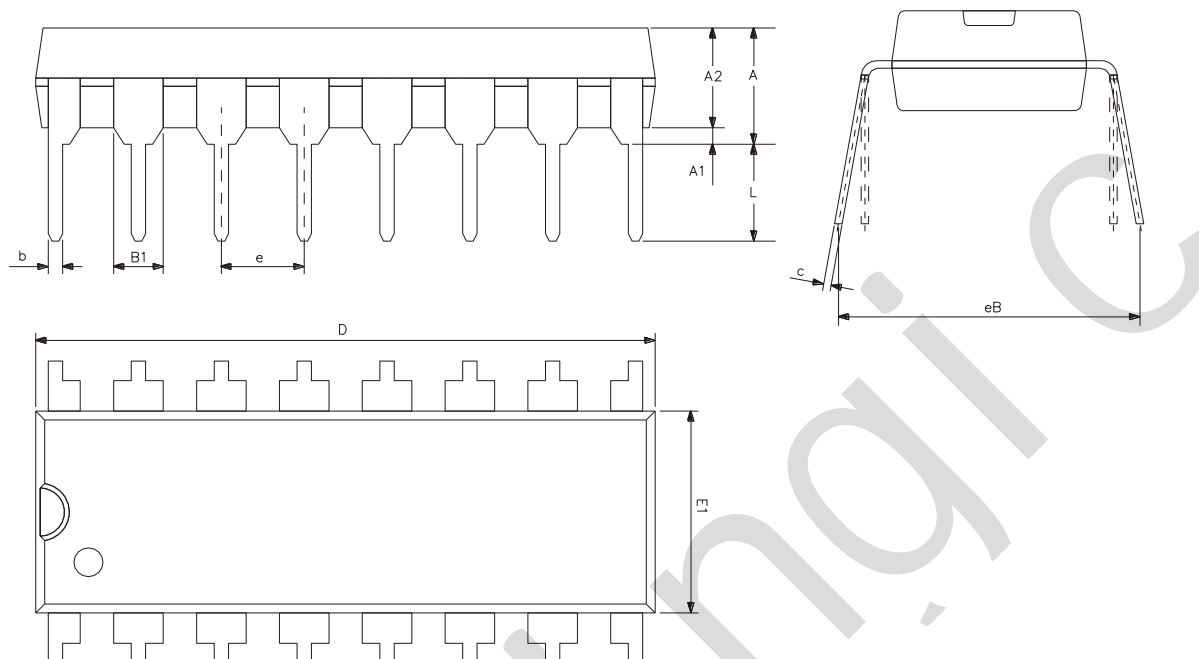
Input		Load		S1 position
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
V_{CC}	6ns	15pF, 50pF	1k Ω	open



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5、Package Information

5.1、DIP16

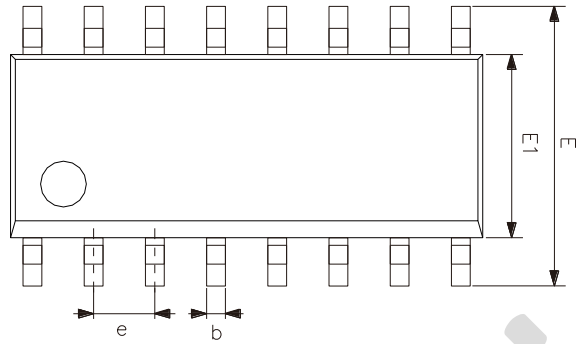
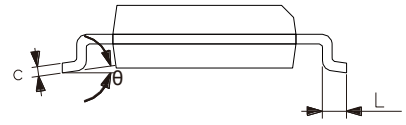
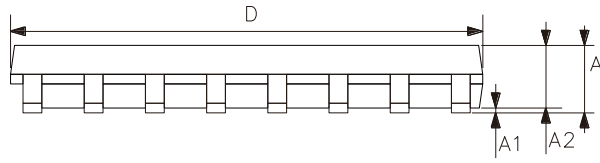


Symbol	Dimensions (mm)	
	Min.	Max.
A2	3.20	3.60
A1	0.51	-
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
c	0.20	0.36
eB	7.62	9.30



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5.2、SOP16

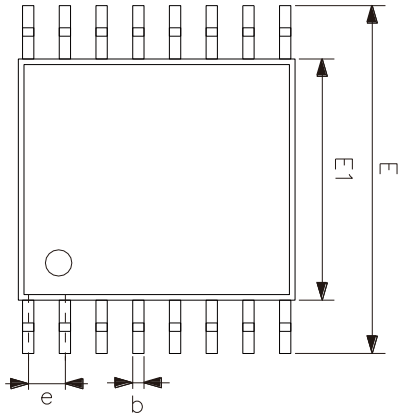
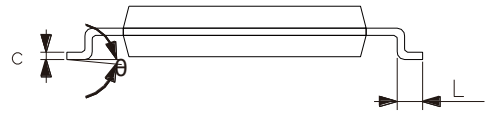
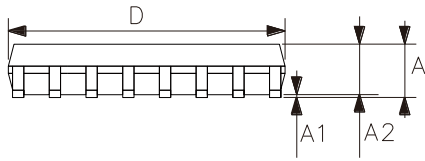


Symbol	Dimensions (mm)	
	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°



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5.3、TSSOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°



6、 Statements And Notes

6.1、 The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、 Notes

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