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LKS32MC03x with built-in 6N Gate Driver
32bit Compact MCU for Motor Control

Features

- 48MHz 32-bit Cortex-M0 core, hardware division coprocessor
- 30uA low-power sleep mode
- -40-105℃ industrial-grade operating temperature range
- MCU uses 2.2V~5.5V single power supply, and gate driver uses 7~20V power supply
- Super antistatic and anti-group pulse capability

Storage

- Three specifications including 16kB flash/16kB flash+16kB ROM/32kB flash, with a flash anti-stealing feature
- 4kB RAM

Timer

- Built-in 4MHz high-precision RC timer, with a full temperature range accuracy of ±1%
- Built-in 64kHz low-speed timer for use in low-power mode
- Internal PLL providing up to a 48MHz timer

Peripherals

- One UART
- One SPI
- One IIC
- General-purpose 16-/32-bit timer, supporting capture and edge-aligned PWM
- Dedicated PWM module for motor control, supporting 6 PWM outputs, independent dead zone control
- Dedicated interface for Hall signals, supporting speed measurement and debounce
- 4-channel DMA
- Hardware watchdog
- Supports up to 25 GPIOs

Analog Module

- Integrated one 12-bit SAR ADC, 1Msps sampling and conversion rate, 11 channels in total
- Integrated 2 OPA, settable for a differential PGA mode
- Integrated two comparators
- Integrated 8-bit DAC digital-to-analog converter as an internal comparator input
- Built-in 1.2V voltage reference with an accuracy of 0.5%
- Built-in 1 low-power LDO and power monitoring circuit
- Integrated high-precision, low-temperature drift high-frequency RC timer

Key Strengths

✧ The internal integration of 2 high-speed operational amplifiers can meet the different requirements of single-resistor/dual-resistance current sampling topology;
✧ The input port of the operational amplifier integrates a voltage clamp protection circuit, and only two external current-limiting resistors are needed to achieve direct current sampling of the MOSFET internal resistance;
✧ ADC module variable gain technology can work with high-speed operational amplifiers to handle a wider dynamic range of current and take into account the sampling accuracy of small current and large current;
✧ Integrated two-way comparator;
✧ Strong ESD and anti-interference ability, stable and reliable;
✧ supply to ensure the versatility of system power supply.

Application Scenarios

Applicable to control systems such as BLDC/ Sensorless BLDC/ FOC/Sensorless FOC and stepping motors, permanent magnet synchronous motors, asynchronous motors, digital power source etc.

1 Overview

1.1 Function Description

The LKS32MC034D(O)F6Q8/LKS32MC034SF6Q8 are 32-bit core compact MCU intended for motor control applications that integrates all the modules required for common motor control systems. LKS32MC034D(O)F6Q8/LKS32MC034SF6Q8 integrates three-phase full-bridge bootstrapping gate drive modules, which can directly drive six N-type MOSFETs.

LKS32MC034DOF6Q8 also integrates a 5V LDO with 7-20V input and 80mA output power capability internally.

- **Performance**
  - 48MHz 32-bit Cortex-M0 core
  - Low-power sleep mode
  - Integrated three-phase full-bridge bootstrapping gate drive modules
  - Industrial-grade operating temperature range
  - Super antistatic and anti-group pulse capability

- **Memory**
  - 32 kB Flash with encryption, a 128-bit chip unique identifier
  - 4kB RAM
- **Operating Range**
  - Dual power supply. The MCU part of LKS32MC034DOF6Q8/LKS32MC034SF6Q8 is powered by a 7V~20V power supply. Two LDOs are integrated inside, one of which is 5V LDO to supply power for the analog circuit and the other for digital circuits. The 6N gate driver module is powered by a 4.5~20V power supply.
  - Operating temperature: -40~105℃
- **Timer**
  - Built-in 4MHz high-precision RC timer, with an accuracy within ±1% in a range of -40~105℃
  - Built-in 64kHz low-speed timer for use in low-power mode
  - Internal PLL providing up to a 48MHz timer
- **Peripheral Module**
  - One UART
  - One SPI for master-slave mode
  - One IIC for master-slave mode
  - One general-purpose 16-bit timer, supporting capture and edge-aligned PWM functions
  - One general-purpose 32-bit timer, supporting capture and edge-aligned PWM functions;

- Dedicated PWM module for motor control, supporting 8 PWM outputs, independent dead zone control
- Dedicated interface for Hall signals, supporting speed measurement and debounce functions
- Hardware watchdog
- 25 GPIOs. Eight GPIOs can be used as wake-up sources for the system. 17 GPIOs can be used as external interrupt source inputs

- **Analog Module**
  - Integrated one 12-bit SAR ADC, 1.2Msps sampling and conversion rate, 11 channels in total
  - Integrated a 2-channel operational amplifier, settable for a differential PGA mode
  - Integrated two comparators
  - Integrated 8-bit DAC digital-to-analog converter
  - Built-in ±2℃ temperature sensor
  - Built-in 1.2V voltage reference with an accuracy of 0.5%
  - Built-in 1 low-power LDO and power monitoring circuit
  - Integrated high-precision, low-temperature drift high-frequency RC timer

- **Packaging:**

Table 1-1 Summary of LKS32MC03x Package Models

Model	Package Type
LKS32MC033H6P8	TSSOP20
LKS32MC033H6Q8	QFN20
LKS32MC034DF6Q8	QFN40
LKS32MC034DOF6Q8	QFN40
LKS32MC035DL6S8	SOP16
LKS32MC035EL6S8	ESOP16
LKS32MC037M6S8	SSOP24
LKS32MC037EM6S8	SSOP24
LKS32MC037FM6S8	SSOP24
LKS32MC037QM6Q8	QFN24
LKS32MC038Y6P8	TSSOP28

1.2 Key Strengths

- High reliability, high integration, small volume of final product, saving BOM costs.
- Internally integrated 2-channel high-speed operational amplifier and two comparators to meet the different requirements of single-resistor/dual-resistor current sampling topologies;
- Internal high-speed operational amplifier integrating high-voltage protection circuits, allowing the high-level common-mode signal to be directly input into the chip, and realizing the direct current sampling mode of MOSFET resistance with the simplest circuit topology;
- The application of patented technology enables the ADC and high-speed operational

amplifier to match best, which can handle a wider current dynamic range, while taking into account the sampling accuracy of high-speed small current and low-speed large current;

- The overall control circuit is simple and efficient, with stronger anti-interference ability, more stable and reliable;
- Integrated three-phase full-bridge bootstrapping gate drive modules;
- LKS32MC034DOF6Q8 with an integrated 5V LDO internally

Applicable to control systems such as inductive BLDC/non-inductive BLDC/inductive FOC/non-inductive FOC and stepping motors, permanent magnet synchronous motors, asynchronous motors, etc.;

1.3 Naming Conventions

LKS32 MC 037 M 6 S 8 YYWWX

Device series

LKS32	= 32bit MCU

Product type

MC	= Motor Control Applications
AT	= Automobile Applications

Device sub family

033	= 1 ADC, 2 PGA
034D	= 1 ADC, 2 PGA, 6N Driver
034DO	= 1 ADC, 2 PGA, 6N Driver, 5V LDO
034S	= 1 ADC, 2 PGA, 6N Driver, 5V LDO, DBOOT
035D,035E	= 1 ADC, 1 PGA, 3P3N Driver, 5V LDO
033,037,038	= 1 ADC, 2 PGA
037E,037F	= 1 ADC, 2 PGA, 3P3N Driver, 5V LDO

Pin count

L	= 16 pins
H	= 20 pins
M	= 24 pins
Y	= 28 pins
K	= 32 pins
F	= 40 pins
C	= 48 pins
N	= 52 pins
R	= 64 pins
V	=100 pins
Z	=144 pins

Code size

4	= 16Kbyte Flash Memory
6	= 32Kbyte Flash Memory
8	= 64Kbyte Flash Memory
B	=128Kbyte Flash Memory
C	=256Kbyte Flash Memory
D	=384Kbyte Flash Memory
E	=512Kbyte Flash Memory

Package

P	= TSSOP
T	= TQFP/LQFP
Q	= QFN
S	= SSOP
H	= BGA

Temperature range

6	= -40~85°
8	= -40~105°
9	= -40~125°

Date Code/Version

YYWW	= Date Code
X	= Version, A~Z

Figure 1-1 LKS32MC03x Device Naming Conventions

1.4 System Resources

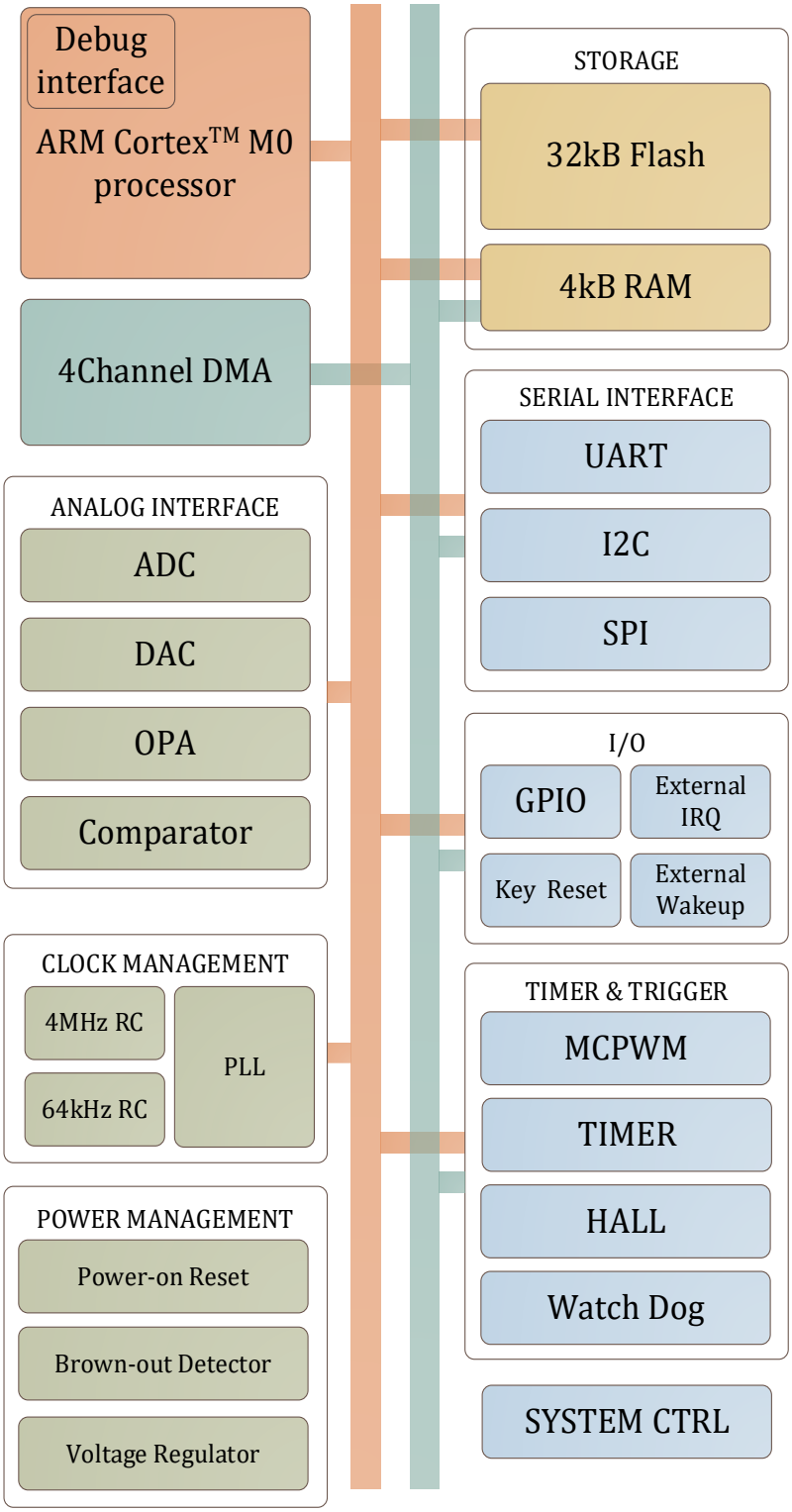

Figure 1-2 LKS32MC03x System Block Diagram

1.5 FOC System

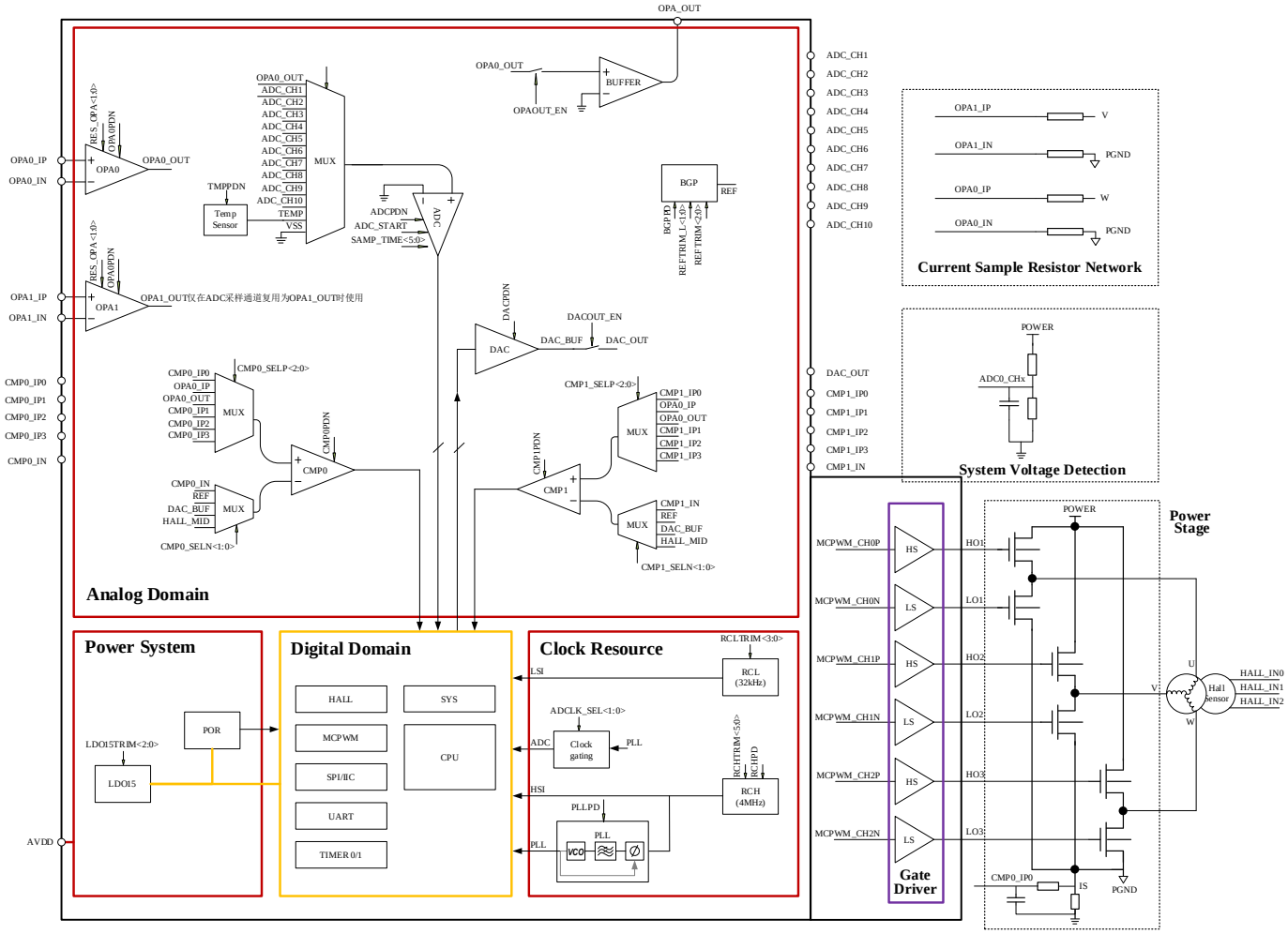

Figure 1-3 Simplified Schematic Diagram of the LKS32MC03x Vector Sinusoidal Control System

2 Device Selection Table

Table 2-1 LKS03x Series Device Selection Table

	Frequency (MHz)	Flash (kB)	RAM (kB)	ADC ch.	DAC	Comparator	Comparator ch.	OPA	HALL	SPI	IIC	UART	CAN	Temp. Sensor	PLL	QEP	Gate driver	Gate Driver current (A)	Pre-drive supply (V)	Gate floating voltage (V)	Others	Package
LKS32MC033H6P8	48	32	4	7	8BITx1	2	5	1	3	1	1	1		Yes	Yes							TSSOP20
LKS32MC033H6Q8	48	32	4	7	8BITx1	2	5	1	3	1	1	1		Yes	Yes							QFN20
LKS32MC034DOF6Q8	48	32	4	9	8BITx1	2	8	2	3	1	1	1		Yes	Yes		6N	+1.2/-1.5	4.5-20	200		QFN40
LKS32MC034DOF6Q8	48	32	4	9	8BITx1	2	8	2	3	1	1	1		Yes	Yes		6N	+1.2/-1.5	4.5-20	200	5V LDO*	QFN40
LKS32MC034SF6Q8	48	32	4	9	8BITx1	2	8	2	3	1	1	1		Yes	Yes		6N	+1/-1.2	4.5~20	280	5V LDO*	QFN40
LKS32MC035DL6S8	48	32	4	6	8BITx1	2	4	1	3	1	1	1		Yes	Yes		3P3N	+0.05/-0.3	7.5-28		5V LDO	SOP16
LKS32MC037M6S8	48	32	4	9	8BITx1	2	8	2	3	1	1	1		Yes	Yes							SSOP24
LKS32MC037EM6S8	48	32	4	9	8BITx1	2	7	2	3	1	1	1		Yes	Yes		3P3N	+0.05/-0.3	7.5-28		5V LDO	SSOP24
LKS32MC037FM6S8	48	32	4	9	8BITx1	2	7	2	3	1	1	1		Yes	Yes		3P3N	+0.05/-0.3	7.5-28		5V LDO	SSOP24
LKS32MC037QM6Q8	48	32	4	9	8BITx1	2	7	2	3	1	1	1		Yes	Yes		3P3N	+0.05/-0.3	7.5~28		5V LDO	QFN24
LKS32MC038Y6P8	48	32	4	9	8BITx1	2	8	2	3	1	1	1		Yes	Yes							TSSOP28

*Some models have integrated 5V LDOs. When the chip is powered by a 7.5-28V VCC, the internal LDOs can generate a 5V power supply for MCUs or to off-chip, as per pin description.

3 Pin Assignment

3.1 Pin Assignment Diagram

3.1.1 Special Notes

PU is short for pull-up. The PU pin in the following pin diagrams is designed with an internal pull-up resistor to the AVDD.

The RSTN pin is equipped with an internal 100kΩ pull-up resistor that is fixed to turn on the pull-up, which can be turned off when the RSTN function is switched to the GPIO function

The SWDIO/SWCLK comes with an internal 10kΩ pull-up resistor that is fixed to turn on the pull-up, which can be turned off when the SWD function is switched to the GPIO function

The remaining PU pins have an internal 10kΩ pull-up resistor that can be turned on or off by software control.

EXTI is external interrupt or GPIO interrupt input pin.

WK is short for wake-up, is external wake-up source.

UARTx_TX(RX): UART supports an interchange between the TX and RX. When the second function of GPIO is selected as UART and GPIO_PIE i.e. input is enabled, it can be used as UART_RX; When GPIO_POE is enabled, it can be used as UART_TX. Generally, the same GPIO does not enable input and output at the same time, otherwise the input PDI will receive the data sent by the PDO.

SPI_DI(DO): The DI and DO of SPI can be interchanged. When the second function of GPIO is SPI, and GPIO_PIE i.e. input is enabled, it can be used as SPI_DI; when GPIO_POE i.e. output is enabled, it can be used as SPI_DO. Generally, the same GPIO does not enable input and output at the same time, otherwise the input PDI will receive the data sent by the PDO.

3.1.1 Version Difference

There are two versions for each package. The major difference is the pin location of ADC_CH6/ ADC_CH7. For details, please refer to the table below.

B version is recommended for new design.

Table 3-1 Version Comparison

A Version (YYWWA)		B Version (YYWWB)	
DAC output range 0~3V		DAC output range0~3V/4.8V	
P0_9	CLKO	P0_9	CLKO
	MCPWM_CH0P		MCPWM_CH0P
	UART0_RXD		UART0_RXD
	SPI_DO		SPI_DO

	SDA		SDA
	TIM0_CH1		TIM0_CH1
	ADC_TRIGGER		ADC_TRIGGER
	CMP0_IN		CMP0_IN
	PU		PU
	EXTI7		EXTI7
			ADC_CH6
	WK3		WK3
P0_10	CLKO	P0_10	CLKO
	MCPWM_CH0P		MCPWM_CH0P
	TIM0_CH0		TIM0_CH0
	TIM1_CH0		TIM1_CH0
	ADC_CH6		
	WK4		WK4
P0_15	MCPWM_CH2N	P0_15	MCPWM_CH2N
	TIM1_CH0		TIM1_CH0
	ADC_CH7		
	EXTI9		EXTI9
P1_6	CMP1_OUT	P1_6	CMP1_OUT
	HALL_IN1		HALL_IN1
	MCPWM_CH2N		MCPWM_CH2N
	UART0_TXD		UART0_TXD
	TIM0_CH1		TIM0_CH1
	ADC_TRIGGER		ADC_TRIGGER
			ADC_CH7
	CMP1_IP2		CMP1_IP2
	PU		PU
	EXTI12		EXTI12
P1_5	SPI_DI	P1_5	SPI_DI
	SCL		SCL
	TIM1_CH1		TIM1_CH1
	OPA1_IN		OPA1_IN
			ADC_CH8
	CMP1_IP0		CMP1_IP0
	PU		PU
	EXTI11		EXTI11
	WK5		WK5

In A Version, the chip doesn't have ADC_CH8 pin. In B Version, users who don't need OPA1, could use ADC_CH8 by setting SYS_OPA_SEL=0.

3.1.2 LKS32MC034DF6Q8-YYWWA

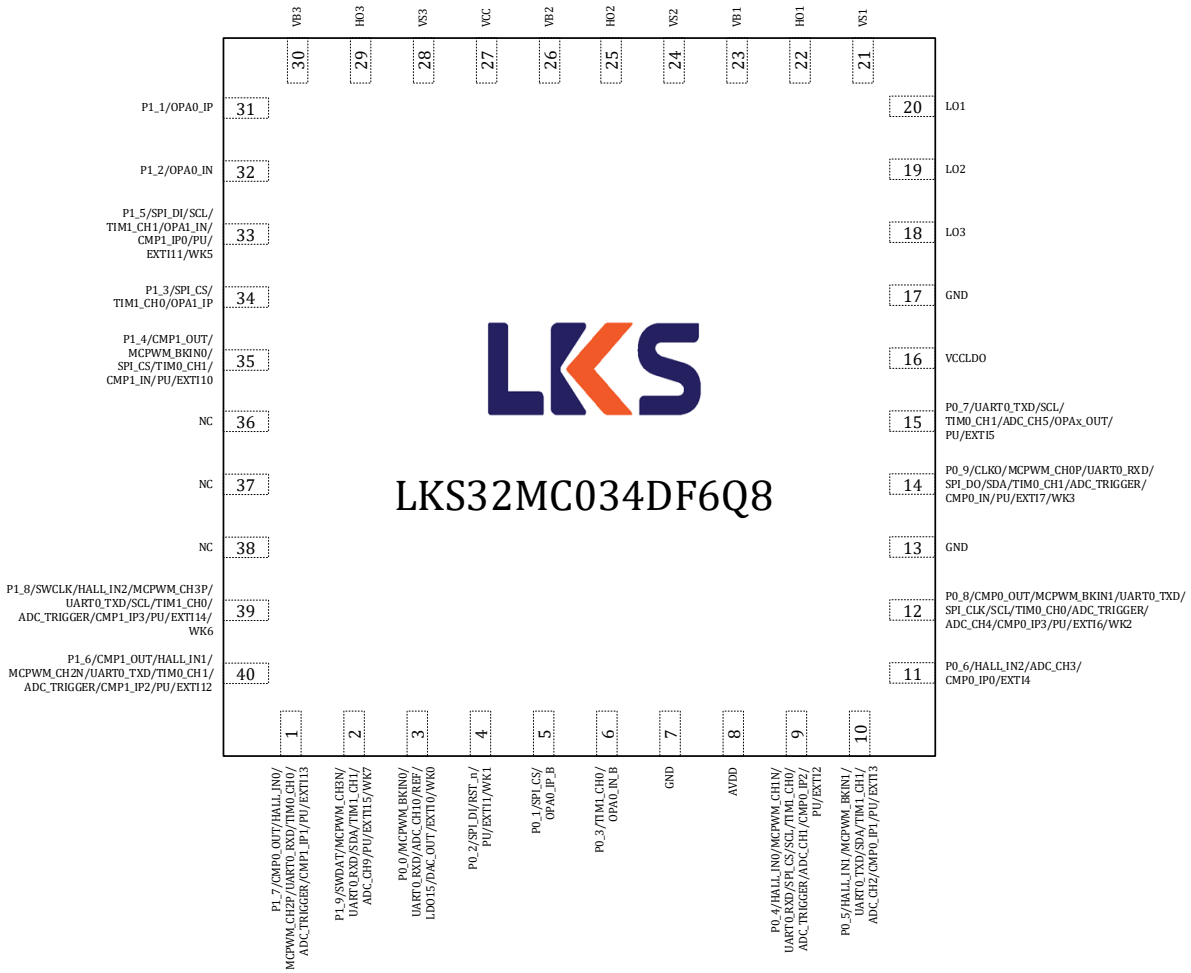

Figure 3-1 LKS32MC034DF6Q8-YYWWA Pin Assignment Diagram

Table 3-2 LKS32MC034DF6Q8-YYWWA Pin Description

1	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0

	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13
2	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
3	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
4	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1
5	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
6	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
7	GND	Ground
8	AVDD	Power supply, 2.2~5.5V
9	P0_4	P0.4
	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side

	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal 2
10	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal 3
11	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3
	CMP0_IP0	Comparator0 positive input0
	EXTI4	External GPIO interrupt input signal 4
12	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
13	GND	Ground
14	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)

	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
15	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
16	NC	Not connected
17	GND	Ground
18	LO3	Phase C low-side output, worked by MCU P0.12; the polarity of LO3 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.
19	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
20	LO1	Phase A low-side output, worked by MCU P0.10; the polarity of LO1 is the same as that of P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
21	VS1	High-side floating bias voltage 1.
22	HO1	Phase A high-side output, worked by MCU P0.13; the polarity of HO1 is the same as that of P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
23	VB1	High-side floating supply voltage 1.
24	VS2	High-side floating bias voltage 2.
25	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
26	VB2	High-side floating supply voltage 2.
27	VCC	Gate driver power supply, 4.5~20V
28	VS3	High-side floating bias voltage 3.
29	HO3	Phase C high-side output, worked by MCU P0.15; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
30	VB3	High-side floating supply voltage 3.
31	P1_1	P1.1
	OPA0_IP	OPA0 positive input
32	P1_2	P1.2
	OPA0_IN	OPA0 negative input
33	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock

	TIM1_CH1	Timer1 channel1
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
34	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
35	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal 10
36	NC	Not connected
37	NC	Not connected
38	NC	Not connected
39	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6
40	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal 12

3.1.3 LKS32MC034DF6Q8-YYWWB

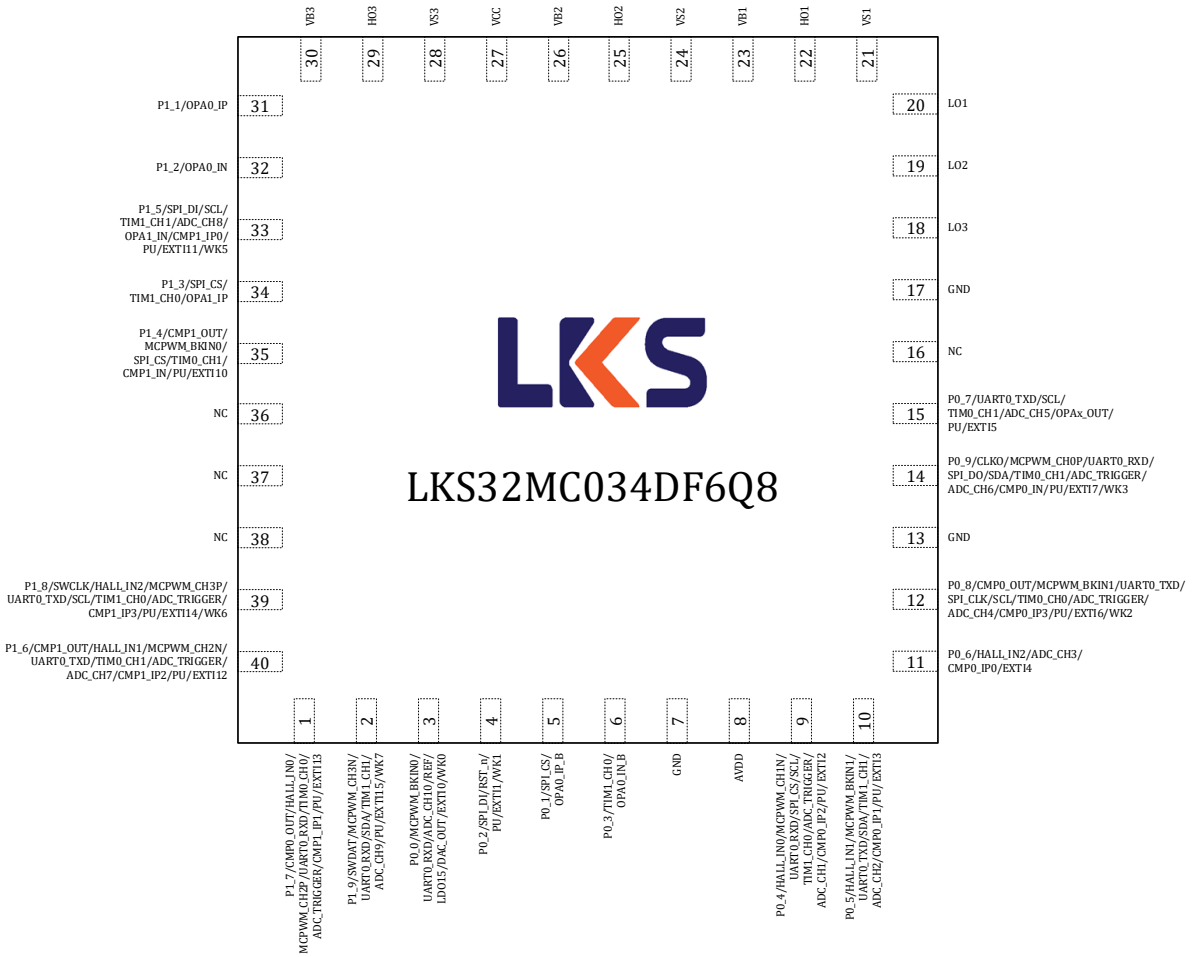

Figure 3-2 LKS32MC034DF6Q8-YYWWB Pin Assignment Diagram

Table 3-3 LKS32MC034DF6Q8-YYWWB Pin Description

1	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1

	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13
2	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
3	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
4	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1
5	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
6	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
7	GND	Ground
8	AVDD	Power supply, 2.2~5.5V
9	P0_4	P0.4
	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select

	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal 2
10	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal 3
11	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3
	CMP0_IP0	Comparator0 positive input0
	EXTI4	External GPIO interrupt input signal 4
12	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
13	GND	Ground
14	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1

	ADC_TRIGGER	ADC trigger for debug
	ADC_CH6	ADC channel 6
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
15	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
16	NC	Not connected
17	GND	Ground
18	LO3	Phase C low-side output, worked by MCU P0.12; the polarity of LO3 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.
19	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
20	LO1	Phase A low-side output, worked by MCU P0.10; the polarity of LO1 is the same as that of P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
21	VS1	High-side floating bias voltage 1.
22	HO1	Phase A high-side output, worked by MCU P0.13; the polarity of HO1 is the same as that of P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
23	VB1	High-side floating supply voltage 1.
24	VS2	High-side floating bias voltage 2.
25	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
26	VB2	High-side floating supply voltage 2.
27	VCC	Gate driver power supply, 4.5~20V
28	VS3	High-side floating bias voltage 3.
29	HO3	Phase C high-side output, worked by MCU P0.15; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
30	VB3	High-side floating supply voltage 3.
31	P1_1	P1.1
	OPA0_IP	OPA0 positive input
32	P1_2	P1.2
	OPA0_IN	OPA0 negative input
33	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1

	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
34	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
35	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal 10
36	NC	Not connected
37	NC	Not connected
38	NC	Not connected
39	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6
40	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH7	ADC channel 7
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software

	EXTI12	External GPIO interrupt input signal 12

3.1.4 LKS32MC034DOF6Q8/LKS32MC034SF6Q8-YYWWA

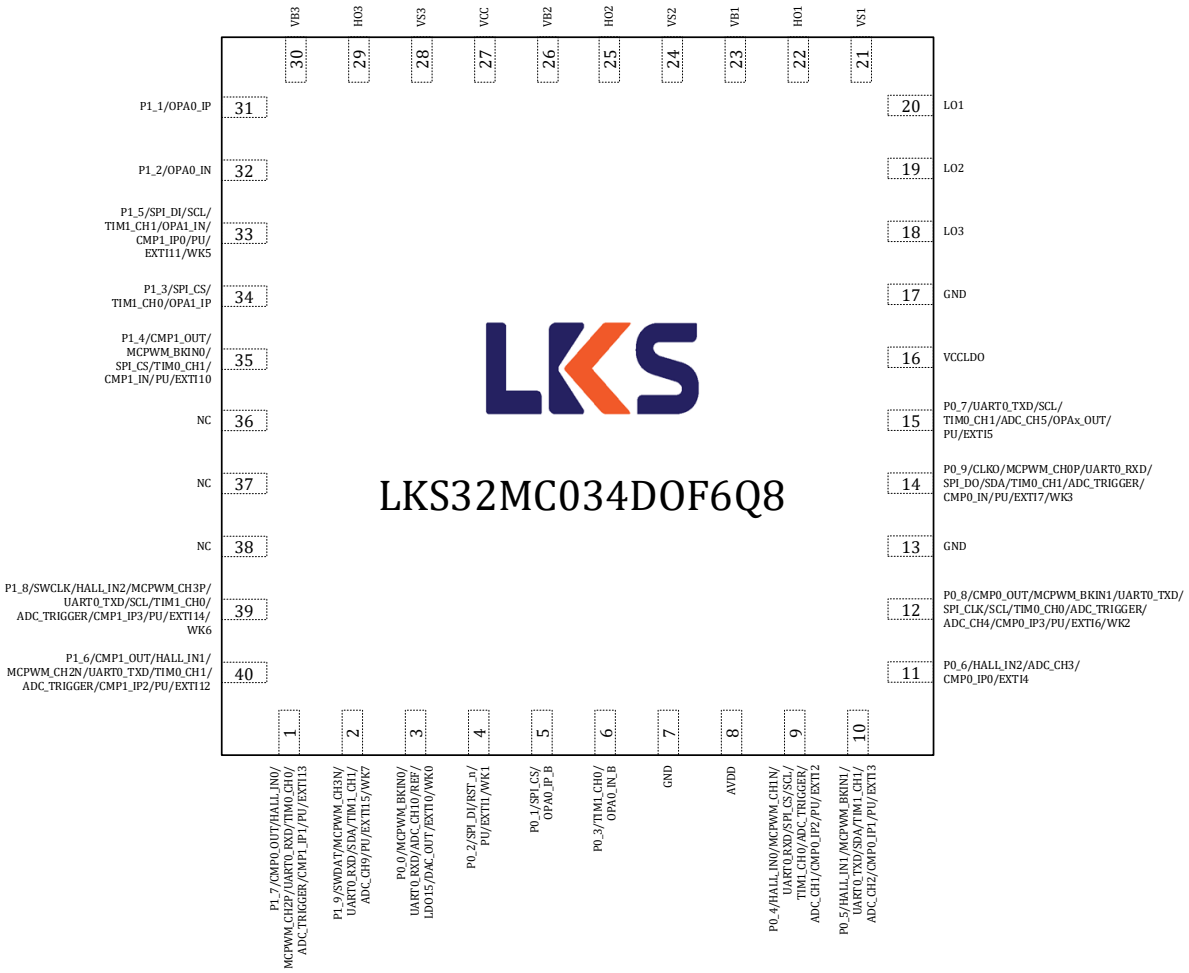

Figure 3-3 LKS32MC034DOF6Q8/LKS32MC034SF6Q8-YYWWA Pin Assignment Diagram

The LKS32MC034DOF6Q8 is pin compatible with the LKS32MC034SF6Q8, which integrates a bootstrap diode between VCC and three-phase VBS.

Table 3-4 LKS32MC034DOF6Q8/LKS32MC034SF6Q8 Pin Description

1	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)

	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13
2	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
3	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
4	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1
5	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
6	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
7	GND	Ground
8	AVDD	5V LDO voltage output
9	P0_4	P0.4
	HALL_IN0	Hall interface input 0

	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal 2
10	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal 3
11	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3
	CMP0_IP0	Comparator0 positive input0
	EXTI4	External GPIO interrupt input signal 4
12	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
13	GND	Ground
14	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)

	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
15	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
16	VCCLDO	5V LDO power supply, 7-20 V, with an output current limit of < 80mA. Decoupling capacitors should be > 0.33uF and placed as close as possible to this pin.
17	GND	Ground
18	LO3	Phase C low-side output, worked by MCU P0.12; the polarity of LO3 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.
19	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
20	LO1	Phase A low-side output, worked by MCU P0.10; the polarity of LO1 is the same as that of P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
21	VS1	High-side floating bias voltage 1.
22	HO1	Phase A high-side output, worked by MCU P0.13; the polarity of HO1 is the same as that of P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
23	VB1	High-side floating supply voltage 1.
24	VS2	High-side floating bias voltage 2.
25	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
26	VB2	High-side floating supply voltage 2.
27	VCC	Gate driver power supply, 4.5~20V
28	VS3	High-side floating bias voltage 3.
29	HO3	Phase C high-side output, worked by MCU P0.15; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
30	VB3	High-side floating supply voltage 3.
31	P1_1	P1.1
	OPA0_IP	OPA0 positive input
32	P1_2	P1.2
	OPA0_IN	OPA0 negative input
33	P1_5	P1.5

	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
34	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
35	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal 10
36	NC	Not connected
37	NC	Not connected
38	NC	Not connected
39	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6
40	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP2	Comparator1 positive input2

	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal 12

3.1.5 LKS32MC034DOF6Q8/LKS32MC034SF6Q8-YYWWB

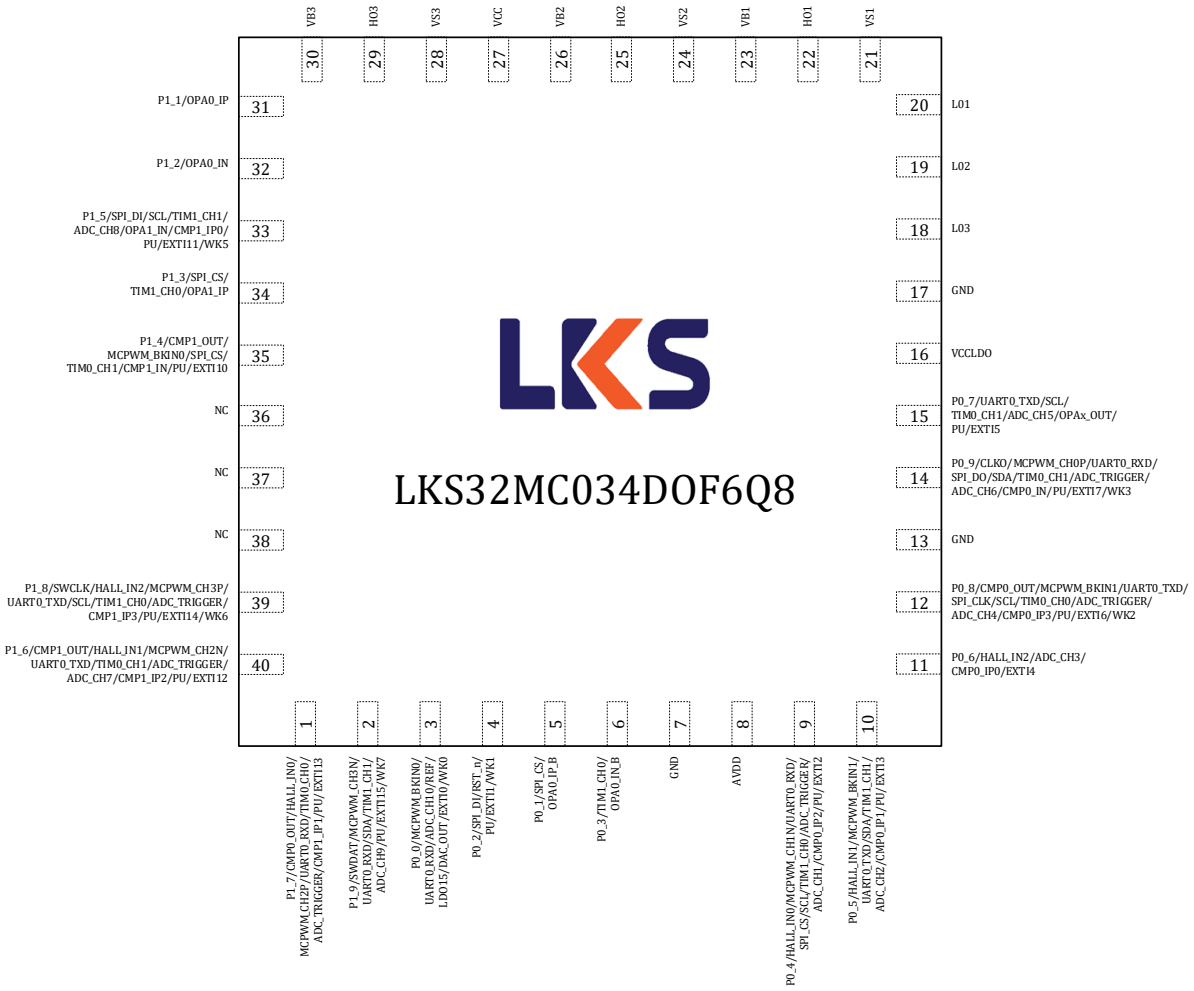

Figure 3-4 LKS32MC034DOF6Q8/LKS32MC034SF6Q8-YYWWB Pin Assignment Diagram

The LKS32MC034DOF6Q8 is pin compatible with the LKS32MC034SF6Q8, which integrates a bootstrap diode between VCC and three-phase VBS.

Table 3-5 LKS32MC034DOF6Q8/LKS32MC034SF6Q8 -YYWWBPin Description

1	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side

	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13
2	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
3	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
4	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1
5	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
6	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
7	GND	Ground
8	AVDD	5V LDO voltage output
9	P0_4	P0.4

	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal 2
10	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal 3
11	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3
	CMP0_IP0	Comparator0 positive input0
	EXTI4	External GPIO interrupt input signal 4
12	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
13	GND	Ground
14	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side

	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH6	ADC channel 6
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
15	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
16	VCCLDO	5V LDO power supply, 7-20 V, with an output current limit of < 80mA. Decoupling capacitors should be > 0.33uF and placed as close as possible to this pin.
17	GND	Ground
18	LO3	Phase C low-side output, worked by MCU P0.12; the polarity of LO3 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.
19	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
20	LO1	Phase A low-side output, worked by MCU P0.10; the polarity of LO1 is the same as that of P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
21	VS1	High-side floating bias voltage 1.
22	HO1	Phase A high-side output, worked by MCU P0.13; the polarity of HO1 is the same as that of P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
23	VB1	High-side floating supply voltage 1.
24	VS2	High-side floating bias voltage 2.
25	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
26	VB2	High-side floating supply voltage 2.
27	VCC	Gate driver power supply, 4.5~20V
28	VS3	High-side floating bias voltage 3.
29	HO3	Phase C high-side output, worked by MCU P0.15; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
30	VB3	High-side floating supply voltage 3.
31	P1_1	P1.1
	OPA0_IP	OPA0 positive input
32	P1_2	P1.2

	OPA0_IN	OPA0 negative input
33	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
34	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
35	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal 10
36	NC	Not connected
37	NC	Not connected
38	NC	Not connected
39	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6
40	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)

	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH7	ADC channel 7
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal 12

3.2 Pin Multiplexing

Table 3-3 LKS32MC03x Pin Function Selection

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF0
P0.0			MCPWM_BKIN0	UART0_R(T)XD						ADC_CH10/REF/LDO15/DAC_OUT
P0.1					SPI_CS					OPA0_IP_B
P0.2					SPI_DI(O)					RST_n
P0.3								TIM1_CH0		OPA0_IN_B
P0.4		HALL_IN0	MCPWM_CH1N	UART0_R(T)XD	SPI_CS	SCL		TIM1_CH0	ADC_TRIGGER	ADC_CH1/CMP0_IP2
P0.5		HALL_IN1	MCPWM_BKIN1	UART0_T(R)XD				TIM1_CH1		ADC_CH2/CMP0_IP1
P0.6		HALL_IN2								ADC_CH3/CMP0_IP0
P0.7				UART0_T(R)XD		SCL	TIM0_CH1			ADC_CH5/OPAx_OUT
P0.8	CMP0_OUT		MCPWM_BKIN1	UART0_T(R)XD	SPI_CLK	SCL	TIM0_CH0		ADC_TRIGGER	ADC_CH4/CMP0_IP3
P0.9	CLKO		MCPWM_CH0P	UART0_R(T)XD	SPI_DO(I)	SDA	TIM0_CH1		ADC_TRIGGER	CMP0_IN
P0.10	CLKO		MCPWM_CH0P				TIM0_CH0	TIM1_CH0		ADC_CH6
P0.11			MCPWM_CH0N		SPI_CLK			TIM1_CH1		
P0.12			MCPWM_CH1P		SPI_DO(I)		TIM0_CH1			
P0.13			MCPWM_CH1N		SPI_DI(O)			TIM1_CH1		
P0.14			MCPWM_CH2P				TIM0_CH0			
P0.15			MCPWM_CH2N					TIM1_CH0		ADC_CH7

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF0
P1.1										OPA0_IP
P1.2										OPA0_IN
P1.3					SPI_CS			TIM1_CH0		OPA1_IP
P1.4	CMP1_OUT		MCPWM_BKIN0		SPI_CS		TIM0_CH1			CMP1_IN
P1.5					SPI_DI(O)	SCL		TIM1_CH1		OPA1_IN/CMP1_IP0
P1.6	CMP1_OUT	HALL_IN1	MCPWM_CH2N	UART0_T(R)XD			TIM0_CH1		ADC_TRIGGER	CMP1_IP2
P1.7	CMP0_OUT	HALL_IN0	MCPWM_CH2P	UART0_R(T)XD			TIM0_CH0		ADC_TRIGGER	CMP1_IP1
P1.8	SWCLK	HALL_IN2	MCPWM_CH3P	UART0_T(R)XD		SCL		TIM1_CH0	ADC_TRIGGER	CMP1_IP3
P1.9	SWDAT		MCPWM_CH3N	UART0_R(T)XD		SDA		TIM1_CH1		ADC_CH9

Table 3-3 LKS32MC03x-YYWWB Pin Function Selection

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF0
P0.0			MCPWM_BKIN0	UART0_R(T)XD						ADC_CH10/REF/LDO15/DAC_OUT
P0.1					SPI_CS					OPA0_IP_B
P0.2					SPI_DI(O)					RST_n
P0.3								TIM1_CH0		OPA0_IN_B
P0.4		HALL_IN0	MCPWM_CH1N	UART0_R(T)XD	SPI_CS	SCL		TIM1_CH0	ADC_TRIGGER	ADC_CH1/CMP0_IP2
P0.5		HALL_IN1	MCPWM_BKIN1	UART0_T(R)XD				TIM1_CH1		ADC_CH2/CMP0_IP1
P0.6		HALL_IN2								ADC_CH3/CMP0_IP0
P0.7				UART0_T(R)XD		SCL	TIM0_CH1			ADC_CH5/OPAx_OUT
P0.8	CMP0_OUT		MCPWM_BKIN1	UART0_T(R)XD	SPI_CLK	SCL	TIM0_CH0		ADC_TRIGGER	ADC_CH4/CMP0_IP3
P0.9	CLKO		MCPWM_CH0P	UART0_R(T)XD	SPI_DO(I)	SDA	TIM0_CH1		ADC_TRIGGER	ADC_CH6/CMP0_IN
P0.10	CLKO		MCPWM_CH0P				TIM0_CH0	TIM1_CH0		
P0.11			MCPWM_CH0N		SPI_CLK			TIM1_CH1		
P0.12			MCPWM_CH1P		SPI_DO(I)		TIM0_CH1			
P0.13			MCPWM_CH1N		SPI_DI(O)			TIM1_CH1		
P0.14			MCPWM_CH2P				TIM0_CH0			
P0.15			MCPWM_CH2N					TIM1_CH0		

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF0
P1.1										OPA0_IP
P1.2										OPA0_IN
P1.3					SPI_CS			TIM1_CH0		OPA1_IP
P1.4	CMP1_OUT		MCPWM_BKIN0		SPI_CS		TIM0_CH1			CMP1_IN
P1.5					SPI_DI(O)	SCL		TIM1_CH1		ADC_CH8/OPA1_IN/CMP1_IP0
P1.6	CMP1_OUT	HALL_IN1	MCPWM_CH2N	UART0_T(R)XD			TIM0_CH1		ADC_TRIGGER	ADC_CH7/CMP1_IP2
P1.7	CMP0_OUT	HALL_IN0	MCPWM_CH2P	UART0_R(T)XD			TIM0_CH0		ADC_TRIGGER	CMP1_IP1
P1.8	SWCLK	HALL_IN2	MCPWM_CH3P	UART0_T(R)XD		SCL		TIM1_CH0	ADC_TRIGGER	CMP1_IP3
P1.9	SWDAT		MCPWM_CH3N	UART0_R(T)XD		SDA		TIM1_CH1		ADC_CH9

4 Package Dimensions

4.1 LKS32MC034D(O)F6Q8/LKS32MC034SF6Q8

QFN40 Profile Quad Flat Package:

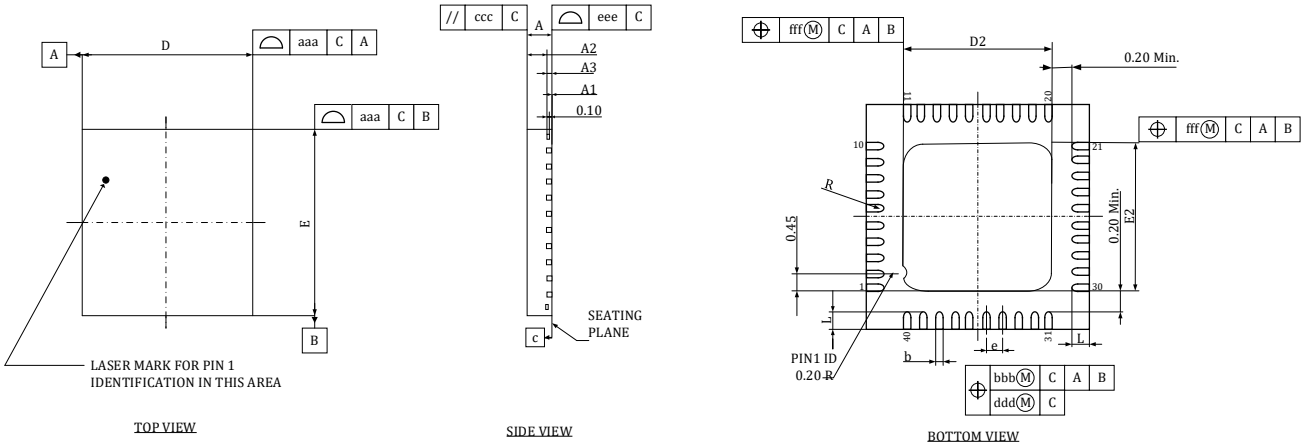

Figure 4-1 LKS32MC034D(O)F6Q8/LKS32MC034SF6Q8 Packaging

Table 4-1 LKS32MC034D(O)F6Q8/LKS32MC034SF6Q8 Package Dimensions

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.0008	0.002
A2	0.50	0.55	0.60	0.020	0.022	0.024
A3	0.2 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	4.90	5.00	5.10	0.193	0.197	0.201
D2	3.60	3.70	3.80	0.142	0.146	0.150
E	4.90	5.00	5.10	0.193	0.197	0.201
E2	3.60	3.70	3.80	0.142	0.146	0.150
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.4 bsc			0.016 bsc		
R	0.075	-	-	0.003	-	-
TOLERANCE OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

5 Electrical Characteristics

The LKS32MC034D(O)F6Q8 chip integrates a 6N Driver, in which some of the electrical parameters of the MCU are shown in the following table, taking the LKS32MC034DOF6Q8 as an example.

Table 5-1 LKS32MC034DOF6Q8 Electrical Limit Parameter

Parameter	Min.	Max.	Unit	Description
MCU Supply Voltage (AVDD)	-0.3	+6.0	V	
Gate Driver Supply Voltage (VCC)	-0.3	+25.0	V	LKS03x with 6N driver
Gate Driver Supply Voltage (VCC)	-0.3	+40.0	V	LKS03x with 3P3N driver
Supply Voltage (VCCLDO, pins in 034DO)	-0.3	+25.0	V	
Operating temperature	-40	+105	˚C	
Storage temperature	-40	+125	˚C	
Junction temperature	-	150	°C	
Pin temperature	-	300	°C	Soldering for 10 sec

Table 5-2 LKS32MC034DOF6Q8 Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit	Description
MCU Supply Voltage (AVDD)	2.2	5	5.5	V	
Analog Operating Voltage ($AVDD_A$)	2.8	5	5.5	V	REF2VDD=0, ADC uses internal 2.4V reference
	2.4	5	5.5	V	REF2VDD=1, ADC uses AVDD as reference
Gate Driver Supply Voltage (VCC)	4.5		20	V	LKS03x with 6N driver
LDO Supply Voltage (VCCLDO)	7		20	V	034DO LDO power supply

OPA could work under 2.2V, but the output range will be limited.

Table 5-3 LKS32MC034DOF6Q8 ESD parameters

Item	Min.	Max.	Unit
ESD test (HBM)	-6000	6000	V

According to "MIL-STD-883J Method 3015.9", under the environment of 25°C and 55% relative humidity, electrostatic discharge is applied to all IO pins of the tested chip for 3 times, with an interval of 1s each time. The test results show that the anti-static discharge level of the chip reaches Class 3A ≧4000V, <8000V.

Table 5-4 LKS32MC034DOF6Q8 Latch-up parameters

Item	Min.	Max.	Unit
Latch-up current (85°C)	-200	200	mA

According to "JEDEC STANDARD NO.78E NOVEMBER 2016", apply an overvoltage of 8V to all power IOs and inject 200mA of current on each signal IO. The test results show that the anti-latch-up level of the chip is 200mA.

Table 5-5 LKS32MC034DOF6Q8 IO Limit Parameter

Parameter	Description	Minimum	Maximum	Unit
V_{IN}	Input voltage range for GPIO signals	-0.3	6.0	V
I_{INJ_PAD}	Maximum injection current for single GPIOs	-11.2	11.2	mA
I_{INJ_SUM}	Maximum injection current for all GPIOs	-50	50	mA

Table 5-6 LKS32MC034DOF6Q8 IO DC Parameter

Parameter	Description	AVDD	Conditions	Min.	Max.	Unit
V_{IH}	High input level of digital IO	5V	-	0.7*AVDD		V
		3.3V		2.0		
V_{IL}	Low input level of digital IO	5V	-		0.3*AVDD	V
		3.3V			0.8	
V_{HYS}	Schmidt hysteresis range	5V	-	0.1*AVDD		V
		3.3V				
I_{IH}	Digital IO current consumption when input is high	5V	-		1	uA
		3.3V				
I_{IL}	Digital IO current consumption when input is low	5V	-	-1		uA
		3.3V				
V_{OH}	High output level of digital IO		Current = 11.2mA	AVDD-0.8		V
V_{OL}	Low output level of digital IO		Current = 11.2mA		0.5	V
R_{pup}	Pull-up resistor*			8	12	kΩ
C_{IN}	Digital IO Input-capacitance	5V	-		10	pF
		3.3V				

* Only part of IOs have built-in pull-up resistors. Please refer to the pin description section for details

Table 5-7 LKS32MC034DOF6Q8 Current Consumption IDDQ

Clock	Operating mode	3.3V	5V	Unit
48MHz	CPU, flash, SRAM, MCPWM, Timer, and all analog modules are active, IOs stay idle	8.570	8.650	mA
4MHz	CPU, flash, SRAM, MCPWM, Timer, and all analog modules except PLL are active, IOs stay idle	3.012	3.165	mA
32kHz		2.445	2.618	mA
-	Deep Sleep Mode, PLL and BGP are turned off, only 32kHz LRC is running	27	30	uA
-	All analog modules	2.4	2.55	mA

Unless otherwise specified, the above tests are all measured at room temperature of 25°. Due to the deviation of the device model in the manufacturing process, the current consumption of different chips will have individual differences.

6 Analog Characteristics

Table 6-1 LKS32MC034DOF6Q8 Analog Characteristics

Parameter	Min.	Typ.	Max.	Unit	Description
ADC					
Supply voltage	2.8	5	5.5	V	REF2VDD=0, ADC uses internal 2.4V reference
	2.4	5	5.5	V	REF2VDD=1, ADC uses AVDD as reference
Output bitrate		1.2		MHz	$f_{adc}/20$
Differential input signal range	-2.4		+2.4	V	When Gain=1;REF=2.4V
	-3.6		+3.6	V	When Gain=2/3; REF=3.6V
Single-ended input signal range	-0.3		AVDD+0.3	V	Limited by IO port input voltage
DC offset		5	10	mV	Correctable
Effective number of bits (ENOB)	10.5	11		bit	
INL		2	3	LSB	
DNL		1	2	LSB	
SNR	63	66		dB	
Input resistance	500k			Ohm	
Input capacitance		10pF		F	
Reference voltage (REF)					
Supply voltage	2.2	5	5.5	V	
Output deviation	-9		9	mV	
Power supply rejection ratio		70		dB	
Temperature coefficient		20		ppm/℃	
Output voltage		2.4		V	
DAC					
Supply voltage	2.2	5	5.5	V	
Load resistance	50k			Ohm	
Load capacitance			50p	F	
Output voltage range	0.05		3.0	V	
Switching speed			1M	Hz	
DNL		1	2	LSB	
INL		2	4	LSB	
OFFSET		5	10	mV	
SNR	57	60	66	dB	
Operational amplifier (OPA)					
Supply voltage	3.1	5	5.5	V	
Bandwidth		10M	20M	Hz	

Parameter	Min.	Typ.	Max.	Unit	Description
Load resistance	20k			Ohm	
Load capacitance			5p	F	
Common-mode input range	0		AVDD	V	
Output signal range	0.1		AVDD-0.1	V	Minimum load resistance
OFFSET		10	15	mV	
Common-mode rejection ratio (CMRR)		80		dB	
Power supply rejection ratio (PSRR)		80		dB	
Load current			500	uA	
Slew rate		5		V/us	
Phase margin		60		°	
Comparator (CMP)					
Supply voltage	2.2	5	5.5	V	
Input signal range	0		AVDD	V	
OFFSET		5	10	mV	
Transmission delay		0.15u		S	Default power consumption
		0.6u		S	Low power consumption
Hysteresis		20		mV	HYS='0'
		0		mV	HYS='1'

Table 6-2 LKS32MC034DO 5V LDO Module Parameter

5V LDO					
Input power	7		20	V	
Output voltage	4.75	5	5.25	V	+/-5% accuracy
Dropout voltage		2		V	
Output current		80		mA	
Ripple rejection		80		dB	
Decoupling capacitor input		0.33		uF	It is added to the VCCLDO pin. Please refer to the pin description section for details
Decoupling capacitor output		1		uF	It is added to the AVDD pin. Please refer to the pin description section for details
Operating temperature range	-40		125	℃	

Description of the analog register table:

The addresses 0x40000010-0x40000028 are the calibration registers for each module, which are provided with calibration values before being shipped from the factory. In general, you are not recommended to configure or change these values. To fine tune the analog parameters, you need to read the original calibration value.

The registers in the blank section must all be configured to 0 (reset to 0 when the chip is powered up). Other registers are configured as required by application scenarios.

7 Power Management System

7.1 Power Supply System for the AVDD Pin

The power management system consists of the LDO15 module, power detection module (PVD) and power-on/power-down reset module (POR).

AVDD is a 5V LDO output for the 034DO/034S chip. It is recommended that the off-chip decoupling capacitor be ≥ 1uF as close as possible to the AVDD pin.

AVDD supplies power to the LDO15 module that powers all internal digital circuits and PLL modules.

LDO15 is automatically enabled after power-up and requires no software configuration, but the output voltage of LDO15 needs to be fine-tuned by software.

The output voltage of LDO15 can be adjusted by setting the register LDO15TRIM<2:0>. Please refer to the description of the analog register table for specific register values. LDO15 is calibrated before the chip is shipped from the factory, and generally, you do not need to configure these additional registers. To fine tune the output voltage of LDO, you need to read the original configuration value and fill in the configuration value corresponding to the fine-tuning amount.

The POR module monitors the voltage of LDO15 and provides a reset signal to the digital circuit when the LDO15 voltage falls below 1.1V (for example, at the beginning of power-up or during power-down), to avoid the abnormal operation of the digital circuit.

7.2 Power Supply System of the VCC Pin

For model 03x that is integrated with a 6N driver module, the VCC pin powers the on-chip driver module with a voltage range of 4.5-20V and the typical undervoltage value of 4.7V.

7.3 Power Supply System of the VCCLDO Pin

The VCCLDO pin in the 034DO/034S model operates from 7-20V to power the on-chip 5V LDO module.

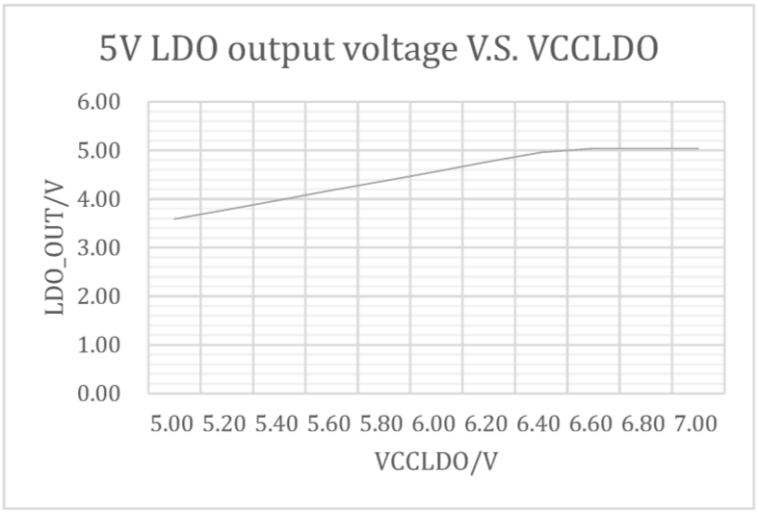

Figure 7-1 034DO 5V LDO output V.S. VCCLDO

External resistor selection for VCCLDO

The 034DO/034S model is internally integrated with a 5V LDO module. Due to the nature of the linear power supply, heat generation on the LDO is noticeable when the input voltage is high (e.g.> = 15V) and the load current is large (e.g.> = 30mAV). It is likely that the chip will trigger thermal protection at an ambient temperature around 125 degrees or less.

The chip itself consumes less than 10mA at 5V. If the 5V LDO supplies more than 10mA to the periphery of the chip, a shunt resistor may be bridged across AVDD and VCCLDO.

The resistance value should be calculated according to the following formula:

$$R>=1.5*(VCCLDO-AVDD)/I$$

Where, I is the total power dissipated on the 5V supply, including the power dissipated by the MCU and that dissipated by the 5V peripheral devices such as HALL.

With an external shunt resistor bridged, a 5.6V regulator should be placed at the AVDD pin.

8 Timer System

The timer system consists of an internal 64kHz RC timer, an internal 4MHz RC timer, and a PLL circuit.

The 64k RC timer is used as an MCU slow timer, a filtration module or an MCU timer in a low power state. The 4MHz RC timer is used as the MCU master timer and, when used in conjunction with the PLL, it can provide a timer up to 48MHz.

The 64k and 4M RC timers are factory calibrated to achieve an accuracy of ±8% for the 64k RC timer and ±1% for the 4M RC timer at room temperature. The 4M RC timer has a customized calibration register to further calibrate the accuracy to ±0.5%. In the temperature range of -40-105℃, the accuracy of the 64k RC timer is ±16% and that of the 4M RC timer is ±1%.

The 64k RC timer frequency can be set with the register RCLTRIM <3:0>, and the 4M RC timer frequency can be set with the register RCHTRIM <5:0>, which corresponds to the values described in the analog register table.

The timer is calibrated before the chip is shipped from the factory, and generally, you do not need to configure these additional registers. To fine tune the frequency, you need to read the original configuration value and fill in the configuration value corresponding to the fine-tuning amount.

The 4M RC timer is turned on by setting RCHPD = '0' (on by default, and off when set to '1'). The RC timer requires the Bandgap voltage reference module to provide reference voltage and current. Therefore, it is necessary to enable the BGP module before turning on the RC timer. The 4M RC timer is turned on and the BGP module is enabled by default in case of chip power-up. The 64k RC timer is always turned on and cannot be turned off.

The PLL multiplies the frequency of the 4M RC timer, to ensure a higher-speed timer for modules such as MCU, ADC, etc. The highest timer of the MCU and PWM modules is 48MHz, while the typical timer of the ADC module is 24MHz.

The PLL module is enabled by setting PLLPDN = '1' (off by default, and on when set to 1). The BGP (Bandgap) module needs to be enabled before the PLL module. After enabling the PLL module, it will take a stabilization time of 6us to output a stable timer. By default when the chip is powered on, the RCH timer is turned on and the BGP module is enabled; however, the PLL module is disabled, and needs to be enabled with software.

9 Reference Voltage Source

The reference voltage source provides reference voltage and current for the ADC, DAC, RC timer, PLL, temperature sensor, operational amplifier, comparator, and FLASH. The reference voltage source of BGP needs to be enabled before using any of these modules.

The BGP module is enabled by default when the chip is powered on. The reference voltage source is enabled by setting BGPPD = '0', and BGP needs about 2us to stabilize from being enabled to disabled. The output voltage of BGP is about 1.2V with an accuracy of ±0.8%

The reference voltage source is measured by setting REF_AD_EN = '1' to send the reference voltage to IO P0.0.

10 ADC Module

A SAR ADC is integrated into the chip. The ADC module is disabled by default when the chip is powered on. Before the ADC is enabled, it is necessary to enable the BGP and PLL modules, turn on the 4M RC timer, and select the ADC operating frequency. The ADC operating timer is 24 M by default.

The ADC requires at least 17 ADC timer cycles to complete a conversion, of which 12 are conversion cycles and 5 are sampling ones. The sampling period can be set by configuring the SAMP_TIME register in SYS_AFE_REG2. It is required to set not less than 3 sampling periods, that is, more than 8 ADC clocks.

The recommended value is 3, which corresponds to an output data rate of 1.2MHz for the ADC.

The ADC operates in the following modes: single single-channel trigger, continuous single-channel trigger, single 1-16 channel scanning, and continuous 1-16 channel scanning. Each ADC has 16 independent sets of registers for each channel.

The ADC trigger event may come from external timer signals T0, T1, T2, T3 for a preset number of times, or may be triggered by software.

The ADC has two gain modes that are set by SYS_AFE_REG0.GA_AD, corresponding to 1 x time and 2/3 x times gains. The 1 x time gain corresponds to an input signal of ±2.4V, and the 2/3 x times gain corresponds to an input signal amplitude of ±3.6V. In measuring the output signal of an operational amplifier, the specific ADC gain is selected based on the maximum possible output signal of the operational amplifier.

11 Operational Amplifier

Two input and output rail-to-rail operational amplifiers, with a built-in feedback resistor R2/R1. External pins should be connected in series with a resistor R0. The value of resistance of the feedback resistors R2:R1 can be set via register RES_OPA <1:0> for different magnification. The values corresponding to the specific registers are described in the analog register table.

The final magnification is R2/(R1+R0), where R0 is the value of resistance of the external resistor.

A capacitor greater than or equal to 15pF is required to be connected across the two input pins of the op amp.

For applications of direct sampling of MOS transistor resistor, it is recommended to connect an external resistor of >20kΩ to reduce the current flowing into the chip pins when the MOS transistor is turned off.

For small resistor sampling applications, external resistors of 100Ω are recommended.

The amplifier can select the output signal in the amplifier by setting OPAOUT_EN to send it to P0.7 IO port through BUFFER for measurement and application. Because BUFFER exists, it is also possible to send one output signal of the op amp under its normal operation mode.

In the default state when the chip is powered up, the amplifier module is turned off. The amplifier can be enabled by setting OPAPDN = '1' and the BGP module should be enabled before enabling the amplifier.

The clamping diode is built into the positive and negative input terminals of the op amp, and the motor phase line is directly connected to the input terminal through a matching resistor, thus simplifying the external circuit of MOSFET current sampling.

12 Comparator

There is a built-in 2 comparators, of which the comparison speed, the hysteresis voltage, and the signal source are programmable.

The comparator has a comparison delay of 0.15us and can also be set to less than 30ns via register CMP_FT. The hysteresis voltage is set to 20mV/0mV via CMP_HYS.

The signal source for both the positive and the negative inputs of the comparator can be programmed through the registers CMP_SELP<2:0> and CMP_SELN<1:0> as described in the register simulation instructions.

The comparator module is turned off by default when the chip is powered on. The comparator can be enabled by setting CMPxPDN =’1’ and the BGP module should be enabled before enabling the comparator.

13 Temperature Sensor

A temperature sensor with an accuracy of ±2℃ is built into the chip. The chip will undergo temperature correction before delivery, and the correction value is saved in the flash info area.

The temperature sensor module is turned off by default when the chip is powered on. The BGP module should be enabled before enabling the temperature sensor.

The temperature sensor is turned on by setting TMPPDN = '1'. It takes approximately 2us to turn on until stable, so it needs to be turned on 2us before the ADC measures the sensor.

14 DAC Module

The chip has a built-in 8bit DAC, and the range of the output signal is 4.8V.

The 8-bit DAC can send the DAC output to IO port P0.0 by setting the resistor as DACOUT_EN=1, which can drive a load resistor of >50KΩ and a load capacitor of 50pF.

The maximum DAC output bitrate is 1MHz.

The DAC module is turned off by default when the chip is powered on. The DAC can be enabled by setting DACPDN = 1 and the BGP module should be enabled before enabling the DAC module.

15 Processor

- 32-bit Cortex-M0 +DIV/SQRT coprocessor
- 2-wire SWD debugging pin
- Maximum operating frequency: 48MHz

16 Storage Resources

16.1 Flash

- The built-in flash includes a main storage area of 16/32kB and an information storage area of 1kB NVR
- Repeatable erasing and write-in of not less than 20,000 times
- Data is maintained for up to 100 years at a room temperature of 25℃
- The single-byte programming time is up to 7.5us, and the Sector erasing time is up to 5ms
- The Sector is 512 bytes, and can be erased or write-in by Sector. It supports runtime programming, and simultaneous erasing of and write-in to one Sector can be made while reading and accessing another Sector
- Flash data anti-theft (the last word must be written to any value other than 0xFFFFFFFF)

16.2 Execute-only Zone

Some 16kB flash capacity models are equipped with an execute-only zone of 16kB. After programming encryption, such models have the execution permission but do not have the read or write permission. Reprogramming with repeated erasure is supported.

16.3 SRAM

- Built-in 4KB SRAM

17 MCPWM Dedicated to Motor Drive

- The maximum operating timer frequency of MCPWM is 48MHz
- Supporting up to 4 channels complementary PWM outputs with adjustable phases
- The dead zone width of each channel can be configured independently
- Edge-aligned PWM mode supported
- Software control IO mode supported
- IO polarity control supported
- Internal short-circuit protection: avoiding short circuits caused by incorrect configuration
- External short-circuit protection: fast shutdown based on monitoring of external signals
- ADC sampling interrupt generates internally
- Use load register pre-memory timer to configure parameters
- The loading time and period of the loading register can be configured

18 Timer

- Two general-purpose timers, one 16bit timer and one 32bit timer
- Capturing mode is supported for measuring external signal width
- Comparison mode is supported for generating edge-aligned PWM/timing interrupts

19 Hall Sensor Interface

- Built-in maximum 1024 filtering
- Three Hall signal input
- 24-bit counter with overflow and capture interrupts

20 General Purpose Peripherals

- One UART works in the full-duplex operation mode, supporting 7/8 bits of data, 1/2 stop bit(s), odd/even/no parity mode, with 1 byte send cache, 1 byte receive cache, with Multi-drop Slave/Master mode, and the baud rate ranging from 300-115200
- One SPI for master-slave mode
- One IIC for master-slave mode
- Hardware watchdog, driven by RC timer, being independent of system high speed timer, write-in protection, 2/4/8/64 seconds reset interval

21 Gate Drive Module

21.1 Module Parameters

21.1.1 LKS32MC034D(O)F6Q8

LKS32MC034D(O)F6Q8/LKS32MC034SF6Q8 is equipped with a 6N type gate drive module.

Table 21-1 LKS32MC034D(O)F6Q8/LKS32MC034SF6Q8 Drive Module Parameter Table

Parameter	Minimum	Typical	Maximum	Unit	Description
Limit parameter					
Supply voltage VCC	-0.3		+25.0	V	Relative to ground
Floating voltage $VB_{1,2,3}$	-0.3		+250	V	
Floating bias $VS_{1,2,3}$	VB-25		VB+0.3	V	
High-side output voltage $HO_{1,2,3}$	VS-0.3		VB+0.3	V	
Low-side output voltage $LO_{1,2,3}$	-0.3		VCC+0.3	V	
Logic input $HIN/LIN_{1,2,3}$	-0.3		VCC+0.3	V	
Swing rate of switching voltage dVs/dt			50	V/ns	
Temperature junction (TJ)	-40		150	℃	
Storage temperature (TS)	-55		150	℃	
Welding temperature			300	℃	Welding 10s
Recommended operating conditions					
Supply voltage VCC	+8		+20.0	V	Relative to ground
Floating voltage $VB_{1,2,3}$	VS+8		VS+20	V	
Floating bias $VS_{1,2,3}$	-5		200	V	
High-side output voltage $HO_{1,2,3}$	VS		VB	V	
Low-side output voltage $LO_{1,2,3}$	0		VCC	V	
Logic input $HIN/LIN_{1,2,3}$	0		VCC	V	
Operating temperature T_A	-40		125	℃	
Electrical parameters of type 6N type gate driver					
VCC static current I_{QCC}		50	100	uA	HIN=LIN=0V
VB static current I_{QBS}		20	40	uA	HIN=LIN=0V
Floating voltage leakage current I_{LK}			10	uA	VB=VS=220V
VCC supply under-voltage trigger voltage	4.0	4.7	6.7	V	
VBS supply under-voltage trigger voltage	3.9	5.6	6.9	V	
VCC supply under-voltage lock -on voltage	3.6	4.4	6.4	V	

VBS supply under-voltage lock -on voltage	3.5	5.0	6.2	V	
VCC supply under-voltage hysteresis voltage	0.25	0.3	0.8	V	
VBS supply under-voltage hysteresis voltage	0.25	0.6	0.8	V	
High input threshold V_{IH}	2.8			V	
Low input threshold V_{IL}			0.8	V	
Input bias current I_{source}		50	120	uA	HIN=LIN=5V
Input bias current I_{sink}			1	uA	HIN=LIN=0V
High level output, V_{BIAS}-V_O			1	V	I_O=20mA
Low level output, V_O			1	V	I_O=20mA
High level output short current I_{O+}	650	1000		mA	V_{CC}/V_{BS}=15V
Low level output short current I_{O-}	650	1000		mA	V_{CC}/V_{BS}=15V
Output rise time T_r		15	30	ns	C_L=1nF
Output fall time T_f		12	30	ns	
Turn-on delay time T_{on}		270	500	ns	
Shutdown delay time T_{off}		80	150	ns	
Dead zone D_T	100	200	400	ns	
Delay matching M_T			80	ns	T_{on} & T_{off} for (HS-LS)

21.1.2 LKS32MC034SF6Q8

A bootstrap diode is integrated in the pre-driver.

Table 21-2 LKS32MC034SF6Q8 Drive Module Parameter Table

Parameter	Minimum	Typical	Maximum	Unit	Description
Limit parameter					
Supply voltage VCC	-0.3		+25.0	V	Relative to ground
Floating voltage $VB_{1,2,3}$	-0.3		+250	V	
Floating bias $VS_{1,2,3}$	VB-25		VB+0.3	V	
High-side output voltage $HO_{1,2,3}$	VS-0.3		VB+0.3	V	
Low-side output voltage $LO_{1,2,3}$	-0.3		VCC+0.3	V	
Logic input $HIN/LIN_{1,2,3}$	-0.3		VCC+0.3	V	
Swing rate of switching voltage dVs/dt			50	V/ns	
Temperature junction (TJ)	-40		150	℃	
Storage temperature (TS)	-55		150	℃	
Welding temperature			300	℃	Welding 10s
Recommended operating conditions					
Supply voltage VCC	+7		+20.0	V	Relative to ground
Floating voltage $VB_{1,2,3}$	VS+10		VS+20	V	

Floating bias $VS_{1,2,3}$	-5		200	V	
High-side output voltage $HO_{1,2,3}$	$VS_{1,2,3}$		$VB_{1,2,3}$	V	
Low-side output voltage $LO_{1,2,3}$	0		VCC	V	
Logic input $HIN/LIN_{1,2,3}$	0		5	V	
Operating temperature T_A	-40		125	℃	
Electrical parameters of type 6N type gate driver					
VCC static current I_{QCC1}	210	330	450	uA	HIN=LIN=0/5V, ENB=0
VCC static current I_{QCC2}		46	80	uA	HIN=LIN=0/5V, ENB=5
VB static current I_{QBS}	25	45	65	uA	HIN=LIN=0V
Floating voltage leakage current I_{LK}			10	uA	VB=VS=200V, VCC=0V
drive current I_{O+}		1		A	
drive current I_{O-}		1.2		A	
VCC undervoltage rising edge trigger voltage	2.9	4.2	5.5	V	
VCC undervoltage falling edge trigger voltage	2.5	3.8	5.1	V	
VCC undervoltage lockout hysteresis		0.4		V	
VBS undervoltage rising edge trigger voltage	2.5	3.8	4.5	V	
VBS undervoltage falling edge trigger voltage	2.2	3.5	4.5	V	
VBS undervoltage lockout hysteresis		0.3		V	
High input threshold V_{IH}	2.5			V	
Low input threshold V_{IL}			0.8	V	
Output rise time T_r		27		ns	C_L=1nF
Output fall time T_f		20		ns	
Turn-on delay time T_{on}		600	700	ns	
Shutdown delay time T_{off}		280	400	ns	
Dead zone D_T	220	280	330	ns	
Delay matching M_T			60	ns	

21.2 Recommended Application Diagram

The output pin signal LO1/HO1 of the driver module corresponds to the MCPWM function output of GPIO P0.10/P0.13, LO2/HO2 corresponds to the MCPWM function output of GPIO P0.11/P0.14, and LO3/HO3 corresponds to the MCPWM function output of GPIO P0.12/P0.15.

The MCPWM_SWAP register must be set for the integrated pre-drive chip, otherwise the PWM cannot be output normally. Write 0x67 to such register to write BIT[0] to 1, and write other values to

write BIT[0] to 0. When the value of MCPWM_SWAP is 1, it is used to include the pre-drive chip application environment. The sequence is converted within the logic to facilitate the interconnection of the chip and the drive chip. In general applications, only three sets of MCPWM channels are required, so only three sets of sequences are converted.

21.2.1 LKS32MC034D(O)F6Q8

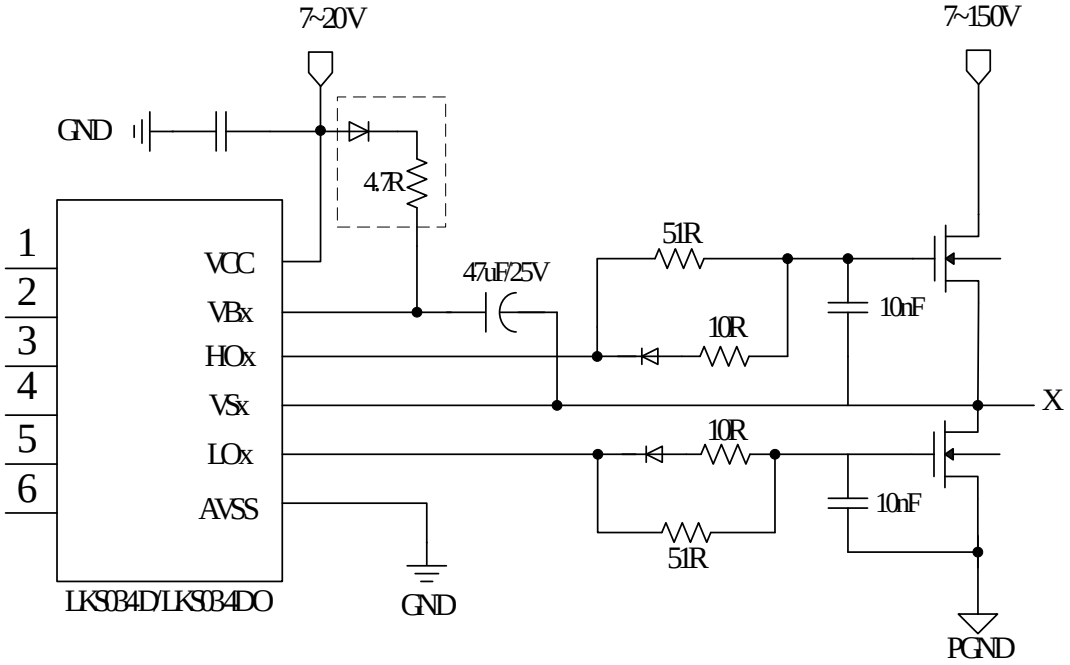

Figure 21-1 Typical Application Diagram of 6N Type Gate Drive Module LKS32MC034D(O)F6Q8

21.2.2 LKS32MC034SF6Q8

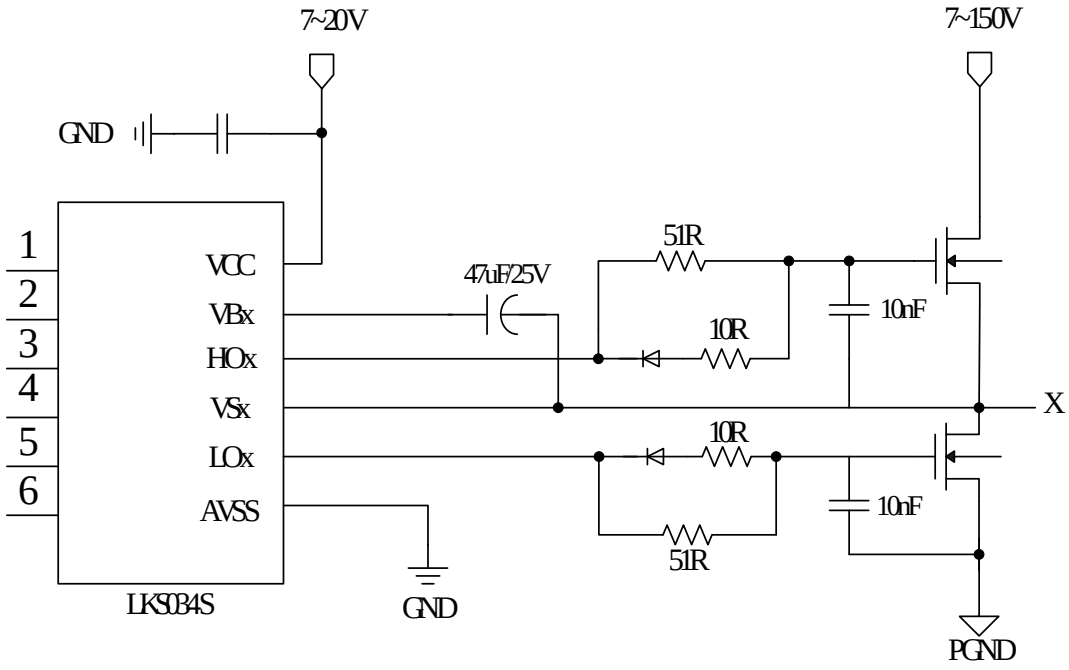

Figure 21-2 Typical Application Diagram of 6N Type Gate Drive Module LKS034S

In the figure, only the pins of the gate drive module are retained, x=1, 2, 3, corresponding to 3 groups of MOS gate drive outputs respectively. The application diagram for each group is shown above.

Each GPIO controlling the LOx of the drive module is a high level '1' corresponding to the LOx output '1'.

The input/output polarity of gate drive module is as follows:

Table 21-3 LKS32MC034D(O)F6Q8/LKS32MC034SF6Q8 Gate Drive Polarity Truth Table

{HIN, LIN}	HO	LO	
00	0	0	Shutdown of upper and lower tubes
01	0	1	Lower tube conduction
10	1	0	Upper tube conduction
11	0	0	The upper and lower tubes are connected simultaneously, and the hardware is under short-circuit protection

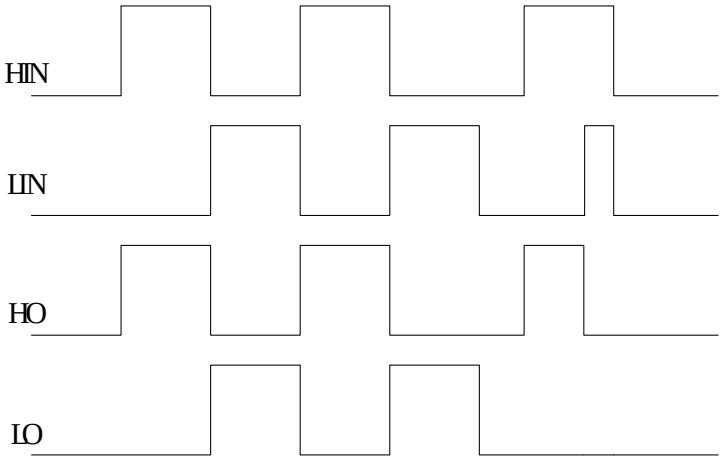

Figure 21-3 Schematic Diagram of LKS32MC034D(O)F6Q8/LKS32MC034SF6Q8 Gate Drive Polarity

22 Special IO Multiplexing

Precautions for LKS03x special IO multiplexing

The SWD protocol consists of two signal lines: SWCLK and SWDIO. The former is a timer signal that, for the chip, is the input state and does not change the input state. The latter is a data signal that switches between an input state and an output state during data transmission for the chip, which defaults to the input state.

LKS03x can realize the function of multiplexing two IOs of SWD into other IOs. IO multiplexed by SWCLK is P1.8, and IO multiplexed by SWDIO is P1.9. The precautions are as follows:

- Multiplexing is disabled by default, and software is needed to write a 1 to SYS_IO_CFG[6] to enable the multiplexing. That is, after the hard reset of the chip is complete, the initial state is for SWD. The two IOs of the SWD have a pull-up inside the chip (the pull-up resistance of the chip is about 10K). When IO functions as SWD, the pull-up is turned on by default and cannot be turned off. When IO functions as GPIO, pull-up can be worked via GPIO1_PUE[8] and GPIO1_PUE[9]. P1.8 and P1.9 are fixed as SWD functions within 30ms of chip power-on reset, the software can write 1 to SYS_IO_CFG[6], but IO function switching takes effect after 30ms. LRC counting was used for 30ms with some deviation due to process reasons.
- When multiplexing is enabled, tools such as KEIL cannot directly access the chip, that is, Debug and erase download are unavailable. There are two options if you need to re-download the program.
- Firstly, it is recommended to use Linko dedicated offline downloader to erase. It is recommended to reserve a certain margin for the time for enabling software multiplexing, for example, approximately 100ms, to ensure that the offline downloader can be erased to prevent deadlock. The amount of margin is to ensure the success rate of offline downloader erasure. The larger the margin, the greater the probability of a successful one-time erase.
- Secondly, there is an exit mechanism inside the program. For example, the change of some other IO level (generally as input) indicates that the external needs to use SWDIO in software reconfiguration and de-multiplexing. At this point, the KEIL function can be restored.

In the packaging of SSOP24, QFN40, and SOP16L, SWDIO, SWCLK may have bonded with other IOs. At this point, it should be noted that other IO action may cause the chip to misinterpret the SWD action.

The considerations for SWCLK multiplexing are as follows:

- Multiplexing is disabled by default, and software is needed to enable the multiplexing. That is, after the hard reset of the chip, the initial state is used for SWCLK, which is pulled up inside the chip (the internal pull-up resistance of the chip is about 10K). Please pay attention if the initial level is required by the application.
- When multiplexing is enabled, tools such as KEIL cannot directly access the chip, that is, Debug and erase download are unavailable. There are two options if you need to re-download the program.

- Firstly, it is recommended to use Linko dedicated offline downloader to erase. It is recommended to reserve a certain margin for the time for enabling software multiplexing, for example, approximately 100ms, to ensure that the offline downloader can be erased to prevent deadlock. The amount of margin is to ensure the success rate of offline downloader erasure. The larger the margin, the greater the probability of a successful one-time erase.
- Second, there is an exit mechanism inside the program. For example, the change of some other IO level (generally as input) indicates that the external needs to use SWCLK in software reconfiguration and de-multiplexing. At this point, the KEIL function can be restored.

➢ If SWCLK is enabled, SWDIO can be kept at 0 level (similar to time division multiplexing) when there is a signal change; If SWDIO cannot be set to 0, it is recommended that SWDCLK be operated with not more than 50 flip times (e.g. flip from 0 to 1 and then flip from 1 to 0, calculate once), or it should be ensured that SWDIO is at 0 level when SWCLK changes from 0 to 1 once during the periods for every 50 flip times (which may be less, e.g. 40 times).

If only SWCLK is multiplexed and SWDIO is not multiplexed at this point, please refer to the above precautions.

RSTN signal is used for external reset pins for the LKS05x chip by default.

LKS03x can realize the functions of RSTN multiplexing into other IO. The multiplexed IO is P0.2. The precautions are as follows:

➢ Multiplexing is disabled by default, and software is needed to write a 1 to SYS_IO_CFG[5] to multiplex RSTN as a normal GPIO. That is, the initial state of the chip is used for RSTN, which is pulled up inside the chip (the internal pull-up resistance of the chip is about 100K). Please pay attention if the initial level is required by the application.

➢ The default state is RSTN. Program execution can only be started after RSTN is released normally. The application needs to ensure that RSTN has adequate protection, such as peripheral circuit pull-up. If capacitance can be added, it is better.

➢ When multiplexing is enabled, the RSTN function becomes invalid. If a hard reset of the chip is required, the source can only be powered down/watchdog.

➢ RSTN multiplexing does not affect the use of KEIL.

23 Version History

Table 23-1 Document Version History

Time	Version No.	Description
10/12/2022	2.14	Add description of MCPWM_SWAP register
9/23/2022	2.13	Revise DateCode format
9/21/2022	2.12	Revise 034DO Pin 8 description
9/16/2022	2.11	034S has LDO inside.
9/6/2022	2.1	Add instructions of version A/B
8/11/2022	2.0	Split 3P3N, 6N and MCU model DS
7/27/2022	1.91	Add 034S
7/21/2022	1.9	Rollback ADC_CH6/7 pin position revision, the second revision time is tentatively scheduled for 2022.10
6/2/2022	1.8	Adjust ADC_CH6/7 Pin location, correct pin multiplexing table. DAC range is changed from 3.0V to 4.8V
3/8/2022	1.7	Add 034D
2/28/2022	1.6	Add 037Q
2/22/2022	1.5	Revise ADC channel number and CMP channel number, remove ADC_CH8 in pin function
1/24/2022	1.4	Revise P0.4, P0.6 Comparator 0 positive input number; Add P0.8 for 033
11/9/2021	1.3	Add 038
11/3/2021	1.2	Add 033, 037F
9/7/2021	1.1	Revised description for VCC power section
9/2/2021	1.0	Initial version

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