Linko Semiconductor Co., Ltd.

LKS32MC08x Datasheet

1 Overview

1.1 Function

LKS32MC08x is a 32-bit main stream MCU targeting motor control applications.

Features

- 96MHz 32-bit RISC core
- Customized instruction set DSP for motor control
- Ultra low power sleep mode, 10uA sleep current with MCU low low power consumption
- Industrial temperature range
- High ESD and group pulse reliability

- **Memory**
  - 64/32kB Flash with optional encryption to prevent hex theft
  - 8kB RAM
- **Operating Conditions**
  - Dual power supply. The MCU is powered by 2.2V ~ 5.5V voltage(B-version chip is powered by 3.0V~5.5V), with an integrated internal LDO for the digital circuit.
  - Operating Conditions: -40~105℃
- **Clock**
  - 4MHz built-in high-precision RC oscillator, with an accuracy of ± 1% at -40~105 ℃
  - 32KHz built-in low-speed clock for low-power mode
  - Operating on an external 4MHz crystal is available
  - Internal PLL up to 96 MHz
- **Peripheral Modules**
  - Two UARTs
  - One SPI, support master-slave mode
  - One IIC, support master-slave mode
  - One CAN-bus (084D without CAN), recommended to use external crystal as reference clock
  - Two 16-bit standard timers (TIM), support capture and edge-aligned PWM function
  - Two 32-bit standard timers (TIM), support capture and edge-aligned PWM function; support orthogonal code input, CW/CCW input, and pulse&symbol input
  - Motor control PWM module, supports 8 channels/4 pairs of PWM waveform output, independent dead-band control
  - Hall signal interface with speed measurement and debouncing function
  - Hardware watchdog
  - 4 Groups of 16bit GPIO at the most. P0.0/P0.1/P1.0/P1.1 could be used as wake-up source。

    P0.15 ~ P0.0 could be used as external IRQ source

- **Analog Modules**
  - 12bit SAR ADC, simultaneous double sampling, 3Msps sampling and conversion rate, up to 13 analog signal channels
  - Four operational amplifiers. Differential PGA mode is available.
  - Two comparators. Hysteresis mode is available.
  - 12bit digital-to-analog converter (DAC)
  - ± 2 ℃ built-in temperature sensor
  - 1.2V 0.8% built-in linear regulator
  - Low-power LDO and power monitoring circuit
  - RC oscillator with high precision and low temperature drift
  - Crystal oscillator circuits

1.2 Performance Advantages

- High reliability, high integration level, small package size, saving BOM cost;
- Integrated 4 channels high-speed OPAs and 2 channels comparators, meeting the needs of different system topology like single resistance/double resistance/three resistance current sampling;
- High-speed OPA is integrated with over-voltage protection circuit, which allows high-voltage common-mode signals to be input, which could support direct current sampling of MOSFET resistance with the simplest circuit topology.
- Via a proprietary technique, ADC and high-speed OPA could cooperate well, making them able to handle a wider current dynamic range, while ensuring the sampling precision of high-speed small current and low-speed hight current;
- The control circuit is simple and efficient, with strong anti-interference ability, stable and reliable;
- Supports IEC/UL60730 functional safety certification;

Applicable to control systems such as inductive BLDC/non-inductive BLDC/inductive FOC/non-inductive FOC and stepper motors, permanent magnet synchronous and asynchronous motors.

1.3 Naming Conventions

LKS32 MC 080 R 8 T 8 XX （X）

Device series

LKS32	= 32bit MCU

Product type

MC	= Motor Control Applications
AT	= Automobile Applications

Device sub family

080/081/082/ 083/085/088	= 2.2~5.5V,1 ADC,4 PGA,DSP
084D/086	= 2.2~5.5V,1 ADC,4 PGA,DSP,6N Driver
087(A)	= 2.2~5.5V,1 ADC,2 PGA
087C	= 2.2~5.5V,1 ADC,2 PGA, CAN
087D/087E	= 7.5~28V, 1 ADC,2 PGA,3P3N Driver
089	= 2.2~5.5V,1 ADC,2 PGA
089XL	= 2.2~5.5V,1 ADC,4 PGA,DSP,6N Driver,LIN

Pin count

L	= 16 pins
H	= 20 pins
M	= 24 pins
K	= 32 pins
F	= 40 pins
C	= 48 pins
N	= 52 pins
R	= 64 pins
V	=100 pins
Z	=144 pins

Code size

4	= 16Kbyte Flash Memory
6	= 32Kbyte Flash Memory
8	= 64Kbyte Flash Memory
B	=128Kbyte Flash Memory
C	=256Kbyte Flash Memory

Package

P	= TSSOP
T	= TQFP/LQFP
Q	= QFN
S	= SSOP
H	= BGA

Temperature range

6	= -40~85°
8	= -40~105°
9	= -40~125°

Options

TR	= Tape and reel packing
P	= Engineering Samples

Version

X	= Version, B~Z

Fig. 1-1 Naming Conventions of Linko Components

1.4 Resource Diagram

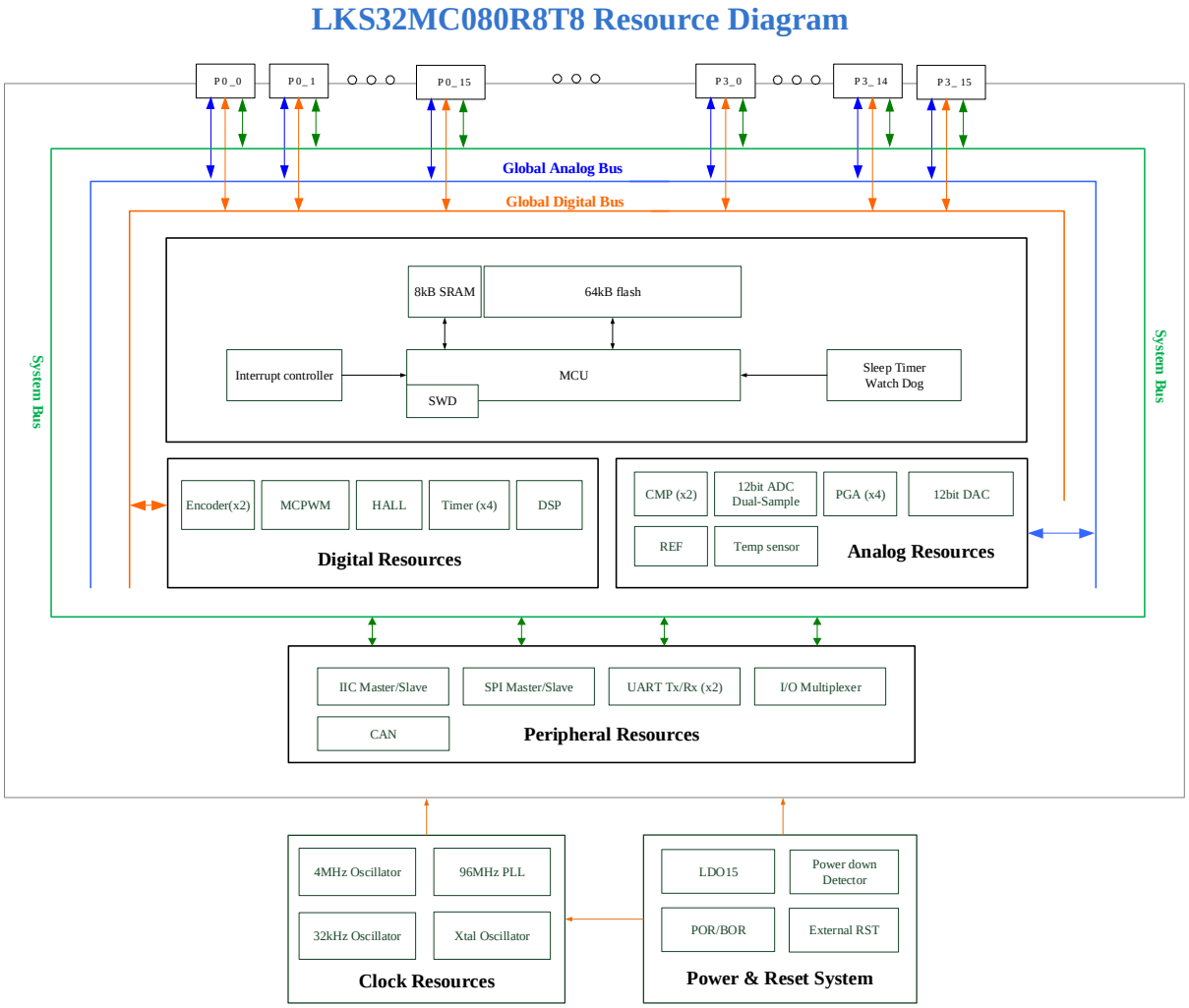

Fig. 1-2 LKS32MC080R8T8 Resource Diagram

For detail resource information of other devices, please refer to chip selection guide.

1.5 FOC System Example

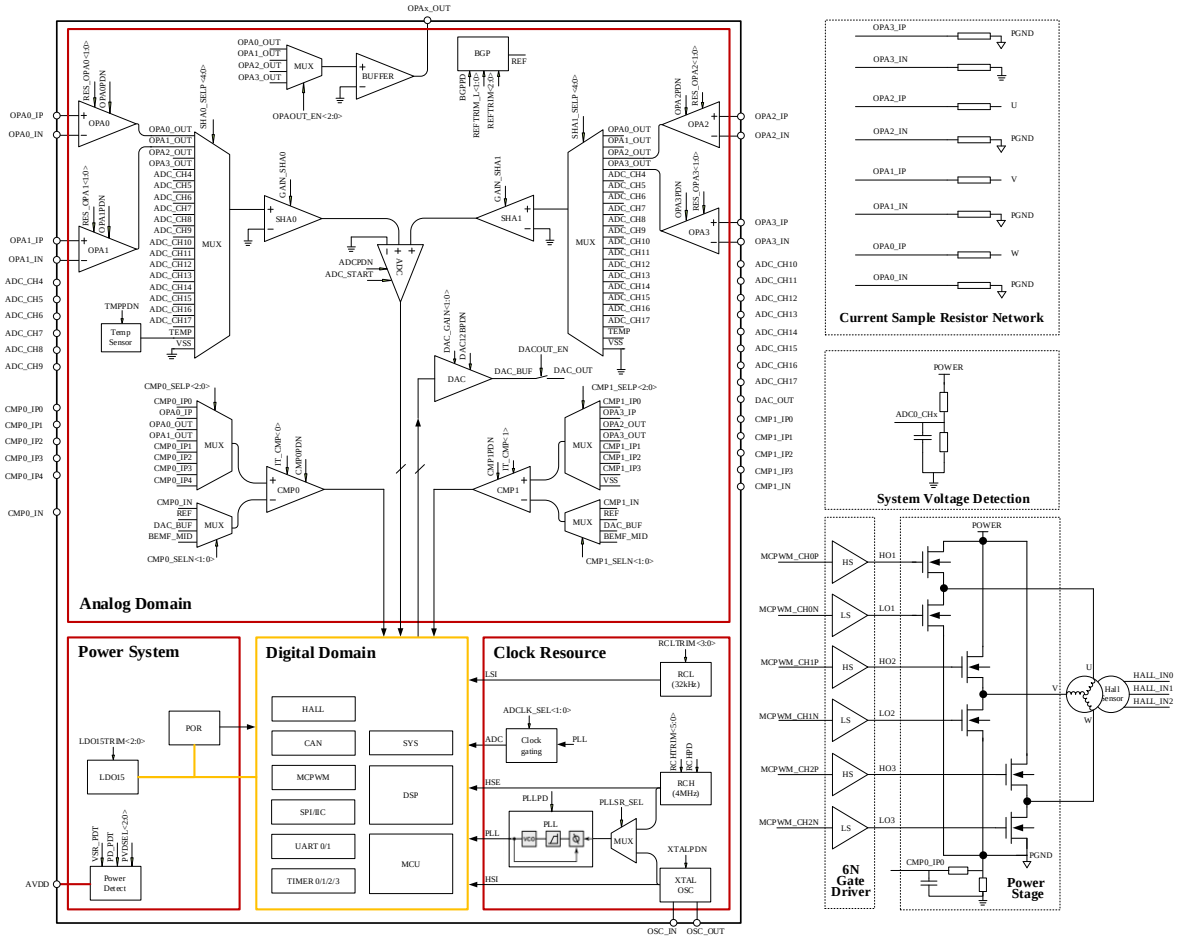

Fig. 1-3 LKS32MC08x Simplified Schematic of FOC System

2 Device Selection Guide

Table 2-1 LKS08x family device selection guide

	Frequency (MHz)	Flash (kB)	RAM (kB)	ADC ch.	DAC	Comparator	Comparator ch.	OPA	HALL	SPI	IIC	UART	CAN	Temp. Sensor	PLL	QEP	Gate driver	Gate Driver current (A)	Pre-drive supply (V)	Gate floating voltage (V)	Others	Package
LKS32MC080R8T8(B)	96	64	8	13	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes						LQFP64
LKS32MC081C8T8(B)	96	64	8	12	12BITx1	2	9	4	3	1	1	2		Yes	Yes							TQFP48
LKS32MC082K8Q8(B)	96	64	8	8	12BITx1	2	6	3	3	1	1	2		Yes	Yes							QFN5*5 32L-0.75
LKS32MC083C8T8(B)	96	64	8	12	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes						TQFP48
LKS32MC084DF6Q8	96	32	8	11	12BITx1	2	7	3	3	1	1	2		Yes	Yes		6N	+1.2/-1.5	4.5~20*1	200		QFN5*5 40L-0.75
LKS32AT085C8Q9	96	64	8	12	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes						QFN6*6 48L-0.55
LKS32AT086N8Q9	96	64	8	11	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes	6N	+1.2/-1.5	4.5~20	200		QFN6*6 52L-0.55
LKS32MC086N8Q8	96	64	8	11	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes	6N	+1.2/-1.5	4.5~20	200		QFN6*6 52L-0.55
LKS32MC087M6S8(B)	96	32	8	5	12BITx1	2	6	2	3			1		Yes	Yes							SSOP24L
LKS32MC087AM6S8(B)	96	32	8	5	12BITx1	2	6	2	3			1		Yes	Yes							SSOP24L
LKS32MC087CM8S8(B)	96	64	8	5	12BITx1	2	6	2	3			1	Yes	Yes	Yes							SSOP24L
LKS32MC087DM6S8	96	32	8	5	12BITx1	2	6	2	3			1		Yes	Yes		3P3N	+0.05/-0.3	7~28		5V LDO*2	SSOP24L
LKS32MC087EM6S8	96	32	8	5	12BITx1	2	7	2	3			1		Yes	Yes		3P3N	+0.05/-0.3	7~28		5V LDO	SSOP24L
LKS32MC088C6T8(B)	96	32	8	12	12BITx1	2	9	4	3	1	1	2		Yes	Yes							TQFP48
LKS32MC088KU8Q8	96	64	8	8	12BITx1	2	7	3	3	1	1	2	Yes	Yes	Yes	Yes	6N	+0.45/-1	4.5~20	600	5V LDO	QFN43L
LKS32AT089XLN8Q9	96	64	8	11	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes	6N	+1.2/-1.5	4.5~20	200	5V LDO	QFN6*6 52L-0.55

*1 : Some devices are divided into different versions due to the integration of multiple pre drives. The power supply voltage range of the pre drive is different. Please refer to the electrical performance parameters for details.

*2 : Some devices are equipped with a 5V LDO, which is powered by 7.5~28V VCC and could supply 5V to MCU or peripheral devices. Please refer to Pin assignment table for more information.

3 Pin Assignment

3.1 Pin Assignment and Pin Function Description

3.1.1 Special Notes

The red pin in the pin assignment figures below has built-in pull-up resistors:
RSTN has a 100kΩbuilt-in pull-up resistor, which is enabled automatically after power-up.
SWDIO/SWCLK has a 10kΩ built-in pull-up resistor, which is enabled automatically after power-up.
The remaining red pins have 10kΩ built-in pull-up resistors, which could be software-enabled.

UARTx_TX(RX): UART TX and RX support interchange. When the second function of GPIO is selected as UART, and GPIO_PIE is input enabled, it can be used as UART_RX; when GPIO_POE is enabled, it can be used as UART_TX. Generally, the same GPIO does not enable input and output at the same time, otherwise the input PDI will receive the data sent by the PDO.
SPI_DI(DO): The DI and DO of SPI can also be interchanged. When the second function of GPIO is SPI, and GPIO_PIE is input enable, it can be used as SPI_DI; when GPIO_POE is output enable, it can be used as SPI_DO. Generally, the same GPIO does not enable input and output at the same time, otherwise the input PDI will receive the data sent by the PDO.

3.1.2 LKS32MC080R8T8(B)

Fig. 3-1 LKS32MC080R8T8(B) Pin Assignment

Table 3-1 LKS32MC080R8T8(B) Pin Function Description

No.	Pin Name	Type	Function
1	ADC_CH4/DAC_OUT/P0.0	Input/Output	ADC channel4/DAC output/P0.0, with a 10k software-enabled built-in pull-up resistor
2	ADC_CH6/ P0.1	Input/Output	ADC channel 6 /P0.1
3	RSTN/P0.2	Input/Output	RSTN/P0.2 is usually used as RSTN. Add a 100nF ground capacitor, plus a 100k built-in pull-up resistor. A 10k~20k pull-up resistor between AVDD and RSTN on PCB is recommended. Use a 100nF capacitor if the pull-up resistor is present.
4	AVSS	Ground	System Ground

No.	Pin Name	Type	Function
5	AVDD	Power	Chip power input. Off-chip decoupling capacitor ≥1uF is recommended, and should be placed as close as possible to the AVDD pin.
6	P3.2	Input/Output	P3.2
7	P3.4	Input/Output	P3.4
8	SCL/TIM2_CH0/ADC_CH7/P0.3	Input/Output	I2C Clock/Timer2 channel0/ADC channel7/P0.3
9	SDA/TIM2_CH1/ADC_CH8/P0.4	Input/Output	I2C Data/Timer2 channel1/ADC channel8/P0.4
10	ADC_CH9/P0.5	Input/Output	ADC channel9/P0.5
11	UART1_TX(RX)/TIM1_CH0/CAN_RX/P0.6	Input/Output	UART1 RXD/Timer1 channel0/CAN RX/P0.6, with a 10k software-controllable built-in pull-up resistor
12	UART1_TX(RX)/TIM1_CH1/CAN_TX/P0.7	Input/Output	UART1 TXD/Timer1 channel1/CAN TX/P0.7, with a 10k software-controllable built-in pull-up resistor
13	SPI_CS/P1.1	Input/Output	SPI CS /P1.1
14	MCPWM_CH1P/TIM2_CH0/P2.11	Input/Output	Motor PWM channel1 high-side output/Timer2 channel0/P2.11
15	MCPWM_CH1N/TIM2_CH1/ADC_TRIG2/P2.12	Input/Output	Motor PWM channel1 low-side output/Timer2 channel1/ADC trigger signal2/P2.12
16	P0.8	Input/Output	P0.8
17	SCL/TIM2_CH0/P0.9	Input/Output	I2C Clock/ Timer2 channel0/P0.9
18	SDA/TIM2_CH1/P0.10	Input/Output	I2C Data/ Timer2 channel1/P0.10
19	HALL_IN0/TIM3_CH0/ADC_CH15/CMP0_IP1/P0.11	Input/Output	Hall sensor A-phase Input/Timer3 channel0/ADC channel15/Comparator0 positive Input1/P0.11
20	HALL_IN1/TIM3_CH1/CAN_RX/ADC_CH16/CMP0_IP2/P0.12	Input/Output	Hall sensor B-phase Input/Timer3 channel1/CAN RX/ADC channel16/ Comparator0 positive Input2/ P0.12
21	HALL_IN2/CAN_TX/ADC_CH17/CMP0_IP3/P0.13	Input/Output	Hall sensor C-phase Input/CAN TX/ADC channel17/ Comparator0 positive Input3/P0.13
22	CMP0_OUT/MCPWM_BKIN1/SPI_CLK/TIM0_CH1/ ADC_TRIG0/SIF/ADC_CH10/CMP0_IP4/P0.14	Input/Output	Comparator0 Output/Motor PWM breaking signal1/SPI Clock/Timer0 channel1/ADC trigger signal0/SIF/ADC channel10/Comparator0 positive Input4/P0.14
23	MCPWM_CH0P/UART0_TX(RX)/SPI_DI(DO)/TIM0_CH0/ADC_TRIG1/CMP0_IN/P0.15	Input/Output	Motor PWM channel0 high-side output/UART0 RXD/SPI Data Output/Timer0 channel0/ADC trigger signal1/Comparator0 negative Input/P0.15
24	MCPWM_CH0N/UART0_TX(RX)/SPI_DI(DO)/P1.0	Input/Output	Motor PWM channel0 low-side output/UART0 TXD/SPI data Input/ P1.0, with a 10k software-controllable built-in pull-up resistor
25	P3.6	Input/Output	P3.6
26	TIM3_CH0/ P1.2	Input/Output	Timer3 channel0/P1.2
27	TIM3_CH1/ADC_CH5/P1.3	Input/Output	Timer3 channel1/ADC channel5/P1.3, with a 10k software-controllable built-in pull-up resistor
28	OPA0_IP/P3.5	Input/Output	OPA0 positive Input/P3.5

No.	Pin Name	Type	Function
29	OPA0_IN/P3.7	Input/Output	OPA0 negative Input/P3.7
30	ADC_CH11/OPAx_OUT/LDO15/P2.7	Input/Output	ADC channel11/OPAx Output/LDO15 Output/P2.7, with a 10k software-controllable built-in pull-up resistor
31	OPA1_IP/P3.0	Input/Output	OPA1 positive Input/P3.0
32	OPA1_IN/P3.1	Input/Output	OPA1 negative Input/P3.1
33	UART1_TX(RX)/TIM3_CH0/OSC_IN/P2.8	Input/Output	UART1 RXD/Timer3 channel0/Crystal Oscillator Input/P2.8, with a 10k software-controllable built-in pull-up resistor, if connected to a crystal, add a 15pf shut capacitor to ground
34	UART1_TX(RX)/TIM3_CH1/OSC_OUT/P3.9	Input/Output	UART1 TXD/Timer3 channel1/Crystal Oscillator Output/P3.9, with a 10k software-controllable built-in pull-up resistor, if connected to a crystal, add a 15pf shut capacitor to ground
35	MCPWM_CH1N/P1.12	Input	Motor PWM channel1 low-side output/P1.12
36	SPI_CLK/TIM0_CH0/P1.13	Input/Output	SPI Clock/ Timer0 channel0/P1.13
37	SPI_DI(DO)/TIM0_CH1/P1.14	Input	SPI DO/ Timer0 channel1/P1.14
38	MCPWM_CH2N/P1.15	Input/Output	Motor PWM channel2 low-side output/P1.15
39	SPI_CS/TIM2_CH1/P2.0	Input/Output	SPI CS/ Timer2 channel1/P2.0
40	LRC/MCPWM_CH0P/P1.4	Input/Output	32kHz RC Clock Output/Motor PWM channel0 high-side output/P1.4
41	HRC/MCPWM_CH0N/P1.5	Input/Output	4MHz RC Clock Output/Motor PWM channel0 low-side output/P1.5
42	MCPWM_CH1P/P1.6	Input/Output	Motor PWM channel1 high-side output/P1.6
43	MCPWM_CH1N/P1.7	Input/Output	Motor PWM channel1 low-side output/P1.7
44	MCPWM_CH2P/P1.8	Input/Output	Motor PWM channel2 high-side output/P1.8
45	MCPWM_CH2N/P1.9	Input/Output	Motor PWM channel2 low-side output/P1.9
46	ADC_CH13/MCPWM_CH3P/UART0_TX(RX)/SCL/TIM0_CH0/ ADC_TRIG2/P1.10	Input/Output	Motor PWM channel3 high-side output/UART0 RXD/I2C Clock/Timer0 channel0/ADC trigger signal2/P1.10, with a 10k software-controllable built-in pull-up resistor
47	MCPWM_CH3N/UART0_TX(RX)/SDA/TIM0_CH1/ ADC_TRIG3/SIF/P1.11	Input/Output	Motor PWM channel3 low-side output/UART0 TXD/I2C Data/Timer0 channel1/ADC trigger signal3/P1.11, with a 10k software-controllable built-in pull-up resistor
48	OPA2_IP/P3.10	Input/Output	OPA2 positive Input/P3.10
49	OPA2_IN/P3.11	Input/Output	OPA2 negative Input/P3.11
50	SPI_DI(DO)/SCL/ADC_CH12/CMP0_IP0/P2.9	Input/Output	SPI DataInput/I2C Clock/ADC channel12/Comparator0 positive Input0/P2.9
51	SPI_DI(DO)/SDA/P2.10	Input/Output	SPI Data Output/I2C Data/P2.10, with a 10k software-controllable built-in pull-up resistor
52	OPA3_IN/P3.14	Input/Output	OPA3 negative Input/P3.14

No.	Pin Name	Type	Function
53	OPA3_IP/P3.15	Input/Output	OPA3 positive Input/P3.15
54	SPI_CLK/ADC_CH14/CMP1_IP0/P2.1	Input/Output	SPI Clock/ADC channel14/Comparator1 positive Input0/P2.1, with a 10k software-controllable built-in pull-up resistor
55	CMP1_IN/P2.2	Input/Output	Comparator1 negative Input/P2.2
56	CMP1_OUT/MCPWM_BKIN0/SPI_CS/REF/P2.3	Input/Output	Comparator1 Output/Motor PWM breaking signal0/SPI chip select signal/Voltage Reference/P2.3
57	HALL_IN0/MCPWM_CH2P/UART1_TX(RX)/TIM1_CH0/ADC_TRIG3/CAN_RX/CMP1_IP1/P2.4	Input/Output	Hall sensor A-phase Input/Motor PWM channel2 high-side output/UART1 RXD/Timer1 channel0/ADC trigger signal3/CAN RX/Comparator1 positive Input1/P2.4, with a 10k software-controllable built-in pull-up resistor
58	HALL_IN1/MCPWM_CH2N/UART1_TX(RX)/TIM1_CH1/ADC_TRIG0/CAN_TX/CMP1_IP2/P2.5	Input/Output	Hall sensor B-phaseInput/Motor PWM channel2 low-side output/UART1 TXD/Timer1 channel1/ADC trigger signal0/CAN TX/Comparator1 positive Input2/P2.5, with a 10k software-controllable built-in pull-up resistor
59	HALL_IN2/MCPWM_CH3P/TIM3_CH0/ ADC_TRIG1/CMP1_IP3/P2.6	Input/Output	Hall sensor C-phase Input/Motor PWM channel3 high-side output /Timer3 channel0/ADC trigger signal1/Comparator1 positive Input3/P2.6, with a 10k software-controllable built-in pull-up resistor
60	MCPWM_CH3N/TIM3_CH1/P2.13	Input/Output	Motor PWM channel3 low-side output /Timer3 channel1/ P2.13
61	SWCLK	Input	SWD Clock , with 10k built-in pull-up resistor
62	SWDIO	Input/Output	SWD Data, with 10k built-in pull-up resistor
63	SCL/P2.14	Input/Output	I2C Clock/P2.14
64	SDA/P2.15	Input/Output	I2C Data/P2.15

3.1.3 LKS32MC081C8T8(B)/LKS32MC088C6T8(B)

Fig. 3-2 LKS32MC081C8T8(B)/LKS32MC088C6T8(B) Pin Assignment

Table 3-2 LKS32MC081C8T8(B)/LKS32MC088C6T8(B) Pin Function Description

No.	Pin Name	Type	Function
1	ADC_CH4/DAC_OUT/P0.0	Input/Output	ADC channel4/DACOutput/P0.0, with a 10k software-controllable built-in pull-up resistor
2	RSTN/P0.2	Input/Output	RSTN/P0.2 is usually used as RSTN. Add a 100nF ground capacitor, plus a 100k built-in pull-up resistor. A 10k~20k pull-up resistor between AVDD and RSTN on PCB is recommended. Use a 100nF capacitor if the pull-up resistor is present.
3	AVSS	Ground	System Ground
4	AVDD	Power	Chip power input. Off-chip decoupling capacitor ≥1uF is recommended, and should be placed as close

No.	Pin Name	Type	Function
			as possible to the AVDD pin.
5	P3.2	Input/Output	P3.2
6	SCL/TIM2_CH0/ADC_CH7/P0.3	Input/Output	I2C Clock/Timer2 channel0/ADC channel7/P0.3
7	SDA/TIM2_CH1/ADC_CH8/P0.4	Input/Output	I2C Data/Timer2 channel1/ADC channel8/P0.4
8	ADC_CH9/P0.5	Input/Output	ADC channel9/P0.5
9	UART1_TX(RX)/TIM1_CH0/P0.6	Input/Output	UART1 RXD/Timer1 channel0/P0.6, with a 10k software-controllable built-in pull-up resistor
10	UART1_TX(RX)/TIM1_CH1/P0.7	Input/Output	UART1 TXD/Timer1 channel1/P0.7, with a 10k software-controllable built-in pull-up resistor
11	MCPWM_CH1P/TIM2_CH0/P2.11	Input/Output	Motor PWM channel1 high-side output/Timer2 channel0/P2.11
12	MCPWM_CH1N/TIM2_CH1/ADC_TRIG2/P2.12	Input/Output	Motor PWM channel1 low-side output/Timer2 channel1/ADC trigger signal2/P2.12
13	HALL_IN0/TIM3_CH0/ADC_CH15/CMP0_IP1/P0.11	Input/Output	Hall sensor A-phase Input/Timer3 channel0/ADC channel15/Comparator0 positive Input1/P0.11
14	HALL_IN1/TIM3_CH1/ADC_CH16/CMP0_IP2/P0.12	Input/Output	Hall sensor B-phaseInput/Timer3 channel1/ADC channel16/Comparator0 positive Input2/P0.12
15	HALL_IN2/ADC_CH17/CMP0_IP3/P0.13	Input/Output	Hall sensor C-phase Input/ADC channel17/Comparator0 positive Input3/P0.13
16	CMP0_OUT/MCPWM_BKIN1/SPI_CLK/TIM0_CH1/ ADC_TRIG0/SIF/ADC_CH10/CMP0_IP4/P0.14	Input/Output	Comparator0 Output/Motor PWM breaking signal1/SPI Clock/Timer0 channel1/ADC trigger signal0/SIF/ADC channel10/Comparator0 positive Input4/P0.14
17	MCPWM_CH0P/UART0_TX(RX)/SPI_DI(DO)/TIM0_CH0/ADC_TRIG1/CMP0_IN/P0.15	Input/Output	Motor PWM channel0 high-side output/UART0 RXD/SPI Data Output/Timer0 channel0/ADC trigger signal1/Comparator0 negative Input/P0.15
18	MCPWM_CH0N/UART0_TX(RX)/SPI_DI(DO)/P1.0	Input/Output	Motor PWM channel0 low-side output/UART0 TXD/SPI DataInput/P1.0, with a 10k software-controllable built-in pull-up resistor
19	TIM3_CH1/ADC_CH5/P1.3	Input/Output	Timer3 channel1/ADC channel5/P1.3, with a 10k software-controllable built-in pull-up resistor
20	OPA0_IP/P3.5	Input/Output	OPA0 positive Input/P3.5
21	OPA0_IN/P3.7	Input/Output	OPA0 negative Input/P3.7
22	ADC_CH11/OPAx_OUT/LDO15/P2.7	Input/Output	ADC channel11/OPAx Output/LDO15 Output/P2.7, with a 10k software-controllable built-in pull-up resistor
23	OPA1_IP/P3.0	Input/Output	OPA1 positive Input/P3.0
24	OPA1_IN/P3.1	Input/Output	OPA1 negative Input/P3.1
25	UART1_TX(RX)/TIM3_CH0/OSC_IN/P2.8	Input/Output	UART1 RXD/Timer3 channel0/Crystal Oscillator Input/P2.8, with a 10k software-controllable built-in pull-up resistor, if connected to a crystal, add a 15pf shut capacitor to ground

No.	Pin Name	Type	Function
26	UART1_TX(RX)/TIM3_CH1/OSC_OUT/P3.9	Input/Output	UART1 TXD/Timer3 channel1/Crystal Oscillator Output/P3.9, with a 10k software-controllable built-in pull-up resistor, if connected to a crystal, add a 15pf shut capacitor to ground
27	LRC/MCPWM_CH0P/P1.4	Input/Output	32kHz RC Clock Output/Motor PWM channel0 high-side output/P1.4
28	HRC/MCPWM_CH0N/P1.5	Input/Output	4MHz RC Clock Output/Motor PWM channel0 low-side output/P1.5
29	MCPWM_CH1P/P1.6	Input/Output	Motor PWM channel1 high-side output/P1.6
30	MCPWM_CH1N/P1.7	Input/Output	Motor PWM channel1 low-side output/P1.7
31	MCPWM_CH2P/P1.8	Input/Output	Motor PWM channel2 high-side output/P1.8
32	MCPWM_CH2N/P1.9	Input/Output	Motor PWM channel2 low-side output/P1.9
33	ADC_CH13/MCPWM_CH3P/UART0_TX(RX)/SCL/TIM0_CH0/ADC_TRIG2/P1.10	Input/Output	Motor PWM channel3 high-side output/UART0 RXD/I2C Clock/Timer0 channel0/ADC trigger signal2/P1.10, with a 10k software-controllable built-in pull-up resistor
34	MCPWM_CH3N/UART0_TX(RX)/SDA/TIM0_CH1/ADC_TRIG3/SIF/P1.11	Input/Output	Motor PWM channel3 low-side output/UART0 TXD/I2C Data/Timer0 channel1/ADC trigger signal3/P1.11, with a 10k software-controllable built-in pull-up resistor
35	OPA2_IP/P3.10	Input/Output	OPA2 positive Input/P3.10
36	OPA2_IN/P3.11	Input/Output	OPA2 negative Input/P3.11
37	SPI_DI(DO)/SCL/ADC_CH12/CMP0_IP0/P2.9	Input/Output	SPI DataInput/I2C Clock/ADC channel12/Comparator0 positive Input0/P2.9
38	SPI_DI(DO)/SDA/P2.10	Input/Output	SPI Data Output/I2C Data/P2.10, with a 10k software-controllable built-in pull-up resistor
39	OPA3_IN/P3.14	Input/Output	OPA3 negative Input/P3.14
40	OPA3_IP/P3.15	Input/Output	OPA3 positive Input/P3.15
41	SPI_CLK/ADC_CH14/CMP1_IP0/P2.1	Input/Output	SPI Clock/ADC channel14/Comparator1 positive Input0/P2.1, with a 10k software-controllable built-in pull-up resistor
42	CMP1_IN/P2.2	Input/Output	Comparator1 negative Input/P2.2
43	CMP1_OUT/MCPWM_BKIN0/SPI_CS/REF/P2.3	Input/Output	Comparator1 Output/Motor PWM breaking signal0/SPI chip select signal/Voltage Reference/P2.3
44	HALL_IN0/MCPWM_CH2P/UART1_TX(RX)/TIM1_CH0/ADC_TRIG3/CMP1_IP1/P2.4	Input/Output	Hall sensor A-phase Input/Motor PWM channel2 high-side output/UART1 RXD/Timer1 channel0/ADC trigger signal3/Comparator1 positive Input1/P2.4, with a 10k software-controllable built-in pull-up resistor
45	HALL_IN1/MCPWM_CH2N/UART1_TX(RX)/TIM1_CH1/ADC_TRIG0/CMP1_IP2/P2.5	Input/Output	Hall sensor B-phaseInput/Motor PWM channel2 low-side output/UART1 TXD/Timer1 channel1/ADC trigger signal0/Comparator1 positive Input2/P2.5, with a 10k software-controllable built-in pull-up

No.	Pin Name	Type	Function
			resistor
46	HALL_IN2/MCPWM_CH3P/TIM3_CH0/ ADC_TRIG1/CMP1_IP3/P2.6	Input/Output	Hall sensor C-phase Input/Motor PWM channel3 high-side output /Timer3 channel0/ADC trigger signal1/Comparator1 positive Input3/P2.6, with a 10k software-controllable built-in pull-up resistor
47	SWCLK	Input	SWD Clock , with 10k built-in pull-up resistor
48	SWDIO	Input/Output	SWD Data, with 10k built-in pull-up resistor

3.1.4 LKS32MC082K8Q8(B)

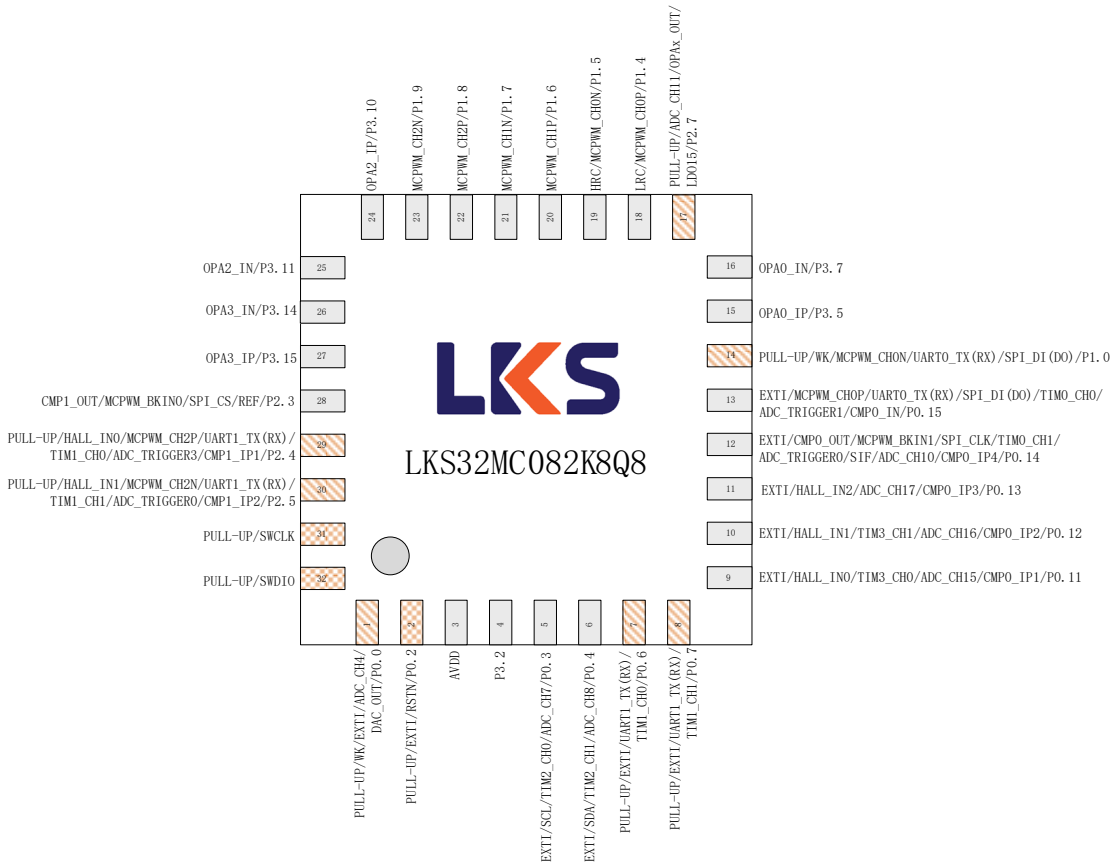

Fig. 3-3 LKS32MC082K8Q8(B) Pin Assignment

Table 3-3 LKS32MC082K8Q8(B) Pin Function Description

No.	Pin Name	Type	Function
0	AVSS	Ground	System ground, Pin 0 is at the bottome of the package
1	ADC_CH4/DAC_OUT/P0.0	Input/Output	ADC channel4/DACOutput/P0.0, with a 10k software-controllable built-in pull-up resistor
2	RSTN/P0.2	Input/Output	RSTN/P0.2 is usually used as RSTN. Add a 100nF

No.	Pin Name	Type	Function
			ground capacitor, plus a 100k built-in pull-up resistor. A 10k~20k pull-up resistor between AVDD and RSTN on PCB is recommended. Use a 100nF capacitor if the pull-up resistor is present.
3	AVDD	Power	Chip power input. Off-chip decoupling capacitor ≥1uF is recommended, and should be placed as close as possible to the AVDD pin.
4	P3.2	Input/Output	P3.2
5	SCL/TIM2_CH0/ADC_CH7/P0.3	Input/Output	I2C Clock/Timer2 channel0/ADC channel7/P0.3
6	SDA/TIM2_CH1/ADC_CH8/P0.4	Input/Output	I2C Data/Timer2 channel1/ADC channel8/P0.4
7	UART1_TX(RX)/TIM1_CH0/P0.6	Input/Output	UART1 RXD/Timer1 channel0/P0.6, with a 10k software-controllable built-in pull-up resistor
8	UART1_TX(RX)/TIM1_CH1/P0.7	Input/Output	UART1 TXD/Timer1 channel1/P0.7, with a 10k software-controllable built-in pull-up resistor
9	HALL_IN0/TIM3_CH0/ADC_CH15/CMP0_IP1/P0.11	Input/Output	Motor PWM channel1 high-side output/Timer2 channel0/P2.11
10	HALL_IN1/TIM3_CH1/ADC_CH16/CMP0_IP2/P0.12	Input/Output	Motor PWM channel1 low-side output/Timer2 channel1/ADC trigger signal2/P2.12
11	HALL_IN2/ADC_CH17/CMP0_IP3/P0.13	Input/Output	Hall sensor A-phase Input/Timer3 channel0/ADC channel15/Comparator0 positive Input1/P0.11
12	CMP0_OUT/MCPWM_BKIN1/SPI_CLK/TIM0_CH1/ ADC_TRIG0/SIF/ADC_CH10/CMP0_IP4/P0.14	Input/Output	Comparator0 Output/Motor PWM breaking signal1/SPI Clock/Timer0 channel1/ADC trigger signal0/SIF/ADC channel10/Comparator0 positive Input4/P0.14
13	MCPWM_CH0P/UART0_TX(RX)/SPI_DI(DO)/TIM0_ CH0/ADC_TRIG1/CMP0_IN/P0.15	Input/Output	Motor PWM channel0 high-side output/UART0 RXD/SPI Data Output/Timer0 channel0/ADC trigger signal1/Comparator0 negative Input/P0.15
14	MCPWM_CH0N/UART0_TX(RX)/SPI_DI(DO)/P1.0	Input/Output	Motor PWM channel0 low-side output/UART0 TXD/SPI DataInput/P1.0, with a 10k software-controllable built-in pull-up resistor
15	OPA0_IP/P3.5	Input/Output	OPA0 positive Input/P3.5
16	OPA0_IN/P3.7	Input/Output	OPA0 negative Input/P3.7
17	ADC_CH11/OPAx_OUT/LDO15/P2.7	Input/Output	ADC channel11/OPAx Output/LDO15 Output/P2.7, with a 10k software-controllable built-in pull-up resistor
18	LRC/MCPWM_CH0P/P1.4	Input/Output	32kHz RC Clock Output/Motor PWM channel0 high-side output/P1.4
19	HRC/MCPWM_CH0N/P1.5	Input/Output	4MHz RC Clock Output/Motor PWM channel0 low-side output/P1.5
20	MCPWM_CH1P/P1.6	Input/Output	Motor PWM channel1 high-side output/P1.6
21	MCPWM_CH1N/P1.7	Input/Output	Motor PWM channel1 low-side output/P1.7
22	MCPWM_CH2P/P1.8	Input/Output	Motor PWM channel2 high-side output/P1.8

No.	Pin Name	Type	Function
23	MCPWM_CH2N/P1.9	Input/Output	Motor PWM channel2 low-side output/P1.9
24	OPA2_IP/P3.10	Input/Output	OPA2 positive Input/P3.10
25	OPA2_IN/P3.11	Input/Output	OPA2 negative Input/P3.11
26	OPA3_IN/P3.14	Input/Output	OPA3 negative Input/P3.14
27	OPA3_IP/P3.15	Input/Output	OPA3 positive Input/P3.15
28	CMP1_OUT/MCPWM_BKIN0/SPI_CS/REF/P2.3	Input/Output	Comparator1 Output/Motor PWM breaking signal0/SPI chip select signal/Voltage Reference/P2.3
29	HALL_IN0/MCPWM_CH2P/UART1_TX(RX)/TIM1_CH0/ADC_TRIG3/CMP1_IP1/P2.4	Input/Output	Hall sensor A-phase Input/Motor PWM channel2 high-side output/UART1 RXD/Timer1 channel0/ADC trigger signal3/Comparator1 positive Input1/P2.4, with a 10k software-controllable built-in pull-up resistor
30	HALL_IN1/MCPWM_CH2N/UART1_TX(RX)/TIM1_CH1/ADC_TRIG0/CMP1_IP2/P2.5	Input/Output	Hall sensor B-phaseInput/Motor PWM channel2 low-side output/UART1 TXD/Timer1 channel1/ADC trigger signal0/Comparator1 positive Input2/P2.5, with a 10k software-controllable built-in pull-up resistor
31	SWCLK	Input	SWD Clock , with 10k built-in pull-up resistor
32	SWDIO	Input/Output	SWD Data, with 10k built-in pull-up resistor

3.1.5 LKS32MC083C8T8(B)

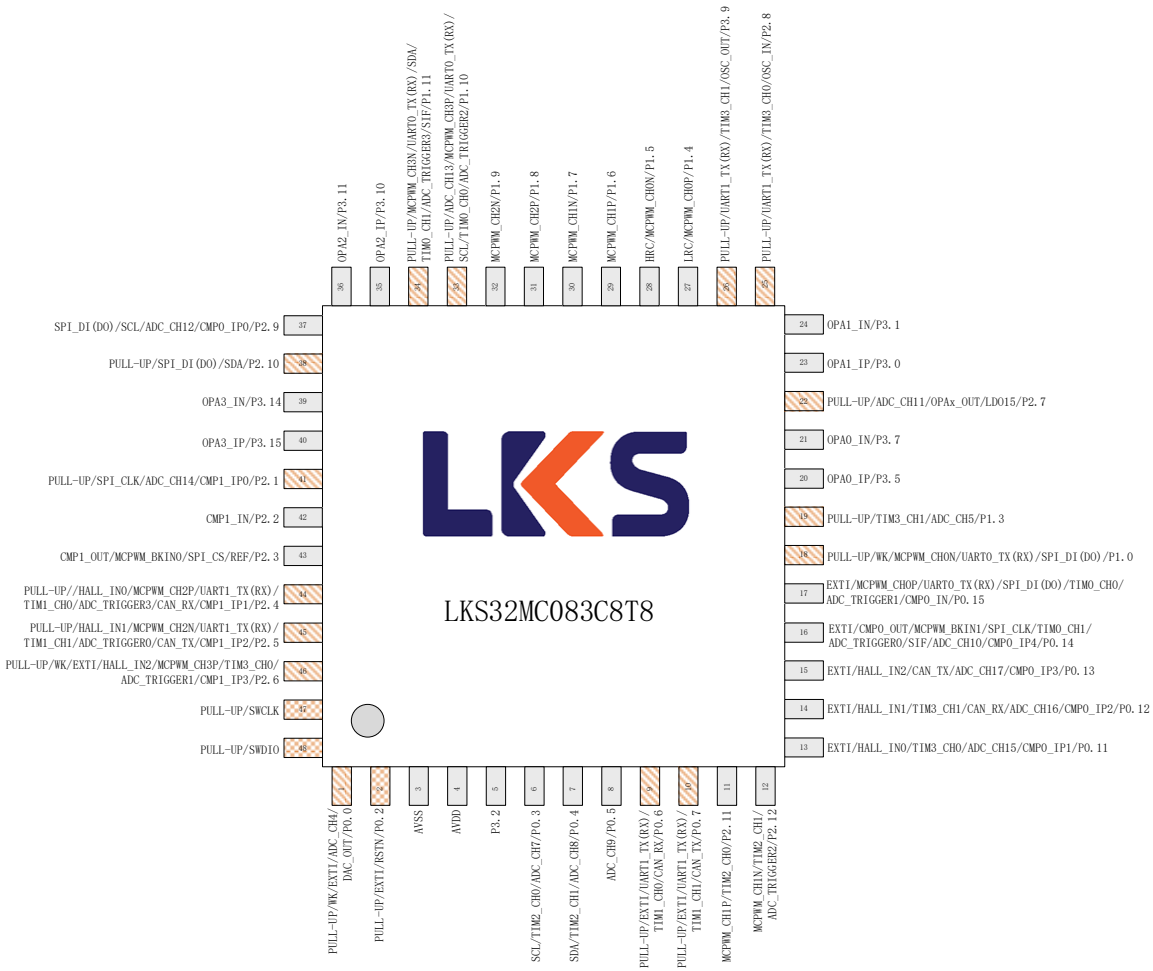

Fig. 3-4 LKS32MC083C8T8(B) Pin Assignment

Caution: LKS32MC083 has CAN module, while LKS32MC081/088 doesn't.

Table 3-4 LKS32MC083C8T8(B) Pin Function Description

No.	Pin Name	Type	Function
1	ADC_CH4/DAC_OUT/P0.0	Input/Output	ADC channel4/DACOutput/P0.0, with a 10k software-controllable built-in pull-up resistor
2	RSTN/P0.2	Input/Output	RSTN/P0.2 is usually used as RSTN. Add a 100nF ground capacitor, plus a 100k built-in pull-up resistor. A 10k~20k pull-up resistor between AVDD and RSTN on PCB is recommended. Use a 100nF capacitor if the pull-up resistor is present.
3	AVSS	Ground	System Ground
4	AVDD	Power	Chip power input. Off-chip decoupling capacitor

No.	Pin Name	Type	Function
			≥1uF is recommended, and should be placed as close as possible to the AVDD pin.
5	P3.2	Input/Output	P3.2
6	SCL/TIM2_CH0/ADC_CH7/P0.3	Input/Output	I2C Clock/Timer2 channel0/ADC channel7/P0.3
7	SDA/TIM2_CH1/ADC_CH8/P0.4	Input/Output	I2C Data/Timer2 channel1/ADC channel8/P0.4
8	ADC_CH9/P0.5	Input/Output	ADC channel9/P0.5
9	UART1_TX(RX)/TIM1_CH0/CAN_RX/P0.6	Input/Output	UART1 RXD/Timer1 channel0/CAN receive/P0.6, with a 10k software-controllable built-in pull-up resistor
10	UART1_TX(RX)/TIM1_CH1/CAN_TX/P0.7	Input/Output	UART1 TXD/Timer1 channel1/CAN transmit/P0.7, with a 10k software-controllable built-in pull-up resistor
11	MCPWM_CH1P/TIM2_CH0/P2.11	Input/Output	Motor PWM channel1 high-side output/Timer2 channel0/P2.11
12	MCPWM_CH1N/TIM2_CH1/ADC_TRIG2/P2.12	Input/Output	Motor PWM channel1 low-side output/Timer2 channel1/ADC trigger signal2/P2.12
13	HALL_IN0/TIM3_CH0/ADC_CH15/CMP0_IP1/P0.11	Input/Output	Hall sensor A-phase Input/Timer3 channel0/ADC channel15/Comparator0 positive Input1/P0.11
14	HALL_IN1/CAN_RX/TIM3_CH1/ADC_CH16/CMP0_IP2/CAN_RX/P0.12	Input/Output	Hall sensor B-phaseInput/CAN Receive/Timer3 channel1/ADC channel16/Comparator0 positive Input2/CAN receive/P0.12
15	HALL_IN2/CAN_TX/ADC_CH17/CMP0_IP3/CAN_TX/P0.13	Input/Output	Hall sensor C-phase Input/CAN Transmit/ADC channel17/Comparator0 positive Input3/CAN transmit/P0.13
16	CMP0_OUT/MCPWM_BKIN1/SPI_CLK/TIM0_CH1/ADC_TRIG0/SIF/ADC_CH10/CMP0_IP4/P0.14	Input/Output	Comparator0 Output/Motor PWM breaking signal1/SPI Clock/Timer0 channel1/ADC trigger signal0/SIF/ADC channel10/Comparator0 positive Input4/P0.14
17	MCPWM_CH0P/UART0_TX(RX)/SPI_DI(DO)/TIM0_CH0/ADC_TRIG1/CMP0_IN/P0.15	Input/Output	Motor PWM channel0 high-side output/UART0 RXD/SPI Data Output/Timer0 channel0/ADC trigger signal1/Comparator0 negative Input/P0.15
18	MCPWM_CH0N/UART0_TX(RX)/SPI_DI(DO)/P1.0	Input/Output	Motor PWM channel0 low-side output/UART0 TXD/SPI DataInput/P1.0, with a 10k software-controllable built-in pull-up resistor
19	TIM3_CH1/ADC_CH5/P1.3	Input/Output	Timer3 channel1/ADC channel5/P1.3, with a 10k software-controllable built-in pull-up resistor
20	OPA0_IP/P3.5	Input/Output	OPA0 positive Input/P3.5
21	OPA0_IN/P3.7	Input/Output	OPA0 negative Input/P3.7
22	ADC_CH11/OPAx_OUT/LDO15/P2.7	Input/Output	ADC channel11/OPAx Output/LDO15 Output/P2.7, with a 10k software-controllable built-in pull-up resistor
23	OPA1_IP/P3.0	Input/Output	OPA1 positive Input/P3.0
24	OPA1_IN/P3.1	Input/Output	OPA1 negative Input/P3.1

No.	Pin Name	Type	Function
25	UART1_TX(RX)/TIM3_CH0/OSC_IN/P2.8	Input/Output	UART1 RXD/Timer3 channel0/Crystal Oscillator Input/P2.8, with a 10k software-controllable built-in pull-up resistor, if connected to a crystal, add a 15pf shut capacitor to ground
26	UART1_TX(RX)/TIM3_CH1/OSC_OUT/P3.9	Input/Output	UART1 TXD/Timer3 channel1/Crystal Oscillator Output/P3.9, with a 10k software-controllable built-in pull-up resistor, if connected to a crystal, add a 15pf shut capacitor to ground
27	LRC/MCPWM_CH0P/P1.4	Input/Output	32kHz RC Clock Output/Motor PWM channel0 high-side output/P1.4
28	HRC/MCPWM_CH0N/P1.5	Input/Output	4MHz RC Clock Output/Motor PWM channel0 low-side output/P1.5
29	MCPWM_CH1P/P1.6	Input/Output	Motor PWM channel1 high-side output/P1.6
30	MCPWM_CH1N/P1.7	Input/Output	Motor PWM channel1 low-side output/P1.7
31	MCPWM_CH2P/P1.8	Input/Output	Motor PWM channel2 high-side output/P1.8
32	MCPWM_CH2N/P1.9	Input/Output	Motor PWM channel2 low-side output/P1.9
33	ADC_CH13/MCPWM_CH3P/UART0_TX(RX)/SCL/TIM0_CH0/ADC_TRIG2/P1.10	Input/Output	Motor PWM channel3 high-side output/UART0 RXD/I2C Clock/Timer0 channel0/ADC trigger signal2/P1.10, with a 10k software-controllable built-in pull-up resistor
34	MCPWM_CH3N/UART0_TX(RX)/SDA/TIM0_CH1/ADC_TRIG3/SIF/P1.11	Input/Output	Motor PWM channel3 low-side output/UART0 TXD/I2C Data/Timer0 channel1/ADC trigger signal3/P1.11, with a 10k software-controllable built-in pull-up resistor
35	OPA2_IP/P3.10	Input/Output	OPA2 positive Input/P3.10
36	OPA2_IN/P3.11	Input/Output	OPA2 negative Input/P3.11
37	SPI_DI(DO)/SCL/ADC_CH12/CMP0_IP0/P2.9	Input/Output	SPI DataInput/I2C Clock/ADC channel12/Comparator0 positive Input0/P2.9
38	SPI_DI(DO)/SDA/P2.10	Input/Output	SPI Data Output/I2C Data/P2.10, with a 10k software-controllable built-in pull-up resistor
39	OPA3_IN/P3.14	Input/Output	OPA3 negative Input/P3.14
40	OPA3_IP/P3.15	Input/Output	OPA3 positive Input/P3.15
41	SPI_CLK/ADC_CH14/CMP1_IP0/P2.1	Input/Output	SPI Clock/ADC channel14/Comparator1 positive Input0/P2.1, with a 10k software-controllable built-in pull-up resistor
42	CMP1_IN/P2.2	Input/Output	Comparator1 negative Input/P2.2
43	CMP1_OUT/MCPWM_BKIN0/SPI_CS/REF/P2.3	Input/Output	Comparator1 Output/Motor PWM breaking signal0/SPI chip select signal/Voltage Reference/P2.3
44	HALL_IN0/CAN_RX/MCPWM_CH2P/UART1_TX(RX)/TIM1_CH0/ADC_TRIG3/CAN_RX/CMP1_IP1/P2.4	Input/Output	Hall sensor A-phase Input/CAN Receive/Motor PWM channel2 high-side output/UART1 RXD/Timer1 channel0/ADC trigger signal3/Comparator1 positive Input1/CAN receive/P2.4, with a 10k software-controllable built-in pull-up resistor

No.	Pin Name	Type	Function
45	HALL_IN1/CAN_TX/MCPWM_CH2N/UART1_TX(RX) /TIM1_CH1/ADC_TRIG0/CAN_TX/CMP1_IP2/P2.5	Input/Output	Hall sensor B-phaseInput/CAN Transmit/Motor PWM channel2 low-side output/UART1 TXD/Timer1 channel1/ADC trigger signal0/Comparator1 positive Input2/CAN transmit/P2.5, with a 10k soft-ware-controllable built-in pull-up resistor
46	HALL_IN2/MCPWM_CH3P/TIM3_CH0/ ADC_TRIG1/CMP1_IP3/P2.6	Input/Output	Hall sensor C-phase Input/Motor PWM channel3 high-side output /Timer3 channel0/ADC trigger signal1/Comparator1 positive Input3/P2.6, with a 10k software-controllable built-in pull-up resistor
47	SWCLK	Input	SWD Clock , with 10k built-in pull-up resistor
48	SWDIO	Input/Output	SWD Data, with 10k built-in pull-up resistor

For more information about LKS32MC083C8T8(B), please refer to the chip selection guide.

3.1.6 LKS32MC087M6S8(B)

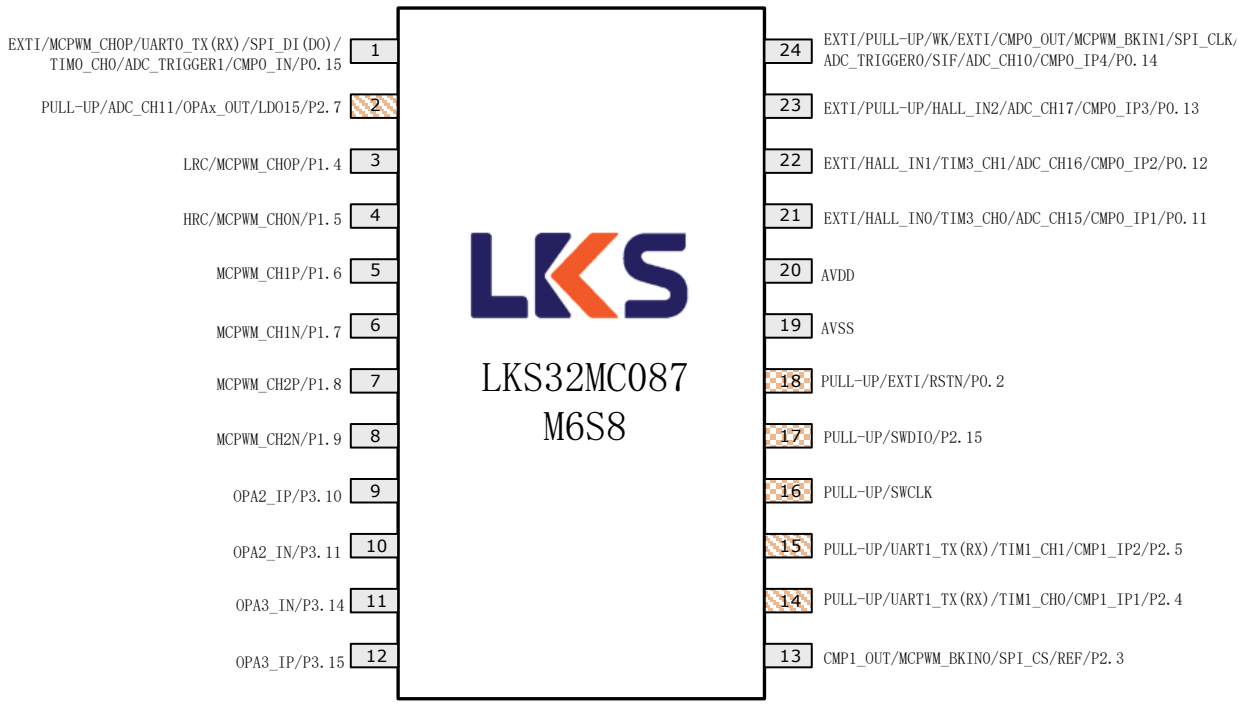

Fig. 3-6 LKS32MC087M6S8(B) Pin Assignment

Table 3-5 LKS32MC087M6S8(B) Pin Function Description

No.	Pin Name	Type	Function
1	MCPWM_CH0P/UART0_TX(RX)/SPI_DI(DO)/TIM0_CH0/ADC_TRIG1/CMP0_IN/P0.15	Input/Output	Motor PWM channel0 high-side output/UART0 RXD/SPI Data Output/Timer0 channel0/ADC trigger signal1/Comparator0 negative Input/P0.15
2	ADC_CH11/OPAx_OUT/LDO15/P2.7	Input/Output	ADC channel11/OPAx Output/LDO15 Output/P2.7, with a 10k software-controllable built-in pull-up

No.	Pin Name	Type	Function
			resistor
3	LRC/MCPWM_CH0P/P1.4	Input/Output	32kHz RC Clock Output/Motor PWM channel0 high-side output/P1.4
4	HRC/MCPWM_CH0N/P1.5	Input/Output	4MHz RC Clock Output/Motor PWM channel0 low-side output/P1.5
5	MCPWM_CH1P/P1.6	Input/Output	Motor PWM channel1 high-side output/P1.6
6	MCPWM_CH1N/P1.7	Input/Output	Motor PWM channel1 low-side output/P1.7
7	MCPWM_CH2P/P1.8	Input/Output	Motor PWM channel2 high-side output/P1.8
8	MCPWM_CH2N/P1.9	Input/Output	Motor PWM channel2 low-side output/P1.9
9	OPA2_IP/P3.10	Input/Output	OPA2 positive Input/P3.10
10	OPA2_IN/P3.11	Input/Output	OPA2 negative Input/P3.11
11	OPA3_IN/P3.14	Input/Output	OPA3 negative Input/P3.14
12	OPA3_IP/P3.15	Input/Output	OPA3 positive Input/P3.15
13	CMP1_OUT/MCPWM_BKIN0/SPI_CS/REF/P2.3	Input/Output	Comparator1 Output/Motor PWM breaking signal0/SPI chip select signal/Voltage Reference/P2.3
14	UART1_TX(RX)/TIM1_CH0/ADC_TRIG3/ CMP1_IP1/P2.4	Input/Output	UART1 RXD/Timer1 channel0/ADC trigger signal3/Comparator1 positive Input1/P2.4, with a 10k software-controllable built-in pull-up resistor
15	UART1_TX(RX)/TIM1_CH1/ADC_TRIG0/ CMP1_IP2/P2.5	Input/Output	UART1 TXD/Timer1 channel1/ADC trigger signal0/Comparator1 positive Input2/P2.5, with a 10k software-controllable built-in pull-up resistor
16	SWCLK	Input	SWD Clock , with 10k built-in pull-up resistor
17	SWDIO/P2.15	Input/Output	SWD Data/P2.15, with 10k built-in pull-up resistor SWD Data IO and P2.15 IO are bonded together. Please take good care of P2.15 Input/Output Enable, in case P2.15interfere SWD access right after chip power-up, which will cause the chip unable to erase or reprogram.
18	RSTN/P0.2	Input/Output	RSTN/P0.2 is usually used as RSTN. Add a 100nF ground capacitor, plus a 100k built-in pull-up resistor. A 10k~20k pull-up resistor between AVDD and RSTN on PCB is recommended. Use a 100nF capacitor if the pull-up resistor is present.
19	AVSS	Ground	System Ground
20	AVDD	Power	Chip power input. Off-chip decoupling capacitor ≥1uF is recommended, and should be placed as close as possible to the AVDD pin.
21	HALL_IN0/TIM3_CH0/ADC_CH15/CMP0_IP1/P0.11	Input/Output	Hall sensor A-phase Input/Timer3 channel0/ADC channel15/Comparator0 positive Input1/P0.11
22	HALL_IN1/TIM3_CH1/ADC_CH16/CMP0_IP2/P0.12	Input/Output	Hall sensor B-phaseInput/Timer3 channel1/ADC channel16/Comparator0 positive Input2/P0.12
23	HALL_IN2/ADC_CH17/CMP0_IP3/P0.13	Input/Output	Hall sensor C-phase Input/ADC chan-

No.	Pin Name	Type	Function
			nel17/Comparator0 positive Input3/P0.13
24	CMP0_OUT/MCPWM_BKIN1/SPI_CLK/TIM0_CH1/ ADC_TRIG0/SIF/ADC_CH10/CMP0_IP4/P0.14	Input/Output	Comparator0 Output/Motor PWM breaking signal1/SPI Clock/Timer0 channel1/ADC trigger signal0/SIF/ADC channel10/Comparator0 positive Input4/P0.14

3.1.7 LKS32MC087AM6S8(B)

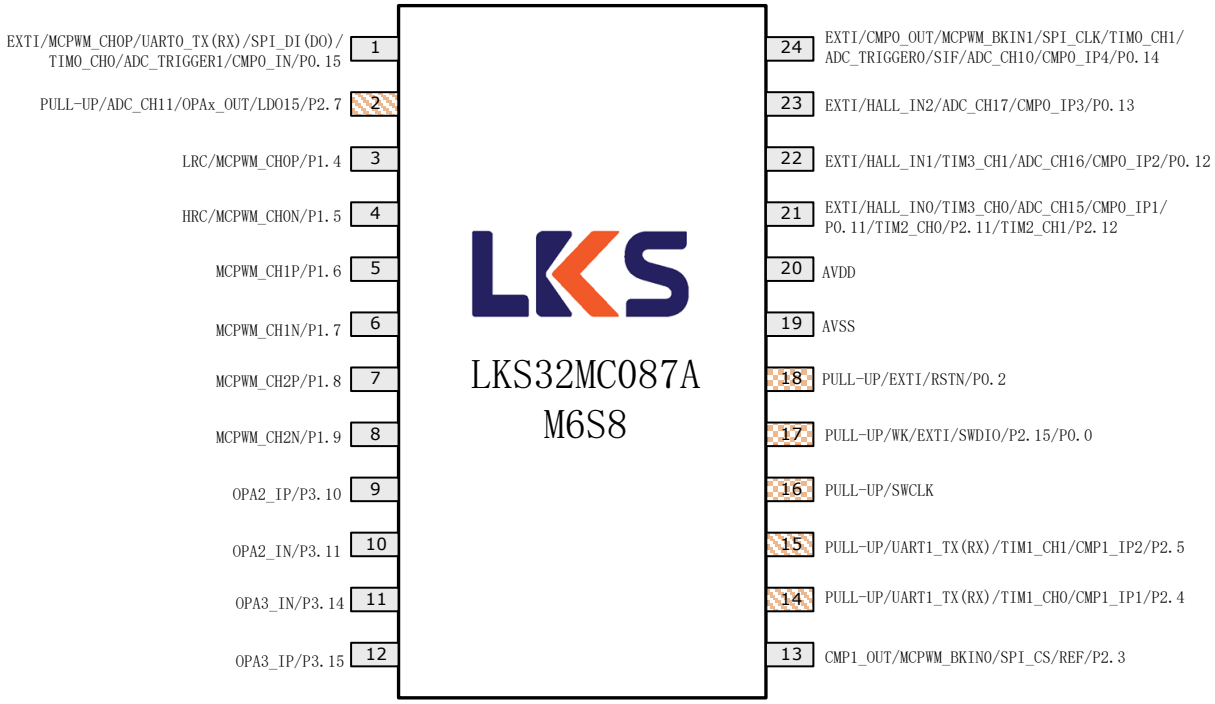

Fig. 3-7 LKS32MC087AM6S8(B) Pin Assignment

Difference from LKS32MC087M6S8(B):

PIN17 is now equipped with P0.0, which could be used as ADC Input or IO wake up signal
PIN21 is now equipped with TIM2_CH0/CH1 fucntions
All the other PINs are the same with LKS32MC087M6S8(B).

Table 3-6 LKS32MC087AM6S8(B) Pin Function Description

No.	Pin Name	Type	Function
1	MCPWM_CH0P/UART0_TX(RX)/SPI_DI(DO)/TIM0_CH0/ADC_TRIG1/CMP0_IN/P0.15	Input/Output	Motor PWM channel0 high-side output/UART0 RXD/SPI Data Output/Timer0 channel0/ADC trigger signal1/Comparator0 negative Input/P0.15
2	ADC_CH11/OPAx_OUT/LDO15/P2.7	Input/Output	ADC channel11/OPAx Output/LDO15 Output/P2.7, with a 10k software-controllable built-in pull-up resistor
3	LRC/MCPWM_CH0P/P1.4	Input/Output	32kHz RC Clock Output/Motor PWM channel0

No.	Pin Name	Type	Function
			high-side output/P1.4
4	HRC/MCPWM_CH0N/P1.5	Input/Output	4MHz RC Clock Output/Motor PWM channel0 low-side output/P1.5
5	MCPWM_CH1P/P1.6	Input/Output	Motor PWM channel1 high-side output/P1.6
6	MCPWM_CH1N/P1.7	Input/Output	Motor PWM channel1 low-side output/P1.7
7	MCPWM_CH2P/P1.8	Input/Output	Motor PWM channel2 high-side output/P1.8
8	MCPWM_CH2N/P1.9	Input/Output	Motor PWM channel2 low-side output/P1.9
9	OPA2_IP/P3.10	Input/Output	OPA2 positive Input/P3.10
10	OPA2_IN/P3.11	Input/Output	OPA2 negative Input/P3.11
11	OPA3_IN/P3.14	Input/Output	OPA3 negative Input/P3.14
12	OPA3_IP/P3.15	Input/Output	OPA3 positive Input/P3.15
13	CMP1_OUT/MCPWM_BKIN0/SPI_CS/REF/P2.3	Input/Output	Comparator1 Output/Motor PWM breaking signal0/SPI chip select signal/Voltage Reference/P2.3
14	UART1_TX(RX)/TIM1_CH0/ADC_TRIG3/ CMP1_IP1/P2.4	Input/Output	UART1 RXD/Timer1 channel0/ADC trigger signal3/Comparator1 positive Input1/P2.4, with a 10k software-controllable built-in pull-up resistor
15	UART1_TX(RX)/TIM1_CH1/ADC_TRIG0/ CMP1_IP2/P2.5	Input/Output	UART1 TXD/Timer1 channel1/ADC trigger signal0/Comparator1 positive Input2/P2.5, with a 10k software-controllable built-in pull-up resistor
16	SWCLK	Input	SWD Clock , with 10k built-in pull-up resistor
17	SWDIO/P2.15/P0.0	Input/Output	SWD Data/P2.15/P0.0, with 10k built-in pull-up resistor SWD Data/P2.15, with 10k built-in pull-up resistor SWD Data IO and P2.15 IO are bonded together. Please take good care of P2.15 Input/Output Enable, in case P2.15interfere SWD access right after chip power-up, which will cause the chip unable to erase or reprogram.
18	RSTN/P0.2	Input/Output	RSTN/P0.2 is usually used as RSTN. Add a 100nF ground capacitor, plus a 100k built-in pull-up resistor. A 10k~20k pull-up resistor between AVDD and RSTN on PCB is recommended. Use a 100nF capacitor if the pull-up resistor is present.
19	AVSS	Ground	System Ground
20	AVDD	Power	Chip power input. Off-chip decoupling capacitor ≥1uF is recommended, and should be placed as close as possible to the AVDD pin.
21	HALL_IN0/TIM3_CH0/ADC_CH15/CMP0_IP1/P0.11/ TIM2_CH0/P2.11/TIM2_CH1/P2.12	Input/Output	Hall sensor A-phase Input/Timer3 channel0/ADC channel15/Comparator0 positive Input1/P0.11/Timer2 channel0/P2.11/ Timer2 channel1/P2.12 Please DO NOT enable any two of P0.11/P2.11/P2.12 outputs at the same time.

No.	Pin Name	Type	Function
22	HALL_IN1/TIM3_CH1/ADC_CH16/CMP0_IP2/P0.12	Input/Output	Hall sensor B-phaseInput/Timer3 channel1/ADC channel16/Comparator0 positive Input2/P0.12
23	HALL_IN2/ADC_CH17/CMP0_IP3/P0.13	Input/Output	Hall sensor C-phase Input/ADC channel17/Comparator0 positive Input3/P0.13
24	CMP0_OUT/MCPWM_BKIN1/SPI_CLK/TIM0_CH1/ ADC_TRIG0/SIF/ADC_CH10/CMP0_IP4/P0.14	Input/Output	Comparator0 Output/Motor PWM breaking signal1/SPI Clock/Timer0 channel1/ADC trigger signal0/SIF/ADC channel10/Comparator0 positive Input4/P0.14

3.1.8 LKS32MC087CM8S8(B)

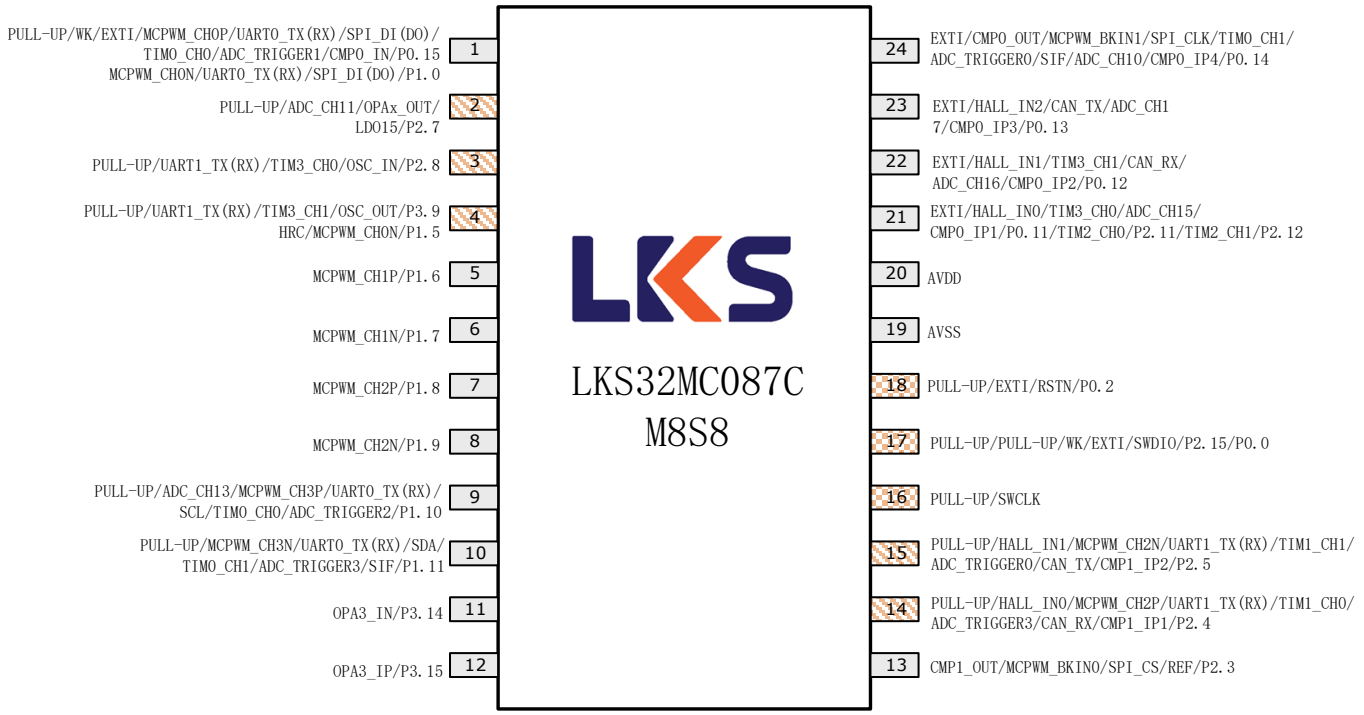

Fig. 3-8 LKS32MC087CM8S8(B) Pin Assignment

Table 3-7 LKS32MC087CM8S8(B) Pin Function Description

No.	Pin Name	Type	Function
1	MCPWM_CH0P/UART0_TX(RX)/SPI_DI(DO)/TIM0_CH0/ADC_TRIG1/CMP0_IN/P0.15 MCPWM_CH0N/UART0_TX(RX)/SPI_DI(DO)/P1.0	Input/Output	Motor PWM channel0 high-side output/UART0 RXD/SPI Data Output/Timer0 channel0/ADC trigger signal1/Comparator0 negative Input/P0.15 Motor PWM channel0 low-side output/UART0 TXD/SPI DataInput/P1.0
2	ADC_CH11/OPAx_OUT/LDO15/P2.7	Input/Output	ADC channel11/OPAx Output/LDO15 Output/P2.7, with a 10k software-controllable built-in pull-up resistor
3	UART1_TX(RX)/TIM3_CH0/OSC_IN/P2.8	Input/Output	UART1 RXD/Timer3 channel0/Crystal Oscillator

No.	Pin Name	Type	Function
			Input/P2.8, with a 10k software-controllable built-in pull-up resistor, if connected to a crystal, add a 15pf shut capacitor to ground
4	UART1_TX(RX)/TIM3_CH1/OSC_OUT/P3.9 HRC/MCPWM_CH0N/P1.5	Input/Output	UART1 TXD/Timer3 channel1/Crystal Oscillator Output/P3.9, with a 10k software-controllable built-in pull-up resistor, if connected to a crystal, add a 15pf shut capacitor to ground 4MHz RC Clock Output/Motor PWM channel0 low-side output/P1.5
5	MCPWM_CH1P/P1.6	Input/Output	Motor PWM channel1 high-side output/P1.6
6	MCPWM_CH1N/P1.7	Input/Output	Motor PWM channel1 low-side output/P1.7
7	MCPWM_CH2P/P1.8	Input/Output	Motor PWM channel2 high-side output/P1.8
8	MCPWM_CH2N/P1.9	Input/Output	Motor PWM channel2 low-side output/P1.9
9	ADC_CH13/MCPWM_CH3P/UART0_TX(RX)/SCL/TIM0_CH0/ADC_TRIG2/P1.10	Input/Output	Motor PWM channel3 high-side output/UART0 RXD/I2C Clock/Timer0 channel0/ADC trigger signal2/P1.10, with a 10k software-controllable built-in pull-up resistor
10	MCPWM_CH3N/UART0_TX(RX)/SDA/TIM0_CH1/ADC_TRIG3/SIF/P1.11	Input/Output	Motor PWM channel3 low-side output/UART0 TXD/I2C Data/Timer0 channel1/ADC trigger signal3/P1.11, with a 10k software-controllable built-in pull-up resistor
11	OPA3_IN/P3.14	Input/Output	OPA3 negative Input/P3.14
12	OPA3_IP/P3.15	Input/Output	OPA3 positive Input/P3.15
13	CMP1_OUT/MCPWM_BKIN0/SPI_CS/REF/P2.3	Input/Output	Comparator1 Output/Motor PWM breaking signal0/SPI chip select signal/Voltage Reference/P2.3
14	UART1_TX(RX)/TIM1_CH0/ADC_TRIG3/ CMP1_IP1/P2.4	Input/Output	UART1 RXD/Timer1 channel0/ADC trigger signal3/Comparator1 positive Input1/P2.4, with a 10k software-controllable built-in pull-up resistor
15	UART1_TX(RX)/TIM1_CH1/ADC_TRIG0/ CMP1_IP2/P2.5	Input/Output	UART1 TXD/Timer1 channel1/ADC trigger signal0/Comparator1 positive Input2/P2.5, with a 10k software-controllable built-in pull-up resistor
16	SWCLK	Input	SWD Clock , with 10k built-in pull-up resistor
17	SWDIO/P2.15/P0.0	Input/Output	SWD Data/P2.15/P0.0, with 10k built-in pull-up resistor SWD Data/P2.15, with 10k built-in pull-up resistor SWD Data IO and P2.15 IO are bonded together. Please take good care of P2.15 Input/Output Enable, in case P2.15interfere SWD access right after chip power-up, which will cause the chip unable to erase or reprogram.
18	RSTN/P0.2	Input/Output	RSTN/P0.2 is usually used as RSTN. Add a 100nF ground capacitor, plus a 100k built-in pull-up resistor. A 10k~20k pull-up resistor between AVDD and

No.	Pin Name	Type	Function
			RSTN on PCB is recommended. Use a 100nF capacitor if the pull-up resistor is present.
19	AVSS	Ground	System Ground
20	AVDD	Power	Chip power input. Off-chip decoupling capacitor ≥1uF is recommended, and should be placed as close as possible to the AVDD pin.
21	HALL_IN0/TIM3_CH0/ADC_CH15/CMP0_IP1/P0.11/TIM2_CH0/P2.11/TIM2_CH1/P2.12	Input/Output	Hall sensor A-phase Input/Timer3 channel0/ADC channel15/Comparator0 positive Input1/P0.11/Timer2 channel0/P2.11/ Timer2 channel1/P2.12 Please DO NOT enable any two of P0.11/P2.11/P2.12 outputs at the same time.
22	HALL_IN1/TIM3_CH1/ADC_CH16/CMP0_IP2/P0.12	Input/Output	Hall sensor B-phaseInput/Timer3 channel1/ADC channel16/Comparator0 positive Input2/P0.12
23	HALL_IN2/ADC_CH17/CMP0_IP3/P0.13	Input/Output	Hall sensor C-phase Input/ADC channel17/Comparator0 positive Input3/P0.13
24	CMP0_OUT/MCPWM_BKIN1/SPI_CLK/TIM0_CH1/ADC_TRIG0/SIF/ADC_CH10/CMP0_IP4/P0.14	Input/Output	Comparator0 Output/Motor PWM breaking signal1/SPI Clock/Timer0 channel1/ADC trigger signal0/SIF/ADC channel10/Comparator0 positive Input4/P0.14

3.2 Description of Pin Multiplex Function

Table 3-8 LKS32MC08X Pin Function Selection

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF0
P0.0												ADC_CH4, DAC_OUT
P0.1												ADC_CH6
P0.2												
P0.3						SCL		TIM2_CH0				ADC_CH7
P0.4						SDA		TIM2_CH1				ADC_CH8
P0.5												ADC_CH9
P0.6				UART1_TX(RX)			TIM1_CH0			CAN_RX		
P0.7				UART1_TX(RX)			TIM1_CH1			CAN_TX		
P0.8												
P0.9						SCL		TIM2_CH0				
P0.10						SDA		TIM2_CH1				
P0.11		HALL_IN0						TIM3_CH0				ADC_CH15/CMP0_IP1
P0.12		HALL_IN1						TIM3_CH1		CAN_RX		ADC_CH16/CMP0_IP2
P0.13		HALL_IN2								CAN_TX		ADC_CH17/CMP0_IP3
P0.14	CMP0_OUT		MCPWM_BKIN1		SPI_CLK		TIM0_CH1		ADC_TRIG0		SIF	ADC_CH10/CMP0_IP4
P0.15			MCPWM_CH0P	UART0_TX(RX)	SPI_DI(DO)		TIM0_CH0		ADC_TRIG1			CMP0_IN

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF0
P1.0			MCPWM_CH0N	UART0_TX(RX)	SPI_DI(DO)							
P1.1					SPI_CS							
P1.2								TIM3_CH0				
P1.3								TIM3_CH1				ADC_CH5
P1.4	LRC		MCPWM_CH0P									
P1.5	HRC		MCPWM_CH0N									
P1.6			MCPWM_CH1P									
P1.7			MCPWM_CH1N									
P1.8			MCPWM_CH2P									
P1.9			MCPWM_CH2N									
P1.10			MCPWM_CH3P	UART0_TX(RX)		SCL	TIM0_CH0		ADC_TRIG2			ADC_CH13
P1.11			MCPWM_CH3N	UART0_TX(RX)		SDA	TIM0_CH1		ADC_TRIG3		SIF	
P1.12			MCPWM_CH1N									
P1.13					SPI_CLK		TIM0_CH0					
P1.14					SPI_DI(DO)		TIM0_CH1					
P1.15			MCPWM_CH2N									

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF0
P2.0					SPI_CS			TIM2_CH1				
P2.1					SPI_CLK							ADC_CH14/ CMP1_IP0
P2.2												CMP1_IN
P2.3	CMP1_OUT		MCPWM_BKIN0		SPI_CS							REF
P2.4		HALL_IN0	MCPWM_CH2P	UART1_TX(RX)			TIM1_CH0		ADC_TRIG3	CAN_RX		CMP1_IP1
P2.5		HALL_IN1	MCPWM_CH2N	UART1_TX(RX)			TIM1_CH1		ADC_TRIG0	CAN_TX		CMP1_IP2
P2.6		HALL_IN2	MCPWM_CH3P					TIM3_CH0	ADC_TRIG1		SIF	CMP1_IP3
P2.7												ADC_CH11/ OPAx_OUT/ LDO15
P2.8				UART1_TX(RX)				TIM3_CH0				OSC_IN
P2.9					SPI_DI(DO)	SCL						ADC_CH12/ CMP0_IP0
P2.10					SPI_DI(DO)	SDA						
P2.11			MCPWM_CH1P					TIM2_CH0				
P2.12			MCPWM_CH1N					TIM2_CH1	ADC_TRIG2			
P2.13			MCPWM_CH3N					TIM3_CH1				
P2.14						SCL						
P2.15						SDA						

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF0
P3.0												OPA1_IP
P3.1												OPA1_IN
P3.2												
P3.3												
P3.4												
P3.5												OPA0_IP
P3.6												
P3.7												OPA0_IN
P3.8												
P3.9				UART1_TX(RX)				TIM3_CH1				OSC_OUT
P3.10												OPA2_IP
P3.11												OPA2_IN
P3.12												
P3.13	HRC		MCPWM_CH0N									
P3.14												OPA3_IN
P3.15												OPA3_IP

4 Package Size

4.1 LKS32MC080R8T8(B)

LQFP64 Profile Quad Flat Package:

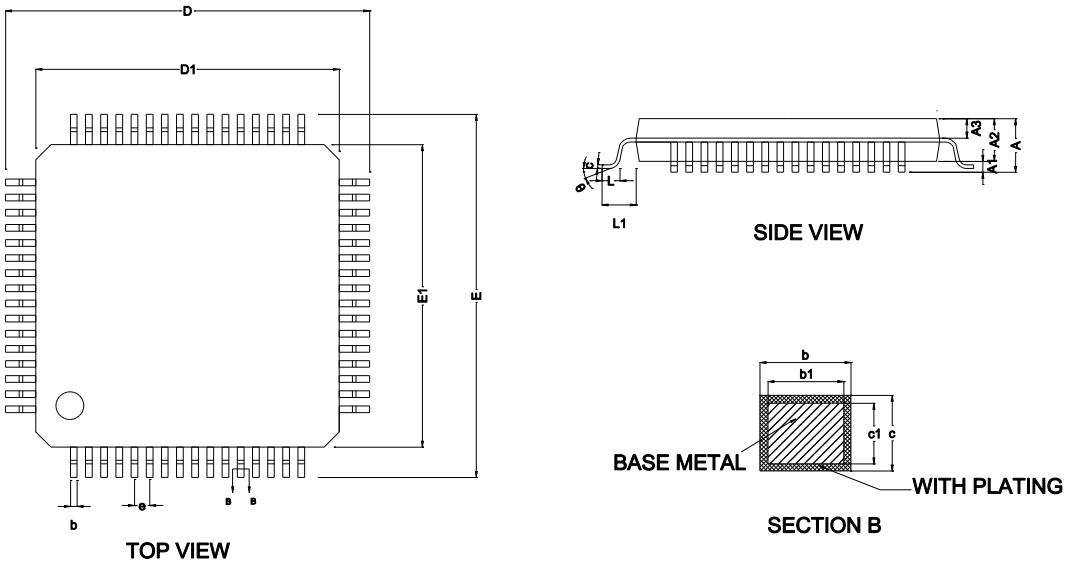

Fig. 4-1 LKS32MC080R8T8(B) Package Diagram

Table 4-1 LKS32MC080R8T8(B) Package Size

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

4.2 LKS32MC081C8T8(B)/LKS32MC083C8T8(B)/LKS32MC088C6T8(B)

TQFP48 Profile Quad Flat Package:

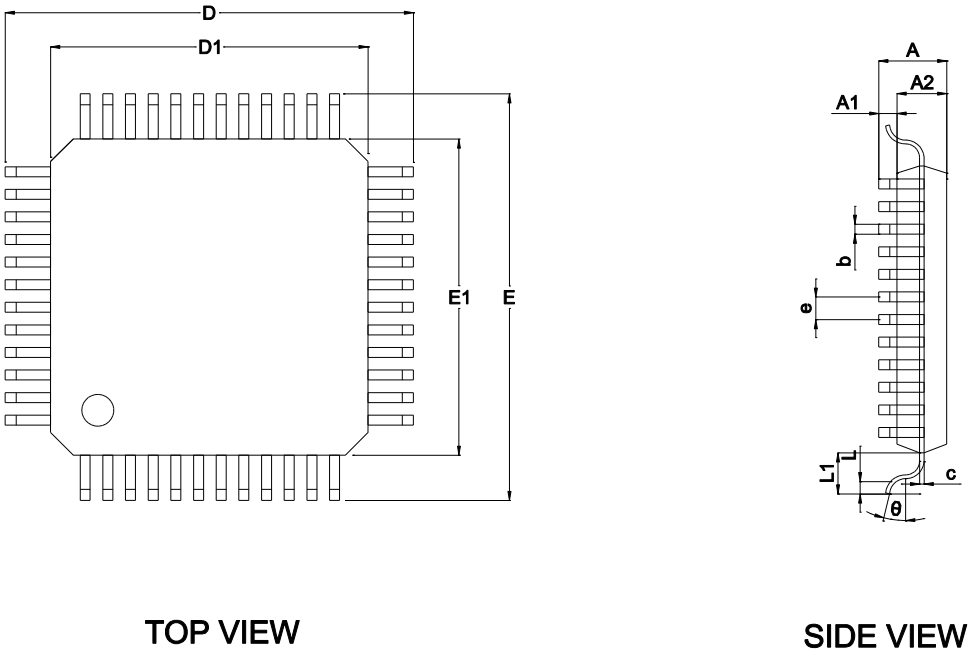

Fig. 4-2 LKS32MC081C8T8(B)/LKS32MC083C8T8(B)/LKS32MC088C6T8(B) Package Diagram

Table 4-2 LKS32MC081C8T8(B)/LKS32MC083C8T8(B)/LKS32MC088C6T8(B) Package Size

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.18	0.22	0.26
c	0.13	-	0.17
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	-	0.50	-
θ	0°	3.5°	7°
L	0.45	0.60	0.75
L1	-	1.00	-

LKS32MC083C8T8(B),LKS32MC088C8T8(B)封装也是 TQFP48,后面就不做赘述。

4.3 LKS32MC082K8Q8(B)

QFN5*5 32L-0.75 Profile Quad Flat Package:

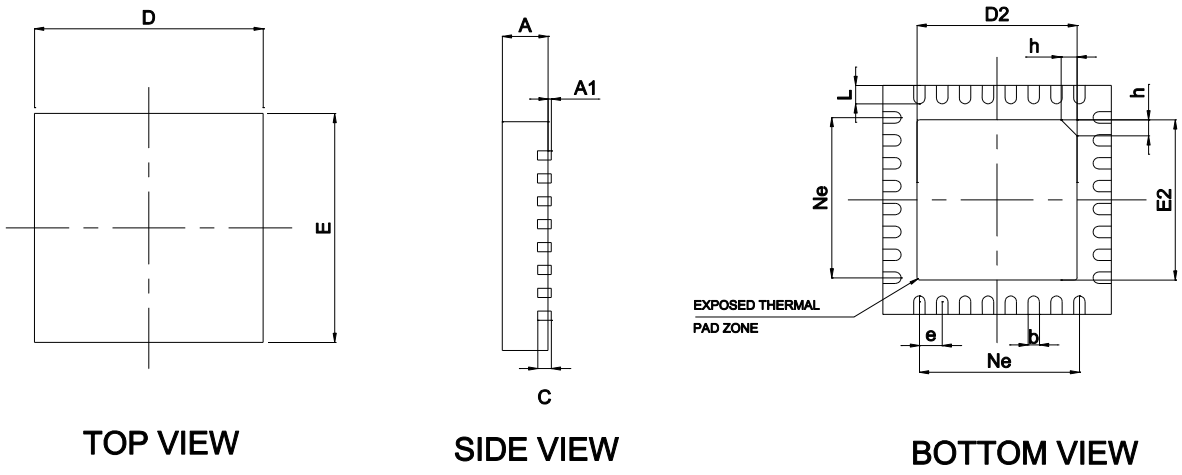

Fig. 4-3 LKS32MC082K8Q8(B) Package Diagram

Table 4-3 LKS32MC082K8Q8(B) Package Size

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.24
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40

4.4 LKS32MC087M6S8(B)/LKS32MC087AM6S8(B)/LKS32MC087CM8S8(B)

SSOP24L Profile Quad Flat Package:

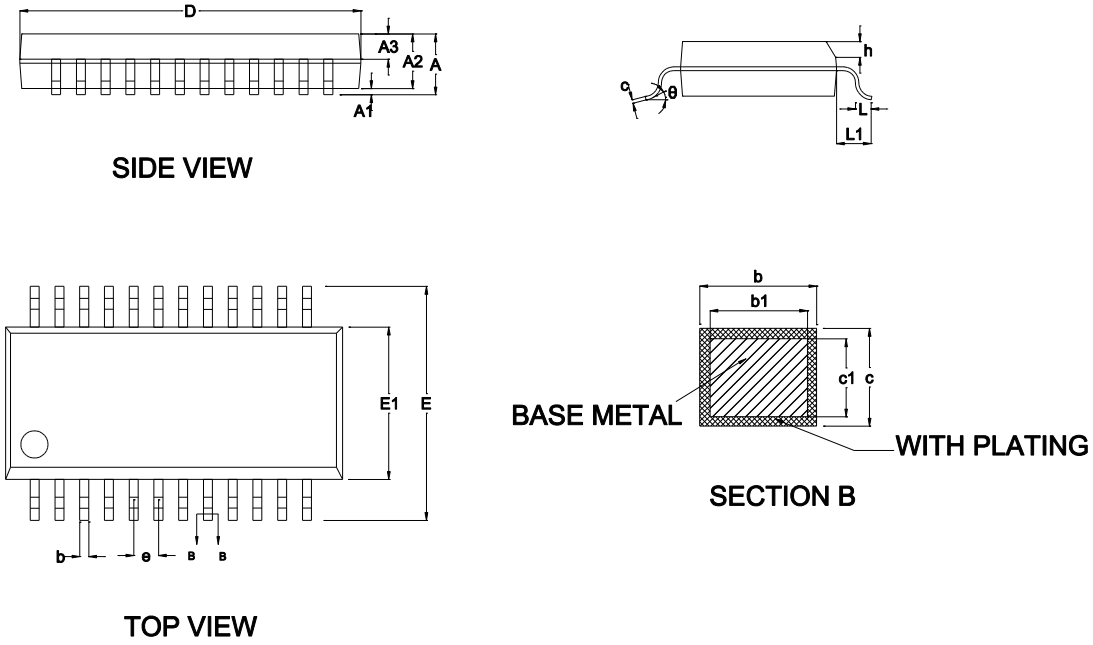

Fig. 4-4 LKS32MC087M6S8(B) Package Diagram

Table 4-4 LKS32MC087M6S8(B) Package Size

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	-	0.31
b1	0.22	0.25	0.28
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

5 Electrical Characteristics

LKS32MC08x is the main stream MCU series. The electrical characteristics of LKS32MC08x are shown in the following table. Take the LKS32MC080R8T8 as an example.

Table 5-1 LKS32MC08x electrical absolute characteristics

Parameter	Min.	Max.	Unit	Description
Voltage (AVDD)	-0.3	+6.0	V	Ground
Operating Temperature	-40	+105	˚C	
Storage Temperature	-40	+150	˚C	
Junction Temperature	-	150	°C	
Pin Temperature (solder for10 seconds)	-	260	°C	

Table 5-2 LKS32MC08x Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit	Description
Power supply voltage (AVDD)	3.0	5	5.5	V	The AVDD reset level of version A chip is 2.2V ± 0.2V
	2.2				The AVDD reset level of version B chip is 2.7V ± 0.2V
Analog power voltage($AVDD_A$)	3.3	5	5.5	V	ADC use 2.4V internal reference
	2.8	5	5.5	V	ADC use 1.2V internal reference

OPA could work under 3.0V, but the output range will be limited.

Table 5-3 LKS32MC08x ESD parameters

Item	Min.	Max.	Unit
ESD test (HBM)	-6000	6000	V

According to "MIL-STD-883J Method 3015.9", under the environment of 25°C and 55% relative humidity, electrostatic discharge is applied to all IO pins of the tested chip for 3 times, with an interval of 1s each time. The test results show that the anti-static discharge level of the chip reaches Class 3A ≧4000V, <8000V.

Table 5-4 LKS32MC08x Latch-up parameters

Item	Min.	Max.	Unit
Latch-up current (85°C)	-200	200	mA

According to "JEDEC STANDARD NO.78E NOVEMBER 2016", apply an overvoltage of 8V to all power IOs and inject 200mA of current on each signal IO. The test results show that the anti-latch-up level of the chip is 200mA.

Table 5-5 LKS32MC08x IO absolute characteristics

Parameter	Description	Min.	Max.	Unit
$V_{IN-GPIO}$	GPIO Signal Input Voltage Range	-0.3	6.0	V
I_{INJ_PAD}	Maximum Injection Current of a Single GPIO	-11.2	11.2	mA

I_{INJ_SUM}	Maximum Injection Current of All GPIOs	-50	50	mA

Table 5-6 LKS32MC08x IO DC Parameters

Parameter	Description		AVDD	Conditions	Min.		Max.	Unit
V_{IH}	High input level of digital IO		5V	-	0.7*AVDD			V
			3.3V		2.0			
V_{IL}	Low input level of digital IO		5V	-			0.3*AVDD	V
			3.3V				0.8	
V_{HYS}	Schmidt hysteresis range		5V	-	0.1*AVDD			V
			3.3V					
I_{IH}	Digital IO current consumption when input is high		5V	-			1	uA
			3.3V					
I_{IL}	Digital IO current consumption when input is low		5V	-	-1			uA
			3.3V					
V_{OH}	High output level of digital IO			Current = 11.2mA	AVDD-0.8			V
V_{OL}	Low output level of digital IO			Current = 11.2mA			0.5	V
R_{pup}	Pull-up resistor*	Reset pin			100	200	400	kΩ
		Normal pin			8	10	12	
$R_{io\text{-}ana}$	Connection resistance between IO and internal analog circuit				100		200	Ω
C_{IN}	Digital IO Input-capacitance		5V	-			10	pF
			3.3V					

* Only some IOs have built-in pull-up resistors, see section “Pin Function Description” for details.

Table 5-7 LKS32MC08x Module Current/IDD

模块	Min	Typ	Max	单位
Comparator x1		0.005		mA
OPA x1		0.450		mA
ADC		3.710		mA
DAC		0.710		mA
Temp Sensor		0.150		mA
Band-Gap		0.154		mA
4MHz RC Clock		0.105		mA

PLL		0.080		mA
CPU+flash+SRAM (96MHz)		8.667		mA
CPU+flash+SRAM (12MHz)		1.600		mA
CRC		0.070		mA
DSP		3.421		mA
UART		0.107		mA
DMA		1.340		mA
MCPWM		0.053		mA
TIMER		0.269		mA
SPI		0.500		mA
IIC		0.500		mA
CAN		2.200		mA
Sleep Mode	10	30	50	uA

All the test results above are based on the chips running 96MHz at room temperature with 5V as power supply. Device charactoristics may vary due to process accuracy.

6 Analog Characteristics

The analog characteristics of integrated 6N Driver for LKS32MC086/084D are shown in the following table. Take the LKS32MC080R8T8 as an example.

Table 6-1 LKS32MC08x analog characteristics

Parameter	Min.	Normal	Max.	Unit	Description
Analog-to-Digital Converter (ADC)					
Power Supply	2.8	5	5.5	V	ADC use 2.4V internal reference
	3.3	5	5.5	V	ADC use 1.2V internal reference
Sampling rate		3		MHz	$f_{adc}/16$
Differential Input Signal Range	-REF		+REF	V	When Gain=1; REF=2.4V
	-3.6		+3.6	V	When Gain=2/3; REF=2.4V
Single-ended Input Signal Range	-0.3		AVDD+0.3	V	Limited by the input voltage of the IO port
DC offset		5	10	mV	Correctable
Effective number of bits (ENOB)	10.5	11		bit	
INL		2	3	LSB	
DNL		1	2	LSB	
SNR	63	66		dB	
Input Resistance	100k			Ohm	
Input Capacitance		10pF		F	
Reference Voltage (REF)					
Power Supply	2.2	5	5.5	V	
Output Deviation	-9		9	mV	
Rejection Ratio of Power Supply		70		dB	
Temperature Coefficient		20		ppm /°C	
Output Voltage		1.2		V	
Digital-to-Analog Converter (DAC)					
Power Supply	2.2	5	5.5	V	
Load Resistance	5k			Ohm	Output BUFFER is on
Load capacitance			50p	F	
Output voltage range	0.05		AVDD-0.1	V	
Conversion speed			1M	Hz	
DNL		1	2	LSB	
INL		2	4	LSB	
OFFSET		5	10	mV	
SNR	57	60	66	dB	
Operational Amplifier (OPA)					
Power Supply	2.8	5	5.5	V	

Parameter	Min.	Normal	Max.	Unit	Description
Bandwidth		10M	20M	Hz	
Load Resistance	20k			Ohm	
Load Capacitance			5p	F	
Input Common Mode Voltage Range (VICM)	0		AVDD	V	
Output Signal Range	0		2*Vcm	V	Under minimum load resistance
OFFSET		10	15	mV	This OFFSET is the equivalent differential input deviation obtained when the OPA differential input is short-circuited and OPA OUT is measured from 0 level. The output deviation of OPA is the OPA magnification xOFFSET
Common Mode Voltage (Vcm)	1.65	1.9	2.2	V	Measurement condition: normal temperature. Operational amplifier swing=2 × min(AVDD-Vcm, Vcm). It is recommended that the application using OPA single output should be powered on to measure Vcm and make software subtraction correction. For more analysis, please refer to the official website application note "ANN009 - Differences between Operational Amplifier Differential and Single Operating Mode".
Common Mode Rejection Ratio (CMRR)		80		dB	
Power Supply Rejection Ratio (PSRR)		80		dB	
Load Current			500	uA	
Slew Rate		5		V/us	
Phase Margin (PM)		60		Degree	
Comparator (CMP)					
Power Supply	2.2	5	5.5	V	
Input Signal Range	0		AVDD	V	
OFFSET		5	10	mV	
Delay		0.15u		S	Default power consumption
		0.6u		S	Low power consumption
Hysteresis		20		mV	HYS='0'

Parameter	Min.	Normal	Max.	Unit	Description
		0		mV	HYS='1'

Description of Analog Register Table:

Address space of 0x40000040 to 0x40000050 are the calibration registers of each analog module. These registers will be set to a unique calibration value in factory. Generally, users are advised not to configure or change these values. If fine-tuning is required, please read the original settings first, and then adjust based on those values.

Addresses space of 0x40000020 to 0x4000003c are registers open to users. The blank registers must be configured to 0 (these registers will be reset to 0 after power on). Other registers could be configured in situations.

7 Power Management System

The power management system is composed of LDO15 module, power detection module (PVD), power-on/power-off reset module (POR).

AVDD is powered by a 2.2V ~ 5.5V supply(The B-version chip is powered by 3.0V~5.5V), and all internal digital circuits and PLL modules are powered by an internal LDO15.

The LDO15 is automatically turned on after power-on. No software configuration is necessary.

LDO15 has been calibrated before it leaves the factory. Generally, users do not need to configure these registers again.

The POR module monitors the voltage of the LDO15. When the voltage of the LDO15 is lower than 1.1V, for example, at the beginning of power-on or at the time of power-off, it will provide a reset signal for the digital circuit to avoid any abnormal operation.

The PVD module monitors the 5V input power. If it is below a certain threshold, it will remind the MCU by sending an alarm (interrupt) signal. The interrupt reminder threshold can be set to different voltages through the PVDSEL<1:0> registers. The PVD module can be turned off by setting PD_PDT = '1'. For the corresponding value of specific register, please refer to the analog register table.

8 Clock System

The clock system consists of a 32KHz RC oscillator, a 4MHz RC oscillator, an external 4MHz crystal oscillator, and a PLL.

The 32K RC clock is used in the MCU system as a slow clock for modules such as reset/wakeup source filters or used in the low power mode; The 4MHz RC clock can be used as the main clock of the MCU, and can provide a reference clock to PLL. PLL clock is up to 96MHz; The external 4MHz crystal oscillator is used as a backup clock.

Both 32k and 4M RC clocks have been calibrated. In the range of -40~105 ℃, the accuracy of the 32K RC clock is ± 50%, and the accuracy of the 4M RC clock is ± 1%.

The 4M RC clock is turned on by setting RCHPD = ’0’ (ON by default, turn off when set to “1’). The RC clock needs a reference voltage and current provided by the Bandgap voltage reference module; thus, do remember to turn on the BGP module before turning on the RC clock. When the chip is powered on, the 4M RC clock and BGP module are both turned on automatically. The 32K RC clock is always on and cannot be turned off.

The PLL multiplies the 4M RC clock to provide a higher frequency clock for modules like MCU and ADC. The highest frequency of MCU and PWM module is 96MHz, and the typical working frequency of ADC module is 48MHz. It can be set to different frequency by the register ADCLKSEL <1:0>.

PLL is turned on by setting PLLPDN = ’1’ (OFF by default, turn on when set to '1'). Before turning on the PLL module, the BGP (Bandgap) module should be turned on first. After the PLL is turned on, it needs a settling time of 6us to achieve a stable frequency output. When the chip is powered on, the RCH clock and BGP module are both turned on. PLL is OFF by default and could be enabled by software.

The crystal oscillator circuit has a built-in amplifier and an oscillator capacitor. Connect a crystal between IO OSC_IN/OSC_OUT and set XTALPDN = ’1’ to start the oscillation.

9 Reference Voltage

Reference voltage and current are provided for ADC, DAC, RC clock, PLL, temperature sensor, operational amplifier, comparator and FLASH. Before using any of the above modules, the BGP voltage reference should be turned on first.

When the chip is powered on, the BGP module is turned on automatically. The voltage reference is turned on by setting BGPPD = '0'. From OFF to ON, BGP needs about 2us to stabilize. BGP output voltage is about 1.2V, and accuracy is ± 0.8%

10 Analog Digital Converter

The chip integrated a synchronous double-sampling SAR ADC which is shut down by default when the chip is powered up. Before turning on ADC, the BGP module, 4M RC clock and PLL should be turned on first. In the default configuration, ADC clock is 48MHz, which corresponds to a conversion rate of 3Msps.

The synchronous double sampling circuit can sample the two input analog signals at the same time. After the sampling is completed, the ADC converts the two signals one by one and writes them into the corresponding data registers.

ADC takes 16 ADC clock cycles to complete one conversion, of which 13 are conversion cycles and 3 are sampling cycles. I.E. $f_{conv}=f_{adc}/16$. When the ADC clock is set to 48MHz, the conversion rate is 3Msps.

When the ADC is working at a lower frequency, the power consumption can be reduced by setting register CURRIT<1:0>.

ADC could work in different modes: One-time single channel trigger mode, continuous single channel sampling mode, One-time 1 to 20 channels scanning mode, continuous 1 to 20 channels scanning mode. It has a set of 20 independent registers for each analog channel.

The ADC trigger can be MCPWM/Timer trigger signals T0, T1, T2 and T3 happened for the preset number of times, or software trigger event.

Among the 20 analog channels, the 19th channel is analog ground and is used to measure the offset of the ADC. The ADC values of other channels will be automatically subtracted by this offset. The offset is calibrated in factory and store in flash. Each time the chip is powered up, this offset will be loaded into ADC_DC register automatically. If the user needs to improve the offset over the whole temperature, it can be recalculated time by time (for example, each hour) when the ADC is idle.

When GAIN_REF = 0, the ADC voltage reference is 2.4V. The ADC has two gain modes, which are set by GAIN_SHAx, corresponding to 1x and 2/3 x gain setting; 1x gain corresponds to an input signal range of ± 2.4V, and 2/3 gain corresponds to an input signal range of ± 3.6V. When measuring the output signal of the OPA, select the specific ADC gain according to the maximum signal that the OPA may output.

11 Operational Amplifier

4-channel of rail-to-rail OPAs (3 channels for 084D) are integrated, with a built-in feedback resistor R2/R1. A resistor R0 is required to be connected in series to the external pin. The resistance of feedback resistors R2:R1 can be adjusted by register RES_OPA0<1:0> to achieve different gain. For the corresponding value of specific register, please refer to the analog register table.

The close-loop gain of OPA is R2/(R1+R0), where R0 is the resistance of the external resistor.

For the application of MOS resistance direct sampling, it is recommended to connect an external resistance of >20kΩ to reduce the current flowing into the chip pin when the MOS is turned off;

For the application of small resistance sampling, it is recommended to connect an external resistor of 100Ω.

The OPA can select one of the output signals of the 4-channels amplifiers by setting OPAOUT_EN <2:0>, and send it to the P2.7 IO port through a buffer for measurement (see the corresponding relationship in the datasheet 'Pin Function Description'). Because of this buffer, the OPA is able to be output to an IO while operating normally.

When the chip is powered on, the OPA module is OFF by default. It can be turned on by setting OPAxPDN = '1', and turn on the BGP module before turning on the amplifier.

For built-in clamp diodes are integrated between the positive and negative OPA inputs, the motor phase line could be directly connected to the OPA input through a matching resistor, thereby simplifying the external circuit for MOSFET current sampling.

12 Comparator

Built-in 2-channel rail-to-rail comparators with programmable comparator speed, hysteresis voltage, and signal source.

The comparison delay can be set to 0.15uS/0.6uS by register IT_CMP. and the hysteresis voltage can be set to 20mV/0mV by CMP_HYS.

The signal sources of the positive and negative inputs can be programmed by register CMP_SELP<2:0> and CMP_SELN<1:0>. For details, please refer to the analog register description.

When the chip is powered on, the comparator module is OFF by default. The comparator is turned on by setting CMPxPDN = ’1’, and turn on the BGP module before turning on the comparator.

13 Temperature Sensor

The chip has a temperature sensor with an accuracy of ±2°C in -40~85℃ and ±3°C in -40~105℃ typically. The temperature sensor will be calibrated in factory, and the calibration value is saved in the flash info area.

When the chip is powered on, the temperature sensor module is OFF by default. Turn on the BGP module before turning on the temperature sensor.

The temperature sensor is turned on by setting TMPPDN = '1', and it takes about 2us to be stable after turning on. Thus, it should be turned on at least 2us ahead before the ADC measures the sensor output.

14 Digital Analog Converter

The chip has a 1-channel 12bit DAC, the maximum range of the output signal can be set to 1.2V/3V/4.85V through the register DAC_GAIN <1:0>.

The 12bit DAC can be output via IO port P0.0 by setting register DACOUT_EN = 1, which can drive a load resistance of over 5kΩ and a load capacitance of 50pF.

The maximum output data rate of the DAC is 1Msps.

When the chip is powered on, the DAC module is OFF by default. DAC can be turned on by setting DAC12BPDN = 1. Turn on the BGP module before turning on the DAC module.

15 Processor

- 32-bit Cortex-M0 + DSP dual-core processor
- Two-wire SWD debug pin
- System frequency up to 96MHz

16 Storage

16.1 Flash

- built-in flash including 32kB/64kB main area and 1kB NVR
- Endurance: 20,000 Cycles(min)
- Data retention: more than 100 years
- Single byte program: 7.5us(max), Sector erase: 5ms(max)
- Sector size 512bytes, supporting Sector erase/program and in-application program, erase/program one sector while accessing another
- Flash data anti-theft by programming the last word of flash to any words other than 0xFFFFFFFF

16.2 SRAM

- built-in 8kB SRAM

17 Motor Control PWM

- MCPWM operating frequency is up to 96MHz
- Supports up to 4 channels of complementary PWM output with adjustable phase
- The width of dead-zone in each channel can be configured independently
- Support edge-aligned PWM
- Support software control IO mode
- Support IO polarity control
- Internal short circuit protection to avoid short circuit due to configuration error
- External short circuit protection, enabling fast shutdown by monitoring the external signals
- Internal ADC sampling interrupt
- Preload MCPWM register configuration and update simutaneously
- Programmable load time and period

18 Timer

- 4-channel standard timer, 2-channel 16-bit timer, 2-channel 32-bit timer.
- Support capture mode for measuring external signal/pulse width
- Support comparison mode for timed interruption of edge-aligned PWM

19 Hall Sensor Interface

- Built-in 1024 cycles filtering
- 3-channel Hall signal input
- 24-bit counter, with overflow and capture interrupt

20 DSP

- Customized DSP instruction set for motor control algorithm, , three-stage pipeline achitecture
- Operating frequency is up to 96MHz
- 32/16-bit divider, could finish one division calculation in 10 cycles
- 32-bit hardware SQRT, could finish one SQRT calculation in 8 cycles
- Q15 format Cordic trigonometric function module, could finish sin/cos/artanc calculation in 8 cycles
- DSP has independent program memory and data memory, DSP could execute its program independently, and can also be called by MCU to perform a certain calculation as a AHB slave like a coprocessor
- Support DSP IRQ and pause state for data exchange purpose with MCU

21 General Peripherals

- Two UART, full-duplex operation, support 7/8 data bit, 1/2 stop bit, odd/even/no parity mode, with 1 byte tx buffer, 1 byte rx buffer, support Multi-drop Slave/Master mode, support 300 to 115200 baud rate
- One SPI, support master-slave mode
- One IIC, support master-slave mode
- One CAN-bus (084D without CAN)
- Hardware watchdog, driven by 32kHz RC clock and which is independent of system high-speed clock, with write protection and 2/4/8/64 seconds reset interval.

22 Special IO Multiplexing

Notes for Special IO Multiplexing of LKS08x

The SWD protocol includes two signals: SWCLK and SWDIO. SWCLK is a clock signal. To the chip, it is an input and will always be an input. SWDIO is a data signal. It switches between the input state and the output state during data transmission, and the default is the input state.

Users could use two IOs of SWD as GPIOs P0.0/P2.15. The precautions are as follows:

- The default state of GPIO multiplexing is disabled, IO are used as SWD. After the hard reset of the chip, the initial state of IOs are SWD. Both IOs of SWD are fixed pull-up inside the chip (the internal pull-up resistor of the chip is about 10K). Please pay attention to the initial IO voltage level if application has specific requirements.
- When GPIO multiplexing is enabled, tools such as KEIL cannot directly access the chip, i.e., the Debug and erase download functions cannot access the chip since SWD are now general GPIO. If the program needs to be downloaded again, there are two solutions.
- Firstly, it is recommended to use Linko's dedicated offline downloader to erase. It is recommended to leave a certain margin before switching SWD to GPIO, such as about 100ms, to ensure that the offline downloader can erase the chip and prevent the deadlock. This margin is to ensure a successful offline downloader erasing. A greater margin means a greater probability of the successful one-time erasion.
- Secondly, the application should have a GPIO multiplexing exit mechanism. For example, some other IO invert (usually input), indicates that the SWDIO is required externally, and the software needs to be reconfigured to disable the multiplexing. At this moment, the KEIL function can access the chip via SWD again.

In SSOP24 package and QFN40 package, SWDIO is directly bonded with P0.0 and P2.15, and the corresponding GPIO can be directly enabled. It is recommended that SWDCLK keep unchanged (constant 1 or constant 0) when multiplexing SWDIO

For LKS087E, SWDCLK is bonded with P2.6 and the corresponding GPIO can be directly enabled. If SWDIO and SWDCLK are multiplexed at the same time, considerations for SWDCLK multiplexing are as follows:

- The default state of GPIO multiplexing is disabled, IO are used as SWD. After the hard reset of the chip, the initial state of IOs are SWD. Both IOs of SWD are fixed pull-up inside the chip (the internal pull-up resistor of the chip is about 10K). Please pay attention to the initial IO voltage level if application has specific requirements.
- When GPIO multiplexing is enabled, tools such as KEIL cannot directly access the chip, i.e., the Debug and erase download functions cannot access the chip since SWD are now general GPIO. If the program needs to be downloaded again, there are two solutions.
- Firstly, it is recommended to use Linko's dedicated offline downloader to erase. It is recommended to leave a certain margin before switching SWD to GPIO, such as about 100ms, to ensure that the offline downloader can erase the chip and prevent the deadlock. This margin is to ensure a successful offline downloader erasing. A greater margin means a greater probability of

the successful one-time erasion.

- Secondly, the application should have a GPIO multiplexing exit mechanism. For example, some other IO invert (usually input), indicates that the SWDIO is required externally, and the software needs to be reconfigured to disable the multiplexing. At this moment, the KEIL function can access the chip via SWD again.

When SWDCLK and SWDIO pins are used as GPIO, they should not act at the same time. That is, when SWDCLK multiplexing is enabled and changes, SWDIO can remain at level 0 (similar to time division multiplexing).

For RSTN signal, the default is for the external reset pin of LKS08x chip.

LKS08x allow users to multiplex RSTN as other IOs, and the multiplexed IO is P0.2. The precautions are as follows:

- The default state of reset IO multiplexing is disabled, and the software needs to write 1 to SYS_RST_CFG[5] to multiplex RSTN as GPIO. I.e., the initial state of P0[2] is RSTN. RSTN is provided with a pull-up resistor inside the chip (the internal pull-up resistor of the chip is about 100K). Attention shall be paid when the application has requirements for initial electric level.
- The default state of P0[2] is used as external reset, and the program can only be executed after the RSTN is released. The application needs to ensure that the RSTN has sufficient protection, such as the peripheral circuit with a pull-up resistor. It is better to add a capacitor.
- After RST IO multiplexing is enabled, the external reset is unavailable to the chip. If a hard reset is required, the reset source can only be power-down/watchdog reset.
- The multiplexing of RSTN does not affect the use of KEIL.

23 Ordering Information

Device	Package Size	Quantity per disc/tube	Quantity in box	Quantity in case
LKS32MC080R8T8(B)	LQFP64	160/disc	1600PCS	9600PCS
LKS32MC081C8T8(B)	TQFP48	250/disc	2500PCS	15000PCS
LKS32MC082K8Q8(B)	QFN5*5 32L-0.75	490/disc	4900PCS	29400PCS
LKS32MC083C8T8(B)	TQFP48	250/disc	2500PCS	15000PCS
LKS32MC087M6S8(B)	SSOP24L	4000/disc	8000PCS	64000PCS
LKS32MC087AM6S8(B)	SSOP24L	4000/disc	8000PCS	64000PCS
LKS32MC087CM8S8(B)	SSOP24L	4000/disc	8000PCS	64000PCS
LKS32MC088C6T8(B)	TQFP48	250/disc	2500PCS	15000PCS

24 Version History

Table 24-1 Document's Version History

Date	Version No.	Description
2024.01.26	1.83	Modified device Selection Guide
2023.12.12	1.82	Added description of pull-up resistance values
2023.11.20	1.81	Modified LKS32MC080R8T8 P1.12、P1.15 PIN Assignment
2023.11.09	1.80	OPA OFFSET Adds the description, Renewal storage temperature
2023.06.04	1.79	Modify pin multiplex function of P3.13、P1.12 and P1.15
2023.04.28	1.78	Add B-version chip with AVDD power supply range of 3.0-5.5V Modify package name
2023.03.23	1.77	Adjust AVDD range from 2.2~5.5 to 3.0~5.5V
2023.03.18	1.76	Modified the description of clock accuracy
2023.01.13	1.75	Add ordering information
2022.11.15	1.74	Revise special IO multiplexing
2022.11.07	1.73	Add connection resistance between IO and internal analog circuit
2022.10.28	1.72	Add characteristic of common mode voltage
2022.09.21	1.71	Add CAN function in pin table for 083 Pin14/15/44/45
2021.05.17	1.7	Add LKS32AT085C8Q9
2021.04.13	1.6	Device selection guide
2020.03.20	1.5	English version minor revision
2020.03.19	1.4	English version minor revision
2019.12.10	1.3	Add 087A difference from 087
2019.09.05	1.2	Minor revision
2019.07.18	1.1	Revise 082's definition
2019.03.10	1.0	Initial version

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