Linko Semiconductor Co., Ltd.

LKS32MC45x Datasheet

1 Overview

1.1 Function Description

LKS32MC45x series MCU is a 32-bit core processor dedicated for motor control applications. It integrates most of the modules needed for common motor control systems.

- **Features**
  - 192MHz 32-bit CortexM4F core
  - Rich DSP instructions
  - Hardware floating point unit
  - MPU (Memory Protection Unit)
  - Supporting trigonometric functions, square root and other operations
  - 14bit SAR ADC, with the sampling rate up to 2MHz, and supporting sampling of three signal channels simultaneously. Supporting up to 27 channels of IO ADC input signals, 6 channels of OPA signals and internal temperature sensor
  - Ultra-low power sleep mode, with sleep current of 10uA
  - Working environment temperature range: - 40~105°C;
  - Supporting dual-motor + PFC control
  - Super ESD and group pulse ability
- **Memory**
  - 256kB built-in Flash with encryption protection
  - Supporting 0-8 MB with external SPI Flash
  - 40kB SRAM, supporting dividing 8/16/24 kB for use as Code RAM
- **Operating Conditions**
  - 2.2V-3.6V single power supply, Some devices support 5V single power supply
  - Working environment temperature range: -40~105°C;
- **Clock**
  - Built-in 12 MHz high-precision RC clock, with accuracy within ±1%, in the temperature range from -40°C~105°C
  - Built-in 32 kHz low-speed clock for low power mode
  - External crystal oscillator of 12-24 MHz
  - Internal PLL supporting up to 192 MHz clock
- **Peripheral module**
  - Three UARTs
  - One SPI, support master-slave mode
  - Two IIC, supporting master/salve mode
  - One CAN-bus. External crystal oscillator must be used as reference clock

- Three universal 16-bit Timers, supporting capturing and edge-aligned PWM
- Two universal 32-bit Timers, supporting capturing and edge-aligned PWM function;
- One 24-bit Systick timer
- Four encoder interfaces, supporting quadrature encoding input, CW/CCW input, pulse + sign input
- Two motor control dedicated PWM module, supporting 16 PWM outputs and independent dead zone control
- Two hall signal interfaces, supporting speed measurement and debouncing
- MAX 84 GPIO
- 2 hardware watchdogs, supporting high-speed clock and low-speed clock respectively

- **DMA**
  - One independent DMA engine
  - 8 channels
  - Supporting 8-bit, 16-bit and 32-bit transmission
  - Supporting transfer from peripherals to memory, memory to peripherals, and Flash to memory
- **Analog module**
  - 14-bit SAR ADC, supporting sampling of three signal channels simultaneously. Supporting up to 27 channels of IO ADC input signals, 6 channels of OPA signals and internal temperature sensor
  - ADC supporting synchronous 3-channel sample-and-hold, 2Msps sampling and conversion rate
  - Built-in six operational amplifiers. Differential PGA mode is available
  - Built-in six comparators. Hysteresis mode, windowing mode, filter mode, and trigger MCU interruption mode are available
  - Built-in two 12-bit digital-to-analog converter (DAC)
  - ±2°C built-in temperature sensor
  - 1.2V 0.5% built-in linear regulator
  - Power-On Reset (POR)
  - Power Voltage Detector (PVD), with three voltages optional
- **Functional safety module (Class C)**
  - ADC self-check module, supporting open circuit and short circuit check
  - One CRC module
- **Packaging**

  LQFP100, LQFP80, LQFP64 ,QFN52

1.2 Performance Advantages

- High reliability, high integration level, small package size, saving BOM cost;
- Integrated at most 6 channels high-speed OPAs and 6 channels comparators, meeting the needs of different system topology like single resistance/double resistance/three resistance current sampling;
- High-speed OPA is integrated with over-voltage protection circuit, which allows high-voltage common-mode signals to be input, which could support direct current sampling of MOSFET resistance with the simplest circuit topology.
- Integrated hardware MOSFET temperature drift compensation circuit to ensure current sampling accuracy;
- Via a proprietary technique, ADC and high-speed OPA could cooperate well, making them able to handle a wider current dynamic range, while ensuring the sampling precision of high-speed small current and low-speed hight current;
- The control circuit is simple and efficient, with strong anti-interference ability, stable and reliable;
- Single power supply ensures the universality of system power supply;
- Support IEC/UL60730 functional security certification;

Applicable to control systems such as inductive BLDC/non-inductive BLDC/inductive FOC/non-inductive FOC and stepper motors, permanent magnet synchronous and asynchronous motors.

1.3 Naming Rules

LKS32 MC 451 V C T 8 YYWWX

Device series

LKS32	= 32bit MCU

Product type

MC	= Motor Control Applications
AT	= Automobile Applications

Device sub family

451,453,	= 2.2~3.6V, 3 ADC, 6 PGA
455,454	= 2.2~3.6V, 3 ADC, 4 PGA
452	= 2.2~3.6V, 3 ADC, 4 PGA, 6N Driver
451L,455L,457L	= 5V to 3.3V LDO

Pin count

L	= 16 pins
H	= 20 pins
M	= 24 pins
K	= 32 pins
F	= 40 pins
C	= 48 pins
N	= 52 pins
R	= 64 pins
P	= 80 pins
V	=100 pins
Z	=144 pins

Code size

4	= 16Kbyte Flash Memory
6	= 32Kbyte Flash Memory
8	= 64Kbyte Flash Memory
B	=128Kbyte Flash Memory
C	=256Kbyte Flash Memory
D	=384Kbyte Flash Memory
E	=512Kbyte Flash Memory

Package

P	= TSSOP
T	= TQFP/LQFP
Q	= QFN
S	= SSOP
H	= BGA

Temperature range

6	= -40~85°
8	= -40~105°
9	= -40~125°

Options

YYWW	= DateCode
X	= Version

Figure 1-1 Linko's device naming rules

1.4 System Resource Block Diagram

LKS32MC451VCT8 is used as an example here. For details of hardware resources of other models, please refer to the selection table.

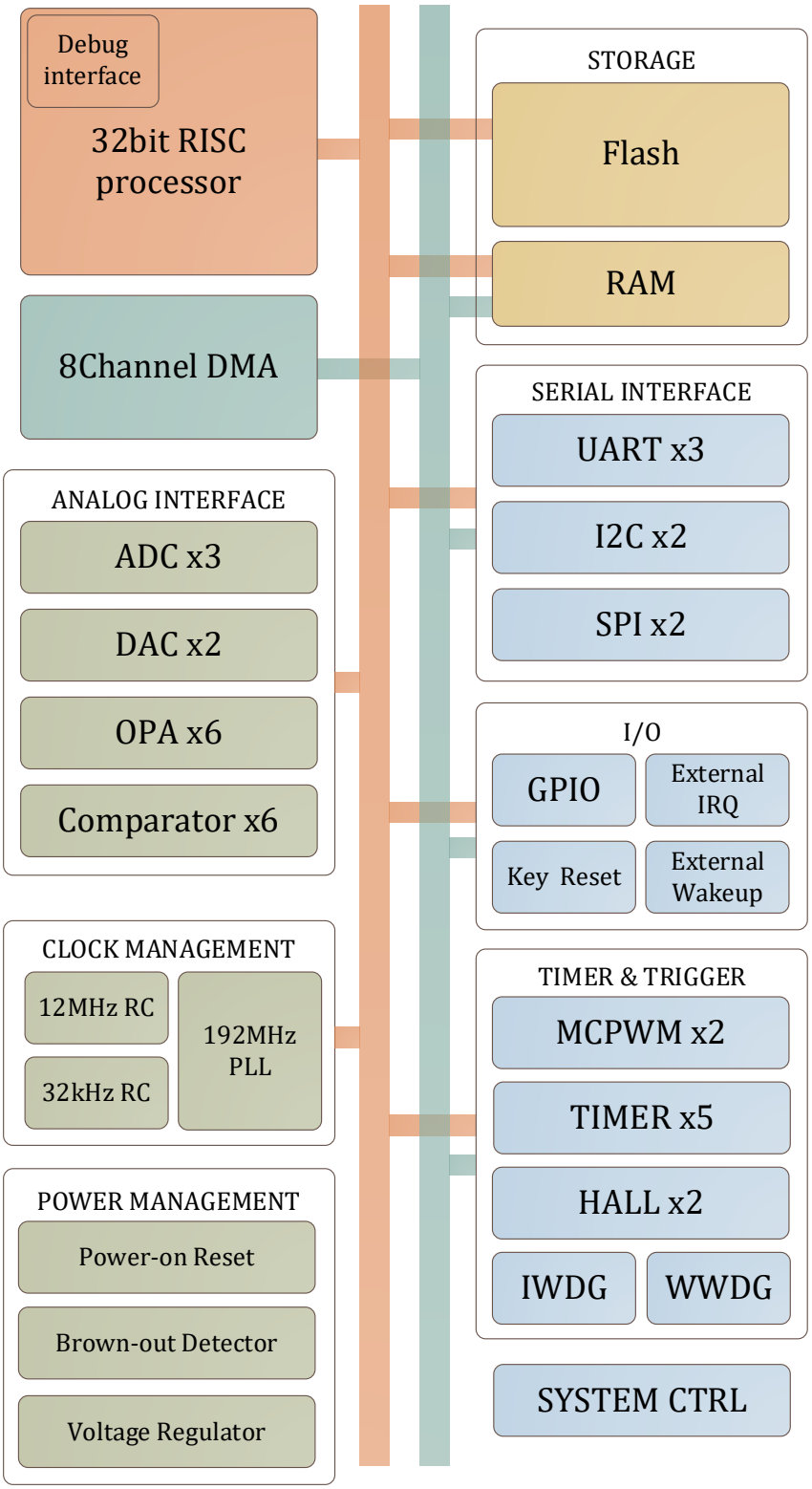

Figure 1-2 LKS32MC451VCT8 system resource block diagram

1.5 Vector Sinusoidal Control System

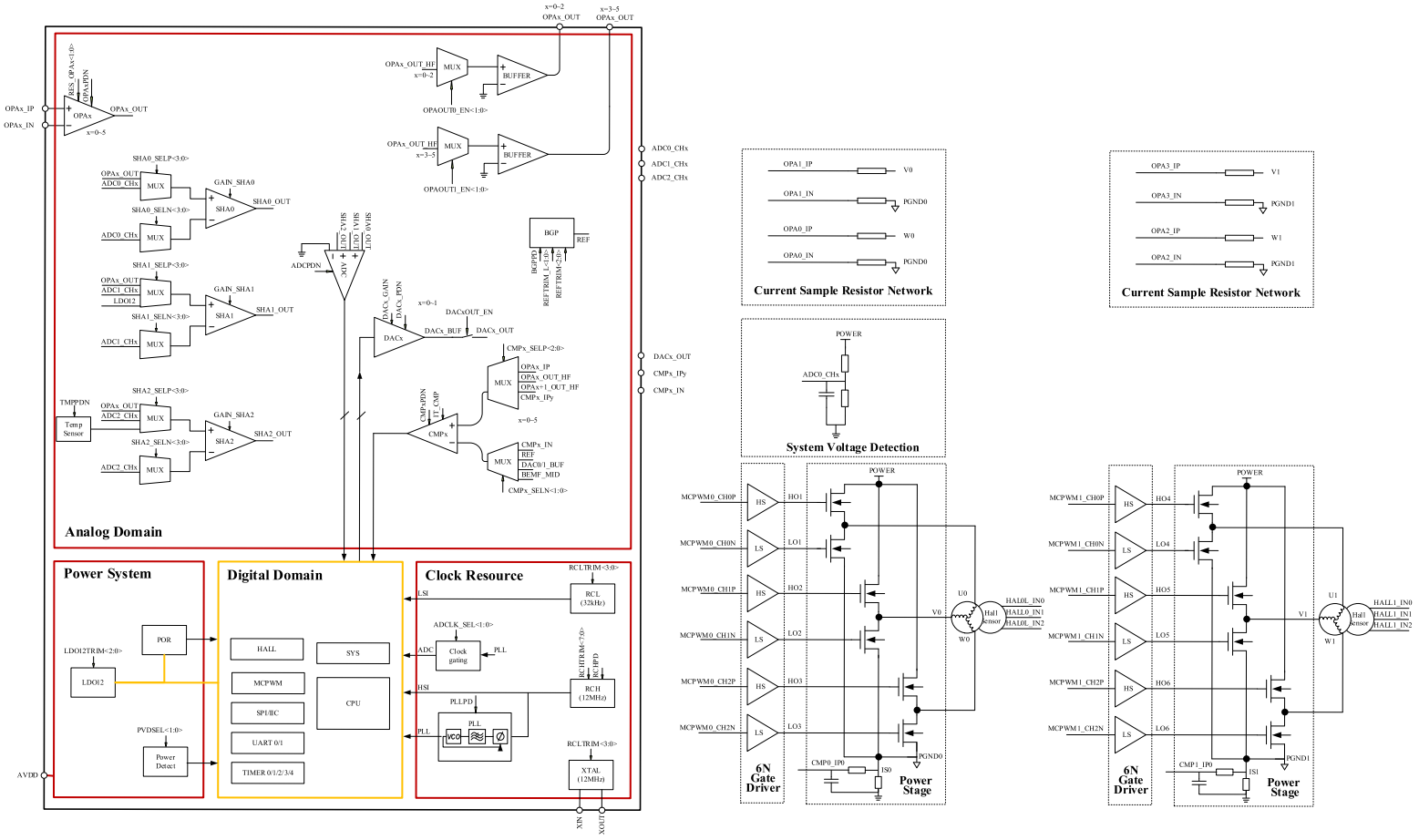

Figure 1-3 Simplified schematic diagram of vector sinusoidal control system

2 Device Selection Table

Table 2-1 Selection table of LKS32MC45x series devices

	Main frequency (MHz)	Flash (kB)	RAM (kB)	ADC	Number of ADC channels	DAC	HALL	MCPWM	Comparator (CMP)	Number of comparator channels	OPA	TIMER	SPI	IIC	UART	CAN	Temp. Sensor	PLL	QEP	Others	Package
LKS32MC451VCT8	192	256	40	14bit, 2Msps×3	27	12bit×2	3Phase×2	4Pair×2	6	24	6	5	2	2	3	1	Yes	Yes	4		LQFP100
LKS32MC451LVCT8	192	256	40		27	12bit×2	3Phase×2	4Pair×2	6	24	6	5	2	2	3	1	Yes	Yes	4	5V AVDD	LQFP100
LKS32MC453RCT8	192	256	40		18	12bit×2	3Phase×2	4Pair×2	6	20	6	5	2	2	3	1	Yes	Yes	4		LQFP64
LKS32MC454CCT8	192	256	40		20	12bit×2	3Phase×2	4Pair×2	6	15	4	5	2	2	3	0	Yes	Yes	4		TQFP48
LKS32MC454NCQ8	192	256	40		15	12bit×2	3Phase×2	4Pair×2	6	15	6	5	2	2	3	1	Yes	Yes	4		QFN52
LKS32MC455RCT8	192	256	40		21	12bit×2	3Phase×2	4Pair×2	6	18	4	5	2	2	3	1	Yes	Yes	4		LQFP64
LKS32MC455LRCT8	192	256	40		22	12bit×2	3Phase×2	4Pair×2	6	19	4	5	2	2	3	1	Yes	Yes	4	5V AVDD	LQFP64
LKS32MC457LRCT8	192	256	40		20	12bit×2	3Phase×2	4Pair×2	6	17	1	5	2	2	3	1	Yes	Yes	4	5V AVDD	LQFP64

3 Pin Assignment

3.1 Pin Assignment and Pin Function Description

The 5VT pin is compatible with 5V input level, allowing input of 5V level signal, but the maximum output signal is still 3.3V.

3.1.1 LKS32MC451VCT8

Figure 3-1 LKS32MC451VCT8 Pin Assignment

3.1.2 LKS32MC451LVCT8

Figure 3-2 LKS32MC451LVCT8 Pin Assignment

3.1.3 LKS32MC453RCT8

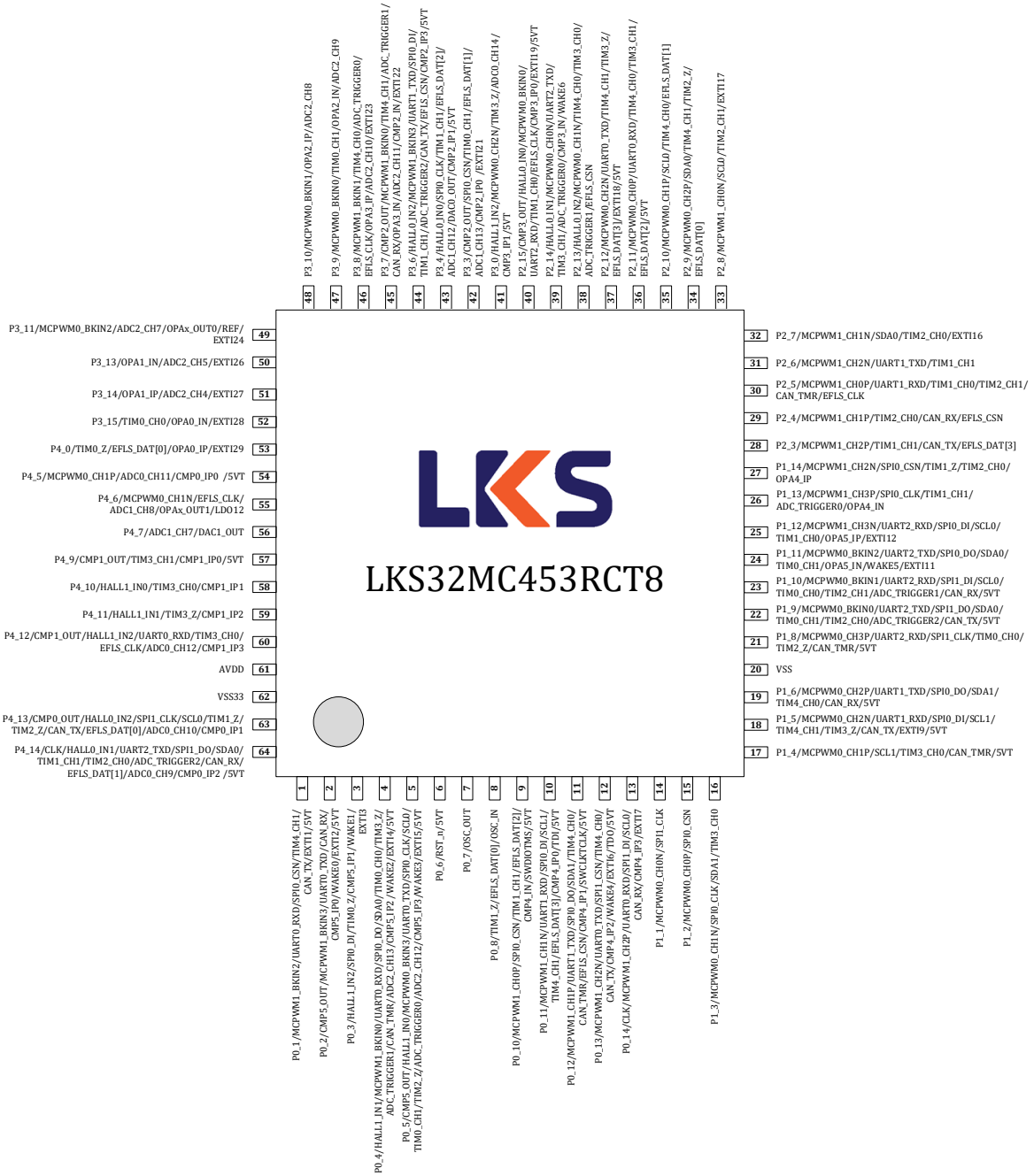

Figure 3-3 LKS32MC453RCT8 Pin Assignment

3.1.4 LKS32MC454CCT8

Figure 3-4 LKS32MC454CCT8 Pin Assignment

3.1.5 LKS32MC454NCQ8

Figure 3-5 LKS32MC454NCQ8 Pin Assignment

3.1.6 LKS32MC455RCT8

Figure 3-6 LKS32MC455RCT8 Pin Assignment

3.1.7 LKS32MC455LRCT8

Figure 3-7 LKS32MC455RCT8 Pin Assignment

3.1.8 LKS32MC457RCT8

Figure 3-8 LKS32MC457RCT8 Pin Assignment

3.1.9 LKS32MC457LRCT8

Figure 3-9 LKS32MC457LRCT8 Pin Assignment

3.2 Pin Description

Table 3-1 LKS32MC45x Pin Description

No.	Pin									Name	Type	Function Description
	451	451L	453	454(48)	454(52)	455	455L	457	457L			
1	1	1								P0_0	IO	P0.0
2	2	2	1		1	1	1	1	1	P0_1/MCPWM1_BKIN2/UART0_RXD/SPI0_CSN/TIM4_CH1/CAN_TX	IO	P0.1/PWM1 stop signal 2/serial port 0 receive/SPI0 chip selection/Timer4 channel 1/CAN send
3	3	3								P5_2	IO	P5.2
4	4	4	2		2	2	2	2	2	P0_2/CMP5_OUT/MCPWM1_BKIN3/UART0_TXD/CAN_RX/CMP5_IP0	IO	P0.2/comparator 5 output/PWM1 stop signal 3/serial port 0 send/CAN receive/comparator 5 positive input 0
5	5									NC		Floating, no connection
						3				VDD	PWR	1.2V digital power, generated by the chip's internal LDO, can be floating or connect with external filter capacitor
		5					3		3	AVDD	PWR	The output of 5V to 3.3V LDO requires external 10uF + 0.1uF capacitor
6	6	6								P5_3	IO	P5.3
7	7	7	3					4	4	P0_3/HALL1_IN2/SPI0_DI/TIM0_Z/CMP5_IP1	IO	P0.3/Hall 1 input signal 2/SPI0 input/Timer0 Z-axis signal/comparator 5 positive input 1
8	8	8	4		3			5	5	P0_4/HALL1_IN1/MCPWM1_BKIN0/UART0_RXD/SPI0_DO/SDA0/TIM0_CH0/TIM3_Z/ADC_TRIGGER1/CAN_TMR/ADC2_CH13/CMP5_IP2	IO	P0.4/Hall 1 input signal 1/PWM1 stop signal 0/serial port 0 receive/SPI0 output/I2C0 data signal/Timer0 channel 0/Timer3 Z-axis signal/ADC trigger debugging signal 1/CAN external timestamp clock/ADC2 channel 13/comparator 5 positive input 2
9	9	9	5		4	11	11	21	21	P0_5/CMP5_OUT/HALL1_IN0/MCPWM0_BKIN3/UART0_TXD/SPI0_CLK/SCL0/TIM0_CH1/TIM2_Z/ADC_TRIGGER0/ADC2_CH1	IO	P0.5/comparator 5 output/Hall 1 input signal 0/PWM1 stop signal 1/serial port 0 send/SPI0 clock/I2C clock signal/Timer0

No.	Pin									Name	Type	Function Description
	451	451L	453	454(48)	454(52)	455	455L	457	457L			
										2/CMP5_IP3		channel 1/Timer2 Z-axis signal/ADC trigger debugging signal 0/ADC2 channel 12/comparator 5 positive input 3
10	10	10	6	1	5	6	6	6	6	P0_6/RSTn	IO	P0.6/external chip reset
11	11	11	7		6	7	7	7	7	P0_7/OSC_OUT	IO	P0.7/Oscillator output
12	12	12		2		8	8	8	8	VSS	GND	VSS
13	13	13	8		7	9	9	9	9	P0_8/TIM1_Z/EFLS_DAT[0]/OSC_IN	IO	P0.8/Timer1 Z-axis signal /external flash data 0/Oscillator input
14	14			3		10				AVDD	PWR	AVDD 3.3V power input
		14							10	NC		Floating, no connection
15	15	15					10	12	12	P0_9/CMP4_OUT/MCPWM1_CH0N/SPI0_CLK/TIM1_CH0/EFLS_DAT[1]/CMP5_IN/nTRST	IO	P0.9/comparator 4 output/PWM1 channel 0 low side/SPI 0 clock/Timer1 channel 0/external flash data 1/comparator 5 negative input /JTAG reset
16	16	16	9	4	8	4	4	13	13	P0_10/MCPWM1_CH0P/SPI0_CSN/TIM1_CH1/EFLS_DAT[2]/CMP4_IN/ SWDIOTMS	IO	P0.10/PWM1 channel 0 high side/SPI0 chip select/Timer1 channel 1/external flash data 2/comparator 4 negative input/SWD Data/JTAG TMS
17	17	17	10	5	9	5	5	14	14	P0_11/MCPWM1_CH1N/UART1_RXD/SPI0_DI/SCL1/TIM4_CH1/ EFLS_DAT[3]/CMP4_IP0/TDI	IO	P0.11/PWM1 channel 1 low side/serial port 1 receive/SPI0 input/I2C1 clock signal/Timer4 channel 1/external flash data 3/comparator 4 positive input 0/JTAG TDI
18	18	18	11	6	10	13	13	15	15	P0_12/MCPWM1_CH1P/UART1_TXD/SPI0_DO/SDA1/TIM4_CH0/ CAN_TMR/EFLS_CSN/CMP4_IP1/SWCLKTCLK	IO	P0.12/PWM1 channel 1 high side/serial port 1 send/SPI0 output/I2C1 data signal/Timer4 channel 0/CAN external timestamp clock /comparator 4 positive input 1/SWD Clock/JTAG TCLK
19	19	19	12	7	11	14	14	16	16	P0_13/MCPWM1_CH2N/UART0_TXD/SPI1_CSN/TIM4_CH0/CAN_TX/ CMP4_IP2/TDO	IO	P0.13/PWM1 channel 2 low side/serial port 0 send/SPI0 chip select/Timer4 channel 0/CAN send/comparator 4 positive input 2/JTAG TDO
20	20	20	13	8	12	15	15	17	17	P0_14/CLK/MCPWM1_CH2P/UART0_RXD/SPI1_DI/SCL0/CAN_	IO	P0.14/clock output/PWM1 channel 2 high side/serial port 0

No.	Pin									Name	Type	Function Description
	451	451L	453	454(48)	454(52)	455	455L	457	457L			
										RX/ CMP4_IP3		receive/SPI1 input/I2C0 clock signal/CAN receive/comparator 4 positive input 3
21	21	21						18	18	P0_15/CMP4_OUT/MCPWM1_CH3N/TIM1_Z	IO	P0.15/comparator 4 output/PWM1 channel 3 low side/Timer1 Z-axis signal
22	22	22		9		16	16	19	19	P1_0/MCPWM1_CH3P/UART0_TXD/SPI1_DO/SDA0/TIM0_Z	IO	P1.0/PWM1 channel 3 high side/serial port 0 send/SPI1 output/I2C0 data signal/Timer0 Z-axis signal
23	23	23	14							P1_1/MCPWM0_CH0N/SPI1_CLK	IO	P1.1/PWM0 channel 0 low side/SPI1 output
24	24	24	15		13					P1_2/MCPWM0_CH0P/SPI0_CSN	IO	P1.2/PWM0 channel 0 high side/SPI0 input
25	25	25	16							P1_3/MCPWM0_CH1N/SPI0_CLK/SDA1/TIM3_CH0	IO	P1.3/PWM0 channel 1 low side/SPI0 clock/I2C1 data signal/Timer3 channel 0
26	26	26	17		14					P1_4/MCPWM0_CH1P/SCL1/TIM3_CH0/CAN_TMR	IO	P1.4/PWM0 channel 1 high side/I2C1 clock signal/Timer3 channel 0/CAN external timestamp clock
27	27	27	18	10	15	17	17			P1_5/MCPWM0_CH2N/UART1_RXD/SPI0_DI/SCL1/TIM4_CH1/ TIM3_Z/CAN_TX	IO	P1.5/PWM0 channel 2 low side/serial port 1 receive/SPI0 input/I2C1 clock signal/Timer4 channel 1/Timer3 Z-axis signal/CAN send
28	28	28	19	11	16	18	18			P1_6/MCPWM0_CH2P/UART1_TXD/SPI0_DO/SDA1/TIM4_CH0 / CAN_RX	IO	P1.6/PWM0 channel 2 high side/serial port 1 send/SPI0 output/I2C1 data signal/Timer4 channel 0/CAN receive
29	29	29								NC		Floating, no connection
30	30	30								P1_7/MCPWM0_CH3N/SPI1_CSN	IO	P1.7/PWM0 channel 3 low side/SPI0 chip select
31	31	31	20		17			22	22	VSS	GND	VSS
32	32	32	21		18	12	12	23	23	P1_8/MCPWM0_CH3P/UART2_RXD/SPI1_CLK/TIM0_CH0/TIM2_Z/ CAN_TMR	IO	P1.8/PWM0 channel 3 high side/serial port 2 receive/SPI1 clock/Timer0 channel 0/Timer2 Z-axis signal/CAN external timestamp clock

No.	Pin									Name	Type	Function Description
	451	451L	453	454(48)	454(52)	455	455L	457	457L			
33	33	33	22	12	19	19	19	24	24	P1_9/MCPWM0_BKIN0/UART2_TXD/SPI1_DO/SDA0/TIM0_CH1/ TIM2_CH0/ADC_TRIGGER2/CAN_TX	IO	P1.9/PWM0 stop signal 0/serial port 2 send/SPI1 output/I2C0 data signal/Timer0 channel 1/Timer2 channel 0/ADC trigger debugging signal 2/CAN send
34	34	34	23	13	20	20	20	25	25	P1_10/MCPWM0_BKIN1/UART2_RXD/SPI1_DI/SCL0/TIM0_CH0/ TIM2_CH1/ADC_TRIGGER1/CAN_RX	IO	P 1.10/PWM0 stop signal 1/serial port 2 receive/SPI1 input/I2C0 clock signal/Timer0 channel 0/Timer2 channel 1/ADC trigger debugging signal 1/CAN receive
35	35	35	24	14	21	21	21	26	26	P1_11/MCPWM0_BKIN2/UART2_TXD/SPI0_DO/SDA0/TIM0_CH1/ OPA5_IN	IO	P1.11/PWM0 stop signal 2/serial port 2 send/SPI0 output/Timer0 channel 1/OPA 5 negative input
36	36	36	25	15	22	22	22			P1_12/MCPWM1_CH3N/UART2_RXD/SPI0_DI/SCL0/TIM1_CH0/ OPA5_IP	IO	P1.12/PWM1 channel 3 low side/serial port 2 receive/SPI0 input/I2C0 clock signal/Timer1 channel 0/OPA 5 positive input
37	37	37	26		23					P1_13/MCPWM1_CH3P/SPI0_CLK/TIM1_CH1/ADC_TRIGGER0/ OPA4_IN	IO	P1.13/PWM1 channel 3 high side/SPI0 clock/Timer1 channel 1/ADC trigger debugging signal 0/OPA 4 negative input
38	38	38	27		24					P1_14/MCPWM1_CH2N/SPI0_CSN/TIM1_Z/TIM2_CH0/OPA4_IP	IO	P1.14/PWM1 channel 2 low side/SPI0 chip select/Timer1 Z-axis signal/Timer2 channel 0/OPA 4 positive input
39	39	39								P1_15/MCPWM1_CH2P/TIM2_CH1/CAN_TMR	IO	P1.15/PWM1 channel 2 high side/Timer2 channel 1/CAN external timestamp clock
40	40	40								P2_0/MCPWM1_CH1N/TIM1_CH0/CAN_RX/EFLS_DAT[0]	IO	P2.0/PWM1 channel 1 low side/Timer1 channel 0/CAN receive/external flash data 0
41	41	41					23			P2_1/MCPWM1_CH1P/TIM1_CH0/ADC_TRIGGER0/CAN_TX/ EFLS_DAT[1]	IO	P2.10/PWM1 channel 1 high side/Timer1 channel 0/ADC trigger debugging signal 0/CAN send/external flash data 1
42	42					23				AVDD	PWR	AVDD 3.3V power input
		42								NC		Floating, no connection

No.	Pin									Name	Type	Function Description
	451	451L	453	454(48)	454(52)	455	455L	457	457L			
43	43	43				24	24			P2_2/MCPWM1_BKIN0/EFLS_DAT[2]	IO	P2.2/PWM1 channel 0 low side/external flash data 2
44	44	44				25	25			VSS33	GND	VSS33
45	45	45	28			26	26	27	27	P2_3/MCPWM1_CH2P/TIM1_CH1/CAN_TX/EFLS_DAT[3]	IO	P2.3/PWM1 channel 2 high side/Timer1 channel 1/CAN send/external flash data 3
46	46	46	29		25	27	27	28	28	P2_4/MCPWM1_CH1P/TIM2_CH0/CAN_RX/EFLS_CSN	IO	P2.4/PWM1 channel 1 high side/Timer2 channel 0/CAN receive/external flash chip select
47	47	47	30	16		28	28	29	29	P2_5/MCPWM1_CH0P/UART1_RXD/TIM1_CH0/TIM2_CH1/CAN_TMR/ EFLS_CLK	IO	P2.5/PWM1 channel 0 high side/serial port 1 receive/Timer1 channel 0/Timer2 channel 1/CAN external timestamp clock/external flash clock
48	48	48	31	17		29	29	30	30	P2_6/MCPWM1_CH2N/UART1_TXD/TIM1_CH1	IO	P2.6/PWM1 channel 2 low side/serial port 1 send/Timer1 channel 1
49	49	49	32		26	30	30	31	31	P2_7/MCPWM1_CH1N/SDA0/TIM2_CH0	IO	P2.7/PWM1 channel 1 low side/I2C0 data signal/Timer2 channel 0
50	50	50	33		27	31	31	32	32	P2_8/MCPWM1_CH0N/SCL0/TIM2_CH1	IO	P2.8/PWM1 channel 0 low side/I2C0 clock signal/Timer2 channel 1
51	51	51	34	18		32	32	33	33	P2_9/MCPWM0_CH2P/SDA0/TIM4_CH1/TIM2_Z/EFLS_DAT[0]	IO	P2.9/PWM0 channel 2 high side/I2C0 data signal/Timer4 channel 1/Timer2 Z-axis signal/external flash data 0
52	52	52	35	19		33	33	34	34	P2_10/MCPWM0_CH1P/SCL0/TIM4_CH0/EFLS_DAT[1]	IO	P2.10/PWM0 channel 1 high side/I2C0 clock signal/Timer4 channel 0/external flash data 1
53	53	53	36	20	28	34	34	35	35	P2_11/MCPWM0_CH0P/UART0_RXD/TIM4_CH0/TIM3_CH1 /EFLS_DAT[2]	IO	P2.11/PWM0 channel 0 high side/serial port 0 receive/Timer4 channel 0/Timer3 channel 1/external flash data 2
54	54	54	37	21	29	35	35	36	36	P2_12/MCPWM0_CH2N/UART0_TXD/TIM4_CH1/TIM3_Z/EFLS _DAT[3]	IO	P2.12/PWM0 channel 2 low side/serial port 0 send/Timer4 channel 1/Timer3 axis signal/external flash data 3
55	55	55	38	22	30	36	36	37	37	P2_13/HALL0_IN2/MCPWM0_CH1N/TIM4_CH0/TIM3_CH0/AD	IO	P2.13/Hall0 input signal 2/PWM0 channel 1 low side imer4

No.	Pin									Name	Type	Function Description
	451	451L	453	454(48)	454(52)	455	455L	457	457L			
										C_TRIGGER1/EFLS_CSN		channel 0/Timer3 channel 0/ADC trigger debugging signal 1/external flash chip select (low)
56	56	56	39	23	31	37	37	38	38	P2_14/HALL0_IN1/MCPWM0_CH0N/UART2_TXD/TIM3_CH1/ ADC_TRIGGER0/CMP3_IN	IO	P2.14/Hall0 input signal 1/PWM0 channel 0 low side/serial port 2 send/Timer3 channel 1/ADC trigger debugging signal 0/comparator 3 negative input
57	57	57	40	24	32	38	38	39	39	P2_15/CMP3_OUT/HALL0_IN0/MCPWM0_BKIN0/UART2_RXD/ TIM1_CH0/EFLS_CLK/CMP3_IP0	IO	P2.15/comparator 3 output/Hall0 input signal0/PWM0 stop signal 0/serial port 2 receive/Timer1 channel 0/external flash clock/comparator 3 positive input 0
58	58	58	41	25	33			40	40	P3_0/HALL1_IN2/MCPWM0_CH2N/TIM3_Z/ADC0_CH14/CMP3 _IP1	IO	P3.0/Hall1 input signal 2/PWM0 channel 2 low side/Timer3 Z-axis signal/ADC0 channel 14/comparator 3 positive input 1
59	59	59		26		39	39	41	41	P3_1/HALL1_IN1/MCPWM0_BKIN3/SDA0/TIM0_Z/TIM3_CH0/ ADC0_CH13/CMP3_IP2	IO	P3.1/Hall1 input signal 1/PWM0 stop signal 3/I2C0 data signal/Timer 0 Z-axis signal/Timer3 channel 0/ADC0 channel 13/comparator 3 positive input 2
60	60	60								NC		Floating, no connection
61	61	61		27		40	40	43	43	P3_2/CMP3_OUT/HALL1_IN0/SCL0/TIM0_CH0/TIM3_CH0/ EFLS_DAT[0]/CMP3_IP3	IO	P3.2/comparator 3 output/Hall1 input signal 0/I2C0 clock signal/Time0 channel 0/Timer3 channel 0/external flash data 0/comparator 3 positive input 3
62	62	62				41	41	44	44	VSS	GND	VSS
63	63	63	42	28	34	42	42	45	45	P3_3/CMP2_OUT/SPI0_CSN/TIM0_CH1/EFLS_DAT[1]/ADC1_C H13/ CMP2_IP0	IO	P3.3/comparator 2 output/SPI0 chip select/Timer0 channel 1/external flash data 1/ADC1 channel 13/comparator 2 positive input 0
64	64	64	43	29	35	43	43	46	46	P3_4/HALL0_IN0/SPI0_CLK/TIM1_CH1/EFLS_DAT[2]/ADC1_C H12/ DAC0_OUT/CMP2_IP1	IO	P3.4/Hall0 input signal 0/SPI0 clock/Timer1 channel 1/external flash data 2/ADC1 channel 12/DAC0 output/comparator 2 positive input 1

No.	Pin									Name	Type	Function Description
	451	451L	453	454(48)	454(52)	455	455L	457	457L			
65	65	65		30		44	44			P3_5/HALL0_IN1/MCPWM1_BKIN2/UART1_RXD/SPI0_DO/TIM1_CH0/CAN_TMR/EFLS_DAT[3]/ADC1_CH11/CMP2_IP2	IO	P3.5/Hall0 input signal PWM1 stop signal 2/serial port1 receive/SPI0 output/Timer1 channel 0/ CAN external timestamp clock/external flash data 3/ADC1 channel 11/comparator 2 positive input 2
66	66	66	44	31	36	45	45	47	47	P3_6/HALL0_IN2/MCPWM1_BKIN3/UART1_TXD/SPI0_DI/TIM1_CH1/ ADC_TRIGGER2/CAN_TX/EFLS_CSN/CMP2_IP3	IO	P3.6/Hall0 input signal 2/PWM1 stop signal 3/serial port1 send/SPI0 input/Timer1 channel 1/ADC trigger debugging signal 2/CAN send/external flash chip select (low)/comparator 2 positive input 3
67	67	67	45	32	37	46	46	48	48	P3_7/CMP2_OUT/MCPWM1_BKIN0/TIM4_CH1/ADC_TRIGGER1/ CAN_RX/OPA3_IN/ADC2_CH11/CMP2_IN	IO	P3.7/comparator 2 output/PWM1 stop signal 0/Timer4 channel 1/ADC trigger debugging signal 1/CAN receive/OPA 3 negative input/ADC2 channel 11/comparator 2 negative input
68	68	68	46	33	38	47	47			P3_8/MCPWM1_BKIN1/TIM4_CH0/ADC_TRIGGER0/EFLS_CLK/ OPA3_IP/ADC2_CH10	IO	P3.8/PWM1 stop signal 1/Timer4 channel 0/ADC trigger debugging signal 0/external flash clock/OPA 3 positive input /ADC2 channel 10
69	69	69	47	34	39	48	48	11	11	P3_9/MCPWM0_BKIN0/TIM0_CH1/OPA2_IN/ADC2_CH9	IO	P3.9/PWM0 stop signal 0/Timer0 channel 1/OPA 2 negative input/ADC2 channel 9
70	70	70	48	35	40	49	49	49	49	P3_10/MCPWM0_BKIN1/OPA2_IP/ADC2_CH8	IO	P3.10/PWM0 stop signal 1/OPA 2 positive input /ADC2 channel 8
71	71									AVDD	PWR	AVDD 3.3V power input
		71								NC		NC
72	72	72								NC	PWR	NC
73	73	73								VSS33	GND	VSS33
74	74	74	49	36	41	50	50	50	50	P3_11/MCPWM0_BKIN2/ADC2_CH7/OPAx_OUT0/REF	IO	P3.11/PWM0 stop signal 2/ADC2 channel 7/OPA output port/内部参考电压
75	75	75				51	51	51	51	P3_12/MCPWM0_BKIN3/SDA0/TIM2_CH1/ADC2_CH6	IO	P3.12/PWM0 stop signal 3/I2C0 data signal/Timer2 channel

No.	Pin									Name	Type	Function Description
	451	451L	453	454(48)	454(52)	455	455L	457	457L			
												1/ADC2 channel 6
76	76	76	50	37	42	52	52	52	52	P3_13/OPA1_IN/ADC2_CH5	IO	P3.13/OPA 1 negative input/ADC2 channel 5
77	77	77	51	38	43	53	53	53	53	P3_14/OPA1_IP/ADC2_CH4	IO	P3.14/OPA 1 positive input /ADC2 channel 4
78	78	78	52		44					P3_15/TIM0_CH0/OPA0_IN	IO	P3.15/Timer0 channel 0/OPA 0 negative input
79	79	79	53		45					P4_0/TIM0_Z/EFLS_DAT[0]/OPA0_IP	IO	P4.0/Timer0 Z-axis signal/external flash data 0/OPA 0 positive input
80	80	80						54	54	P4_1/MCPWM0_CH3N/UART0_TXD/SDA0/TIM0_CH1/EFLS_DAT[1]/ ADC1_CH10	IO	P4.1/PWM0 channel 3 low side/serial port0 send/I2C0 data signal/Timer0 channel 1/external flash data 1/ADC1 channel 10
81	81	81						55	55	P4_2/MCPWM0_CH3P/UART0_RXD/SCL0/TIM0_CH0/ADC_TRIGGER2/CAN_TMR/EFLS_DAT[2]/ADC1_CH9	IO	P4.2/PWM0 channel 3 high side/serial port0 receive/I2C0 clock signal/Timer0 channel 0/ADC trigger debugging signal 2/CAN external timestamp clock/external flash data 2/ADC1 channel 9
82	82	82								P4_3/MCPWM0_CH2N/CAN_TX/EFLS_DAT[3]	IO	P4.3/PWM0 channel 2 low side/CAN send/external flash data 3
83	83	83								P4_4/MCPWM0_CH2P/CAN_RX/EFLS_CSN	IO	P4.4/PWM0 channel 2 high side/CAN receive/external flash chip select (low)
84	84	84	54			56	56			P4_5/MCPWM0_CH1P/ADC0_CH11/CMP0_IP0	IO	P4.5/PWM0 channel 1 high side/ADC0 channel 11/comparator 0 positive input 0
85	85	85	55	39	46	57	57	56	56	P4_6/MCPWM0_CH1N/EFLS_CLK/ADC1_CH8/ OPAx_OUT1/LDO12	IO	P4.6/PWM0 channel 1 low side/external flash clock/ADC1 channel 8/OPA output port/1.2V LDO output
86	86	86	56	40	47	58	58			P4_7/ADC1_CH7/ DAC1_OUT	IO	P4.7/ADC1 channel 7/DAC1 output
87	87	87		41		59	59			P4_8/CLK/ADC1_CH6/CMP1_IN	IO	P4.8/clock gating output/ADC1 channel 6/comparator 1 negative input
88	88	88	57		48	59	59			P4_9/CMP1_OUT/TIM3_CH1/CMP1_IP0	IO	P4.9/comparator 1 output/Timer3 channel 1/comparator 1 positive input 0

No.	Pin									Name	Type	Function Description
	451	451L	453	454(48)	454(52)	455	455L	457	457L			
89	89	89	58		49					P4_10/HALL1_IN0/TIM3_CH0/CMP1_IP1	IO	P4.10/Hall1 input signal 0/Timer3 channel 0/comparator 1 positive input 1
90	90	90	59							P4_11/HALL1_IN1/TIM3_Z/CMP1_IP2	IO	P4.11/Hall1 input signal 1/Timer3 Z-axis signal/comparator 1 positive input 2
91	91	91	60				60		57	P4_12/CMP1_OUT/HALL1_IN2/UART0_RXD/TIM3_CH0/EFLS_CLK/ ADC0_CH12/CMP1_IP3	IO	P4.12/comparator 1 output/Hall1 input signal 2/serial port0 receive/Timer3 channel 0/external flash clock/ADC0 channel 12/comparator 1 positive input 3
92	92		61	42	50	60		57		AVDD	PWR	AVDD 3.3V power input
		92					61		58	VCC	PWR	VCC 5V power input
93	93					61		58		AVDD	PWR	AVDD 3.3V power input
		93										NC
		94					62		59	AVSS		AVSS
94	94			43		62		59		VSS33	GND	VSS33
95	95	95	62		51			60		VSS33	GND	VSS33
96	96	96	63	44		54	54		60	P4_13/CMP0_OUT/HALL0_IN2/SPI1_CLK/SCL0/TIM1_Z/TIM2_Z/ CAN_TX/EFLS_DAT[0]/ADC0_CH10/CMP0_IP1	IO	P4.13/comparator 0 output/Hall0 input signal 2/SPI1 clock/I2C0 clock signal/Timer1 Z-axis signal/Timer2 Z-axis signal/CAN send/external flash data 0/ADC0 channel 10/comparator 0 positive input 1
97	97	97	64	45	52	55	55	63		P4_14/CLK/HALL0_IN1/UART2_TXD/SPI1_DO/SDA0/TIM1_CH1/TIM2_CH0/ADC_TRIGGER2/CAN_RX/EFLS_DAT[1]/ADC0_CH9/CMP0_IP2	IO	P4.14/ clock output/Hall0 input signal 1/serial port2 send/SPI1 output/I2C0 data signal/Timer1 channel 1/Timer2 channel 0/ADC Trigger signal2/CAN receive/external flash data 1/ADC0 channel 9/comparator 0 positive input 2
98	98	98		46		63	63	64	63	P4_15/HALL0_IN0/UART2_RXD/SPI1_D1/SCL0/TIM1_CH0/TIM2_CH1/	IO	P4.15/Hall0 input signal 0/serial port2 receive/SPI1 input/I2C0 clock signal/Timer1 channel 0/Timer2 channel 1/ADC trigger

No.	Pin									Name	Type	Function Description
	451	451L	453	454(48)	454(52)	455	455L	457	457L			
										ADC_TRIGGER1/CAN_TMR/EFLS_DAT[2]/ADC0_CH8/CMP0_IP3		debugging signal 1/ CAN external timestamp clock/CAN external timestamp clock/external flash data 2/ADC0 channel 8/comparator 0 positive input 3
99	99	99		47		64	64	61	64	P5_0/CMP0_OUT/MCPWM0_CH3N/SDA1/TIM3_CH0/ADC_TRIGGER0/EFLS_DAT[3]/ADC0_CH7/CMP0_IN	IO	P5.0/comparator 0 output/PWM0 channel 3 low side/Timer3 channel 0/ADC trigger debugging signal 0/external flash data 3/ADC0 channel 7/comparator 0 negative input
100	100	100		48				62	61	P5_1/MCPWM0_CH3P/SPI1_CSN/SCL1/TIM4_CH1/TIM3_CH1/EFLS_CSN/ADC0_CH6	IO	P5.1/PWM0 channel 3 high side/SPI0chip select/I2C1 clock signal/Timer4 channel 1/Timer3 channel 1/external flash chip select (low)/ADC0 channel 6

3.3 Description of Pin Multiplex Function

Table 3-2 LKS32MC45x Pin Function Selection

	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AFA	AFB	AF0	
P0_0													EXTI0
P0_1			MCPWM1_BKIN2	UART0_RXD	SPI0_CSN		TIM4_CH1			CAN_TX			EXTI1/5VT
P0_2	CMP5_OUT		MCPWM1_BKIN3	UART0_TXD						CAN_RX		CMP5_IP0	WAKE0/EXTI2/5VT
P0_3		HALL1_IN2			SPI0_DI		TIM0_Z					CMP5_IP1	WAKE1/EXTI3
P0_4		HALL1_IN1	MCPWM1_BKIN0	UART0_RXD	SPI0_DO	SDA0	TIM0_CH0	TIM3_Z	ADC_TRIGGER1	CAN_TMR		ADC2_CH13/CMP5_IP2	WAKE2/EXTI4/5VT
P0_5	CMP5_OUT	HALL1_IN0	MCPWM0_BKIN3	UART0_TXD	SPI0_CLK	SCL0	TIM0_CH1	TIM2_Z	ADC_TRIGGER0			ADC2_CH12/CMP5_IP3	WAKE3/EXTI5/5VT
P0_6												RST_n	5VT
P0_7												OSC_OUT	
P0_8							TIM1_Z				EFLS_DAT[0]	OSC_IN	
P0_9	CMP4_OUT		MCPWM1_CH0N		SPI0_CLK		TIM1_CH0				EFLS_DAT[1]	CMP5_IN	nTRST
P0_10			MCPWM1_CH0P		SPI0_CSN		TIM1_CH1				EFLS_DAT[2]	CMP4_IN	SWDIOTMS/5VT
P0_11			MCPWM1_CH1N	UART1_RXD	SPI0_DI	SCL1	TIM4_CH1				EFLS_DAT[3]	CMP4_IP0	TDI/5VT
P0_12			MCPWM1_CH1P	UART1_TXD	SPI0_DO	SDA1	TIM4_CH0			CAN_TMR	EFLS_CSN	CMP4_IP1	SWCLKTCLK/5VT
P0_13			MCPWM1_CH2N	UART0_TXD	SPI1_CSN		TIM4_CH0			CAN_TX		CMP4_IP2	WAKE4/EXTI6/TDO/5VT
P0_14	CLK		MCPWM1_CH2P	UART0_RXD	SPI1_DI	SCL0				CAN_RX		CMP4_IP3	EXTI7
P0_15	CMP4_OUT		MCPWM1_CH3N				TIM1_Z						EXTI8

	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AFA	AFB	AF0	
P1_0			MCPWM1_CH3P	UART0_TXD	SPI1_DO	SDA0	TIM0_Z						
P1_1			MCPWM0_CH0N		SPI1_CLK								
P1_2			MCPWM0_CH0P		SPI0_CSN								
P1_3			MCPWM0_CH1N		SPI0_CLK	SDA1		TIM3_CH0					
P1_4			MCPWM0_CH1P			SCL1		TIM3_CH0		CAN_TMR			5VT
P1_5			MCPWM0_CH2N	UART1_RXD	SPI0_DI	SCL1	TIM4_CH1	TIM3_Z		CAN_TX			EXTI9/5VT
P1_6			MCPWM0_CH2P	UART1_TXD	SPI0_DO	SDA1	TIM4_CH0			CAN_RX			5VT
P1_7			MCPWM0_CH3N		SPI1_CSN								EXTI10/5VT
P1_8			MCPWM0_CH3P	UART2_RXD	SPI1_CLK		TIM0_CH0	TIM2_Z		CAN_TMR			5VT
P1_9			MCPWM0_BKIN0	UART2_TXD	SPI1_DO	SDA0	TIM0_CH1	TIM2_CH0	ADC_TRIGGER2	CAN_TX			5VT
P1_10			MCPWM0_BKIN1	UART2_RXD	SPI1_DI	SCL0	TIM0_CH0	TIM2_CH1	ADC_TRIGGER1	CAN_RX			5VT
P1_11			MCPWM0_BKIN2	UART2_TXD	SPI0_DO	SDA0	TIM0_CH1					OPA5_IN	WAKE5/EXTI11
P1_12			MCPWM1_CH3N	UART2_RXD	SPI0_DI	SCL0	TIM1_CH0					OPA5_IP	EXTI12
P1_13			MCPWM1_CH3P		SPI0_CLK		TIM1_CH1		ADC_TRIGGER0			OPA4_IN	
P1_14			MCPWM1_CH2N		SPI0_CSN		TIM1_Z	TIM2_CH0				OPA4_IP	
P1_15			MCPWM1_CH2P					TIM2_CH1		CAN_TMR			

	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AFA	AFB	AF0	
P2_0			MCPWM1_CH1N				TIM1_CH0			CAN_RX	EFLS_DAT[0]		EXTI13
P2_1			MCPWM1_CH1P				TIM1_CH0		ADC_TRIGGER0	CAN_TX	EFLS_DAT[1]		EXTI14
P2_2			MCPWM1_BKIN0								EFLS_DAT[2]		EXTI15/5VT
P2_3			MCPWM1_CH2P				TIM1_CH1			CAN_TX	EFLS_DAT[3]		
P2_4			MCPWM1_CH1P					TIM2_CH0		CAN_RX	EFLS_CSN		
P2_5			MCPWM1_CH0P	UART1_RXD			TIM1_CH0	TIM2_CH1		CAN_TMR	EFLS_CLK		
P2_6			MCPWM1_CH2N	UART1_TXD			TIM1_CH1						
P2_7			MCPWM1_CH1N			SDA0		TIM2_CH0					EXTI16
P2_8			MCPWM1_CH0N			SCL0		TIM2_CH1					EXTI17
P2_9			MCPWM0_CH2P			SDA0	TIM4_CH1	TIM2_Z			EFLS_DAT[0]		
P2_10			MCPWM0_CH1P			SCL0	TIM4_CH0				EFLS_DAT[1]		
P2_11			MCPWM0_CH0P	UART0_RXD			TIM4_CH0	TIM3_CH1			EFLS_DAT[2]		5VT
P2_12			MCPWM0_CH2N	UART0_TXD			TIM4_CH1	TIM3_Z			EFLS_DAT[3]		EXTI18/5VT
P2_13		HALL0_IN2	MCPWM0_CH1N				TIM4_CH0	TIM3_CH0	ADC_TRIGGER1		EFLS_CSN		
P2_14		HALL0_IN1	MCPWM0_CH0N	UART2_TXD				TIM3_CH1	ADC_TRIGGER0			CMP3_IN	WAKE6
P2_15	CMP3_OUT	HALL0_IN0	MCPWM0_BKIN0	UART2_RXD			TIM1_CH0				EFLS_CLK	CMP3_IP0	EXTI19/5VT

	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AFA	AFB	AF0	
P3_0		HALL1_IN2	MCPWM0_CH2N					TIM3_Z				ADC0_CH14/CMP3_IP1	5VT
P3_1		HALL1_IN1	MCPWM0_BKIN3			SDA0	TIM0_Z	TIM3_CH0				ADC0_CH13/CMP3_IP2	5VT
P3_2	CMP3_OUT	HALL1_IN0				SCL0	TIM0_CH0	TIM3_CH0			EFLS_DAT[0]	CMP3_IP3	WAKE7/EXTI20/5VT
P3_3	CMP2_OUT				SPI0_CSN		TIM0_CH1				EFLS_DAT[1]	ADC1_CH13/CMP2_IP0	EXTI21
P3_4		HALL0_IN0			SPI0_CLK		TIM1_CH1				EFLS_DAT[2]	ADC1_CH12/DAC0_OUT /CMP2_IP1	5VT
P3_5		HALL0_IN1	MCPWM1_BKIN2	UART1_RXD	SPI0_DO		TIM1_CH0			CAN_TMR	EFLS_DAT[3]	ADC1_CH11/CMP2_IP2	5VT
P3_6		HALL0_IN2	MCPWM1_BKIN3	UART1_TXD	SPI0_DI		TIM1_CH1		ADC_TRIGGER2	CAN_TX	EFLS_CSN	CMP2_IP3	5VT
P3_7	CMP2_OUT		MCPWM1_BKIN0				TIM4_CH1		ADC_TRIGGER1	CAN_RX		OPA3_IN/ADC2_CH11/ CMP2_IN	EXTI22
P3_8			MCPWM1_BKIN1				TIM4_CH0		ADC_TRIGGER0		EFLS_CLK	OPA3_IP/ADC2_CH10	EXTI23
P3_9			MCPWM0_BKIN0				TIM0_CH1					OPA2_IN/ADC2_CH9	
P3_10			MCPWM0_BKIN1									OPA2_IP/ADC2_CH8	
P3_11			MCPWM0_BKIN2									ADC2_CH7/OPAx_OUT0 /REF	EXTI24
P3_12			MCPWM0_BKIN3			SDA0		TIM2_CH1				ADC2_CH6	EXTI25
P3_13												OPA1_IN/ADC2_CH5	EXTI26
P3_14												OPA1_IP/ADC2_CH4	EXTI27
P3_15							TIM0_CH0					OPA0_IN	EXTI28

	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AFA	AFB	AF0	
P4_0							TIM0_Z				EFLS_DAT[0]	OPA0_IP	EXTI29
P4_1			MCPWM0_CH3N	UART0_TXD		SDA0	TIM0_CH1				EFLS_DAT[1]	ADC1_CH10	EXTI30/5VT
P4_2			MCPWM0_CH3P	UART0_RXD		SCL0	TIM0_CH0		ADC_TRIGGER2	CAN_TMR	EFLS_DAT[2]	ADC1_CH9	EXTI31/5VT
P4_3			MCPWM0_CH2N							CAN_TX	EFLS_DAT[3]		
P4_4			MCPWM0_CH2P							CAN_RX	EFLS_CSN		
P4_5			MCPWM0_CH1P									ADC0_CH11/CMP0_IP0	5VT
P4_6			MCPWM0_CH1N								EFLS_CLK	ADC1_CH8/OPAx_OUT1 /LDO12	
P4_7												ADC1_CH7/DAC1_OUT	
P4_8	CLK											ADC1_CH6/CMP1_IN	
P4_9	CMP1_OUT							TIM3_CH1				CMP1_IP0	5VT
P4_10		HALL1_IN0						TIM3_CH0				CMP1_IP1	
P4_11		HALL1_IN1						TIM3_Z				CMP1_IP2	
P4_12	CMP1_OUT	HALL1_IN2		UART0_RXD				TIM3_CH0			EFLS_CLK	ADC0_CH12/CMP1_IP3	
P4_13	CMP0_OUT	HALL0_IN2			SPI1_CLK	SCL0	TIM1_Z	TIM2_Z		CAN_TX	EFLS_DAT[0]	ADC0_CH10/CMP0_IP1	
P4_14	CLK	HALL0_IN1		UART2_TXD	SPI1_DO	SDA0	TIM1_CH1	TIM2_CH0	ADC_TRIGGER2	CAN_RX	EFLS_DAT[1]	ADC0_CH9/CMP0_IP2	5VT
P4_15		HALL0_IN0		UART2_RXD	SPI1_D1	SCL0	TIM1_CH0	TIM2_CH1	ADC_TRIGGER1	CAN_TMR	EFLS_DAT[2]	ADC0_CH8/CMP0_IP3	5VT

	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AFA	AFB	AF0	
P5_0	CMP0_OUT		MCPWM0_CH3N			SDA1		TIM3_CH0	ADC_TRIGGER0		EFLS_DAT[3]	ADC0_CH7/CMP0_IN	EXTI32
P5_1			MCPWM0_CH3P		SPI1_CSN	SCL1	TIM4_CH1	TIM3_CH1			EFLS_CSN	ADC0_CH6	EXTI33
P5_2													
P5_3													

4 Package Dimension

4.1 LKS32MC451VCT8/ LKS32MC451LVCT8

LQFP100 Profile Quad Flat Package:

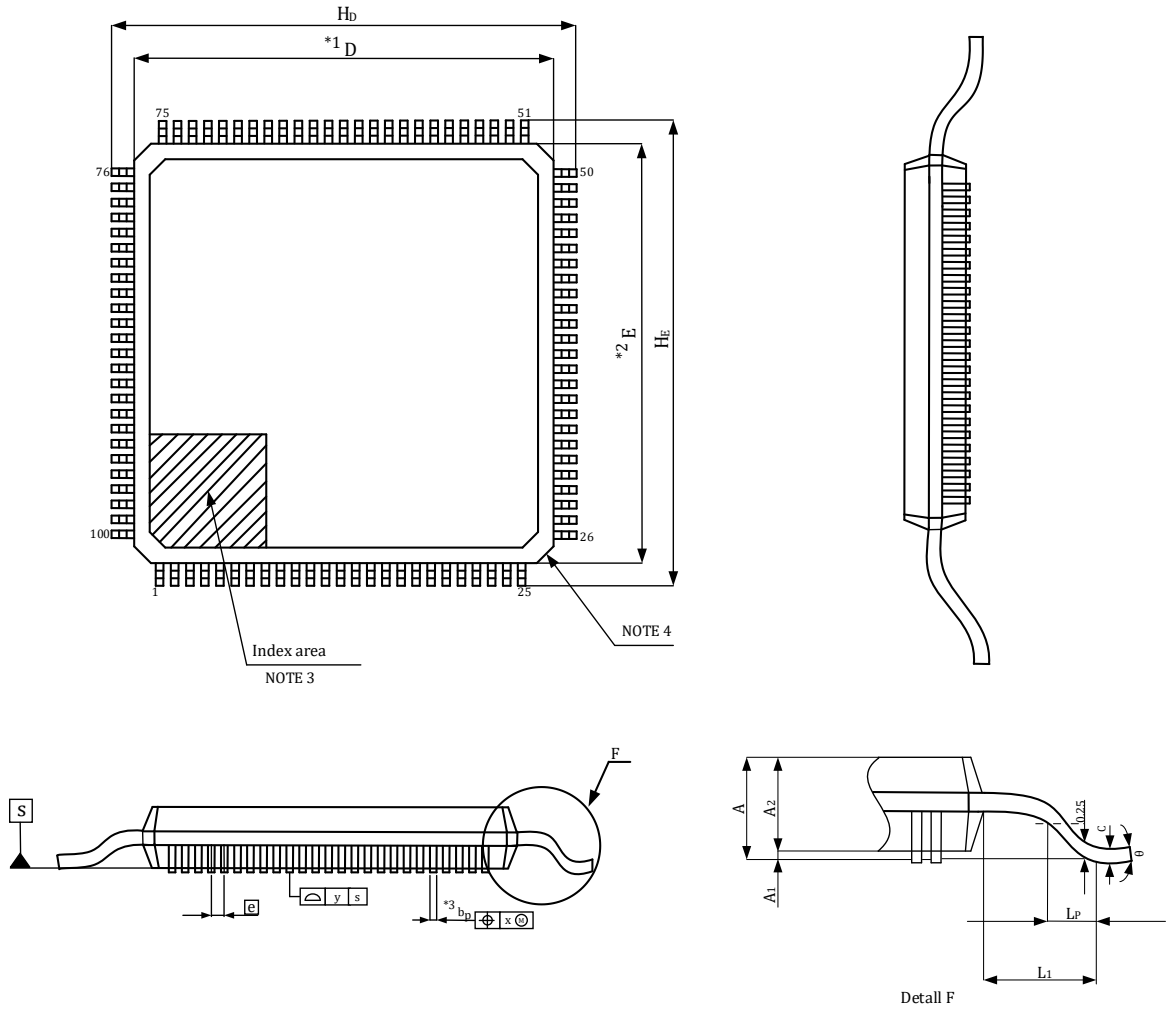

Figure 4-1 LKS32MC451VCT8 package diagram

Table 4-1 LKS32MC451VCT8 package dimension

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.7
A1	0.05	-	0.15
A2	1.35	1.40	1.45
bp	0.17	0.20	0.23
c	0.09	-	0.20
x	-	-	0.08
y	-	-	0.08
D	13.90	14.00	14.10

E	13.90	14.00	14.10
H_D	15.80	16.00	16.20
H_E	15.80	16.00	16.20
e	0.50BSC		
Lp	0.45	0.60	0.75
L1	1.00REF		
θ	0	3.5°	8°

4.2 LKS32MC453RCT8/LKS32MC455RCT8/ LKS32MC455LRCT8/LKS32MC457LRCT8

LQFP64 Profile Quad Flat Package:

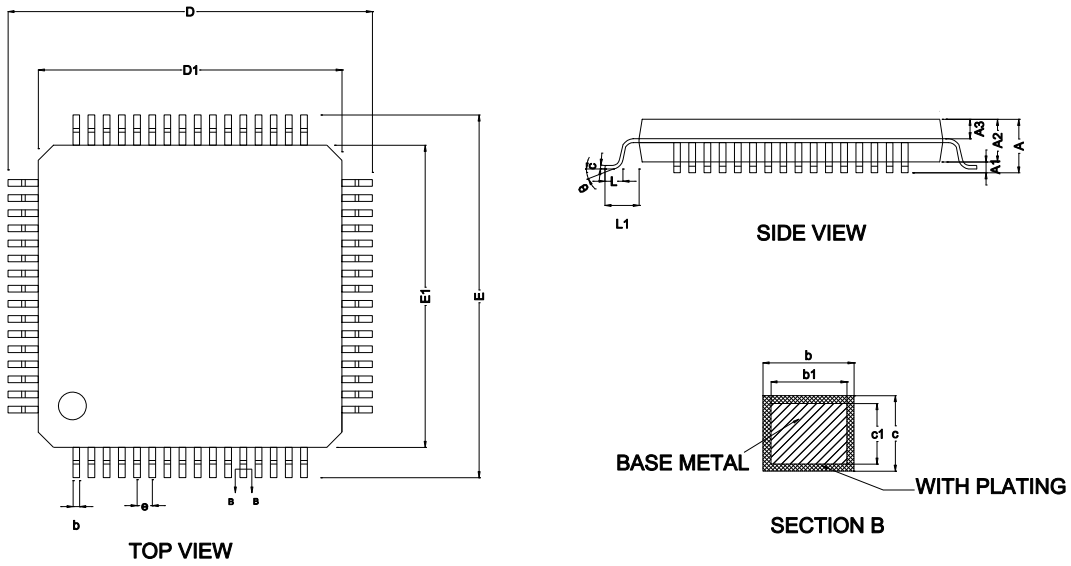

Figure 4-2 LKS32MC453RCT8/LKS32MC455RCT8/ LKS32MC455LRCT8/LKS32MC457LRCT8 package diagram

Table 4-2 LKS32MC453RCT8/LKS32MC455RCT8/ LKS32MC455LRCT8 /LKS32MC457LRCT8 package dimension

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23

c	0.13	-	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

4.3 LKS32MC457RCT8

LQFP64 14×14-0.80 Profile Quad Flat Package:

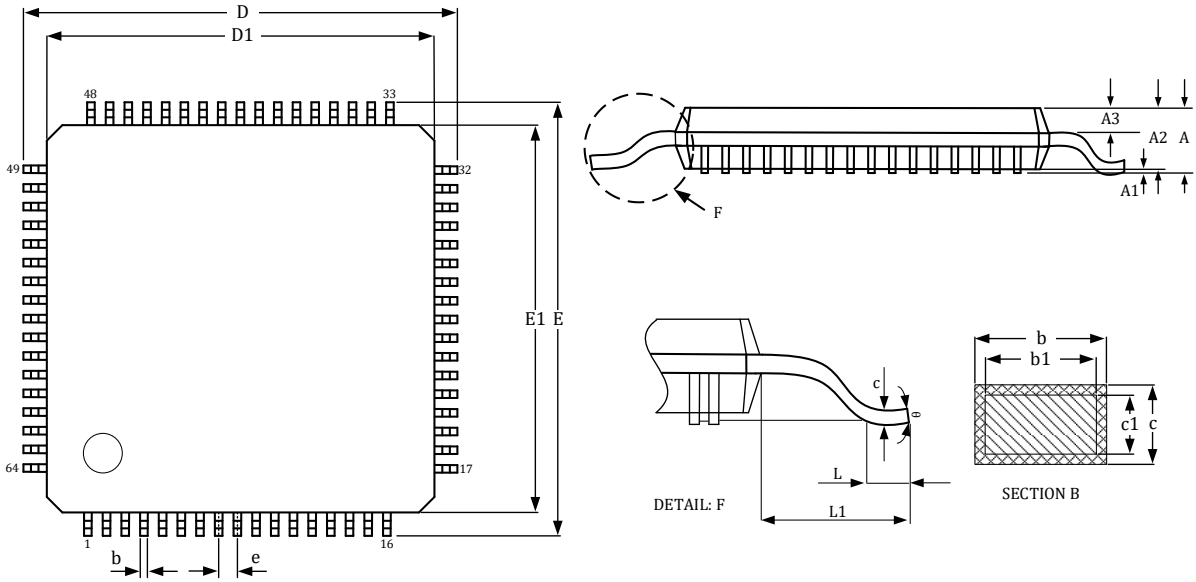

Figure 4-3 LKS32MC457RCT8 package diagram

Table 4-3 LKS32MC457RCT8 package dimen

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.70
A1	0.05	0.1	0.2
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.32	0.37	0.42
b1	-	0.35	-
c	0.09	0.145	0.20
c1	-	0.125	-
D	15.80	16.00	16.20

D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	0.80BSC		
L	0.30	-	0.70
L1	1.00REF		
θ	0	-	8°

4.4 LKS32MC454CCT8

TQFP48 Profile Quad Flat Package:

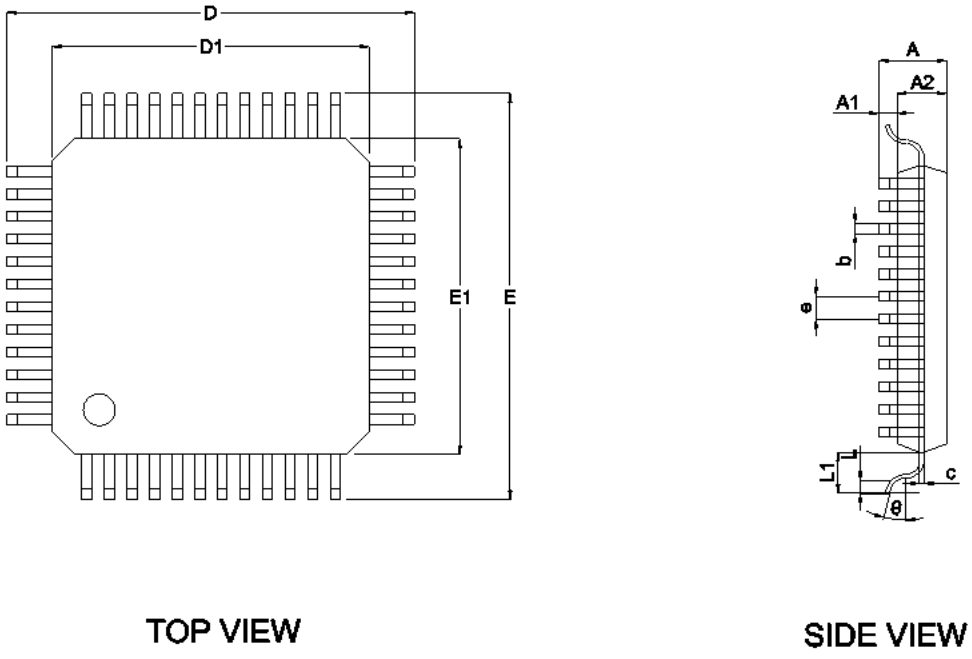

Figure 4-4 LKS32MC454CCT8 package diagram

Table 4-4 LKS32MC454CCT8 package dimension

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.18	0.22	0.26
c	0.13	-	0.17
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	-	0.50	-

θ	0°	3.5°	7°
L	0.45	0.60	0.75
L1	-	1.00	-

4.5 LKS32MC454NCQ8

QFN52 Profile Quad Flat Package:

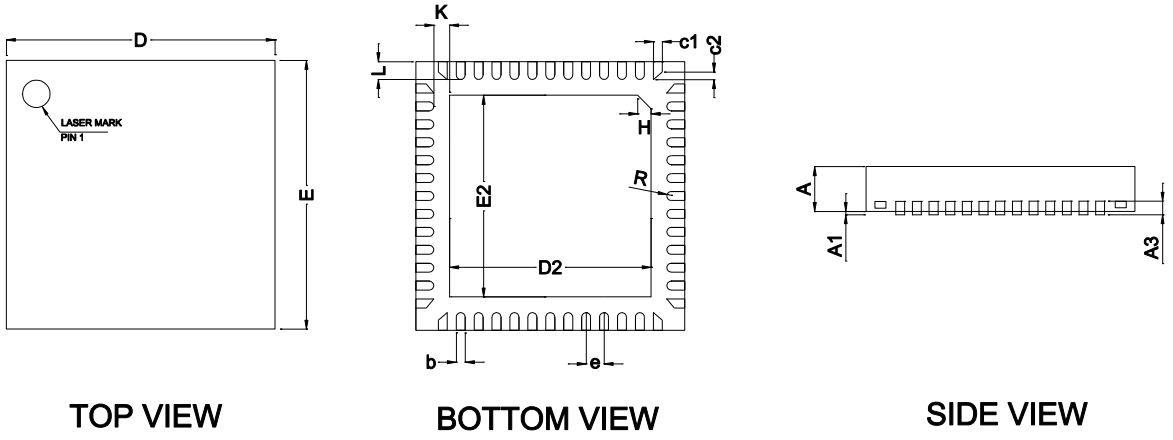

Figure 4-5 LKS32MC454NCQ8 package diagram

Table 4-5 LKS32MC454NCQ8 package dimension

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	4.40	4.50	4.60
E2	4.40	4.50	4.60
e	0.30	0.40	0.45
H		0.35REF	
K	0.25	-	-
L	0.35	0.40	0.45
R	0.075	-	-
c1	-	0.17	-
c2	-	0.17	-

5 Electrical Performance Parameters

Table 5-1 LKS32MC45x electrical limit parameters

Parameter	Min.	Max.	Unit	Description
MCU Supply Voltage (AVDD)(451/453/455/454)	-0.3	+3.6	V	
LDO Supply Voltage (AVDD)(451L/455L/457L)	-0.3	+8	V	
LDO Supply Current (451L/455L/457L)		+80	mA	
Operating temperature	-40	+105	˚C	
Storage temperature	-40	+150	˚C	
Junction temperature	-	150	°C	
Pin temperature (welding, 10s)	-	260	°C	

Table 5-2 LKS32MC45x recommended operating parameters

Parameter	Min.	Typ.	Max.	Unit	Description
MCU Supply Voltage (AVDD)(451/453/455/454)	2.2	3.3	3.6	V	
Analog power voltage ($AVDD_A$)	2.8	3.3	3.6	V	REF2VDD=0, ADC uses internal 2.4V reference
	2.4	3.3	3.6	V	REF2VDD=1 , ADC uses AVDD as reference
LDO Supply Voltage (AVDD)(451L/455L/457L)	4.5	5	5.5	V	Output 3.3v

Table 5-3 LKS32MC45x ESD parameters

Item	Pin	Min.	Max.	Unit
ESD test (HBM)	MCU PIN	-6000	6000	V
	451L/455L/457L 3.3V LDO PIN	-2500	2500	V

According to "MIL-STD-883J Method 3015.9", under the environment of 25°C and 55% relative humidity, electrostatic discharge is applied to all IO pins of the tested chip for 3 times, with an interval of 1s each time. The test results show that the anti-static discharge level of the chip reaches Class 3A ≧4000V, <8000V.

Table 5-4 LKS32MC45x Latch-up parameters

Item	Min.	Max.	Unit
Latch-up current (85°C)	-200	200	mA

According to "JEDEC STANDARD NO.78E NOVEMBER 2016", apply an overvoltage of 5.445V to inject a 200mA current on each signal IO or an undervoltage of -1.815V to pull a -200mA current. The test results show that the anti-lockup level of the chip is 200mA.

Table 5-5 LKS32MC45x IO limit parameters

Parameter	Description	Min.	Max.	Unit

V_{IN}	Input voltage range of GPIO signal (not 5V tolerant)	-0.3	3.6	V
V_{IN}(5VT)	Input voltage range of GPIO signal (5V tolerant)	-0.3	5.5	V
I_{INJ_PAD}	Maximum input current of single GPIO	-18	18	mA
I_{INJ_SUM}	Maximum input current of all GPIOs	-50	50	mA

Table 5-6 LKS32MC45x IO DC parameters

Parameter	Description	AVDD	Min.	Typ.	Max.	Unit
V_{IH}	Digital IO input HV	3.3	2		AVDD	V
V_{IL}	Digital IO input LV	3.3			0.8	V
I_{IH}	Digital IO input HV, current consumption	3.3			10	uA
I_{IL}	Digital IO input LV, current consumption	3.3	-10			uA
V_{OH}	Digital IO output HV	3.3	AVDD-0.4			V
V_{OL}	Digital IO output LV	3.3			0.4	V
I	IO Drive current	3.3	4.5mA		18mA	
$R_{pull-pp}$	Pull-up resistance	3.3				KOhm
$R_{pull-down}$	Pull-down resistance	3.3				
R_{io-ana}	Connection resistance between IO and internal analog circuit			100	200	Ω

Table 5-1 LKS32MC45x Circuit Current Consumption IDD

Module	Min	Typ	Max	Unit
CMP×1		0.02		mA
OPA×1		0.85		mA
ADC×3		8.50		mA
DAC×1		0.35		mA
Temp Sensor		0.18		mA
XTAL oscillator		0.20		mA
BGP		0.34		mA
PLL		0.05		mA
CPU+flash+SRAM (192MHz)		15.47		mA
CAN-FD		1.38		mA
CORDIC		0.21		mA
CRC		0.08		mA
UART×1		0.11		mA
MCPWM		0.74		mA
TIMER×5+QEP×4		1.01		mA
SPI×1		0.17		mA
IIC×1		0.03		mA
HALL×1		0.05		

High speed clock turn-off sleep	0.4	0.5	0.7	mA
Power gating sleep	7	9	20	uA

Unless otherwise specified, the above tests are under 3.3V power supply at room temperature 25°, and the chip is running at a 192MHz clock. Due to the device model deviation in the manufacturing process, there will be individual differences in the current consumption of different chips.

6 Analog Performance Parameters

LKS32MC451 and other models are single-MCU chips with electrical parameters as shown in the table below, taking LKS32MC451 as an example.

Table 6-1 LKS32MC451VCT8 analog performance parameters

Parameter	Min.	Typ.	Max.	Unit	Description
Analog-to-digital converter (ADC)					
Operating power	2.8	3.3	3.6	V	REF2VDD=0, ADC uses internal 2.4V reference
	2.4	3.3	3.6	V	REF2VDD=1, ADC uses AVDD as reference
Output bit rate		2		Msps	$f_{adc}/16$
Differential input signal range	-REF		+REF	V	Gain=1 hour; REF=2.4V
	-3.3		+3.3	V	Gain=2/3 hour; REF=2.4V
Single-end input signal range	-0.3		AVDD+0.3	V	Limited by IO input voltage
DC offset		5	10	mV	Can be calibrated
Effective number of bits (ENOB)	10.5	11.5		bit	
INL		2	3	LSB	
DNL		1	2	LSB	
SNR	63	69		dB	
Input resistance	500k			Ohm	
Input capacitance		10pF		F	
Reference voltage (REF)					
Operating power	2.2	3.3	3.6	V	
Output deviation	-9		9	mV	
Power supply rejection ratio		70		dB	
Temperature coefficient		20		ppm/°C	
Output voltage		1.2		V	
Digital-to-analogue converter (DAC)					
Operating power	2.2	3.3	3.6	V	
Load resistance	5k			Ohm	Output BUFFER enabled
Load capacitance			50p	F	
Output voltage range	0.05		AVDD-0.1	V	
Conversion speed			1M	Hz	
DNL		1	2	LSB	
INL		2	4	LSB	

Parameter	Min.	Typ.	Max.	Unit	Description
OFFSET		5	10	mV	
SNR	57	60	66	dB	
Operational amplifier (OPA)					
Operating power	2.8	3.3	3.6	V	
Bandwidth		20M	30M	Hz	
Load resistance	20k			Ohm	
Load capacitance			5p	F	
Input common-mode range	0		AVDD-1	V	
Output signal range	0.1		AVDD-0.2-Voffset*Gain	V	When selecting the amplifier magnification of the application scheme, it should be ensured that the maximum signal multiplied by the magnification of the application is <=AVDD-0.2-Voffset*Gain, where Voffset is calculated with its maximum value
OFFSET		5	10	mV	This OFFSET is the equivalent differential input deviation obtained when the OPA differential input is short-circuited and OPA OUT is measured from 0 level. The output deviation of OPA is the OPA magnification xOFFSET
Common mode rejection ratio (CMRR)		80		dB	
Power supply rejection ratio (PSRR)		80		dB	
Load current			500	uA	
Slew rate		5		V/us	
Phase margin		60		Degree	
Comparator (CMP)					
Operating power	2.2	3.3	3.6	V	
Input signal range	0		AVDD	V	
OFFSET		10	15	mV	
Transmission delay		0.15u		S	Default power consumption
		0.6u		S	Low power
Hysteresis		20		mV	HYS='0'

Parameter	Min.	Typ.	Max.	Unit	Description
		0		mV	HYS='1'

7 Power Management System (POWER)

The power management system is composed of LDO12 module, power detection module (PVD), and power-on/power-off reset module (POR).

The chip is powered by single 2.2V-3.6V power supply to save off-chip power costs, and all internal digital circuits and PLL modules are powered by a built-in LDO12.

The LDO is automatically turned on after power on, without requiring software configuration, but the LDO output voltage can be fine-tuned by software.

LDO is divided into low-power mode and normal operation mode. The low-power mode is entered during sleep mode. At this time, most of the digital circuits will be powered off, and only some of the on-duty circuits and SRAM maintains power-on.

In normal operation mode, the BGP module needs to be turned on.

The output voltage of LDO12 can be adjusted by setting the register LDO12TRIM<2:0>, and the corresponding value of the register is described in the analog register table. LDO12 has been calibrated before the chip leaves the factory, and generally, users do not need to configure these registers additionally. To fine-tune the output voltage of the LDO, you need to read the original configuration value and fill in the register with the configuration value corresponding to the fine-tuning value plus the original value.

The POR module monitors the voltage of the LDO12 and provides a reset signal for the digital circuit to avoid faults occurred when the voltage of LDO12 is lower than 0.8V (e.g.: power-on or power-off).

The PVD module detects the 3.3V input power supply and generates an alarm (interrupt) signal to alert the MCU if it falls below a set threshold value, which can be set to a different voltage by register PVDSEL<1:0>. The PVD module can be disabled by setting PD_PDT= '1'. The values corresponding to the specific registers are described in the analog register table.

8 Clock System (CLOCK)

The clock system consists of an internal 64KHz RC clock, an internal 12MHz RC clock, an external 12MHz crystal oscillator circuit, and a PLL circuit.

32K RC clock is used as a slow clock in MCU system and as an MCU clock in filter module or in low power state. 12MHz RC clock is used as the master clock in MCU system, and can provide up to 192MHz when used together with PLL. The external 12MHz crystal oscillator circuit is used as a backup clock.

Both 32K and 12M RC clocks have been correctly calibrated at the factory, In the temperature range of -40 - 105°C, the accuracy of the 32KHz RC clock is ±50%, and the accuracy of the 12M RC clock is ±1%.

The 12M RC clock is turned on by setting RCHPD = '0' (ON by default, OFF when set to '1'). The RC clock needs a reference voltage and current provided by the Bandgap voltage reference module. Therefore, BGP must be enabled before the RC clock is enabled. When the chip is powered on, the 12M RC clock and BGP module are both turned on automatically. The 32K RC clock is always on and cannot be turned off.

The PLL multiplies the 12M RC clock to provide a higher frequency clock for modules like MCU and ADC. The maximum clock of MCU and PWM modules is 192MHz, and the typical operating clock of ADC module is 32MHz, which can be set to different ADC operating frequency by register ADCLKSEL<1:0>.

PLL is turned on by setting PLLPDN = '1' (OFF by default, turn on when set to '1'). Before turning on the PLL module, the BGP (Bandgap) module should be turned on first. After the PLL is turned on, it needs a settling time of 8us to achieve a stable frequency output. When the chip is powered on, the RCH clock and BGP module are both turned on. PLL is OFF by default and enabled by software.

The crystal oscillator circuit has a built-in amplifier and oscillation capacitor, and it only needs to connect a crystal between IO OSC_IN/OSC_OUT and set XTALPDN='1' to start oscillation.

9 Bandgap Voltage Reference (BGP)

The Bandgap voltage reference provides reference voltage and current for ADC, DAC, RC clock, PLL, temperature sensor, operational amplifier, comparator and FLASH. Turn on the Bandgap voltage reference before using any of the above modules.

When the chip is powered on, the BGP module is turned on automatically. The voltage reference is turned on by setting BGPPD = '0'. From OFF to ON, BGP needs about 2us to stabilize. BGP output voltage is about 1.2V, and accuracy is ± 0.8%

The voltage reference can be measured by setting REF_AD_EN = '1' and via IO .

10 ADC Module

The chip has 3-channel built-in SAR ADCs with sampling rate of 14BIT and 2MHz. The ADC module is off when the chip is powered on. Before the ADC is turned on, the BGP, 12M RC clock and PLL modules need to be turned on and the ADC operating frequency needs to be selected. The default configuration of ADC operating clock is 32M, corresponding to 2MHz conversion data rate.

3-channel ADCs sample according to the 3 trigger signal sources. If 3 trigger sources come at the same moment, 3-channel ADCs also finish sampling at the same time and then convert.

ADC needs 16 ADC clock cycles to complete a conversion. In this case, the sampling and conversion is carried out continuously, and the previous conversion and the current sampling can overlap in time. $f_{conv} = f_{adc}/16$. The conversion rate is 2MHz when the ADC clock is set to 32M.

The ADC power consumption level can be reduced by register CURRIT<1:0> when the ADC is used in downgrade frequency applications.

The ADC can operate in the following modes: one-time single channel trigger, continuous single channel, single 1-16 channel scan, continuous 1-16 channel scan. Each ADC has 16 sets of independent registers corresponding to each channel.

ADC trigger event can be triggered by the external timer signals, including T0, T1 and T2, to a preset number of times, or triggered by software.

The ADC has two gain modes which is set via GAIN_SHAx, namely 1x and 2/3x gain. In 1x gain, the input signal amplitude is ±2.2V; in 2/3 gain, the input signal amplitude is ±3.3V. When measuring the output signal of OPA, the specific ADC gain is selected according to the maximum possible output signal of OPA.

11 Operational Amplifier (OPA)

The 6-channel IO rail-to-rail OPAs is integrated, with a built-in feedback resistor R2/R1, and an external resistor R0 connected to the external pin. The resistance of feedback resistors R2: R1 can be adjusted by register RES_OPAx<2:0> to achieve different gains. The values corresponding to the specific registers are described in the analog register table.

The final amplification is R2/(R1+R0), where R0 is the resistance value of the external resistor.

For applications using MOS tube resistance for direct sampling, it is recommended to connect an external resistor of >20kΩ, to reduce the current flowing into the chip pin when the MOS tube is turned off.

For applications with small resistance sampling, it is recommended to connect an external resistor of 100Ω.

The OPA can select two output signals of the 6-channel amplifier by setting OPAOUTx_EN<1:0>, and send it to two IO ports through a buffer for measurement (see the corresponding relationship in the datasheet 'Pin Function Description"). Because of the BUFFER, the OPAMP is able to send two output signals in the normal working mode.

When the chip is powered on, the OPA module is OFF by default. The OPA can be turned on by setting OPAxPDN = '1'. Turn on the BGP module before turning on the OPA.

For built-in clamp diodes integrated between the positive and negative OPA inputs, the motor phase line could be directly connected to the OPA input through a matching resistor, thereby simplifying the external circuit for MOSFET current sampling.

12 Comparator (CMP)

Built-in 6-channel rail-to-rail comparators with programmable comparator speed, hysteresis voltage, and signal source.

The comparison delay can be set to 0.15uS/0.6uS through the register IT_CMP, and the hysteresis voltage can be set to 20mV/40mV through CMP_HYS.

The signal sources of the positive and negative inputs of the comparator can be set by the registers CMPx_SELP<2:0> and CMPx_SELN<1:0>. For details, refer to the description of register simulation.

When the chip is powered on, the comparator module is OFF by default. The comparator is turned on by setting CMPxPDN = '1', and turn on the BGP module before turning on the comparator.

13 Temperature sensor

The chip has a built-in temperature sensor with the accuracy of ±2°C. The operating temperature of chips will be corrected before leaving the factory, and the corrected value is saved in the flash info area.

When the chip is powered on, the temperature sensor module is OFF by default. Turn on the BGP module before turning on the temperature sensor.

The temperature sensor is turned on by setting TMPPDN = '1', and it takes about 2us to be stable after turning on. Thus, it should be turned on at least 2us ahead before the ADC measures the sensor output.

14 Digital-to-analog Converter (DAC)

The chip has 2-channel 12bit DACs, and the maximum range of the output signal can be set to 1.2V/3V through the register DACx_GAIN.

The 12bit DACx can be output via IO ports P3.4 and P4.7 by setting register DACx_OUTEN = 1, which can drive a load resistance of over 5kΩ and a load capacitance of 50pF.

The maximum output code rate of the DAC is 1MHz.

When the chip is powered on, the DAC module is OFF by default. DAC can be turned on by setting DACx_PDN = 1. Turn on the BGP module before turning on the DAC module.

15 Processor Core

- 32bit RISC core, hardware floating point/DSP, with maximum operating frequency of 192MHz
- 2-wire SWD debug pin/4-wire Jtag debug pin

16 Storage Resources

16.1 Flash

- Built-in flash including 128kB/256kB main storage area and NVR information storage area
- Supporting repeatedly erasing and writing of no less than 20,000 times
- Data retention up to 20 years at room temperature 25°C
- Programming by Quad Word of up to 10us
- Erasing by Sector of 1024 bytes, with erasing time up to 4ms
- Flash data anti-theft (the last word must be written to any value other than 0xFFFFFFFF)

16.2 SRAM

- Built-in 40kB SRAM
- Supporting SRAM as Code RAM for key program acceleration

17 MCPWM for Motor Drive

- Two MCPWM modules
- Maximum operating clock frequency of 192 MHz
- Supporting up to 4 channels of phase-adjustable complementary PWM outputs, of which channels 2/3 can optionally be counted with a different time basis than 0/1
- Each channel deadband width supporting independent configuration
- Supporting edge-aligned PWM mode
- Supporting software-controlled IO mode
- Supporting IO polarity control function
- Internal short circuit protection to avoid short circuit due to configuration error
- External short-circuit protection for fast shutdown based on monitoring of external signals
- Internal ADC sampling interruption
- Pre-stored timer configuration parameters using load registers
- Configurable load register to load time and period

18 Timer

- 5-channel universal timer, 3-channel 16bit timer, 2-channel 32bit timer
- Supporting capture mode for measuring external signal width
- Supporting comparison mode for generating edge-aligned PWM/timing interruption
- There are four encoder modules integrated on the timer module, where the encoder 0/1/2/3 inputs are from Timer0/1/2/3 channel 0/1, respectively

19 Hall Sensor Interface

- Two Hall interface modules
- Built-in maximum 1024 filter
- 3-channel Hall signal input
- 24-bit counter, providing overflow and capture interruption

20 DMA

- One DMA engine
- Supporting up to 8 channels
- Supporting byte/halfword/word transfers of different sizes
- Supporting different address increment mode
- Supporting data transfer between flash/ram/peripherals
- Supporting cycle mode

21 FMAC

- 16-bit x 16-bit multiplier
- 24+2-bit accumulator, supporting saturation process
- 16-bit data input/output
- 256×16-bit local data storage
- Local memory can define up to 3 data cache areas (two input caches and one output cache). The cache base address and cache size can be configured via registers
- Input and output caches can be used as circular buffer
- Filtering functions: FIR, direct Type 1 IIR
- Vector operations: Dot product, convolution, correlation
- AHB bus interface
- Supporting DMA read/write data

22 CRC

- Supporting polynomials of different bit widths such as 7/8/16/32
- Supporting polynomial coefficient configuration
- Supporting input and output data flipping

23 Cordic

- Dedicated DSP for motor control algorithm, independent instruction set, three-stage pipeline
- Maximum operating frequency of 192 MHz
- Q15 format Cordic trigonometric function module, completing sin/cos/artanc calculation in 8 cycles

24 General Peripherals

- Three channel UART, full duplex operation, supporting 8/9 data bit, 1/2 stop bit, odd/even/no parity mode, with 1-byte forward cache, 1-byte receive cache, supporting Multi-drop Slave/Master mode, and baud rate of 300-115200
- Two channel SPI, supporting master/salve mode
- Two channel IIC, supporting master/salve mode
- One CAN
- Hardware watchdog: Independent watchdog using 32kHz RC clock drive, independent of the system high-speed clock, write-protected, with reset interval of 0.128~65 seconds; window watchdog using the system PLL divider clock for counting, which can provide accurate timing.

For different models of peripherals, please refer to the selection table in Section 2.

25 Special IO Multiplexing

Precautions for LKS45x Special I/O Multiplexing

SWD protocol contains two signal lines: SWDCLK and SWDIO. The former is the clock signal, which is in input state and will not change the state for the chip; and the latter is the data signal, which switches between input and output states during data transfer for the chip, with the default being the input state.

JTAG usually contains 5 signal lines, namely nTRST, TMS, TDI, TDO, TCLK.

LKS45x can multiplex Jtag/SWD into other IOs, and the multiplexed IO is P0 [13:9]. The precautions are as follows:

- By default, the multiplexing function is disabled, which can be enabled by software. That is, after the end of the chip hard reset, the initial state is Jtag/SWD, and Jtag/SWD has pull-up resistor inside the chip (with the pull-up resistance of about 40K inside the chip). Special attention shall be paid to the applications having requirements for the initial level.
- After enabling multiplexing, KEIL and other tools can not directly access the chip, that is, Debug and erase download functions are disabled. If you need to re-download the program, there are two options.
- First, it is recommended to use Linko's special offline downloader to erase. It is recommended to reserve a certain amount of time for software to enable multiplexing, for example, about 100ms, to ensure that the offline downloader can erase the program and prevent deadlock. The amount of time is to ensure the erasing success rate of offline downloader. The larger the time, the greater the probability of successful one-time erasure.
- Second, the program has an internal exit mechanism. For example, if an IO level changes (generally the input level), it indicates that Jtag/SWD needs to be used and the software will reconfigure to release the multiplexing. At this point, the KEIL function can be restored.

The RSTN signal is used as the external reset pin of the LKS45x chip by default.

LKS45x can multiplex RSTN into other IOs, and the multiplexed IO is P0.6. The precautions are as follows.

- By default, the multiplexing function is disabled, which can be enabled by software. That is, the initial state of the chip is RSTN, and RSTN has pull-up resistor inside the chip (with the pull-up resistance of about 40K inside the chip). Special attention shall be paid to the applications having requirements for the initial level.
- The default state is RSTN, and only after the normal release of RSTN can start the execution of the program. The application needs to ensure that RSTN has sufficient protection, such as peripheral circuits with pull-up resistor, and better if it can add a capacitor.
- After the multiplexing is enabled, the RSTN is disabled. To generate hard reset of the chip, it can only be implemented by power down/watchdog.
- The multiplexing of RSTN does not affect the use of KEIL.

BIT[5] of SYS_RST_CFG register is the multiplexing control switch for RSTN and P0.6.

26 Ordering Information

Device	Package Size	Quantity per disc/tube	Quantity in box	Quantity in case
LKS32MC451VCT8	LQFP100	90/disc	900PCS	5400PCS
LKS32MC451LVCT8	LQFP100	90/disc	900PCS	5400PCS
LKS32MC453RCT8	LQFP64	160/disc	1600PCS	9600PCS
LKS32MC454CCT8	TQFP48	250/disc	2500PCS	15000PCS
LKS32MC454NCQ8	QFN52	490/disc	4900PCS	29400PCS
LKS32MC455RCT8	LQFP64	160/disc	1600PCS	9600PCS
LKS32MC455LRCT8	LQFP64	160/disc	1600PCS	9600PCS
LKS32MC457LRCT8	LQFP64	160/disc	1600PCS	9600PCS

27 Version history

Table 27-1 Document's Version History

Time	Version No.	Description
2024.01.03	1.54	Added 457RCT8 model, updated 457L pin layout
2023.11.20	1.53	Update storage temperature, add description of OPA offset
2023.09.25	1.52	Update welding temperature
2023.07.09	1.51	Add LKS32MC457LRCT8
2023.04.07	1.50	Add model 454(QFN52)
2023.03.22	1.49	Add 454 and modified the LSI accuracy range
2023.02.06	1.48	Modify order packaging information,and the instruction that CAN must use external crystal
2023.02.04	1.47	ESD description minor revision
2023.01.15	1.46	Add ordering information and suggestion that CAN use XTAL
2023.01.12	1.45	Deleted reference to ADC having a 6MHz sampling rate
2022.12.14	1.44	Added a description of the maximum current value that LDO can provide
2022.11.10	1.43	Add connection resistance between IO and internal analog circuit
2022.09.28	1.42	Revised the naming rules of Section 1.2 and the ADC and OPA ranges
2022.08.04	1.41	Add LKS32MC455LRCT8
2022.05.27	1.4	Revised PIN4,5,11,12,19,20,21,22,54,55,59,63 of LKS32MC455RCT8
2022.04.09	1.3	Added LKS32MC455
2022.03.18	1.2	Changed the naming rules from 09x to 45x
2022.03.02	1.1	Revised the 451L electrical parameters of 5V power supply
2022.02.10	1.0	Released the official version

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