Linx TECHNOLOGIES

TRM-915-DTS / TRM-915-DTS-BRZ

Data Guide

(Preliminary)

Wireless made simple®

Electrical Specifications

Absolute Maximum Ratings

Operating the module in conditions that exceed the absolute maximum ratings may cause damage to the device. Operation at these ratings is not implied. Exposure to maximum rating conditions for an extended period of time may adversely affect device reliability.

Absolute Maximum Ratings			
Parameter	**Min.**	**Max.**	**Units**
Vdd – Power Supply		3.9	VDC
Voltage on any I/O pin	–0.3	5.3	VDC
Allowed Vdd Rise Time		1	ms
Input RF level		–1	dBm
Storage Temperature	–40	+85	°C

Figure 1: Absolute Maximum Ratings

Detailed Electrical Specifications

AC Specifications – RX					
Parameter	**Min.**	**Typ.**	**Max.**	**Units**	**Notes**
Receiver Frequency	902.2		927.8	MHz	At antenna pin
Channels: DTS Mode		32			
Channels: LP Mode		84			
Channel Spacing: DTS Mode		750		kHz	
Channel Spacing: LP Mode		300		kHz	
Receiver Sensitivity: DTS Mode		–100		dBm	152.34kbps RF
Receiver Sensitivity: DTS Mode		–102		dBm	38.4kbps RF
Receiver Sensitivity: DTS Mode		–104		dBm	9.6kbps RF
Receiver Sensitivity: LP Mode		–104		dBm	38.4kbps RF
Receiver Sensitivity: LP Mode		–105		dBm	9.6kbps RF
Input IP3		–40		dBm	F_{LO}+1MHz and F_{LO}+1.945MHz
Input Impedance		50		Ohms	No matching required
LO Leakage		–65		dBm	50ohm termination at ANT
Adjacent Channel Rejection		–48		dBc	Fc ± 650kHz
IF Bandwidth: DTS Mode		600		kHz	
IF Bandwidth: LP Mode		200		kHz	

Figure 2: AC Specifications – RX

DC Specifications					
Parameter	**Min.**	**Typ.**	**Max.**	**Units**	**Notes**
Operating Temperature	–40		+85	°C	HW Revision C and later
Supply Voltage	2.7	3.3	3.6	VDC	
Receive Current Consumption		16–24		mA	Continuous operation, Cdd = 3.3VDC, varies with UART data rate selected
Transmit Current Consumption					
Low Power		26–35		mA	Output into 50-ohm load, Vdd=3.3VDC, depends on data rate selected
Mid-Low Power		33–44		mA	
Mid-High Power		48–56		mA	
High Power		63-72		mA	
Standby Current Consumption		850		µA	Vdd = 3.3VDC
Sleep Current Consumption		35		µA	Vdd = 3.3VDC
Vih: Logic High Level Input	0.7*Vcc		5.0	VDC	
Vil: Logic Low Level Input	0		0.3*Vcc	VDC	
Voh: Logic High Level Output	2.5		Vcc	VDC	
Vol: Logic Low Level Output	0		0.4	VDC	

Figure 4: DC Specifications

Flash Specifications (Non-Volatile Registers)					
Parameter	**Min.**	**Typ.**	**Max.**	**Units**	**Notes**
Flash Write Duration		16	21	ms	Module stalled during write operation
Flash Write Cycles	20k	100k		cycles	

Figure 5: Flash Specifications (Non-Volatile Registers)

The module has a UART-type serial interface and contains special application software to create a transparent UART-to-antenna wireless solution capable of direct wire replacement in most embedded RS-232/422/485 applications.

> Note: Although the module is capable of supporting the typical serial communications required by RS-232, RS-422, and RS-485 networks, it is not compatible with the electrical interfaces for these types of networks. The module has CMOS inputs and outputs and would require an appropriate converter for the particular type of network it is connected to.

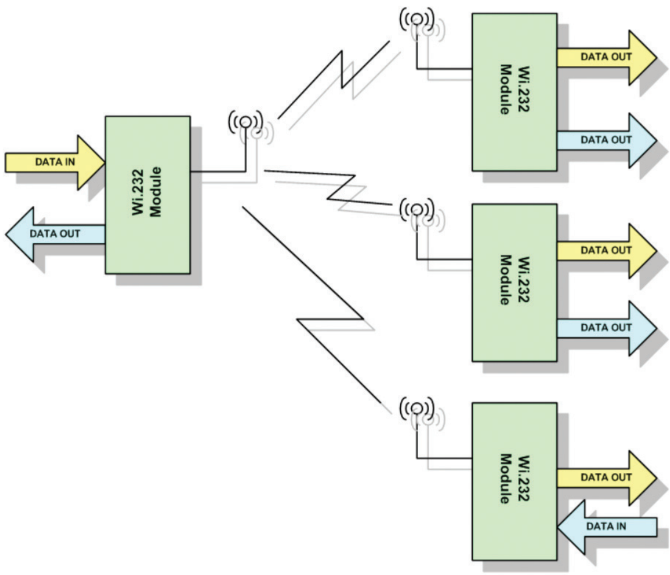

Figure 8: Wi.232DTS Networking Concept

The module is designed to interface directly to a host UART. Three signals are used to transfer data between the module and the host UART: **TXD**, **RXD** and **CTS**. **TXD** is the data output from the module. **RXD** is the data input to the module. **CTS** data output indicates the status of the module's data interface. If **CTS** is low, the module is ready to accept data. If **CTS** is high, the module is busy and the host UART should not send any further data.

Internally, the module has a 192 byte buffer for incoming characters from the host UART. The module can be programmed to automatically transmit for applications that are replacing legacy RS-485 networks. In peer-to-peer mode, any module can hear any other module. In both modes, group integrity is enforced.

When a module transmits a packet, all other modules on the same channel will receive the packet, check the packet for errors, and determine whether the received group ID matches the local group ID. If the packet is error free and the group IDs match, the module will decrypt the data if necessary, and send the error free data to its host UART for processing. The modules only implement the ISO reference network stack up to the MAC layer, so they are transparent to link layer addressing schemes. Therefore, the modules can work with any link-layer and higher protocols in existence today.

Certain features of the module are controlled through programmable registers. Registers are accessed by bringing **CMD** low. When **CMD** is low, all data transfers from the host UART are considered to be register access commands. When **CMD** is high, all data transfers from the host UART are considered to be raw data that needs to be transparently transmitted across the wireless link. The module maintains two copies of each register: one in flash and one in RAM. On reset, the module loads the RAM registers from the values in the flash registers. The module is operated out of the RAM registers. Applications that need to change parameters of the module often would simply modify the RAM registers. Putting default settings in the flash registers ensures the module always comes up in a preconfigured state, which is useful for applications that do not have external microcontrollers, such as RS-232 adapters.

The UART interface is capable of operating in full duplex at baud rates from 2.4 to 115.2kbps.

The module has ten power modes: High LP, Mid-High LP, Mid-Low LP, Low DTS, High DTS, Mid-High DTS, Mid-Low DTS, Low LP, Standby, and Sleep.

The DTS Series is the first module in the world to take advantage of the DTS digital spread spectrum provision in FCC part 15 rules. Under this provision, transmitters can operate at a higher output power if the transmission bandwidth is at least 500kHz. Through an encoding technique we call DirectSPREAD™, the outgoing RF data is encoded with symbols selected to ensure its average duty cycle is 50%. This allows the

MAC address that can be used by the host application for higher level, connection oriented protocols. This MAC address can be read through the command interface.

Operating States

The primary active state is the IDLE state. When the module is not actively transmitting or receiving data, it is in this state. While in this state, the receiver is enabled and the module is continuously listening for incoming data. If the module detects a pre-amble and valid start-code, it will enter the RX_HEADER state.

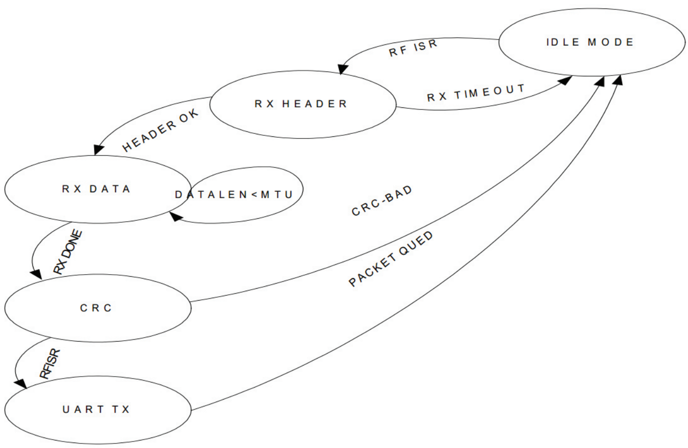

Figure 9: RX State Machine

If the module is in the IDLE state and a byte is received by the UART, it will enter the TX_WAIT state.

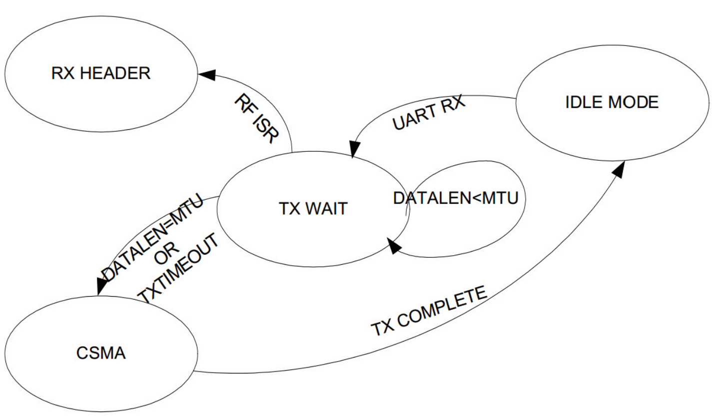

Figure 10: TX State Machine

Application Information

Pin-out Diagram

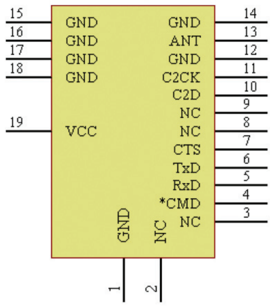

Figure 11: Pinout Diagram

Pin Descriptions

Pin Descriptions

No.	Description
1	Ground
2	No connect – reserved
3	No connect – reserved
4	Command input – active low
5	UART receive input
6	UART transmit output
7	UART clear to send output – active low
8	No connect – reserve
9	No connect – reserve
10	Reserved – ISP pin C2D
11	ISP pin C2CK/RST
12	Ground
13	Antenna port – 50ohm
14	Ground
15	Ground
16	Ground
17	Ground
18	Ground
19	VCC – 2.7 to 3.6 VDC

Legend

- (yellow) Signals used in this implementation
- (green) Signals not used in this implementation – do not connect
- (orange) Signals used for in-system programming

Figure 12: Pin Descriptions

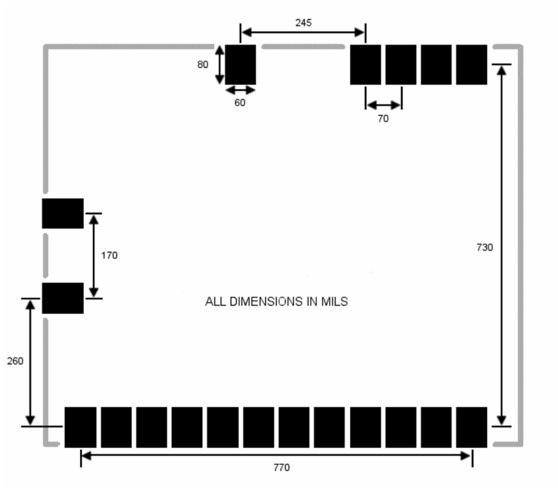

Figure 14: DTS Series Module Suggested Footprint

Example Circuit

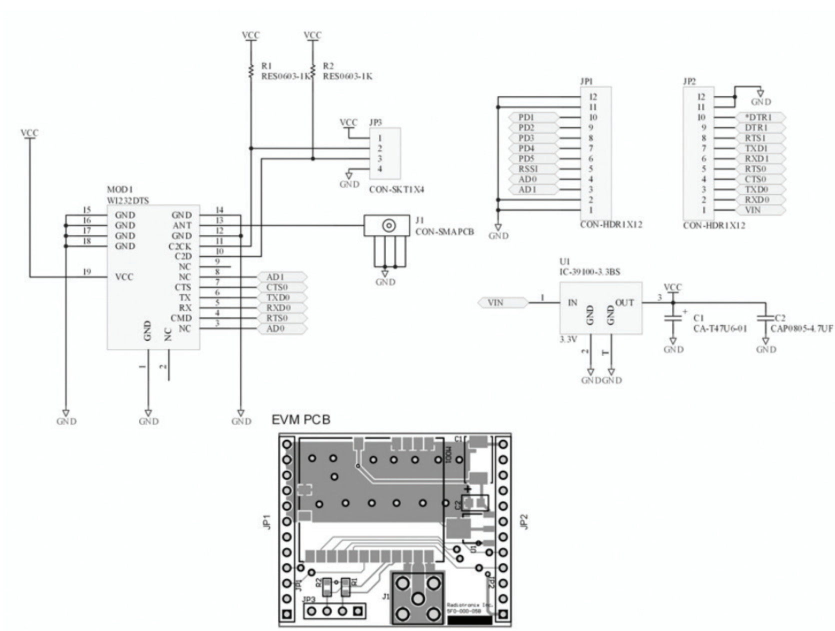

Figure 15: Evaluation Module Circuit

UART Interface

The UART interface is very simple; it is comprised of four CMOS compatible digital lines.

Pin Description		
Line	**Direction**	**Description**
CTS	Out	Clear to send – this pin indicates to the host micro when it is ok to send data. When CTS is high, the host micro should stop sending data to the module until CTS returns to the low state.
CMD	In	Command – the host micro will bring this pin low to put the module in command mode. Command mode is used to set and read the internal registers that control the operation of the module. When CMD is high, the module will transparently transfer data to and from other modules on the same channel. NOTE: If this pin is low when the module comes out of reset, the non-volatile registers will be reset to their factory programmed defaults. It is important to ensure that CMD is held high or left floating during power-up under normal conditions.
RXD	In	Receive data input.
TXD	Out	Transmit data output.

Figure 16: DTS Series UART Interface Lines

Antenna

The module is designed to work with any 900MHz 50ohm antenna, including PCB trace antennas.

Antenna selection is usually governed by application requirements. In general, external antennas perform better. Linx Technologies has a line of antennas and connectors that are compatible with the modules. Information on these products is available on our website at www.linxtechnologies.com/antennas.

As a rule, a ¼ wave whip or ½ wave dipole antenna with a good, solid ground plane (well-coupled, 3.5" x 3.5" or larger is optimal) is the best choice. Dipoles yield better performance than monopoles (whip) when the ground plane is smaller than optimal. However, many embedded applications cannot support an externally mountedantenna. If this is the case, a PCB antenna must be used. The designer can either use an off-of-the-shelf PCB antenna, such as the ANT-915-SP, or design a trace antenna. There are several good antenna tutorials and references on the Internet and we encourage the designer to use these resources.

For example, the link budget for a pair of modules in DTS mode at the maximum data rate and using 3dBi dipole antennas would be:

+11dBm + 3dB – (–100dBm) + 3dB = 117dB

A link budget of 117dB should easily yield a range of ¼ mile or more outdoors. If the environment is open and the antennas are 8 to 10 feet off of the ground, the range could be a mile. Indoors, this link budget should yield a range of several hundred feet.

This is a well-balanced link budget. More than 10dB of the budget is achieved through transmit power, which will allow good performance indoors in the presence of multi-path while keeping the overall operating current low, making the module suitable for primary battery powered applications such as RFID and automated meter reading.

The following equations can be used to calculate transmit center frequency in LP and DTS modes,remembering the exceptions listed above for the Anatel versions.

Fc = 902.271 + chan *.3007MHz(LP)
Fc = 902.272 + chan*.7517MHz(DTS)

All modules in a network must be in the same mode (LP or DTS) and must have the same transmit and receive channels programmed in order to communicate properly.

Power Mode

The transmission and reception modes of the module are determined by the settings of the **regPWRMODE** register. It is important to note that a module configured to operate in LP mode cannot "hear" another module transmitting in DTS mode, or vice versa. However, a module configured to operate in any of the three DTS modes can "hear" any other module transmitting in any of the DTS modes (provided that they are within range of one another). LP mode operation must be low power. Additional power settings are included for cases where the antenna circuit is very lossy, such as a PCB loop antenna.

regNVPWRMODE (0x02)					regPWRMODE (0x4D)		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
NA	NA	NA	NA	NA	PM2	PM1	PM0
7	6	5	4	3	2	1	0

Figure 18: Power Mode

Power Mode Register Settings			
PM1	**PM1**	**PM0**	**Mode**
0	0	0	LP Mode: low power setting
0	0	1	DTS Mode: mid-low power setting
0	1	0	DTS Mode: mid-high power setting
0	1	1	DTS Mode: high power setting
1	0	0	DTS Mode: low power setting
1	0	1	LP Mode: mid-low power setting
1	1	0	LP Mode: mid-high power setting
1	1	1	LP Mode: high power setting

Figure 19: Power Mode Register Settings

UART Data Rate

regNVDATARATE (0x03)					regDATARATE (0x4E)		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RES	RES	RES	RES	RES	BR2	BR1	BR0
7	6	5	4	3	2	1	0

Figure 22: UART Data Rate

By default, the UART data rate is set to 2.4kbps at the factory. This data rate can be changed by setting the **regDATARATE** register. Valid settings are shown in Figure 23.

Data Rate Register Settings

Baud Rate	BR2	BR1	BR0
2400	0	0	0
9600	0	0	1
19200	0	1	0
38400	0	1	1
57600	1	0	0
115200	1	0	1
10400*	1	1	0
31250*	1	1	1

* These data rates are not supported by PC serial ports. Selection of these rates may cause the module to fail to respond to a PC, requiring a reset to factory defaults.

Figure 23: Data Rate Register Settings

Troubleshooting Hint: Baud Rate Problems

If you lose track of the baud rate setting of the module, it will be impossible to program the module. You can either try every possible baud rate to discover the setting, or force a power-on reset with CMD held low to set the baud rate to its default: 2.4kbps.

Network Group

regNVNETGRP (0x06)					regNETGRP (0x51)		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
B7	B6	B5	B4	B3	B2	B1	B0
7	6	5	4	3	2	1	0

Figure 26: Network Group

Modules can be grouped into networks. Although only modules with the group ID will be able to talk to each other, modules in different groups but on the same channel will still coordinate transmissions through the CSMA mechanism. Valid values for this register are 0 to 127. The default group setting is 0.

CRC Control

regNVUSECRC (0x08)					regUSECRC (0x53)		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
B7	B6	B5	B4	B3	B2	B1	B0
7	6	5	4	3	2	1	0

Figure 27: CRC Control

Set to 0x01 to enable receive CRC checking, or 0x00 to disable it. The default CRC mode setting is enabled.

UART Minimum Transmission Unit

regNVUARTMTU (0x09)					regUARTMTU (0x54)		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
B7	B6	B5	B4	B3	B2	B1	B0
7	6	5	4	3	2	1	0

Figure 28: UART Minimum Transmission Unit

This register determines the UART buffer level that will trigger the transmission of a packet. The minimum value is 1 and the maximum value is 144. The default value for this register is 64, which provides a good mix of throughput and latency

By default, the module will send an acknowledgement character (0x06) to the UART TxD pin to let the calling application know that it is awake and ready. To control this feature, see “ACK on Wake” in this section.

ACK on Wake

regNVACKONWAKE (0x0E)					regACKONWAKE (0x59)		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
B7	B6	B5	B4	B3	B2	B1	B0
7	6	5	4	3	2	1	0

32: ACK on Wake

When the module’s RF components are ready to transmit/receive, the module can send an ACK character (0x06) to the host through the UART TxD pin. This notification let the host processor know when the module is ready to commence RF communications. Set this register to 0x00 to prevent the sending of this character, or 0x01 to allow the character to be sent. The default value for this register is 0x01.

MAC Address

regMAC5- regMAC0 (0x22-0x27)					N/A		
R	R	R	R	R	R	R	R
D7	D6	D5	D4	D3	D2	D1	D0
7	6	5	4	3	2	1	0

Figure 33: MAC Address

These registers make a unique 48-bit MAC address. These values are factory preset and cannot be altered. These address bytes are not used by the module. They are provided for customer applications as a unique address.

Register Summary

Volatile Read/Write Registers		
Name	**Address**	**Description**
regTXCHANNEL	0x4B	Transmit channel setting
regRXCHANNEL	0x4C	Receive channel setting
regPWRMODE	0x4D	Operating mode settings
regDATARATE	0x4E	UART data rate
regNETMODE	0x4F	Network mode (normal or slave)
regTXTO	0x50	Transmit wait timeout
regNETGRP	0x51	Network group ID
regUSECRC	0x53	Enable/disable CRC
regUARTMTU	0x54	Minimum transmission unit
regSHOWVER	0x55	Enable/disable start-up message
regCSMAMODE	0x56	Enable/disable CSMA
regSLPMODE	0x58	Power state of module
regACKONWAKE	0x59	Send ACK character to host on wake

Figure 36: Volatile Read/Write Registers

Non-Volatile Read-Only Registers		
Name	**Address**	**Description**
regMAC5	0x22	These registers form the unique 48-bit MAC address
regMAC4	0x23	
regMAC3	0x24	
regMAC2	0x25	
regMAC1	0x26	
regMAC0	0x27	
regRELEASENUM	0x78	Firmware release number

Figure 37: Volatile Read-Only Registers

Using Configuration Registers

CMD Pin

The CMD pin is used to inform the module where incoming UART information should be routed. When the CMD pin is high or left floating, all incoming UART information is treated as payload data and transferred over the wireless interface. If the CMD pin is low, the incoming UART data is routed to the command parser for processing. Since the module's processor looks at UART data one byte at a time, the CMD line must be held low for the entire duration of the command plus a 20µs margin for processing. Leaving the CMD pin low for additional time (for example, until the ACK byte is received by your application) will not adversely affect the module. If RF packets are received while the CMD line is active, they are still processed and presented to the module's UART for transmission.

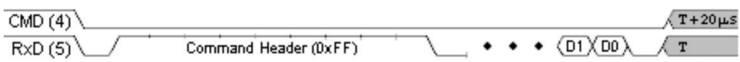

Figure 39: Command and CMD Pin Timing

Command Formatting

The DTS Series module contains several volatile and non-volatile registers that control its configuration and operation. The volatile registers all have a non-volatile mirror registers that are used to determine the default configuration when power is applied to the module. During normal operation, the volatile registers are used to control the module.

Placing the module in the command mode allows these registers to be programmed. Byte values in excess of 127 (0x80 or greater) must be changed into a two-byte escape sequence of the format: 0xFE, [value - 128]. For example, the value 0x83 becomes 0xFE, 0x03. The following function will prepend a 0xFF header and size specifier to a command sequence and create escape sequences as needed. It is assumed that *src is populated with either the register number to read (one byte, pass 1 into `src_len`) or the register number and value to write (two bytes, pass 2 into `src_len`). It is also assumed that the ***dest** buffer has enough space for the two header characters plus, the encoded command, and the null terminator.

Writing to Registers

Writing to a volatile register is nearly instantaneous. Writing to a non-volatile register, however, takes typically 16ms. Because the packet size can vary based on the need for encoding, there are two possible packet structures. The following tables show the byte sequences for writing a register in each case.

> **Warning:** Be sure that the module is properly powered and remains powered for the duration of the register write. Loss of important configuration information could occur if the unit loses power during a non-volatile write cycle.

<table>
<tr><th colspan="8">Byte 0</th><th colspan="8">Byte 1</th><th colspan="8">Byte 2</th><th colspan="8">Byte 3</th></tr>
<tr><td colspan="8">Header</td><td colspan="8">Size</td><td colspan="8">Register</td><td colspan="8">Value</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">0xFF</td><td colspan="8">0x02</td><td>0</td><td colspan="7">Register</td><td>0</td><td colspan="7">Value</td></tr>
</table>

Figure 41: Write Register Command, Value to be written is less than 128 (0x80)

<table>
<tr><th colspan="8">Byte 0</th><th colspan="8">Byte 1</th><th colspan="8">Byte 2</th><th colspan="8">Byte 3</th><th colspan="8">Byte 4</th></tr>
<tr><td colspan="8">Header</td><td colspan="8">Size</td><td colspan="8">Register</td><td colspan="8">Escape</td><td colspan="8">Value</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">0xFF</td><td colspan="8">0x03</td><td>0</td><td colspan="7">Register</td><td colspan="8">0xFE</td><td>0</td><td colspan="7">Lower 7 bits of Value</td></tr>
</table>

Figure 42: Write Register Command, Value to be written is greatre than or equal to 128 (0x80)

The module will respond to this command with an ACK (0x06). If an ACK is not received, the command should be resent. If a write is attempted to a read-only or invalid register, the module will respond with a NAK (0x15).

AC Specifications – TX					
Parameter	**Min.**	**Typ.**	**Max.**	**Units**	**Notes**
Transmit Frequency	902.2		927.8	MHz	
Maximum Effective RF Data Rate		100		kbps	Encoding/over-head losses included, 144 byte MTU
Center Frequency Error		2	5	ppm	915MHz at 25°C
Frequency Deviation: DTS Mode		235		kHz	
Frequency Deviation: LP Mode		75		kHz	
Low Output Power, Conducted		–4	–1	dBm	915MHz into 50ohm load
Mid-Low Output Power, Conducted		1	4	dBm	915MHz into 50ohm load
Mid-High Output Power, Conducted		11	14	dBm	915MHz into 50ohm load
Output Impedance		50		ohms	915MHz into 50ohm load
Carrier Phase Noise		TBD		dBc	Into 50ohm load
Harmonic Output		–50		dBc	Into 50ohm load

Figure 45: AC Specifications – TX

Custom Applications

For cost-sensitive applications, such as wireless sensors and AMR, Linx Technologies can embed the application software directly into the microcontroller built into the module. For more information on this service, please contact Linx Technologies.

Ordering Information

Ordering Information		
Product Part No.	**Description**	**Radiotronix Part No.**
TRM-915-DTS	North American Embedded Wireless Module (902–928Hz)	Wi.232DTS-R
TRM-915-DTS-BRZ	Brazilian Embedded Wireless Module (902–907, 915–928MHz)	Wi.232DTSB-R
TRM-868-EUR	European Union Embedded Wireless Module (868–870MHz)	WI.232EUR

Figure 48: Ordering Information

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Boulder, CO 80301

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