Linx TECHNOLOGIES

TRM-915-R250
RF Transceiver Module
Data Guide

Wireless made simple®

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Do not use this or any Linx product to trigger an action directly from the data line or RSSI lines without a protocol or encoder/ decoder to validate the data. Without validation, any signal from another unrelated transmitter in the environment received by the module could inadvertently trigger the action.

All RF products are susceptible to RF interference that can prevent communication. RF products without frequency agility or hopping implemented are more subject to interference. This module does have a frequency hopping protocol built in, but the developer should still be aware of the risk of interference.

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Ordering Information

Ordering Information		
Product Part No.	**Description**	**Radiotronix Part No.**
TRM-915-R250	Embedded Wireless Module, 250mW (900MHz)	Wi.232FHSS-250-R
TRM-915-R250-CFT	Embedded Wireless Module, 250mW (900MHz), Mexico	Wi.232-FHSS-250-CFTC-R
EVM-915-250-FCx	Pinned, Pre-Certified Module, 250mW (900MHz)	Wi.232FHSS-250-FCC-xx-R
EVM-915-250-CFx	Pinned, Pre-Certified Module, 250mW (900MHz), Mexico	Wi.232FHSS-250-FCC-CFTC-xx-R

x = 'R' for right angle connector, 'S' for straight connector
Transceivers are supplied in trays of 50 pieces

Figure 2: Ordering Information

Absolute Maximum Ratings

Absolute Maximum Ratings				
Supply Voltage V_{cc}	0	to	4.2	VDC
Any Input or Output Pin	0	to	5.0	VDC
Max Supply Voltage Rise Time (GND to 2.7V)			1	ms
Max RF Input		12		dBm
Operating Temperature	–40	to	+85	ºC
Storage Temperature	–40	to	+85	ºC

Exceeding any of the limits of this section may lead to permanent damage to the device. Furthermore, extended operation at these maximum ratings may reduce the life of this device.

Figure 3: Absolute Maximum Ratings

Warning: This product incorporates numerous static-sensitive components. Always wear an ESD wrist strap and observe proper ESD handling procedures when working with this device. Failure to observe this precaution may result in module damage or failure.

250 Series Transceiver Specifications						
Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Interface Section						
Input Logic Low	V_{IL}	0		0.8	VDC	
Input Logic High	V_{IH}	2.0		V_{CC}	VDC	
Output Logic Low	V_{OL}					
I_{OL} = 8.5mA				0.6	VDC	
I_{OL} = 10µA				0.1	VDC	
I_{OL} = 25mA			1.0		VDC	
Output Logic High	V_{OH}					
I_{OH} = -3mA		V_{CC}–0.7			VDC	
I_{OH} = -10µA		V_{CC}–0.1				
I_{OH} = -10mA			V_{CC}-0.8			
Flash Specifications (Non-Volatile Registers)						
Flash Write Duration			16		ms	
Flash Write Cycles		20k	100k		cycles	

1. V_{CC} = 3.3V
2. Into a 50-ohm load
3. At 25ºC
4. 26 channels each
5. At 10^{-3} BER
6. P_{in} = -20dBm, 2 CW interferers, F_{RF} = 915MHz, $F_1 = F_{RF}$ + 3MHz, $F_2 = F_{RF}$ + 6MHz, max gain, high-sensitivity
7. Desired signal 3dB above input sensitivity level, CW interferer power level increased until BER = 10^{-2}, +/–1MHz

Figure 4: Electrical Specifications

Pin Assignments

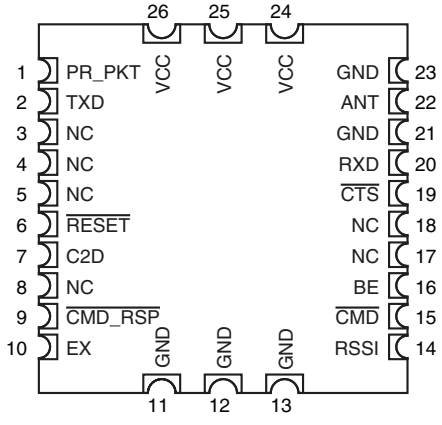

Figure 5: 250 Series Transceiver Pin Assignments (Top View)

Theory of Operation

The 250 Series transceiver is a low-cost, high-performance synthesized FSK transceiver. Its wideband operation gives it outstanding range while still meeting regulatory requirements. Figure 7 shows a block diagram for the module.

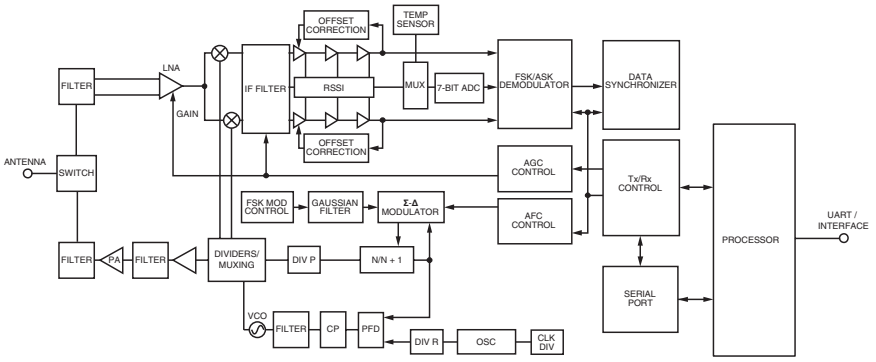

Figure 7: 250 Series Transceiver Block Diagram

The 250 Series transceiver is designed for operation in the 902 to 928MHz frequency band. The RF synthesizer contains a VCO and a low-noise fractional-N PLL. The receive and transmit synthesizers are integrated, enabling them to be automatically configured to achieve optimum phase noise, modulation quality and settling time.

The transmitter output power is programmable from +8dBm to +23.5dBm with automatic PA ramping to meet transient spurious specifications. The ramping and frequency deviation are optimized to deliver the highest performance over a wide range of data rates.

The receiver incorporates highly efficient low-noise amplifiers that provide up to –105dBm sensitivity.

An onboard controller performs the radio control and management functions. A processor performs the higher level protocol functions and controls the serial and hardware interfaces.

Module Operation

The module employs a Frequency Hopping Spread Spectrum (FHSS) algorithm. It has 32 channels spaced on 750kHz boundaries with a guard band on either side. These channels are pseudo-randomly arranged into six unique hopping tables comprised of 26 channels. The order of these tables is chosen so that cross-correlation is minimized, allowing multiple networks to operate in proximity with minimal interference.

When the module is not actively transmitting or receiving packets, it is in a scan state. It cycles through the channels in the hop sequence looking for a synchronizing packet. If it detects a preamble, it pauses to wait for the start code and packet header. If the packet is addressed to it, the module processes the packet and outputs the payload on the UART. If the packet is not addressed to the module or the start code and header fail their checks, the module resumes scanning for another packet.

When data is input on the RXD line for transmission, the module fills a buffer. Once the UART has buffered enough data to send (either regUARTMTU bytes input or regTXTO has expired between bytes on the RXD line), it transmits the data. The protocol engine makes a best-effort attempt to keep the data in at least regUARTMTU-sized packets, but splits the data based on the remaining dwell time before hopping. New data is not sent within the last 5% of the hop sequence, but data which is already in the process of being sent is processed normally.

The module prefixes the data with a packet header and postfixes the data with a 16-bit CRC. The 16-bit CRC error checking can be disabled to allow the host application to do its own error checking.

Initially, the transmission of the packet begins on a random hop index within the current hop sequence, and follows the hop sequence thereafter until synchronization is lost. The module uses a Carrier-Sense-Multiple-Access (CSMA) protocol to determine if another module is already transmitting on the selected channel. If the channel is occupied then the module waits for it to clear before transmitting its data.

Once the module gains access to the channel, if it is not already synchronized, it assigns itself master status, and sends a synchronizing preamble. Following a hop, the module that sends the first transmission assigns itself master status, sends a synchronizing preamble, and communications resume.

Low-Power States

The module supports three power saving modes: Standby, Sleep and Deep Sleep. Standby and Sleep are included primarily for legacy compatibility with DTS and EUR Series modules. The hardware required to support these two low-power modes fully is not present in the 25 Series modules. As a result, the current consumption in these two modes is considerably higher than their DTS / EUR counterparts. It is recommended that applications utilize the Deep Sleep mode for power savings.

In the Sleep and Deep Sleep modes, the transceiver is powered down and does not synchronize with other modules. Sleep mode draws more current than Deep Sleep mode. In Deep Sleep mode the module draws the least current. To wake the module up from this mode the $\overline{\text{RESET}}$ line must be held low for at least 20µs and then taken high. The module does not monitor the receive channel in either mode. Therefore, a sleeping module cannot be woken through the RF interface.

If regACKONWAKE is enabled, the module transmits a 0x06 character on the TXD line once awakened from a low-power mode or power-off state. This indicates that the module is ready to resume operations.

Figure 8 indicates the line states while in a low-power mode.

250 Series Transceiver Low-Power Line States

Line Name	Pin Number	Pin State
PR_PKT	1	Driven low
TXD	2	Input with weak pull-up
$\overline{\text{RESET}}$	6	Input with weak pull-up
C2D	7	Input with weak pull-up
$\overline{\text{CMD\_RSP}}$	9	Input with weak pull-up
EX	10	Driven low
RSSI	14	Driven low
$\overline{\text{CMD}}$	15	Input with weak pull-up
BE	16	Input with weak pull-up
$\overline{\text{CTS}}$	19	In Standby, Sleep: Driven Low, In Deep Sleep: Driven High
RXD	20	Input with weak pull-up

Figure 8: 250 Series Transceiver Low-Power Line States

Reset to Factory Default

It may be necessary to reset the non-volatile registers to their factory defaults. To reset the module, hold the $\overline{\text{CMD}}$ line low and cycle power to hardware-reset the module. The $\overline{\text{CMD}}$ line must remain low for a minimum of 600ms after resetting the module. Once the $\overline{\text{CMD}}$ line is released, the module's non-volatile registers are reset to factory defaults.

Compatibility Mode

The 250 Series modules support a mode that allows them to communicate with the smaller, lower power 25 Series modules. The 250 Series operates at a much narrower receive bandwidth (200kHz) than the 25 Series (600kHz). To allow interoperability, the 250 and 25 Series transceivers support a compatibility mode that allows the modules to communicate effectively with each other.

Compatibility mode reduces the maximum RF data rate to 76.8kbps. All UART baud rates are supported, although the RF data rates associated with baud rates 31,250; 38,400; 57,600 and 115,200 are reduced.

Automatic Gain Control and Manual Gain Control

The gain setting of the receiver's low noise amplifier (LNA) is adjustable. By default, the 250 Series is factory-configured to use its internal automatic gain control (AGC) circuit to manage receiver sensitivity. Reducing the gain increases the linearity of the receiver, but reduces maximum sensitivity; increasing the gain does the opposite. Generally speaking, higher linearity (increased third order input intercept point, IIP3) gives improved performance in high-interference environments; high gain yields better performance in low-interference environments.

The module contains an AGC circuit that manages these settings automatically, and it should be used whenever possible. However, when attempting to make analog RSSI measurements, fixing the LNA gain produces more meaningful results. Digital RSSI readings are internally compensated and may be taken with AGC enabled.

Exception Engine

The modules are equipped with an internal exception engine. If errors occur during module operation, an exception is raised. Exception codes are stored in the *regEXCEPTION* register and are cleared once they are read. If an exception code is already present in *regEXCEPTION* when an error occurs, the new exception code overwrites the old value.

Networking Modes

The module has a very flexible addressing and networking scheme selected with the regNVNETWORKMODE and regNETWORKMODE registers. It can be changed during operation. The transmitting module addresses packets according to the network mode configuration. The receiving module processes all addressing types regardless of the network mode configuration. If the received message matches the addressing criteria, it is output on the UART. Otherwise it is discarded.

There are three networking modes: GUID, User and Extended User. Each mode offers different communications schemes, but all use source and destination addressing. The source address is for the transmitting unit, the destination address is the intended receiver. Each mode uses different registers for the source and destination addresses.

The module supports an automatic addressing mode that reads the Source Address from a received packet and uses it to fill the Destination Address register. This makes sure that a response is sent to the device that transmitted the original message. This also allows the host microcontroller to read out the address of the sending unit.

The automatic addressing is enabled for the different networking modes with register regAUTADD and regNVAUTADD.

User Networking Mode

User Networking Mode is a more complicated scheme than GUID mode. It uses the customer ID bytes (regCUSTID[0-1]) and two of the user destination bytes (regUSERDESTID[0-1]) as a destination address. The customer ID bytes are programmed at the factory and cannot be changed. The module's local address is contained in two of the user source ID registers (regUSERSRCID[0-1]). Each module also has a user ID mask (regUSERIDMASK[0-1]) that provides an additional logical layer of addressing and can be used to create sub-networks. The receiving module masks its local address and the received destination address by calculating the logical AND with the user ID mask. If the results are equal, then the payload is output on the UART. The customer ID bytes are not masked, but must match the local value.

If acknowledgements are enabled, only the module with a user source ID that matches the transmitted user destination ID responds. The mask is not used for this determination.

If the result of the user ID Mask AND the received user destination address equals the same value as the user ID mask, then the payload data is output on the UART. This acts as a broadcast message to the network.

Setting the mask to 0xFFFF removes the mask and only the source and destination addresses are used for networking. When using user network mode to send packets to multiple users and the mask is not equal to 0xFFFF, acknowledgements must be disabled. Failure to do so could cause extreme delays in transmission and loss of data.

As an example, if the mask is 0xFFF0 and the destination address transmitted by the sender is 1234, then all modules with a source ID of 123x respond. This gives a subnet of 16 modules (where x = 0 to F) and acts as a broadcast message to the sub-net. Acknowledgements should be disabled.

Figure 14 shows this example and Figure 12 and Figure 13 show some more examples of user networking mode.

250 Series Transceiver User Network Mode Examples					
Destination ID from Received Packet	Receiver Source ID	Receiver User ID Mask	Result of Dest AND Mask	Result of Source AND Mask	Action
1234	Any module with 123x	FFF0	1230	1230	The results are equal, so the payload is output on the UART. **Do not enable acknowledgements**

Figure 14: 250 Series Transceiver User Network Mode Examples

Extended User Addressing Mode

Extended User Networking Mode is the same as User Networking Mode but uses longer addresses. The two customer ID bytes are still used (regCUSTID[0-1]) but all four bytes are used for the user destination address (regUSERDESTID[0-3]), user source ID (regUSERSRCID[0-3]) and user ID mask (regUSERIDMASK[0-3]). This provides more addressing capabilities at the expense of more overhead in the packet. Otherwise all functionality is the same.

250 Series Transceiver Extended User Network Mode Examples					
Sender			Receiver		
Network Mode	User SRCID	User DESTID	User SRCID	User IDMASK	Response
0x07	0x10000000	0xFFFFFFFF	0x20000001	0XFFFFFFFF	Data output by both modules. No ACK sent by either module.
			0x20000002	0xFFFFFFFF	
0x17	0x10000000	0xFFFFFFFF	0x20000001	0xFFFFFFFF	Data output by both modules. No ACK sent by either module. This configuration will cause transmission problems.
			0x20000002	0xFFFFFFFF	
0x17	0x10000000	0x30000001	0x20000001	0xE0000000	Data output. No ACK sent.
			0x30000001	0xE0000000	Data output. ACK sent to 0x1000.
0x07	0x10000000	0x30000002	0x20000001	0xF0000000	Not processed – discarded.
			0x30000001	0xF0000000	Data output. No ACK sent.

Figure 15: 250 Series Transceiver Extended User Network Mode Examples

Extended Preamble

As the receivers scan the hop sequence channels they look for the preamble from a transmitter. When they detect this preamble, they stop scanning and wait for a packet header. From the packet header they are able to lock on to the transmitter and synchronize the timing.

It is an advantage in some applications to keep the receivers asleep for long periods of time and wake them up only periodically to look for data. In this scenario it is quite possible for the receivers to miss the preamble from the transmitter and go to sleep without finding the transmission.

To address this issue, the modules can send an extended preamble. The extended preamble is much longer than the normal preamble and gives modules a larger window to detect and lock on to the transmitter.

There are two types of packets sent by the transmitter: synchronizing packets and data packets. The receivers use the synchronizing packets to lock on to the transmitters and follow them through the next hop. This packet is the first packet sent after every hop. The packets sent after the synchronizing packet and before the next hop are data packets. Receivers can catch and process data packets, but do not lock on and follow the transmitter unless they process the synchronizing packet.

It is important to note that an extended preamble packet may not be a synchronizing packet. If it is a data packet the receiver processes the packet and begins scanning again. It is important for the external processor or application to keep modules awake long enough to catch the synchronizing packet on the next hop. This ensures that the modules lock on to the transmitting module and receive all of the data.

The dwell time on each channel is approximately 395ms plus the times per baud rate shown in Figure 39. This can be shorter if the host processor determines that the necessary information has been received. Additionally the PR_PKT line can be used to determine that the module is processing a packet and keep it awake.

Voltage Supply Rise Time

The power supply rise time is extremely important. It must rise from ground to 2.7V in less than 1ms. If this specification cannot be met, an external reset supervisor circuit must be used to hold the module in reset until the power supply stabilizes. Failure to ensure adequate power supply rise time can result in loss of important module configuration information.

Using the Buffer Empty (BE) Line

The BE line indicates the state of the module's UART buffer. When the module receives data in the RXD line and the $\overline{\text{CMD}}$ line is high, the BE line is lowered until all data in the buffer has been processed by the protocol engine. If acknowledgement is not enabled, the BE line is raised as soon as the protocol engine processes the outgoing packets. If acknowledgement is enabled, the buffer is not updated until either the data transmissions are acknowledged by the remote end or delivery fails after the maximum number of retries. When the BE line returns high, the EX line may be sampled, or the regEXCEPTION register polled to determine if an error occurred during transmission.

Using the Exception (EX) Line

The EX line indicates whether or not a module exception has occurred. The line is normally low, but it is raised if an exception occurs that passes masking. When the regEXCEPTION register is read, the exception is cleared and the EX line returns low. If more than one exception occurs before the regEXCEPTION register is read, the old exception is overwritten by the new one. Please see the Exception Engine section for more details.

Using the Processing Incoming Packet (PR_PKT) Line

The PR_PKT line indicates whether the protocol engine has determined there to be valid or potentially valid data incoming. The line is normally low (not processing). When awake and not transmitting, the protocol engine is constantly searching for incoming data. When scoring indicates that a potential packet is inbound, this line is raised until either the scoring falls below a given threshold or the complete packet is received. It is possible that the packet scoring will fall below the threshold during reception, causing the line to be lowered. Such an instance can occur when the module hops to a channel late in the transmitter's extended preamble. Since there aren't a large number of valid bits to score, the line may fall during the packet start sequence. Once this sequence arrives, the PR_PKT signal rises and latches for the duration of the packet reception.

Using the $\overline{\text{RESET}}$ Line

The $\overline{\text{RESET}}$ line has different functions depending on the state the module is in. It is an open-drain input/output line with an integrated weak pull-up, so it is normally high. Because it periodically operates as an output, external control should only pull this line low, not high.

Hardware Reset (Input)

During normal operation, the $\overline{\text{RESET}}$ line functions as an active-low hardware reset input. Taking this line low for at least 15µs forces the module's controller into hardware reset. While the line is low, execution of module operations are suspended and all module lines revert to open-drain inputs with weak pull-ups. This behavior can be exploited during power-up if the V_{CC} ramp time exceeds 1ms. By suspending execution, the dangers associated with slow V_{CC} ramp are eliminated.

Wake from Deep Sleep (Input)

When the module is in deep sleep, all execution is suspended in the controller and the radio is in its lowest power mode. The $\overline{\text{RESET}}$ line must be lowered for at least 15µs to wake the module. When the $\overline{\text{RESET}}$ line is raised, execution begins in the controller. The module maintains its state engine while asleep. Because of this, it can detect whether the hardware reset was intended to cause a hard reset or wake the module. The controller's RAM is preserved during deep sleep. The RAM is checked prior to entering deep sleep, and examined upon waking. If the RAM contents are corrupted upon wake, the module issues itself a software reset to reinitialize the module.

Hardware Reset Indicator (Output)

When the module starts from power-off, or is reset by the internal V_{CC} monitor circuitry, the $\overline{\text{RESET}}$ line is driven low to indicate the reset state. During power-on reset, assuming the V_{CC} ramp time is valid, $\overline{\text{RESET}}$ is driven low from the time that V_{CC} reaches approximately 1V until V_{CC} reaches $V_{RST} + T_{PORDelay}$. $T_{PORDelay}$ is the power-on reset delay imposed by the controller's hardware.

The other event that drives the $\overline{\text{RESET}}$ line low is a low-voltage or brown-out condition. In this case, the V_{CC} monitor holds the module in reset, thus driving the $\overline{\text{RESET}}$ line low. It remains low until the power drops below the operating threshold for that circuit (becoming indeterminate), or until the module's power supply returns to V_{RST}. Figure 17 illustrates the operation of $\overline{\text{RESET}}$ as an output.

Using the Command Response ($\overline{\text{CMD\_RSP}}$) Line

The $\overline{\text{CMD\_RSP}}$ line is normally high, but the module lowers this line when responding to a UART command. This indicates to an external processor that the data on the TXD line is a response to a command and not data received over-the-air.

The module outputs received RF data immediately following the command response. The $\overline{\text{CMD\_RSP}}$ line does rise before resuming RF data, but some processors cannot react quickly enough to this signal and may not able to separate the command responses from RF data.
The regCMDHALT register controls the behavior of the TXD line when the $\overline{\text{CMD}}$ line is low and the external processor is configuring the module.
If this register is set to 0x01 and the $\overline{\text{CMD}}$ line is low, the module stops outputting the RF data and internally buffers it. Once the $\overline{\text{CMD}}$ line is raised, the buffered RF data is output on the TXD line. This allows the external processor to have separate configuration times and data times instead of potentially having to handle both at once.

The UART Interface

The module uses a standard UART interface for both data to be sent over the air and for configuring the module. The $\overline{\text{CMD}}$ line is used to tell the module if the data on the UART is for configuration or transmission. The lines follow the standard UART naming convention, so RXD is the data input into the module and TXD is the data output from the module. The UART interface expects 1 start bit, 8 data bits (LSB first), and 1 stop bit per byte with no parity (8-N-1).

The module has a 256 byte buffer for incoming data. The module can be programmed to automatically transmit when the buffer reaches a limit or based on the time between bytes on the UART. This allows the designer to optimize the module for fixed length and variable length data. The module supports streaming data as well. To optimize the module for streaming data, regUARTMTU should be set to 128, and regTXTO should be set to a value greater than 1 UART byte time at the current UART data rate (10 bit times rounded up) or 2, whichever is greater.

If the buffer gets nearly full (about 224 bytes), the module pulls the $\overline{\text{CTS}}$ line high, indicating that the host should not send any more data. Data sent by the host while the buffer is full is lost, so the the $\overline{\text{CTS}}$ line provides a warning and should be monitored. When there is data in the UART receive buffer, the BE line is low; when this buffer is empty, BE is high.

Configuration Command Formatting

The 250 Series module contains several volatile and non-volatile registers that control its configuration and operation. The volatile registers all have non-volatile mirror registers that are used to determine the default configuration when power is applied to the module. During normal operation, the volatile registers are used to control the module.

Placing the module in the command mode allows these registers to be programmed. Byte values in excess of 127 (0x80 or greater) must be changed into a two-byte escape sequence of the format:

0xFE, [value - 128]

For example, the value 0x83 becomes 0xFE, 0x03. The function in Figure 20 prepends a 0xFF header and size specifier to a command sequence and creates escape sequences as needed. It is assumed that *src is populated with either the register number to read (one byte, pass 1 into

Module Configuration

The 250 Series module contains several registers that control its configuration and operation. The module's default settings allow it to operate out of the box without any changes; however the registers allow the link to be customized to better suit the application if necessary. The register settings are stored in two types of memory inside the module. Volatile memory is quick to access, but it is lost when power is removed from the module. Non-volatile memory takes longer to access, but is retained when power is removed.

All of the configuration settings have registers in both types of memory. The settings are read from non-volatile registers on power up and saved in volatile registers. The values in the volatile registers are used during normal operation since it is faster to read and write the volatile memory locations. There are commands to read and write both locations.

Figure 21 shows the volatile read-only registers. Figure 22 shows the volatile read and write registers. Figure 23 shows the non-volatile read-only registers. Figure 24 shows the non-volatile read and write registers.

250 Series Volatile Read-Only Configuration Registers		
Name	**Address**	**Description**
regEXCEPTION	0x79	Stores latest exception code
regLGPRSSI	0x7B	Last Good Packet RSSI value
regIMMEDRSSI	0x7C	Current RSSI value

Figure 21: 250 Series Volatile Read Only Configuration Registers

250 Series Volatile Read / Write Configuration Registers		
Name	**Address**	**Description**
regCRCERRCOUNT	0x40	CRC error count value
regHOPTABLE	0x4B	Hop table
regPWRMODE	0x4D	Power amplifier setting
regUARTDATARATE	0x4E	UART data rate
regNETWORKMODE	0x4F	Sets the networking mode
regTXTO	0x50	UART to transmit timeout
regMAXTXRETRY	0x52	Maximum times to retry packet transmission
regUSECRC	0x53	Enable / Disable CRC checking
regUARTMTU	0x54	Minimum transmission unit
regCSMAMODE	0x56	Enable / Disable CSMA

250 Series Non-Volatile Read-Only Registers		
Name	**Address**	**Description**
regMyGUID[3]	0x34	Factory programmed GUID used in GUID Networking Mode
regMYGUID[2]	0x35	Factory programmed GUID used in GUID Networking Mode
regMYGUID[1]	0x36	Factory programmed GUID used in GUID Networking Mode
regMYGUID[0]	0x37	Factory programmed GUID used in GUID Networking Mode
regCUSTID[1]	0x39	Factory programmed customer ID, default 0xFF
regCUSTID[0]	0x3A	Factory programmed customer ID, default 0xFF
regRELEASENUM	0x78	Holds release number indicating h/w and f/w

Figure 23: 250 Series Non-volatile Read-Only Configuration Registers

250 Series Non-Volatile Read / Write Registers			
Name	**Address**	**Description**	**Factory Default**
regNVHOPTABLE	0x00	Hop table	0
regNVPWRMODE	0x02	Power amplifier setting	3 (High Power)
regNVUARTDATARATE	0x03	UART data rate	0 (2400)
regNVNETWORKMODE	0x04	Sets the networking mode	4 (MAC/GUID)
regNVTXTO	0x05	UART to transmitter timeout	16 (15–16ms)
regNVMAXTXRETRY	0x07	Maximum times to retry packet transmission	26
regNVUSECRC	0x08	Enable/Disable CRC checking	1 (Enable)
regNVUARTMTU	0x09	Minimum transmission unit	64 (64 bytes)
regNVSHOWVERSION	0x0A	Enable/disable startup message	1 (Enabled)
regNVCSMAMODE	0x0B	Enable/Disable CSMA	1 (Enable)
regNVOPMODE	0x0D	Sets operating mode	0 (Awake)
regNVACKONWAKE	0x0E	Enable/Disable ACK sent to UART upon wake from	1 (Enable)
regNVUSERDESTID[3]	0x0F	Destination Address for Extended User Networking Mode	0xFF
regNVUSERDESTID[2]	0x10	Destination Address for Extended User Networking Mode	0xFF
regNVUSERDESTID[1]	0x11	Destination Address for User and Extended User Networking Mode	0xFF

Writing to Registers

Writing to a volatile register is nearly instantaneous. Writing to a non-volatile register typically takes 16ms. Because the packet size can vary based on the need for encoding, there are two possible packet structures. The first structure writes a value that is less than 128 (0x80) and the second writes a value that is higher. The higher value must be split into two values. Figure 25 shows the byte sequences for writing a register in each case.

250 Series Write to Configuration Register Command

Command for a Value less than 128 (0x80)

Header	Size	Address	Value
0xFF	0x02	REG	V1

Command for a Value greater than 128 (0x80)

Header	Size	Address	Value 1	Value 2
0xFF	0x03	REG	0xFE	V2

Figure 25: 250 Series Write to Configuration Register Command

The module responds with an ACK (0x06). If it is not received, the command should be resent. The module responds with a NACK (0x15) if a write is attempted to a read-only or invalid register.

Warning: The module must remain powered for the duration of the register write or important configuration information could be lost.

Reading from Registers

A register read command is constructed by placing an escape character (0xFE) before the register number. The module responds by sending an ACK (0x06) followed by the register number and register value. The register value is sent unmodified, so if the register value is 0x83, 0x83 is returned. If the register number is invalid, the module responds with a NACK (0x15). The command and response are shown in Figure 26.

250 Series Read From Configuration Register

Command

Header	Size	Escape	Address
0xFF	0x02	0xFE	REG

Response

ACK	Address	Value
0x06	REG	V1

Figure 26: 250 Series Read from Configuration Register Command and Response

250 Series RF Channels and Hop Sequences							
Channel Number	Frequency (MHz)	Hop Sequence by Channel Number					
		0	1	2	3	4	5
0	902.971	16	15	3	28	22	9
1	903.723	1	30	20	11	7	24
2	904.475	2	29	21	10	8	23
3	905.226	5	26	24	7	11	20
4	905.978	10	21	29	2	16	15
5	906.730	21	10	8	23	27	4
6	907.482	11	20	30	1	17	14
7	908.234	23	8	10	21	29	2
8	908.986	14	17	1	30	20	11
9	909.737	29	2	16	15	3	28
10	910.489	27	4	14	17	1	30
11	911.241	22	9	9	22	28	3
12	911.993	12	19	31	0	18	13
13	912.745	24	7	11	20	30	1
14	913.496	17	14	4	27	23	8
15	914.248	3	28	22	9	9	22
16	915.000	7	24	26	5	13	18
17	915.752	15	16	2	29	21	10
18	916.504	31	0	18	13	5	26
19	917.255	30	1	17	14	4	27
20	918.007	28	3	15	16	2	29
21	918.759	25	6	12	19	31	0
22	919.511	19	12	6	25	25	6
23	920.263	6	25	25	6	12	19
24	921.015	13	18	0	31	19	12
25	921.766	26	5	13	18	0	31
26	922.518						
27	923.270						
28	924.022						
29	924.774						
30	925.525						
31	926.277						

Figure 29: 250 Series RF Channels and Hop Sequences

UART Data Rate - Address = 0x4E; NV Address = 0x03

The value in regUARTDATARATE sets the data rate of the UART interface. Changing the non-volatile register changes the data rate on the following power-up or reset. Changing the volatile register changes the data rate immediately following the command acknowledgement. Figure 32 shows the command and response and Figure 33 shows the valid settings.

250 Series UART Data Rate

Read Command

Header	Size	Escape	Address
0xFF	0x02	0xFE	0x4E 0x03

Read Response

ACK	Address	Value
0x06	0x4E 0x03	V1

Write Command

Header	Size	Address	Value
0xFF	0x02	0x4E 0x03	V1

Figure 32: 250 Series UART Data Rate Command and Response

250 Series UART Data Rate Register Settings

V1	Baud Rate
0x00	2,400
0x01	9,600
0x02	19,200
0x03	38,400
0x04	57,600
0x05	115,200
0x06	10,400*
0x07	31,250*

* These data rates are not supported by PC serial ports. Selection of these rates may cause the module to fail to respond to a PC, requiring a reset to factory defaults.

Figure 33: 250 Series UART Data Rate Settings

If the UART rate is different than the host processor UART rate then the module will not communicate correctly. If mismatched, every rate can be tested until the correct one is found or the module can be reset to factory defaults.

Transmit Wait Timeout - Address = 0x50; NV Address = 0x05

When a byte is received from the UART, the module starts a timer that counts down every millisecond. The timer is restarted when each byte is received. The value for the regTXTO register is the number of milliseconds to wait before transmitting the data in the UART receive buffer. The default setting for this register is 0x10 (~16ms delay).

If the timer reaches zero before the next byte is received from the UART, the module begins transmitting the data in the buffer. This timeout value should be greater than one byte time at the current UART data rate with a minimum of 0x02. It should not be set to a value of 0x01 or any value less than one byte time as unpredictable results could occur.

If the timeout value is set to 0x00, the transmit wait timeout is deactivated. In this case, the transceiver waits until a number of bytes equal to the Minimum Transmission Unit (MTU) have been received by the UART. All of the bytes are sent once the MTU has been reached. Figure 36 shows examples of the commands. Figure 37 shows the minimum timeout values based on baud rate.

250 Series Transmit Wait Timeout

Read Command

Header	Size	Escape	Address
0xFF	0x02	0xFE	0x50 0x05

Read Response

ACK	Address	Value
0x06	0x50 0x05	V1

Write Command

Header	Size	Address	Value
0xFF	0x02	0x50 0x05	V1

Figure 36: 250 Series Transmit Wait Timeout Command and Response

250 Series Minimum TXTO Values

Baud Rate	Minimum TXTO
2,400	6ms
9,600	3ms
19,200	2ms
38,400	2ms
57,600	2ms
115,200	2ms

Figure 37: 250 Series Transmit Wait Timeout Minimum Values

CRC Control - Address = 0x53; NV Address = 0x08

The 250 Series protocol includes a Cyclic Redundancy Check on the received packets to make sure that there are no errors. Any packets with errors are discarded and not output on the UART. This feature can be disabled if it is desired to perform error checking outside the module. Set the regUSECRC register to 0x01 to enable CRC checking, or 0x00 to disable it. The default CRC mode setting is enabled. Figure 40 shows examples of the commands and Figure 41 shows the available values.

250 Series CRC Control

Read Command

Header	Size	Escape	Address
0xFF	0x02	0xFE	0x53 0x08

Read Response

ACK	Address	Value
0x06	0x53 0x08	V1

Write Command

Header	Size	Address	Value
0xFF	0x02	0x53 0x08	V1

Figure 40: 250 Series CRC Control Command and Response

250 Series CRC Control Register Settings

V1	Mode
0x00	CRC Disabled
0x01	CRC Enabled

Figure 41: 250 Series CRC Control Register Settings

Show Version - Address = 0x0A

Setting this register to 0x00 suppresses the start-up message, including firmware version, which is sent to the UART when the module is reset. A value of 0x01 causes the message to be output after reset. By default, the module start-up message is output. Figure 43 shows examples of the commands and Figure 44 shows the available values.

250 Series Show Version

Read Command

Header	Size	Escape	Address
0xFF	0x02	0xFE	0x0A

Read Response

ACK	Address	Value
0x06	0x0A	V1

Write Command

Header	Size	Address	Value
0xFF	0x02	0x0A	V1

Figure 43: 250 Series Show Version Command and Response

250 Series Show Version Register Settings

V1	Meaning
0x00	Startup message is NOT output on reset or power-up.
0x01	Startup message is output on reset or power-up. This is a blocking call, and any incoming UART data is lost during the transmission of this message through the TXD line. All UART commands must be sent after this message has completed.
0x02	Startup message is displayed upon reset or power-up. This is a non-blocking call. Any incoming UART data is buffered, and incoming UART commands are processed. If a change of baud rate is commanded while the startup message is being output, the current byte finishes at the current baud rate, and subsequent bytes are transmitted at the new baud rate.

Figure 44: 250 Series Show Version Register Settings

Operating Mode - Address = 0x58; NV Address = 0x0D

The value in the regOPMODE register sets the operating mode of the transceiver. If the module remains properly powered, and is awakened from a low power mode properly, the volatile registers retain their values when awakened. If the volatile registers become corrupted during low power, a software reset is forced and the module reboots.

Awake mode is the normal operating mode. This is the only mode in which the RF circuitry is able to receive and transmit RF messages.

Standby leaves the RF oscillator circuit operating for faster wakeup, whereas Sleep does not. One byte of 0x0F to the module's RXD line at the current baud rate wakes the modules.

Deep Sleep mode disables all circuitry on-board the module. This is the lowest-power mode available for the module. A low pulse on the $\overline{\text{RESET}}$ line of at least 15µs wakes the module. The module begins the wake process once the $\overline{\text{RESET}}$ line is returned high.

Please see the Low Power States section for more details. Figure 47 shows examples of the commands and Figure 48 shows the available values.

250 Series Operating Mode

Read Command

Header	Size	Escape	Address
0xFF	0x02	0xFE	0x58 0x0D

Read Response

ACK	Address	Value
0x06	0x58 0x0D	V1

Write Command

Header	Size	Address	Value
0xFF	0x02	0x58 0x0D	V1

Figure 47: 250 Series Operating Mode Command and Response

250 Series Operating Mode Register Settings

V1	Mode
0x00	Awake Mode
0x01	Sleep Mode
0x02	Standby Mode
0x03	Deep Sleep Mode

Figure 48: 250 Series Operating Mode Register Settings

User Destination ID

These registers contain the address of the destination module when User Networking mode or Extended User Networking mode are enabled. User Networking mode uses bytes 0 and 1 to determine the destination address. Extended User Networking mode uses all four bytes. Please see the Networking Modes section for more details. Each register byte is read and written separately.

Figure 51 shows the User Destination ID Registers.

250 Series User Destination ID Registers

Name	Volatile Address	Non-Volatile Address	Description
regUSERDESTID[3]	0x5A	0x0F	MSB of the extended destination address
regUSERDESTID[2]	0x5B	0x10	Byte 2 of the extended destination address
regUSERDESTID[1]	0x5C	0x11	Byte 1 of the extended destination address, MSB of the short destination address
regUSERDESTID[0]	0x5D	0x12	LSB of the extended destination address and short destination address

Figure 51: 250 Series User Destination ID Registers

User Source ID

These registers contain the address of the source module when User Networking mode or Extended User Networking mode are enabled. User Networking mode uses bytes 0 and 1 to determine the source address. Extended User Networking mode uses all four bytes. Please see the Networking Modes section for more details. Each register byte is read and written separately.

Figure 52 shows the User Source ID Registers.

250 Series User Source ID Registers

Name	Volatile Address	Non-Volatile Address	Description
regUSERSRCID[3]	0x5E	0x13	MSB of the extended source address
regUSERSRCID[2]	0x5F	0x14	Byte 2 of the extended source address
regUSERSRCID[1]	0x60	0x15	Byte 1 of the extended source address MSB of the short source address
regUSERSRCID[0]	0x61	0x16	LSB of the extended source address and short source address

Figure 52: 250 Series User Source ID Registers

Exception Mask - Address = 0x6C; NV Address = 0x21

The module has a built-in exception engine that can notify the host processor of an unexpected event. When an exception occurs, this register is ANDed with the exception code. A non-zero result causes the EX line to be asserted. Reading the regEXCEPTION register clears the exception and resets the EX line. If the result is zero, the EX line is not asserted but the exception code is stored in the regEXCEPTION register.

Figure 55 shows examples of the commands and Figure 56 shows the available values.

250 Series Exception Masks

Read Command

Header	Size	Escape	Address
0xFF	0x02	0xFE	0x6C 0x21

Read Response

ACK	Address	Value
0x06	0x6C 0x21	V1

Write Command

Header	Size	Address	Value
0xFF	0x02	0x6C 0x21	V1

Figure 55: 250 Series Transceiver Exception Mask Command and Response

250 Series Example Exception Masks

V1	Exception Name
0x08	Allows only EX_BUFOVFL and EX_RFOVFL to trigger the EX line
0x10	Allows only EX_WRITEREGFAILED to trigger the EX line
0x20	Allows only EX_NORFACK to trigger the EX line
0x40	Allows only EX_BADCRC, EX_BADHEADER, EX_BADSEQID and EX_ BADFRAMETYPE exceptions to trigger the EX line
0x60	Allows EX_BADCRC, EX_BADHEADER, EX_BADSEQID, EX_BADFRAMETYPE and EX_NORFACK exceptions to trigger the EX line
0xFF	Allows all exceptions to trigger the EX line

Figure 56: 250 Series Transceiver Example Exception Masks

Receiver LNA Mode - Address = 0x6F; NV Address = 0x24

By default, the module is factory-configured to use its internal Automatic Gain Control (AGC) circuit to manage receiver sensitivity. Reducing the gain increases the linearity of the receiver, but reduces maximum sensitivity; increasing the gain does the opposite. Generally speaking, higher linearity (increased third order input intercept point, IIP3) gives improved performance in high-interference environments; high gain yields better performance in low-interference environments.

The module contains an AGC circuit that manages these settings automatically, and it should be used whenever possible. When reading the digital RSSI registers (regIMMEDRSSI, regLGPRSSI), the internal calculation automatically compensates for the current LNA gain setting. However, when attempting to make analog RSSI measurements, fixing the LNA gain produces more meaningful results.

Figure 59 shows examples of the commands and Figure 60 shows the available values.

250 Series LNA Mode

Read Command

Header	Size	Escape	Address
0xFF	0x02	0xFE	0x6F 0x24

Read Response

ACK	Address	Value
0x06	0x6F 0x24	V1

Write Command

Header	Size	Address	Value
0xFF	0x02	0x6F 0x24	V1

Figure 59: 250 Series Transceiver LNA Mode Command and Response

250 Series LNA Mode Register Settings

V1	Meaning	IIP3 Increase	Sensitivity Decrease
0x00	AGC Enabled	Variable	Variable
0x01	High Sensitivity	Reference	Reference
0x02	Mid Linearity	19.1dB	6.5dB
0x03	High Linearity	41.8dB	9.5dB

Figure 60: 250 Series Transceiver LNA Mode Register Settings

As an example, if regAUTADD is set to 0x0F (Any Auto Address) and a GUID packet is received from another module, then regAUTADD reads back as 0x4F. The lower 4 bits indicate that the module is set to any auto address (0xF). The upper 4 bits indicate that the packet that was just received was a GUID Network Mode packet (0x4).

Figure 63 summarizes the configuration values for the lower 4 bits of the register.

250 Series Auto Addressing Register Settings

Auto Address Value	Meaning	Action
0x00	Auto Addressing disabled	Destination Registers not populated
0x04	GUID Auto Address	Auto-populates GUID Address Destination Register Only
0x06	User Auto Address Mode	Auto-populates User Address Destination Register
0x07	Extended User Auto Address Mode	Auto-populates User Address Destination Register
0x0F	Any Auto Address Mode	Auto-populates GUID Address Destination Register

Figure 63: 250 Series Transceiver Auto Addressing Register Settings

Figure 64 shows the Network Mode values that the module writes to the upper 4 bits after successfully receiving a packet.

250 Series Auto Addressing Network Mode Indicator

Network Mode	Meaning
0x4	GUID Networking Mode
0x6	User Networking Mode
0x7	Extended User Networking Mode

Figure 64: 250 Series Transceiver Auto Addressing Network Mode Indicator

Exception - Address = 0x79

The module has a built-in exception engine that can notify the host processor of an unexpected event. If an exception occurs, the exception code is stored in this register. Reading from this register clears the exception and, if applicable, resets the EX line. If an exception occurs before the previous exception code is read, the previous value is overwritten. Figure 68 shows examples of the commands and Figure 69 shows the available values.

250 Series Exception

Read Command				Read Response		
Header	Size	Escape	Address	ACK	Address	Value
0xFF	0x02	0xFE	0x79	0x06	0x79	V1

Figure 68: 250 Series Transceiver Exception Command and Response

250 Series Transceiver Exception Codes

V1	Exception Name	Description
0x08	EX_BUFOVFL	Internal UART buffers overflowed.
0x09	EX_RFOVFL	Internal RF packet buffer overflowed.
0x13	EX_WRITEREGFAILED	Attempted write to register failed.
0x20	EX_NORFACK	Acknowledgement packet not received after maximum number of retries.
0x40	EX_BADCRC	Bad CRC detected on incoming packet.
0x42	EX_BADHEADER	Bad CRC detected in packet header.
0x43	EX_BADSEQID	Sequence ID was incorrect in ACK packet.
0x44	EX_BADFRAMETYPE	Unsupported frame type specified.

Figure 69: 250 Series Transceiver Exception Codes

Custom ID

These registers contain the factory-programmed custom ID. A value is assigned to OEM customer with a custom version of the module. Contact Linx for details. Figure 70 shows the GUID Registers.

250 Series Custom ID Registers

Name	Non-Volatile Address	Description
regCUSTID[1]	0x39	MSB of the custom ID
regCUSTID[0]	0x3A	LSB of the custom ID

Figure 70: 250 Series Transceiver Custom ID

Typical Applications

Figure 73 shows a circuit using the 250 Series transceiver.

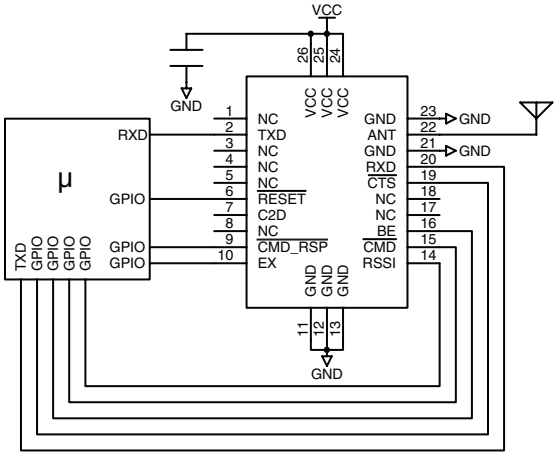

Figure 73: 250 Series Transceiver Basic Application Circuit

The transceiver UART is connected to a microcontroller UART for communication of configuration data and data to be sent over the air. The microcontroller is connected to the $\overline{\text{CMD-RSP}}$, EX, $\overline{\text{CMD}}$, BE and $\overline{\text{CTS}}$ lines to monitor the current state of the module. It monitors the RSSI line to monitor the strength of the incoming RF signal.

There is no need for buffering or other circuitry between the transceiver and microcontroller provided that both are operating on the same voltage.

Power Supply Requirements

The module does not have an internal voltage regulator, therefore it requires a clean, well-regulated power source. The power supply noise should be less than 20mV. Power supply noise can significantly affect the module's performance, so providing a clean power supply for the module should be a high priority during design.

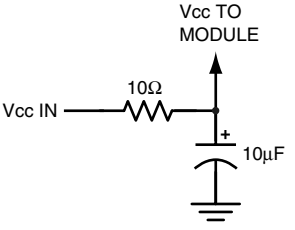

Figure 74: Supply Filter

A 10Ω resistor in series with the supply followed by a 10μF tantalum capacitor from V_{cc} to ground helps in cases where the quality of supply power is poor (Figure 74). This filter should be placed close to the module's supply lines. These values may need to be adjusted depending on the noise present on the supply line.

Interference Considerations

The RF spectrum is crowded and the potential for conflict with unwanted sources of RF is very real. While all RF products are at risk from interference, its effects can be minimized by better understanding its characteristics.

Interference may come from internal or external sources. The first step is to eliminate interference from noise sources on the board. This means paying careful attention to layout, grounding, filtering and bypassing in order to eliminate all radiated and conducted interference paths. For many products, this is straightforward; however, products containing components such as switching power supplies, motors, crystals and other potential sources of noise must be approached with care. Comparing your own design with a Linx evaluation board can help to determine if and at what level design-specific interference is present.

External interference can manifest itself in a variety of ways. Low-level interference produces noise and hashing on the output and reduces the link's overall range.

High-level interference is caused by nearby products sharing the same frequency or from near-band high-power devices. It can even come from your own products if more than one transmitter is active in the same area. It is important to remember that only one transmitter at a time can occupy a frequency, regardless of the coding of the transmitted signal. This type of interference is less common than those mentioned previously, but in severe cases it can prevent all useful function of the affected device.

Although technically not interference, multipath is also a factor to be understood. Multipath is a term used to refer to the signal cancellation effects that occur when RF waves arrive at the receiver in different phase relationships. This effect is a particularly significant factor in interior environments where objects provide many different signal reflection paths. Multipath cancellation results in lowered signal levels at the receiver and shorter useful distances for the link.

Pad Layout

The pad layout diagram in Figure 79 is designed to facilitate both hand and automated assembly.

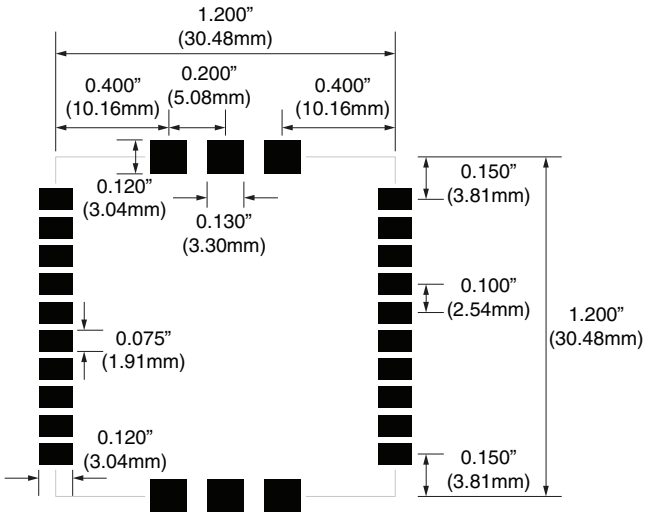

Figure 79: Recommended PCB Layout

Board Layout Guidelines

The module's design makes integration straightforward; however, it is still critical to exercise care in PCB layout. Failure to observe good layout techniques can result in a significant degradation of the module's performance. A primary layout goal is to maintain a characteristic 50-ohm impedance throughout the path from the antenna to the module. Grounding, filtering, decoupling, routing and PCB stack-up are also important considerations for any RF design. The following section provides some basic design guidelines.

During prototyping, the module should be soldered to a properly laid-out circuit board. The use of prototyping or "perf" boards results in poor performance and is strongly discouraged. Likewise, the use of sockets can have a negative impact on the performance of the module and is discouraged.

The module should, as much as reasonably possible, be isolated from other components on your PCB, especially high-frequency circuitry such as crystal oscillators, switching power supplies, and high-speed bus lines.

When possible, separate RF and digital circuits into different PCB regions.

Production Guidelines

The module is housed in a hybrid SMD package that supports hand and automated assembly techniques. Since the modules contain discrete components internally, the assembly procedures are critical to ensuring the reliable function of the modules. The following procedures should be reviewed with and practiced by all assembly personnel.

Hand Assembly

Pads located on the bottom of the module are the primary mounting surface (Figure 80). Since these pads are inaccessible during mounting, castellations that run up the side of the module have been provided to facilitate solder wicking to the module's underside. This allows for very quick hand soldering for prototyping and small volume production. If the recommended pad guidelines have been followed, the pads will protrude slightly past the edge of the module. Use a fine soldering tip to heat the board pad and the castellation, then introduce solder to the pad at the module's edge. The solder will wick underneath the module, providing reliable attachment. Tack one module corner first and then work around the device, taking care not to exceed the times in Figure 81.

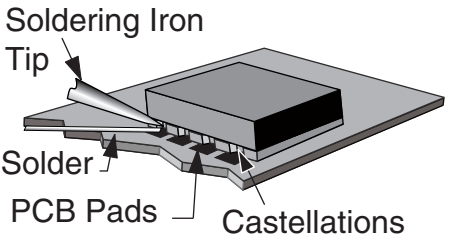

Figure 80: Soldering Technique

Warning: Pay attention to the absolute maximum solder times.

Absolute Maximum Solder Times
Hand Solder Temperature: +225ºC for 10 seconds
Reflow Oven: +225ºC max (see Figure 82)

Figure 81: Absolute Maximum Solder Times

Automated Assembly

For high-volume assembly, the modules are generally auto-placed. The modules have been designed to maintain compatibility with reflow processing techniques; however, due to their hybrid nature, certain aspects of the assembly process are far more critical than for other component types. Following are brief discussions of the three primary areas where caution must be observed.

General Antenna Rules

The following general rules should help in maximizing antenna performance.

1. Proximity to objects such as a user's hand, body or metal objects will cause an antenna to detune. For this reason, the antenna shaft and tip should be positioned as far away from such objects as possible.

2. Optimum performance is obtained from a ¼- or ½-wave straight whip mounted at a right angle to the ground plane (Figure 83). In many cases, this isn't desirable for practical or ergonomic reasons, thus, an alternative antenna style such as a helical, loop or patch may be utilized and the corresponding sacrifice in performance accepted.

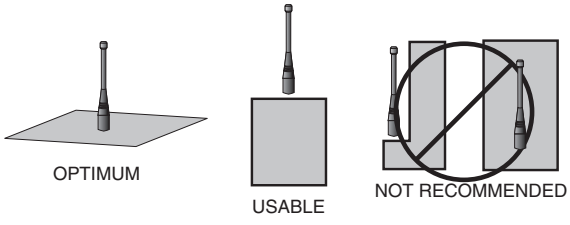

Figure 83: Ground Plane Orientation

3. If an internal antenna is to be used, keep it away from other metal components, particularly large items like transformers, batteries, PCB tracks and ground planes. In many cases, the space around the antenna is as important as the antenna itself. Objects in close proximity to the antenna can cause direct detuning, while those farther away will alter the antenna's symmetry.

4. In many antenna designs, particularly ¼-wave whips, the ground plane acts as a counterpoise, forming, in essence, a ½-wave dipole (Figure 84). For this reason, adequate ground plane area is essential. The ground plane can be a metal case or ground-fill areas on a circuit board. Ideally, it should have a surface area less than or equal to the overall length of the ¼-wave radiating element. This is often not practical due to size and configuration constraints. In these instances, a designer must make the best use of the area available to create as much ground

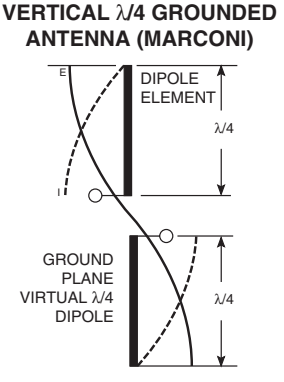

Figure 84: Dipole Antenna

Common Antenna Styles

There are hundreds of antenna styles and variations that can be employed with Linx RF modules. Following is a brief discussion of the styles most commonly utilized. Additional antenna information can be found in Linx Application Notes AN-00100, AN-00140, AN-00500 and AN-00501. Linx antennas and connectors offer outstanding performance at a low price.

Whip Style

A whip style antenna (Figure 86) provides outstanding overall performance and stability. A low-cost whip can be easily fabricated from a wire or rod, but most designers opt for the consistent performance and cosmetic appeal of a professionally-made model. To meet this need, Linx offers a wide variety of straight and reduced height whip style antennas in permanent and connectorized mounting styles.

Figure 86: Whip Style Antennas

The wavelength of the operational frequency determines an antenna's overall length. Since a full wavelength is often quite long, a partial ½- or ¼-wave antenna is normally employed. Its size and natural radiation resistance make it well matched to Linx modules. The proper length for a straight ¼-wave can be easily determined using the formula in Figure 87. It is also possible to reduce the overall height of the antenna by using a helical winding. This reduces the antenna's bandwidth but is a great way to minimize the antenna's physical size for compact applications. This also means that the physical appearance is not always an indicator of the antenna's frequency.

$$L = \frac{234}{F_{MHz}}$$

Figure 87:
L = length in feet of quarter-wave length
F = operating frequency in megahertz

Specialty Styles

Linx offers a wide variety of specialized antenna styles (Figure 88). Many of these styles utilize helical elements to reduce the overall antenna size while maintaining reasonable performance. A helical antenna's bandwidth is often quite narrow and the antenna can detune in proximity to other objects, so care must be exercised in layout and placement.

Figure 88: Specialty Style Antennas

Regulatory Considerations

Note: Linx RF modules are designed as component devices that require external components to function. The purchaser understands that additional approvals may be required prior to the sale or operation of the device, and agrees to utilize the component in keeping with all laws governing its use in the country of operation.

When working with RF, a clear distinction must be made between what is technically possible and what is legally acceptable in the country where operation is intended. Many manufacturers have avoided incorporating RF into their products as a result of uncertainty and even fear of the approval and certification process. Here at Linx, our desire is not only to expedite the design process, but also to assist you in achieving a clear idea of what is involved in obtaining the necessary approvals to legally market a completed product.

For information about regulatory approval, read AN-00142 on the Linx website or call Linx. Linx designs products with worldwide regulatory approval in mind.

In the United States, the approval process is actually quite straightforward. The regulations governing RF devices and the enforcement of them are the responsibility of the Federal Communications Commission (FCC). The regulations are contained in Title 47 of the United States Code of Federal Regulations (CFR). Title 47 is made up of numerous volumes; however, all regulations applicable to this module are contained in Volume 0-19. It is strongly recommended that a copy be obtained from the FCC's website, the Government Printing Office in Washington or from your local government bookstore. Excerpts of applicable sections are included with Linx evaluation kits or may be obtained from the Linx Technologies website, www.linxtechnologies.com. In brief, these rules require that any device that intentionally radiates RF energy be approved, that is, tested for compliance and issued a unique identification number. This is a relatively painless process. Final compliance testing is performed by one of the many independent testing laboratories across the country. Many labs can also provide other certifications that the product may require at the same time, such as UL, CLASS A / B, etc. Once the completed product has passed, an ID number is issued that is to be clearly placed on each product manufactured.

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