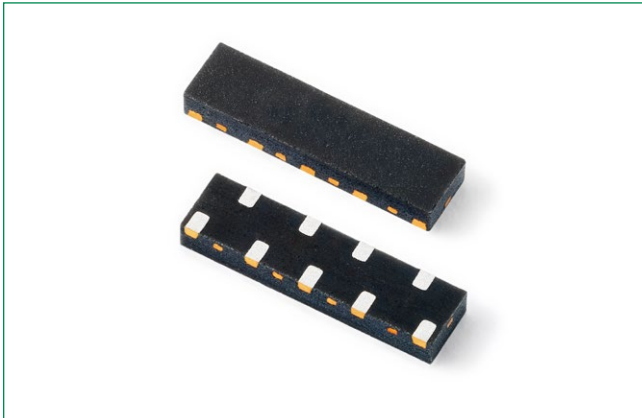
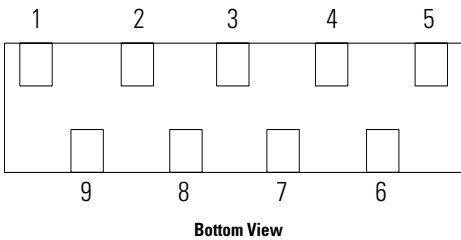
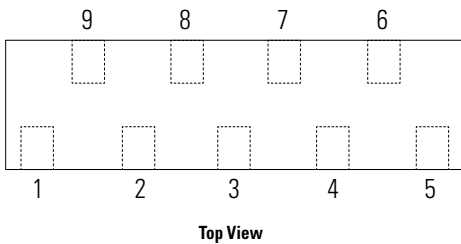


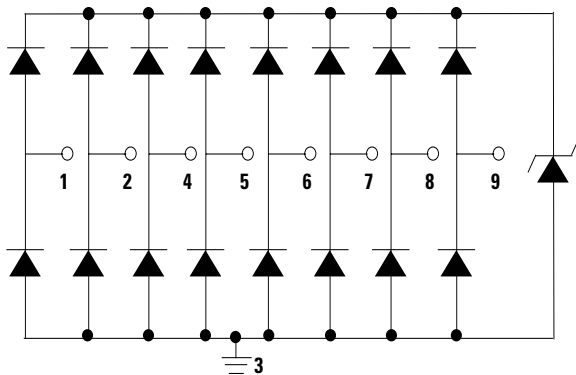
**SP7538P Series 0.5pF 12KV Diode Array**



**Pinout**



**Functional Block Diagram**



Life Support Note:

**Not Intended for Use in Life Support or Life Saving Applications**

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

**Description**

The SP7538P integrates 8 channels of ultra low capacitance rail-to-rail diodes and an additional zener diode to provide protection for electronic equipment that may experience destructive electrostatic discharges (ESD). This robust device can safely absorb repetitive ESD strikes above the maximum level maximum level,  $\pm 8\text{kV}$  contact discharge, as specified in the international standard IEC 61000-4-2, without performance degradation standard ( $\pm 8\text{kV}$  contact discharge) without performance degradation. The extremely low loading capacitance also makes it ideal for protecting high speed signal pins such as V-By-One, HDMI, USB3.0, USB2.0, and IEEE 1394.

**Features**

- ESD, IEC61000-4-2,  $\pm 12\text{kV}$  contact,  $\pm 25\text{kV}$  air
- EFT, IEC61000-4-4, 40A ( $t_p=5/50\text{ns}$ )
- Lightning, IEC61000-4-5 2<sup>nd</sup> edition, 4A ( $t_p=8/20\mu\text{s}$ )
- Low capacitance of 0.5pF (TYP) per I/O
- Low leakage current of  $1.5\mu\text{A}$  (MAX) at 5V
- Halogen free, Lead free and RoHS compliant
- AEC-Q101 qualified

**Applications**

- V-By-One
- Embedded DisplayPort
- USB 2.0/3.0 Ports
- HDMI
- Flat Panel Displays
- LCD/LED TVs
- Smartphones
- Mobile Computing

### Absolute Maximum Ratings

Symbol	Parameter	Value	Units
$I_{PP}$	Peak Current ( $t_p=8/20\mu s$ )	4.0	A
$T_{OP}$	Operating Temperature	-40 to 150	°C
$T_{STOR}$	Storage Temperature	-55 to 150	°C

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

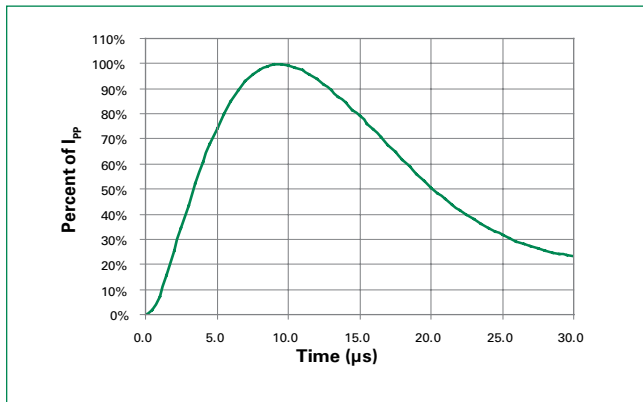
### Electrical Characteristics ( $T_{OP}=25^\circ C$ )

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	$V_{RWM}$	$I_R \leq 1\mu A$			5.0	V
Reverse Leakage Current	$I_{LEAK}$	$V_R=5V$ , Any I/O to GND			1.5	$\mu A$
Clamp Voltage <sup>1</sup>	$V_C$	$I_{PP}=1A$ , $t_p=8/20\mu s$ , Fwd		6.6		V
		$I_{PP}=2A$ , $t_p=8/20\mu s$ , Fwd		7.0		V
Dynamic Resistance <sup>2</sup>	$R_{DYN}$	TLP, $t_p=100ns$ , I/O to GND		0.3		$\Omega$
ESD Withstand Voltage <sup>1</sup>	$V_{ESD}$	IEC 61000-4-2 (Contact)	$\pm 12$			kV
		IEC 61000-4-2 (Air)	$\pm 25$			kV
Diode Capacitance <sup>1</sup>	$C_{I/O-GND}$	Reverse Bias=0V, f=1 MHz		0.5		pF
Diode Capacitance <sup>1</sup>	$C_{I/O-I/O}$	Reverse Bias=0V, f=1 MHz		0.3		pF

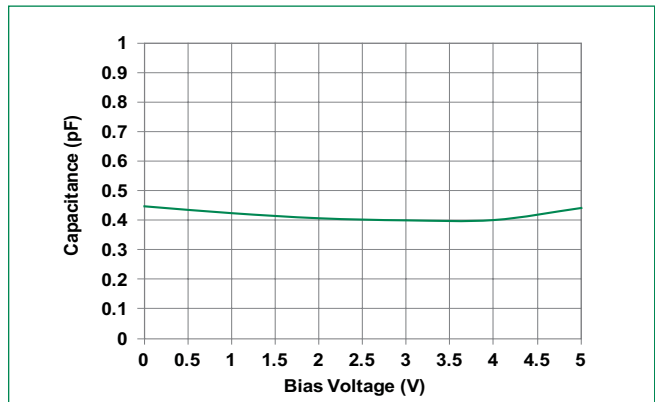
Note: <sup>1</sup> Parameter is guaranteed by design and/or device characterization.

<sup>2</sup> Transmission Line Pulse (TLP) with 100ns width and 2ns rise time.

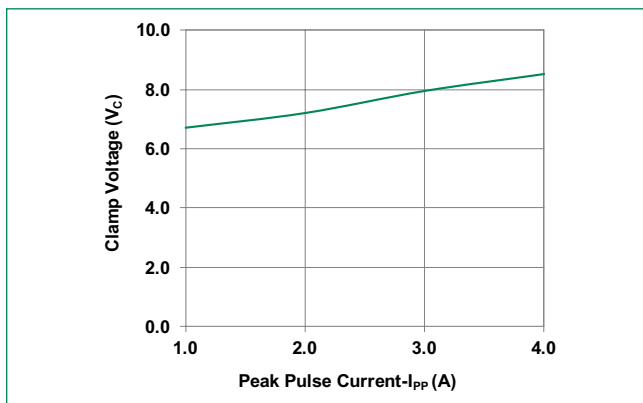
### 8/20 $\mu s$ Pulse Waveform



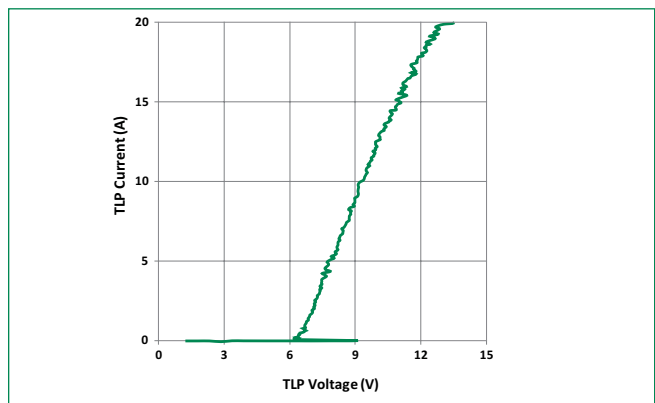
### Capacitance vs. Reverse Bias



### Clamping Voltage vs $I_{PP}$

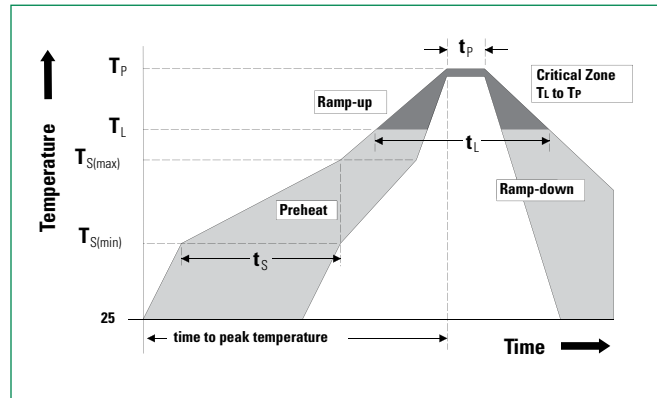


### Transmission Line Pulsing (TLP) Plot

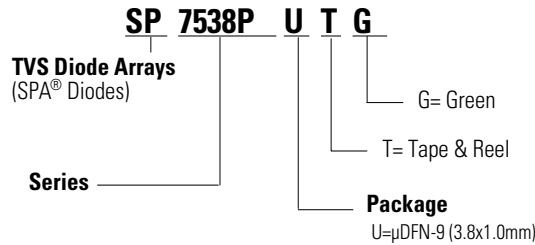


### Soldering Parameters

<b>Reflow Condition</b>		Pb – Free assembly
<b>Pre Heat</b>	- Temperature Min ( $T_{s(min)}$ )	150°C
	- Temperature Max ( $T_{s(max)}$ )	200°C
	- Time (min to max) ( $t_s$ )	60 – 180 secs
<b>Average ramp up rate (Liquidus) Temp (<math>T_L</math>) to peak</b>		3°C/second max
<b><math>T_{s(max)}</math> to <math>T_L</math> - Ramp-up Rate</b>		3°C/second max
<b>Reflow</b>	- Temperature ( $T_L$ ) (Liquidus)	217°C
	- Temperature ( $t_L$ )	60 – 150 seconds
<b>Peak Temperature (<math>T_p</math>)</b>		260 <sup>+0/-5</sup> °C
<b>Time within 5°C of actual peak Temperature (<math>t_p</math>)</b>		20 – 40 seconds
<b>Ramp-down Rate</b>		6°C/second max
<b>Time 25°C to peak Temperature (<math>T_p</math>)</b>		8 minutes Max.
<b>Do not exceed</b>		260°C



### Part Numbering System



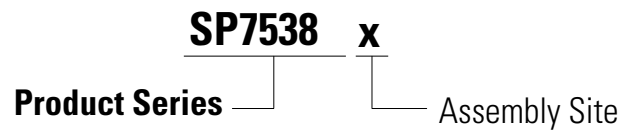
### Product Characteristics

<b>Lead Plating</b>	Matte Tin
<b>Lead Material</b>	Copper Alloy
<b>Substrate material</b>	Silicon
<b>Body Material</b>	Molded Compound
<b>Flammability</b>	UL Recognized compound meeting flammability rating V-0

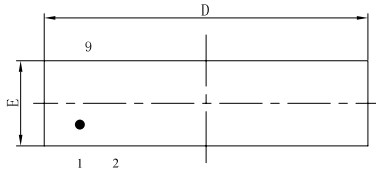
### Ordering Information

Part Number	Package	Min. Order Qty.
SP7538PUTG	μDFN-9	3000

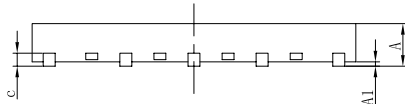
### Part Marking System



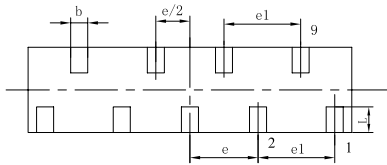
**Package Dimensions**



TOP VIEW



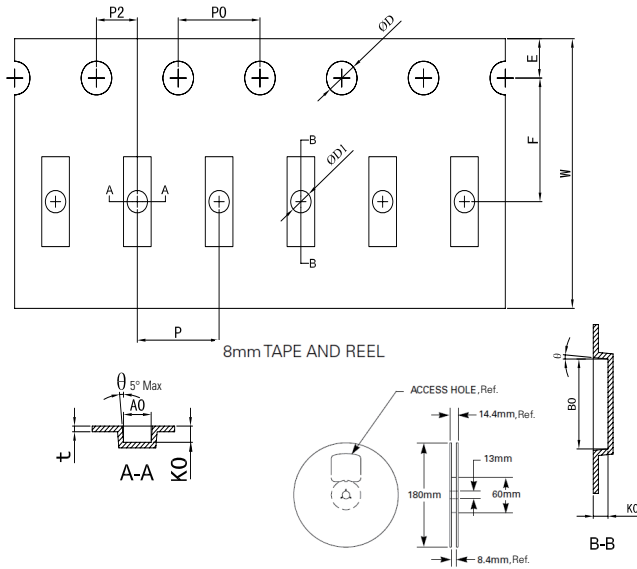
SIDE VIEW



BOTTOM VIEW

μDFN-9 (3.8x1.0mm)						
JEDEC MO-229						
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
<b>A</b>	0.45	0.50	0.55	0.018	0.020	0.022
<b>A1</b>	-	0.02	0.05	-	0.001	0.002
<b>b</b>	0.15	0.20	0.25	0.006	0.008	0.010
<b>c</b>	0.10	0.15	0.20	0.004	0.006	0.008
<b>D</b>	3.70	3.80	3.90	0.146	0.150	0.154
<b>e</b>	0.80 BSC			0.031 BSC		
<b>e1</b>	0.90 BSC			0.035 BSC		
<b>E</b>	0.90	1.00	1.10	0.035	0.039	0.043
<b>L</b>	0.20	0.30	0.40	0.008	0.012	0.016

**Embossed Carrier Tape & Reel Specification**



Symbol	Millimeters
<b>A0</b>	1.35 +/- 0.10
<b>B0</b>	4.00 +/- 0.05
<b>D</b>	Ø 1.50 + 0.1/-0
<b>D1</b>	Ø 1.00 +/-0.05
<b>E</b>	1.75 +/- 0.10
<b>F</b>	5.50 +/- 0.05
<b>K0</b>	0.72 +/- 0.05
<b>P</b>	4.00 +/- 0.10
<b>P0</b>	4.00 +/- 0.10
<b>P2</b>	2.00 +/- 0.05
<b>T</b>	0.25 +/- 0.02
<b>W</b>	12.00 + 0.30 /- 0.10

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