

Lonten N-channel 40V, 120A, 2.5mΩ Power MOSFET

Description

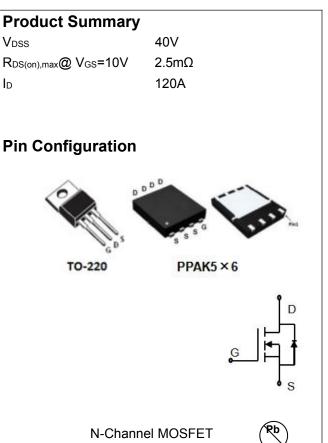
These N-Channel enhancement mode power field effect transistors are using split gate trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and with stand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Features

- 40V,120A, R_{DS(on),max} = 2.5mΩ@V_{GS} = 10V
- Improved dv/dt capability
- Fast switching
- 100% EAS Guaranteed
- Green device available

Applications

- Motor Drives
- UPS
- DC-DC Converter



Absolute Maximum Ratings Tc = 25°C unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	40	V
Continuous drain current ($T_c = 25^{\circ}C$) ¹⁾		120	A
Continuous drain current ($T_{\rm C}$ = 100°C)	Ι _D	81	A
Pulsed drain current ²⁾	I _{DM}	360	A
Gate-Source voltage	V _{GSS}	±18	V
Avalanche energy ³⁾	E _{AS}	225	mJ
Power Dissipation ($T_c = 25^{\circ}C$)	P _D	57.6	W
Storage Temperature Range	T _{STG}	-55 to +150	°C
Operating Junction Temperature Range	TJ	-55 to +150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	R _{eJC}	1.67	°C/W



Package Marking and Ordering Information

Device	Device Package	Marking
LSGN04R025	PPAK5X6	LSGN04R025
LSGC04R025	TO-220	LSGC04R025

Electrical Characteristics T_J = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min.	Тур.	Max.	Unit
Static characteristics		1				
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0 V, I _D =250uA	40			V
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1.0		2.2	V
Drain-source leakage current	I _{DSS}	V _{DS} =40 V, V _{GS} =0V, T _J = 25°C			1	μA
Gate leakage current, Forward	I _{GSSF}	V _{GS} =18 V, V _{DS} =0 V			100	nA
Gate leakage current, Reverse	I _{GSSR}	V _{GS} =-18 V, V _{DS} =0 V			-100	nA
5		V _{GS} =10 V, I _D =50 A			2.5	mΩ
Drain-source on-state resistance	R _{DS(on)}	V _{GS} =4.5 V, I _D =20 A			5	mΩ
Forward transconductance	g _{fs}	V _{DS} =10V , I _D =20A		131		S
Dynamic characteristics						
Input capacitance	C _{iss}			3210		
Output capacitance	C _{oss}	$V_{DS} = 15 V, V_{GS} = 0 V,$		2130		pF
Reverse transfer capacitance	C _{rss}	- F = 1MHz -		343		I
Turn-on delay time	t _{d(on)}			9		
Rise time	tr	$V_{DD} = 15V, V_{GS} = 10V, I_D = 20A$		4		ns
Turn-off delay time	t _{d(off)}	R _G =1.6Ω		45		
Fall time	t _f			7		
Gate charge characteristics						
Gate to source charge	Q _{gs}			7		
Gate to drain charge	Q _{gd}	- V _{DS} =15V, I _D =15A,		17.5		nC
Gate charge total	Qg	- V _{GS} = 10 V		67		
Drain-Source diode characterist	ics and Maxi	mum Ratings				
Continuous Source Current	Is				120	A
Pulsed Source Current ⁴⁾	I _{SM}				360	A
Diode Forward Voltage	V _{SD}	V_{GS} =0V, I _S =40A, T _J =25 $^{\circ}$ C		0.85	1.2	V
Reverse Recovery Time	t _{rr}				26	ns
Reverse Recovery Charge	Q _{rr}	I _S =I _F , di/dt=100A/us, T _J =25 $^{\circ}$ C $^{-5)}$ -			95	nC

Notes:

1: The maximum junction current rating is package limited.

2: Repetitive Rating: Pulse width limited by maximum junction temperature.

3: V_DD=23V, V_GS=10V, L=0.5mH, I_{AS}=30A, R_G=25\Omega, Starting T_J=25 $^\circ\!\!\mathrm{C}.$

4: Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

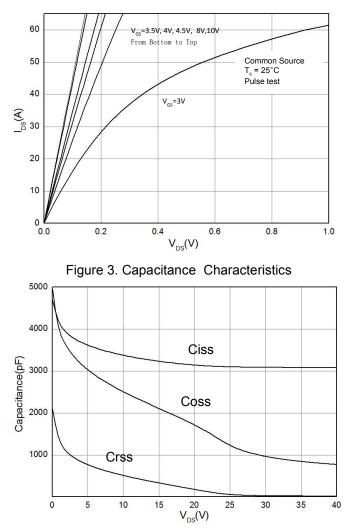
5: Guaranteed by design, not subject to production.



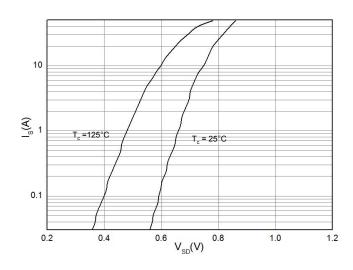
LSGN04R025/LSGC04R025

Electrical Characteristics Diagrams

Fig 1: Output Characteristics







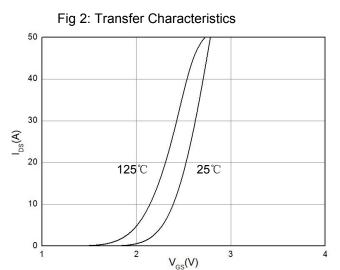
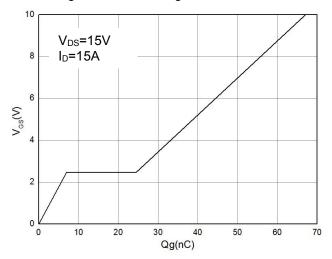
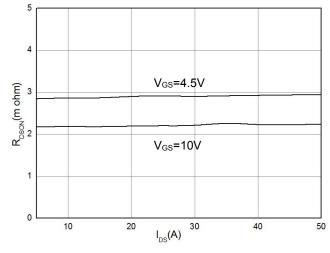


Figure 4. Gate Charge Waveform







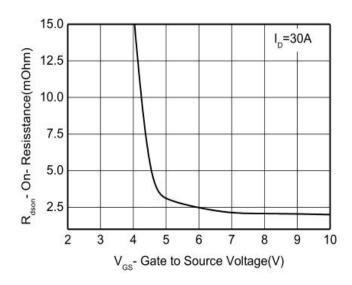
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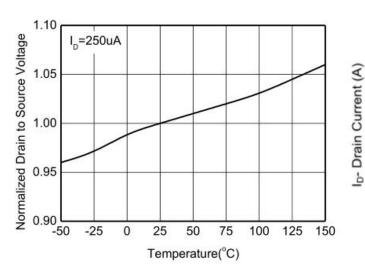
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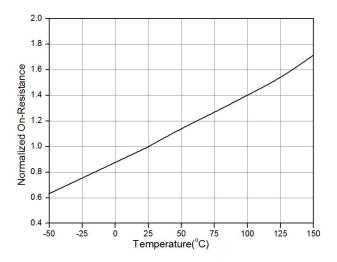
Fig 7: Rds(on) vs Gate Voltage

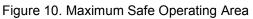
Fig 8: Rdson-Junction Temperature(℃)

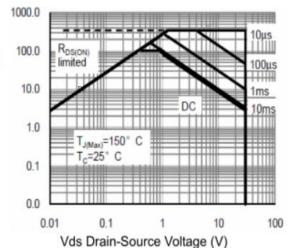




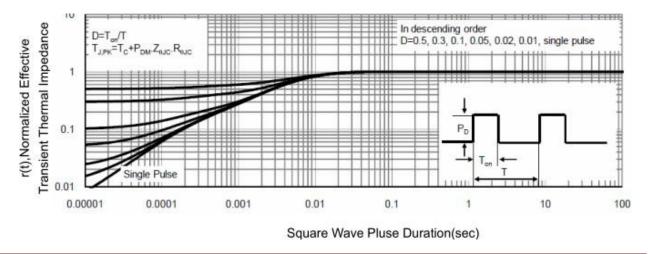








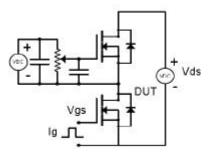


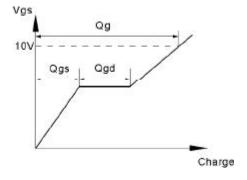


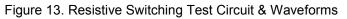


Test Circuit & Waveform

Figure 12. Gate Charge Test Circuit & Waveform







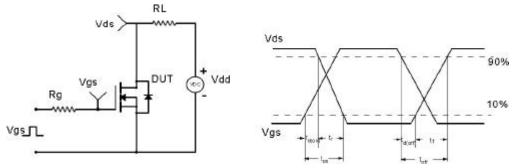


Figure 14. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

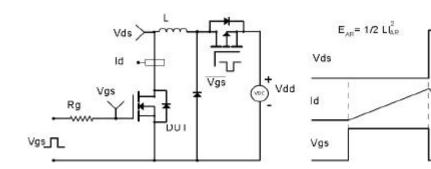
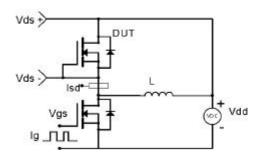
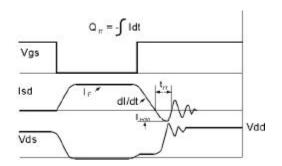


Figure 15. Diode Recovery Circuit & Waveform





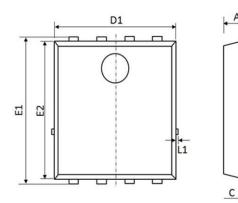
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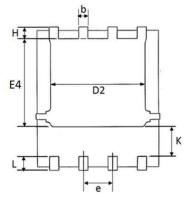
BV₀₅₅

AR



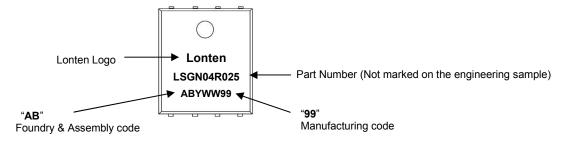
Mechanical Dimensions for PPAK5×6





COMMON DIMENSIONS							
	MILLIMETERS				INCHS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX	
A	1	1.1	1.2	0.039	0.043	0.047	
b	0.3	0.4	0.5	0.012	0.016	0.020	
С	0.154	0.254	0.354	0.006	0.010	0.014	
D1	5	5.2	5.4	0.197	0.205	0.213	
D2	3.8	4.1	4.25	0.150	0.161	0.167	
E1	5.95	6.15	6.35	0.234	0.242	0.250	
E2	5.66	5.86	6.06	0.223	0.231	0.239	
E4	3.52	3.72	3.92	0.139	0.146	0.154	
е		1.27	BSC		0.050	BSC	
н	0.4	0.5	0.6	0.016	0.020	0.024	
L	0.5	0.6	0.7	0.020	0.024	0.028	
L1	-	-	0.12	-	-	0.005	
к	1.14	1.29	1.44	0.045	0.051	0.057	

PPAK5×6 Part Marking Information



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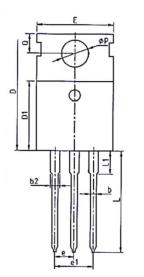
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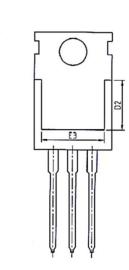
Calendar Year	Year Code	Calendar Week	Week Code
2018	G	Workweek 01	01
2019	Н	Workweek 02	02
2020	1	Workweek 03	03
2021	J	Workweek 04	04
2022	К	Workweek 05	05
2023	L	Workweek 06	06
2024	М		



TO-220 PACKAGE INFORMATION

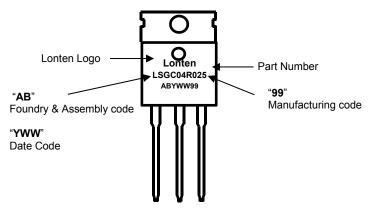
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COMMON DIMENSIONS						
SYMBOL	MM			INCH		
STWDUL	MIN	NOM	MAX	MIN	NOM	MAX
А	4.37	4.57	4.70	0.172	0.180	0.185
A1	1.25	1.30	1.40	0.049	0.051	0.055
A2	2.20	2.40	2.60	0.087	0.094	0.102
b	0.70	0.80	0.95	0.028	0.031	0.037
b2	1.17	1.27	1.47	0.046	0.050	0.058
С	0.45	0.50	0.60	0.018	0.020	0.024
D	15.10	15.60	16.10	0.594	0.614	0.634
D1	8.80	9.10	9.40	0.346	0.358	0.370
D2	5.50	-	-	0.217	-	-
E	9.70	10.00	10.30	0.382	0.394	0.406
E3	7.00	-	-	0.276	-	-
е	2.54BCS				0.1BSC	
e1		5.08BCS 0.2REF				
H1	6.25	6.50	6.85	0.246	0.256	0.270
L	12.75	13.50	13.80	0.502	0.531	0.543
L1	-	3.10	3.40	-	0.122	0.134
ØP	3.40	3.60	3.80	0.134	0.142	0.150
Q	2.60	2.80	3.00	0.102	0.110	0.118

TO-220 Part Marking Information



Calendar Year	Year Code	Calendar Week	Week Code
2018	G	Workweek 01	01
2019	Н	Workweek 02	02
2020	I	Workweek 03	03
2021	J	Workweek 04	04
2022	К	Workweek 05	05
2023	L	Workweek 06	06
2024	М		



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