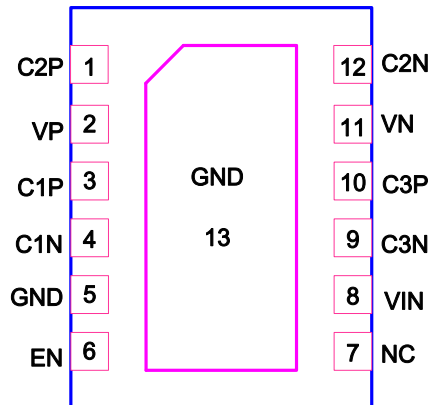






## Pin Configurations

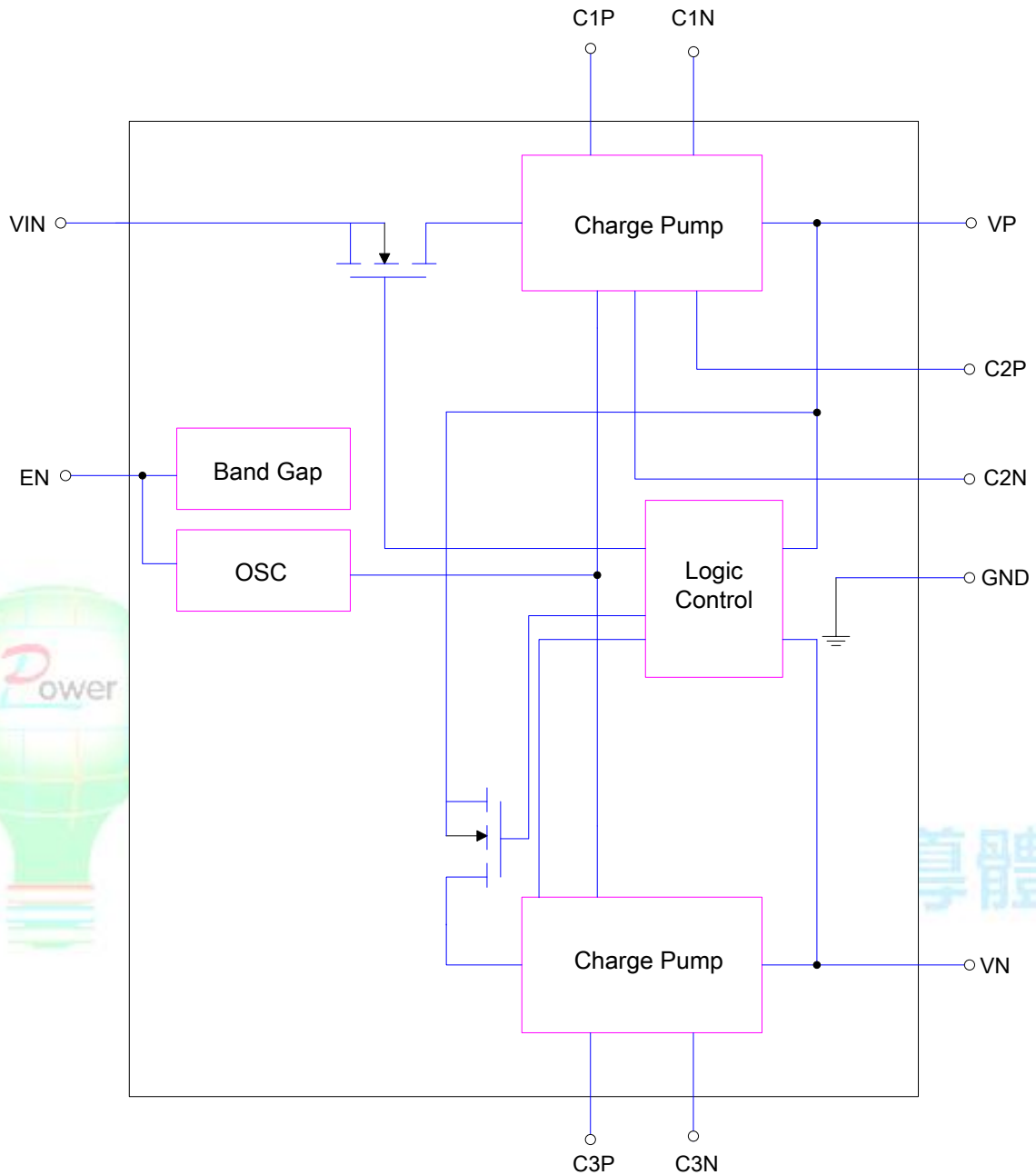


## Functional Pin Description

Pin No.	Pin Name	Description
1	C2P	Flying Capacitor 2 Positive Terminal (C5).
2	VP	Positive output pin.
3	C1P	Flying Capacitor 1 Positive Terminal (C4).
4	C1N	Flying Capacitor 1 Negative Terminal (C4).
6	EN	Device Enable pin.
7	NC	No connector.
8	VIN	Input Supply Voltage. Bypass VIN with a low ESR ceramic capacitor to GND.
9	C3N	Flying Capacitor 3 Negative Terminal (C6).
10	C3P	Flying Capacitor 3 Positive Terminal (C6).
11	VN	Negative output pin.
12	C2N	Flying Capacitor 2 Negative Terminal (C5).
5,13(Pad)	GND	Ground pin.



### Function Block Diagram



### Absolute Maximum Ratings

- ✧ Input/Output Voltage to GND ----- -0.3V to +6V
- ✧ EN to GND ----- 0 V to VIN
- ✧ Operating Junction Temperature Range (T<sub>J</sub>) ----- -40°C to 150°C
- ✧ Maximum Soldering Temperature (at leads, 10sec) ----- 260°C
- ✧ Storage Temperature Range ----- -65°C to 150°C
- ✧ Operation Ambient Temperature Range ----- 0°C to 85°C
- ✧ Maximum Power Dissipation (P<sub>D</sub>, T<sub>A</sub><40°C) ----- 1.5W
- ✧ Thermal Resistance (J<sub>A</sub>) ----- 68°C/W



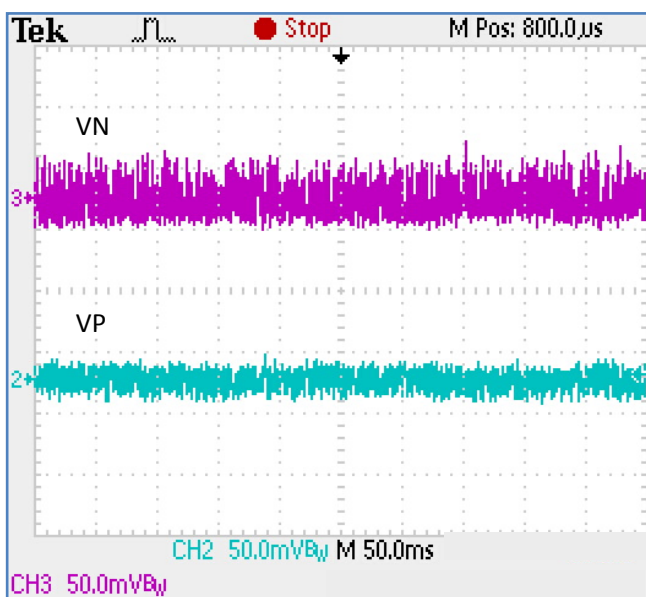
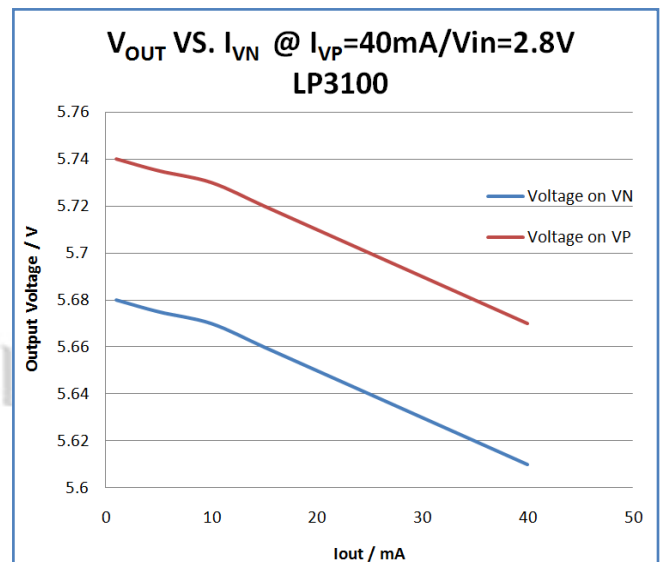
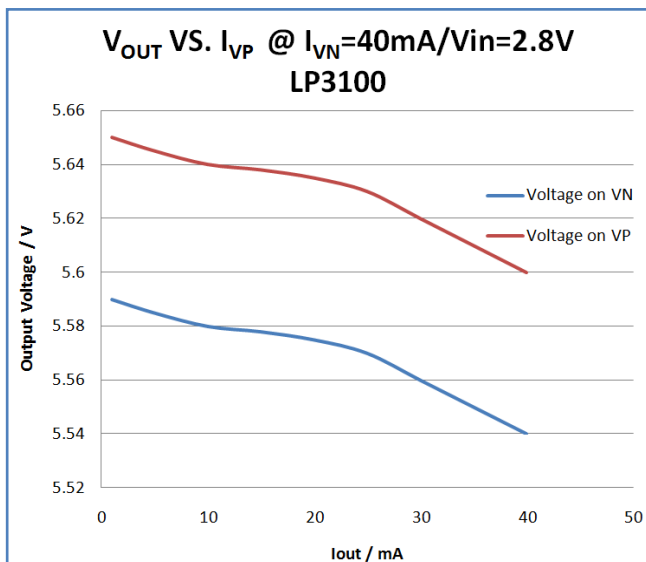
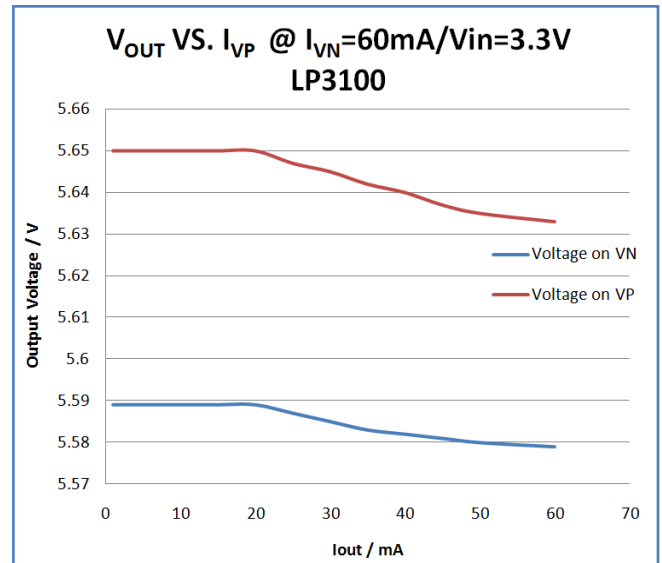
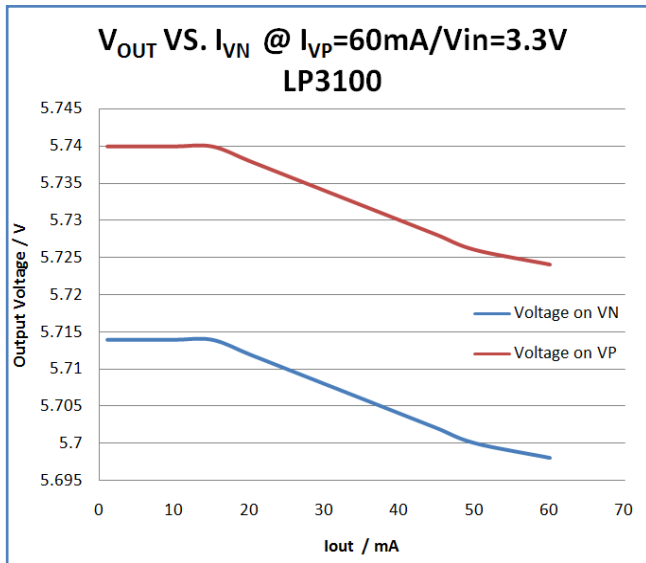
## Electrical Characteristics for Each Channel

(VIN =VEN , C1 = C2=C3 = 2.2uF , C4=C5=C6=1uF, Typical values are TA=25°C )

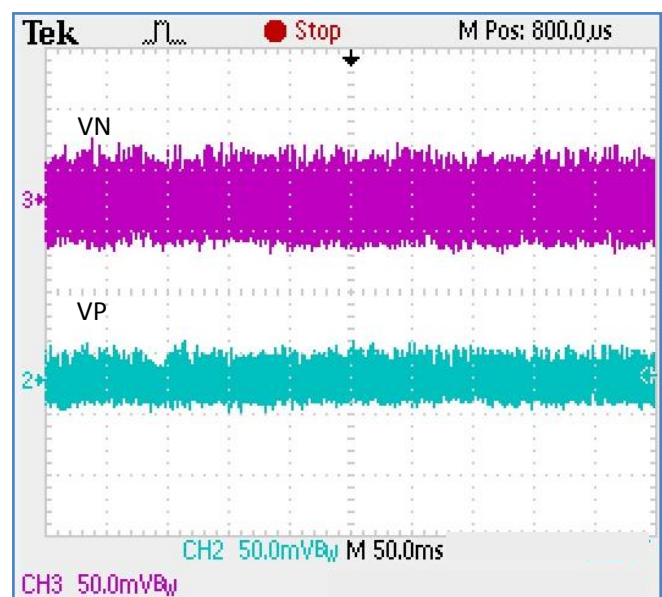
Symbol	Parameter	Conditions	LP3100			Unit
			Min.	Typ.	Max.	
VIN	Input Voltage		2.5		4.8	V
Io	Output Current	Positive Output Current, Vin=2.8V		40		mA
		Negative Output Current, Vin=2.8V		40		
		Positive Output Current, Vin=3.3V		60		
		Negative Output Current, Vin=3.3V		60		
VP	Positive Output Voltage	Loading=1mA	5.4		5.9	V
VN	Negative Output Voltage	Loading=1mA	-5.9		-5.4	
ISHDN	Shutdown Current	EN = GND, VIN = 3.6V			1	μA
FOSC	Oscillator Frequency	I <sub>VP</sub> =I <sub>VN</sub> =10mA		300		KHz
VoL	EN Logic Low				0.4	V
VoH	EN Logic High		1.4			V
IEN	EN Pin Current				0.5	uA
TSD	Thermal Shutdown Temperature			145		°C



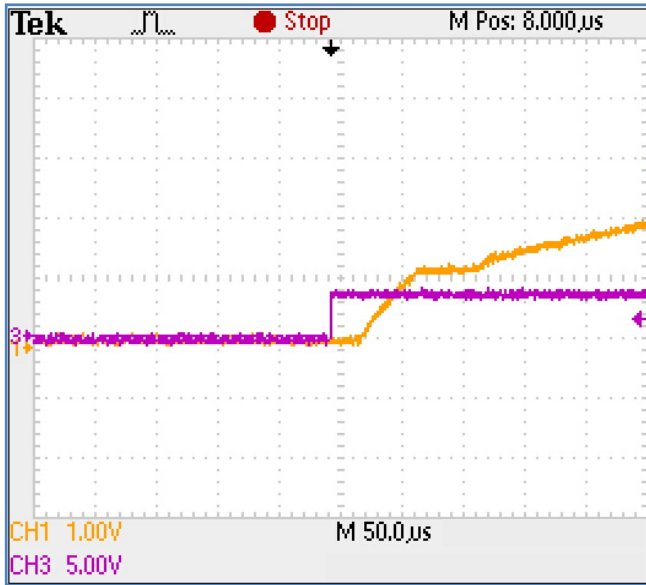
## Typical Operating Characteristics



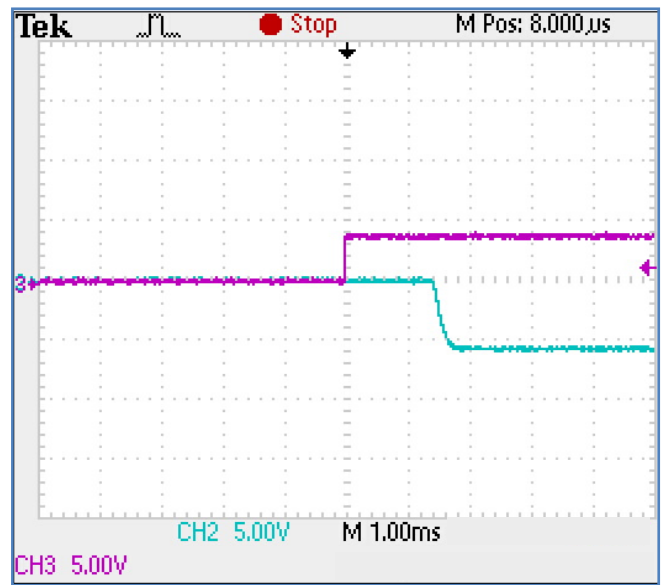
$V_{in}=3.3\text{V}, C_{out}=2.2\mu\text{F}, I_{VP}=I_{VN}=10\text{mA}$



$V_{in}=3.3\text{V}, C_{out}=2.2\mu\text{F}, I_{VP}=I_{VN}=60\text{mA}$



Start up Waveform with VP



Start up Waveform with VN





## Application Information

The LP3100 offers dual channel output voltage for powering on specified power in TFT LCD panels. The device integrates a positive charge pump and a negative charge pump.

**Enable Control (EN)** To turn on the LP3100, the EN pin must be at logic high. When the EN pin is pulled to a logic low, the device is disabled and the supply current reduces to less than 1 $\mu$ A.

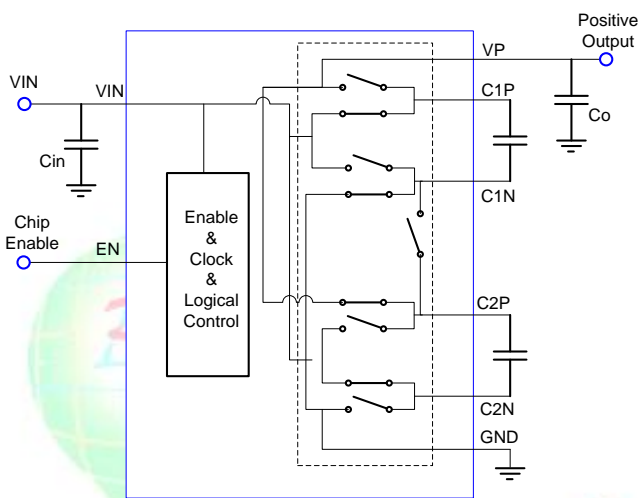


Figure 1. Positive Charge Pump Functional Block Diagram

The LP3100 positive charge pump provides an output voltage VP of 1.5x or 2x the input voltage. The positive charge pump uses two external flying capacitors to generate the required output voltage. For the selected output to input ratio, the charge pump will configure the internal switches to charge the flying capacitors. Figure 1 shows the functional diagram of the positive charge pump.

## Negative Charge Pump Controller

The negative charge pump uses one external flying capacitor to generate an inverted negative voltage that is  $-1x$  of VP. Figure 2 shows the functional block diagram of the negative charge pump.

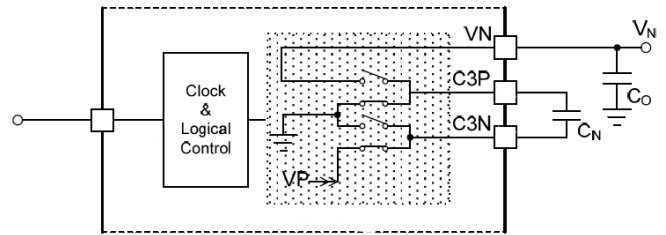


Figure 2. Negative Charge Pump Functional Block Diagram

## LAYOUT CONSIDERATION

Use a ground plane for the LP3100 device that can be connected to the device expose pad and ground pin for optimal thermal characteristics.

### Bypass Capacitors

Place VIN, VP, and VN bypass capacitors as close as possible to the device pin. Keep the ground traces from the bypass to the ground plane as short as possible.

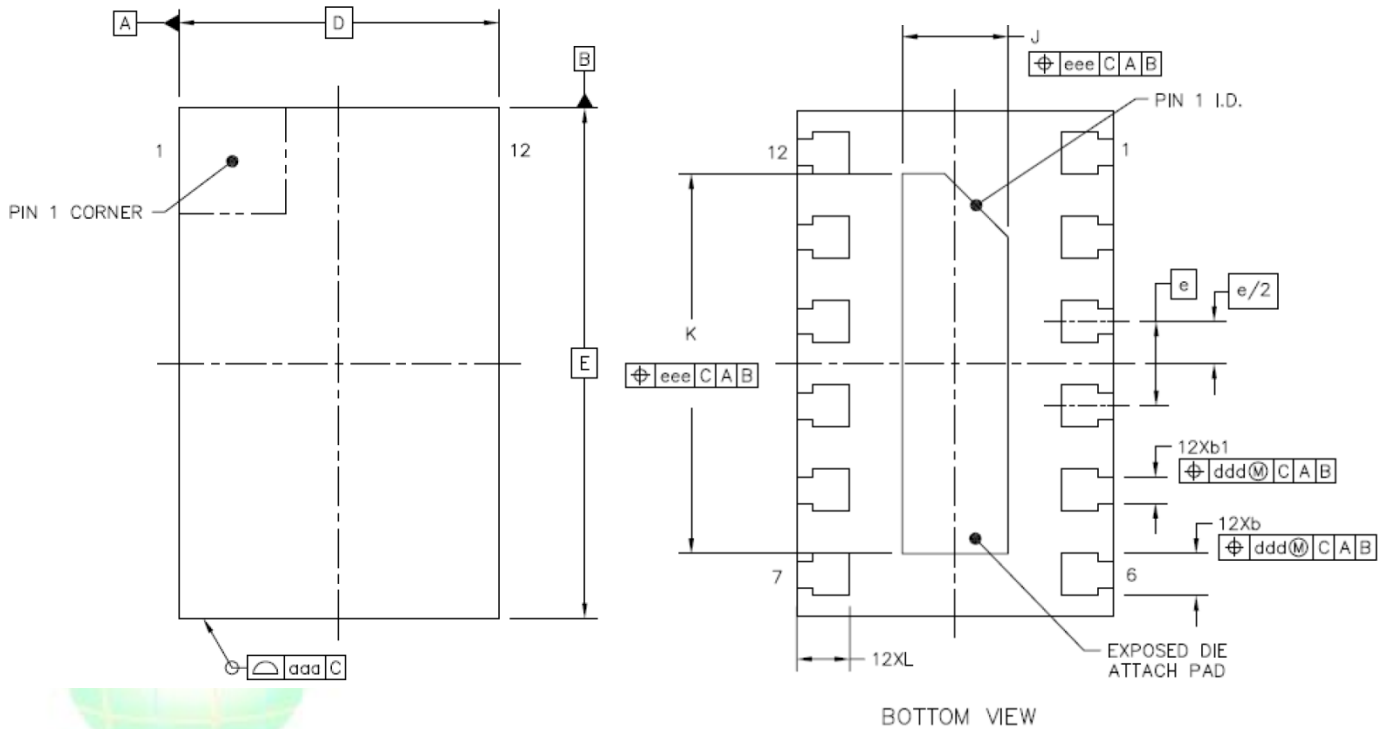
### Flying Capacitors

Place the flying capacitors as close to the device pins as possible to minimize trace noise since the flying capacitors to the pins will generate high transient voltage (dv/dt) switching signals.

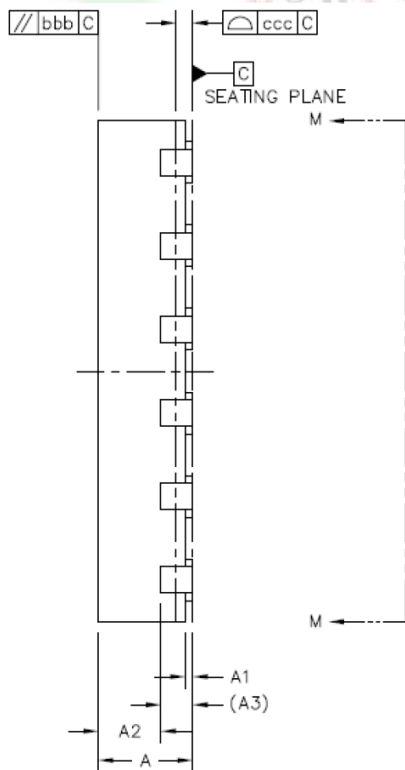


## Packaging Information

### TDFN-12



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	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.4	0.45	0.5
STAND OFF	A1	0	0.035	0.05
MOLD THICKNESS	A2	---	0.3	---
L/F THICKNESS	A3	0.152 REF		
LEAD WIDTH	b	0.15	0.2	0.25
	b1	0.075	0.125	0.175
BODY SIZE	X	D		
	Y	E		
LEAD PITCH	e	0.4 BSC		
EP SIZE	X	J	0.4	0.5
	Y	K	1.7	1.8
LEAD LENGTH	L	0.2	0.25	0.3
PACKAGE EDGE TOLERANCE	aaa	0.1		
MOLD FLATNESS	bbb	0.1		
COPLANARITY	ccc	0.08		
LEAD OFFSET	ddd	0.1		
EXPOSED PAD OFFSET	eee	0.1		



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