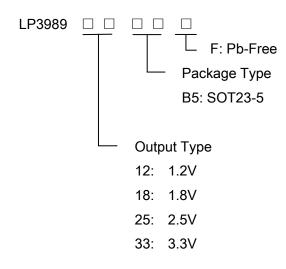
## 600mA, Ultra-low noise, Small Package, **Ultra-Fast CMOS LDO Regulator**

### **General Description**

The LP3989 is designed for portable RF and wireless applications with demanding performance and space requirements. The LP3989 performance is optimized for battery-powered systems to deliver ultra low noise and low guiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life. The LP3989 also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices. The LP3989 consumes less than 0.01µA in shutdown mode and has fast turn-on time less than 50µs. The other features include ultra low dropout voltage, high feedback accuracy, current limiting protection, and high ripple rejection ratio. It is available in the 5-lead of SOT23-5 packages. LowPowerSem

### Order Information



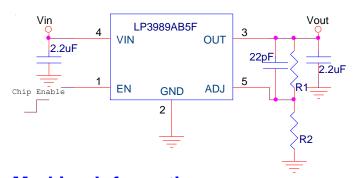
#### **Features**

- Ultra-Low-Noise for RF Application
- 2.2V- 6V Input Voltage Range
- Low Dropout: 280mV @ 400mA
- 600mA Output Current, 750mA Peak Current
- High PSRR: -68dB at 1KHz
- < 0.01uA Standby Current When Shutdown
- Available in SOT23-5 and SOT223 Package
- Ultra-Fast Response in Line/Load transient
- Current Limiting and Thermal Shutdown Protection

### **Applications**

- Portable Media Players/MP3 players
- Cellular and Smart mobile phone
- **LCD**
- **DSC Sensor**
- Wireless Card

### **Typical Application Circuit**



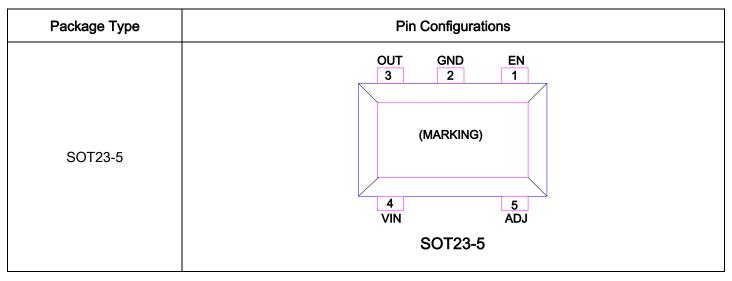
## **Marking Information**

Device	Marking	Package	Shipping
LP3989AB5F		SOT23-5	3K/REEL

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# **Functional Pin Description**

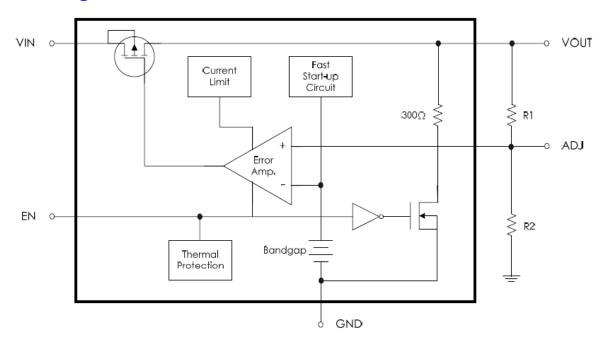


# **Pin Description**

Pin	Name	Description		
4	EN	Chip Enable (Active High). There is an integrated pull low 1M $\Omega$ resistor connected		
1 EN P Semi		to GND when the EN pin is floating.		
2	GND	Ground.		
3	VOUT	Output Voltage. $V_{out}=V_{FB} \times (1+R1/R2)$ , which $V_{FB}=0.8V$		
4	VIN	Power Input Voltage.		
5	ADJ	Feedback pin. The reference voltage is 0.8V.		

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# **Function Diagram**



# **Absolute Maximum Ratings**

$\diamond$	Supply Input Voltage	
$\diamondsuit$	EN Pin Voltage	0.3V to Vin+0.3V
Po	EN Pin Voltage ower Dissipation, PD @ TA = 25°C  SOT23-5	
<b></b>	SOT23-5	500mW
Pa	ackage Thermal Resistance	
<b></b>	SOT23-5, θJA	195°C/W
<b></b>	Lead Temperature (Soldering, 10 sec.)	260°C
$\diamondsuit$	Storage Temperature Range	−40°C to 165°C
E	SD Susceptibility	
<b></b>	HBM (Human Body Mode)	2kV
$\diamond$	MM(Machine-Mode)	200V
R	ecommended Operating Conditions	
<b>\$</b>	Supply Input Voltage	2.5V to 6V
$\diamondsuit$	Operation Ambient Temperature Range	20°C to 85°C

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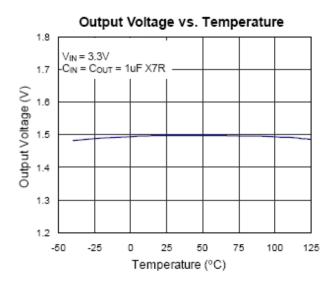
### **Electrical Characteristics**

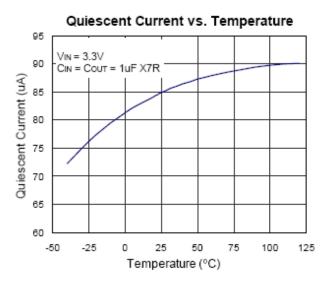
 $(V_{IN} = V_{OUT} + 1V, C_{IN} = C_{OUT} = 2.2 \mu F, C_{FB} = 22 pF, T_A = 25^{\circ} C$ , unless otherwise specified)

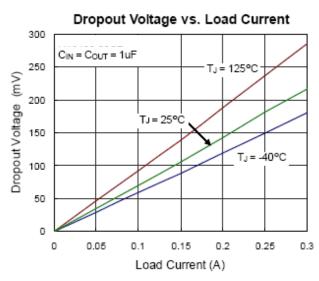
Parameter		Symbol	Test Conditions	Min	Тур.	Max	Units	
Output Loading Current		ILOAD	V <sub>EN</sub> =V <sub>IN</sub> ,V <sub>IN</sub> >2.5V		600		mA	
Curre	nt Limit	I <sub>LIM</sub>	$R_{LOAD} = 1\Omega$		750		mA	
Adjustable vo	Itage reference	$V_{FB}$	I <sub>OUT</sub> =1mA	0.784	8.0	0.816	V	
Quiesce	nt Current	IQ	V <sub>EN</sub> ≥ 1.4V, I <sub>OUT</sub> = 0mA		90	130	μΑ	
			I <sub>OUT</sub> = 200mA, V <sub>OUT</sub> >2.8V		140	160		
Dropou	t Voltage	V <sub>DROP</sub>	I <sub>OUT</sub> = 400mA, V <sub>OUT</sub> >2.8V		280	320	mV	
			I <sub>OUT</sub> = 600mA, V <sub>OUT</sub> >2.8V		420	480		
Line Regulation		ΔV <sub>LINE</sub>	$V_{IN} = (V_{OUT} + 1V) \text{ to } 5.5V,$ $I_{OUT} = 1\text{mA}$			0.3	%	
Load R	Load Regulation		1mA < I <sub>OUT</sub> < 400mA			2	%	
Standby Current		I <sub>STBY</sub>	V <sub>EN</sub> = GND, Shutdown		0.01	1	μΑ	
EN Input E	EN Input Bias Current		V <sub>EN</sub> = 1V or 5V	0.8		5.3	μΑ	
Logic-Low Voltage		V <sub>IL</sub>	$V_{IN} = 3V$ to 5.5V, Shutdown			0.4	V	
EN Threshold	Logic-High		$V_{IN} = 3V \text{ to } 5.5V,$	4.4		VIN+	V	
	Voltage	V <sub>IH</sub>	Start-Up	1.4	直思題	0.3		
Output Noise Voltage		OWLOW	10Hz to 100kHz, Ι <sub>Ουτ</sub> =200mA, Cout=1μF		100	n.i	uVRMS	
Power Supply f = 100Hz		PSRR	$C_{OUT} = 1\mu F$ ,		-76		dВ	
Rejection Rate f = 1kHz			I <sub>OUT</sub> = 10mA		-68		dB	
Thermal Shutdown Temperature		T <sub>SD</sub>			150		°C	

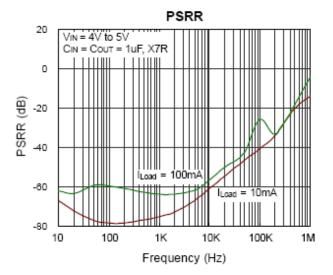
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# **Typical Operating Characteristics**









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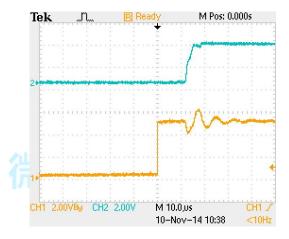
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### **Applications Information**

Like any low-dropout regulator, the external capacitors used with the LP3989 must be carefully selected for regulator stability and performance. Using a capacitor whose value is > 2µF on the LP3989 input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. There is a special attention which is the input capacitance should not be less than output capacitance. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The LP3989 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least  $1\mu F$  with ESR is >  $25m\Omega$  on the LP3989 output ensures stability. The LP3989 still works well with output capacitor of other types due to the wide stable ESR range. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the V<sub>OUT</sub> pin of the LP3989 and returned to a clean analog ground.

#### **Start-up Function Enable Function**

The LP3989 features an LDO regulator enable/disable function. To assure the LDO regulator will switch on, the EN turn on control level must be greater than 1.4 volts but not above Vin+0.3V. The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4 volts. For protecting the system, the LP3989 have a quick-discharge function. If the enable function is not needed in a specific application, it may be tied to  $V_{\text{IN}}$  to keep the LDO regulator in a continuously on state.



#### Feedback Capacitor and Voltage

For adjustable version, connecting a 22pF between output pin and FB pin significantly reduces output voltage ripple, it is critical that the capacitor connection should be direct and PCB traces should be as short as possible.

The output voltage of LDO could be set by the formula below:

$$V_{out}=V_{FB} \times (1+R1/R2)$$

which  $V_{FB} = 0.8V$ 

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## **Preliminary Datasheet**

LP3989

The power dissipation definition in device is:

$P_D = 0$	$(V_{IN}-V_{I})$	X (TUC	l <sub>OUT</sub> +	$V_{IN} \times I_{Q}$
-----------	------------------	--------	--------------------	-----------------------

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction and ambient.

The maximum power dissipation can be calculated by following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$$

Where  $T_{J(MAX)}$  is the maximum operation junction temperature 125°C,  $T_A$  is the ambient temperature and the  $\theta_{JA}$  is the junction to ambient thermal resistance. For recommended operating conditions specification of LP3989, where  $T_{J(MAX)}$  is the maximum junction temperature of the die (125°C) and  $T_A$  is the maximum ambient temperature. The junction to ambient thermal resistance ( $\theta_{JA}$  is layout dependent) for SOT23-5 package is 195°C/W.

#### $P_{D(MAX)} = (125^{\circ}C - 25^{\circ}C) / 195 = 500 \text{mW (SOT23-5)}$

The maximum power dissipation depends on operating ambient temperature for fixed  $T_{J(MAX)}$  and thermal resistance  $\theta_{JA}$ . Considering the PCB thermal feather, the  $P_{D(MAX)}$  may be higher than 500mW.

Vout(V)	R2(KΩ)	R1(KΩ)
1.2	51	25.5
1.5	51	44.6
1.8	51	63.8
2	47	70.5
2.5	47	99.9
2.8	47	117.5
3	33	90.8
3.3	33	103.1
3.5	33	111.4
4	33	132.0
4.2	33	140.3
4.5	33	152.6

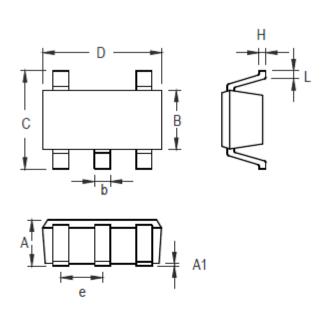
Considering the practical application, we may add a small capacitor with R1 in parallel which could be 22pF or 47pF.

#### Thermal Considerations(for SOT23-5)

Thermal protection limits power dissipation in LP3989. When the operation junction temperature exceeds 150°C, the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turns on again after the junction temperature cools by 25°C. For continue operation, do not exceed absolute maximum operation junction temperature 125°C.

# **Packaging Information**

#### SOT23-5



Comple el	Dimensions I	n Millimeters	Dimensions In Inches		
Symbol	Min	Max	Min	Max	
Α	0.889	1.295	0.035	0.051	
A1	0.000	0.152	0.000	0.006	
В	1.397	1.803	0.055	0.071	
b	0.356	0.559	0.014	0.022	
С	2.591	2.997	0.102	0.118	
D	2.692	3.099	0.106	0.122	
е	0.838	1.041	0.033	0.041	
Н	0.080	0.254	0.003	0.010	
L	0.300	0.610	0.012	0.024	

SOT-23-5 Surface Mount Package

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TCR3DF27,LM(CT TCR3DF19,LM(CT TCR3DF125,LM(CT TCR2EN18,LF(S MAX15103EWL+T TS2937CZ-5.0 C0 MAX8878EUK30-T MAX663CPA NCV4269CPD50R2G NCV8716MT30TBG AZ1117IH-1.2TRG1 MP2013GQ-P