800mA Linear Li-Ion Battery Charger with Protection of Reverse Connection of Battery

General Description

The LP4055A is a complete constant-current/constant- voltage linear charger for single cell lithium-ion batteries. Its TDFN-6 package and low external component count make the LP4055A ideally suited for portable applications. Furthermore, the LP4055A is specifically designed to work within USB power specifications. No external sense resistor is needed, and no blocking diode is required due to the internal MOSFET architecture. Thermal feedback regulates the charge current to limit the die temperature during high power operation or high ambient temperature. The charge voltage is fixed at 4.2V, and the charge current can be programmed externally with a single resistor. The LP4055A automatically terminates the charge cycle when the charge current drops to 1/10th the programmed value after the final float voltage is reached. When the input supply (wall adapter or USB supply) is removed, the LP4055A automatically enters a low current state, dropping the battery drain current to less than 1μA. Other features include charge current monitor, automatic recharge and a status pin to indicate charge termination.

Order Information

LP4055A □□ □

F: Pb-Free

Package Type
QV: TDFN-6

Features

- Programmable Charge Current Up to 800mA
- No MOSFET, Sense Resistor or Blocking Diode Required
- Protection of Reverse Connection of Battery
- Constant-Current/Constant-Voltage Operation with Thermal Regulation to Maximize
- Charge Rate Without Risk of Overheating
- Charge Current Monitor Output for Gas Gauging
- Automatic Recharge
- 2.9V Trickle Charge Threshold
- Output OCP
- Charging OTP

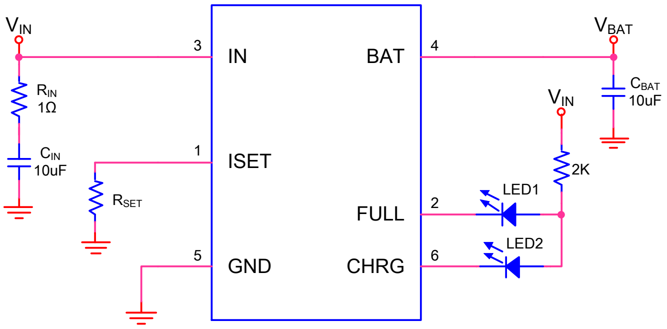
Applications

- Portable Media Players/MP3 players
- Cellular and Smart mobile phone
- PDA/DSC
- Bluetooth Applications

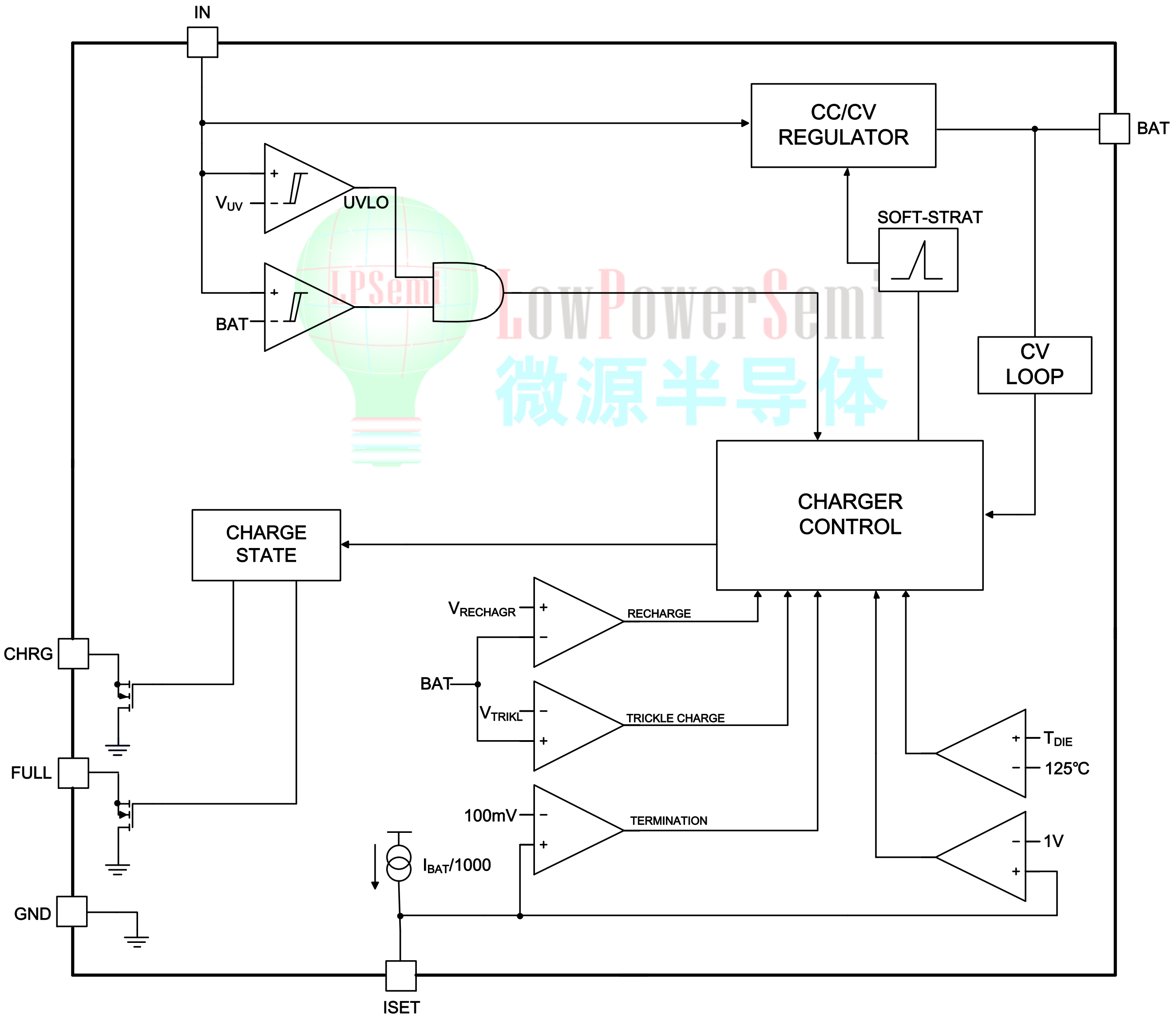
Marking Information

Part	Marking	Package	Shipping
LP4055AQVF	LPS BDYW	TDFN-6	4K/REEL
Marking indication: Y:Production year W:Production week			

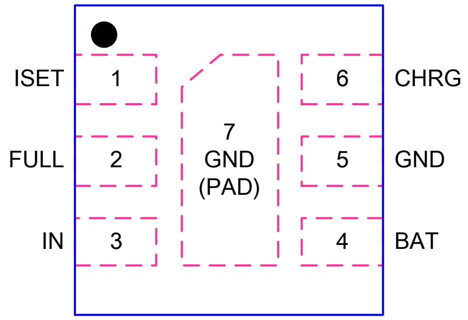
Typical Application Circuit



Functional Block Diagram



Functional Pin Description

Package Type	Pin Configurations
TDFN-6	 DFN-6 (Top View)

Pin Description

Pin	Name	Description
1	ISET	Charge Current Program and Charge Current Monitor Pin. The charge current is programmed by connecting a 1% resistor to ground. When charging in constant-current mode, this pin servos to 1V. In all modes, the voltage on this pin can be used to measure the charge current using the following formula: $I_{BAT}=1000/R_{ISET}$
2	FULL	Open-Drain Charge Complete Status Output. When the battery charge complete, the FULL pin is pulled low by an internal N-channel MOSFET. When the LP4055A is charging, FULL is forced high impedance.
3	IN	Positive Input Supply Voltage. Provide power to the charger. V_{IN} can range from 4.5V to 6.5V and should be bypassed with at least a 1μF capacitor.
4	BAT	Charge Current Output. Provides charge current to the battery and regulates the final float voltage to 4.2V. An internal precision resistor divider from this pin sets the float voltage.
5,7	GND	Ground.
6	CHRG	Open-Drain Charge Status Output. When the battery is charging, the CHRG pin is pulled low by an internal N-channel MOSFET. When the LP4055A detects an under voltage lockout condition or charge complete, CHRG is forced high impedance.

Absolute Maximum Ratings Note 1

- ✧ Input to GND(IN) -- -0.3V to 10V
- ✧ BAT to GND -- -5V to 8V
- ✧ IN to BAT -- 8V
- ✧ Other Pin to GND -- -0.3V to 6V
- ✧ BAT Pin Current -- 800mA
- ✧ BAT Short-circuit Duration -- Continuous
- ✧ Maximum Junction Temperature (T_J)-- 125℃
- ✧ Operating Ambient Temperature Range -- -40℃ to 85℃
- ✧ Storage Temperature -- -60℃ to 125℃
- ✧ Maximum Soldering Temperature (at leads, 10 sec) -- 260℃

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Maximum Power Dissipation (TDFN-6, P_D, T_A=25℃) -- 1W
- ✧ Thermal Resistance (TDFN-6, θ_{JA}) -- 95℃/W

ESD Susceptibility

- ✧ HBM(Human Body Model) -- 2KV
- ✧ MM(Machine Model) -- 200V

Electrical Characteristics

(T_A=25℃, V_{IN}=5V, LP4055AQVF,the specifications which apply over the full operating temperature range, unless otherwise noted.)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IN}	Adapter/USB Voltage Range		4.5	5	6.5	V
I_{CC}	Input Supply Current	Charge Mode, R_{ISET} =10K		200	1000	µA
		Standby Mode (Charge Terminated)		50		
V_{FLOAT}	Regulated Output (Float) Voltage	0℃≤T_A≤85℃	4.158	4.2	4.242	V
I_{BAT}	BAT Pin Current	R_{ISET}=10K, Current Mode	85	100	115	mA
		R_{ISET}=2K, Current Mode	450	500	550	
		Standby Mode, V_{BAT}=4.2V			-1	µA
		Shutdown Mode (R_{ISET} NC)		0.1	±2	
		Sleep Mode, V_{IN}=0V			±2	
V_{TRIKL}	Trickle Charge Threshold Voltage	R_{ISET}=10K, V_{BAT} Rising	2.8	2.9	3.0	V
I_{TRIKL}	Trickle Charge Current	$V_{BAT} < V_{TRIKL}$		80		%I_{BAT}
$V_{TR\text{-}HYS}$	Trickle Charge Hysteresis Voltage	R_{ISET}=10K	60	80	110	mV
V_{UV}	V_{IN} Undervoltage Lockout Threshold	V_{IN} Rising	3.7	3.8	3.9	V
$V_{UV\text{-}HYS}$	V_{IN} Undervoltage Lockout Hysteresis		150	200	300	mV
V_{ASD}	V_{IN}–V_{BAT} Lockout Threshold Voltage			150		mV
V_{ISET}	ISET Pin Voltage	R_{ISET}=10K, Charge Mode		1		V
$V_{CHRG/FULL}$	CHRG/FULL Pin Output Low Voltage	$I_{CHRG/FULL}$=5mA			0.5	V
$I_{CHRG/FULL}$	CHRG/FULL Pin Weak Pull-Down Current	I_{STAT} = 5V			5	uA
ΔV_{RECHRG}	Recharge Battery Threshold Voltage	V_{FLOAT}-V_{RECHRG}	100	150	200	mV
T_{LIM}	Junction Temperature in Constant Temperature Mode			125		℃
t_{SS}	Soft-Start Time	I_{BAT}=0 to I_{BAT}=1000V/R_{ISET}		200		µs

Application Information

The LP4055A is a single cell lithium-ion battery charger using a constant-current/constant-voltage algorithm. It can deliver up to 800mA of charge current (using a good thermal PCB layout) with a final float voltage accuracy of ± 1%. The LP4055A includes an internal P-channel power MOSFET and thermal regulation circuitry. No blocking diode or external current sense resistor is required; thus, the basic charger circuit requires only three external components. Furthermore, the LP4055A is capable of operating from a USB power source.

Normal Charge Cycle

A charge cycle begins when the voltage at the IN pin rises above the UVLO threshold level and a 1% program resistor is connected from the ISET pin to ground or when a battery is connected to the charger output. If the BAT pin is less than 2.9V, the charger enters trickle charge mode to bring the battery voltage up to a safe level for full current charging.

When the BAT pin voltage rises above 2.9V, the charger enters constant-current mode, where the programmed charge current is supplied to the battery. When the BAT pin approaches the final float voltage (4.2V), the LP4055A enters constant-voltage mode and the charge current begins to decrease. The charge cycle ends when the charge current drops to 1/10 of the programmed value.

Charge Current Program

The charge current is programmed using a single resistor from the ISET pin to ground. The battery charge current is 1000 times the current out of the ISET pin. The program resistor and the charge current are calculated using the following equations:

$$R_{ISET}=1000V/I_{BAT}$$

$$I_{BAT}=1000V/R_{ISET}$$

The charge current out of the BAT pin can be determined at any time by monitoring the ISET pin voltage using the following equation:

$$I_{BAT}=V_{ISET}/R_{ISET}\times1000$$

Charge Termination

A charge cycle is terminated when the charge current falls to 1/10th the ISET rammed value after the final float voltage is reached. This condition is detected by using an internal, filtered comparator to monitor the ISET pin. When the ISET pin voltage falls below 200mV for longer than t_{TERM}(typically 1ms), charging is terminated. The charge current is latched off and the LP4055A enters standby mode, where the input supply current drops to 200μA. In this state, all loads on the BAT pin must be supplied by the battery. (Note: C/10 termination is disabled in trickle charging and thermal limiting modes).

Charge Status Indicator (CHRG&FULL)

The charge status output has two different states: strong pull-down (~5mA) and high impedance. The strong pull-down state indicates that the LP4055A is in a charge cycle. Once the charge cycle has terminated, the pin state is determined by under voltage lockout conditions. High impedance indicates that the charge cycle complete or the LP4055A is in under voltage lockout mode: either V_{IN} is less than 150mV above the BAT pin voltage or insufficient voltage is applied to the IN pin. A microprocessor can be used to distinguish between these two states.

Function	CHRG	FULL
Charging	LOW	Hi-Z
Charge Complete	Hi-Z	LOW

Charge Current

An internal thermal feedback loop reduces the programmed charge current if the die temperature attempts to rise above a preset value of approximately 125℃. This feature protects the LP4055A from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the LP4055A. The charge current can be set according to typical (not worst-case) ambient temperature with the assurance that the charger will automatically reduce the current in worst-case conditions. SOT power considerations are discussed further in the Applications Information section.

Stability Considerations

The constant-voltage mode feedback loop is stable without an output capacitor provided a battery is connected to the charger output. With no battery present, an output capacitor is recommended to reduce ripple voltage. When using high value, low ESR ceramic capacitors, it is recommended to add a 1Ω resistor in series with the capacitor. No series resistor is needed if tantalum capacitors are used.

Automatic Recharge

Once the charge cycle is terminated, the LP4055A continuously monitors the voltage on the BAT pin using a comparator with a 2ms filter time (t_{RECHRG}). A charge cycle restarts when the battery voltage falls below 4.05V (which corresponds to approximately 80% to 90% battery capacity). This ensures that the battery is kept at or near a fully charged condition and eliminates the need for periodic charge cycle initiations. CHRG output enters a strong pull-down state during recharge cycles.

Under voltage Lockout (UVLO)

An internal under voltage lockout circuit monitors the input voltage and keeps the charger in shutdown mode until V_{IN} rises above the under voltage lockout threshold .The UVLO circuit has a built-in hysteresis of 500mV. Furthermore, to protect against reverse current in the power MOSFET, the UVLO circuit keeps the charger in shutdown mode if V_{IN} falls to within 30mV of the battery voltage. If the UVLO comparator is tripped, the charger will not come out of shutdown mode until V_{IN} raises 100mV above the battery voltage.

Power Dissipation

The conditions that cause the LP4055A to reduce charge current through thermal feedback can be approximated by considering the power dissipated in the IC. Nearly all of this power dissipation is generated by the internal MOSFET—this is calculated to be approximately:

$$P_D=(V_{IN}-V_{BAT})\times I_{BAT}$$

Where PD is the power dissipated, V_{IN} is the input supply voltage, VBAT is the battery voltage and IBAT is the charge current. The approximate ambient temperature at which the thermal feedback begins to protect the IC is:

$$T_A=125℃-P_D\times\theta_{JA}$$

$$T_A=125℃-(V_{IN}-V_{BAT})\times I_{BAT}\times\theta_{JA}$$

IN Bypass Capacitor

Many types of capacitors can be used for input bypassing; however, caution must be exercised when using multilayer ceramic capacitors. Because of the self-resonant and high Q characteristics of some types of ceramic capacitors, high voltage transients can be generated under some start-up conditions, such as connecting the charger input to a live power source .Adding a 1.5Ω resistor in series with an X5R ceramic capacitor will minimize start-up voltage transients.

Layout Considerations

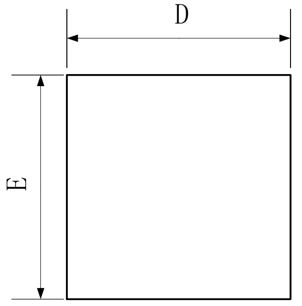
For the main current paths as indicated in bold lines, keep their traces short and wide.

Put the input and output capacitor as close as possible to the device pins (IN, BAT and GND).

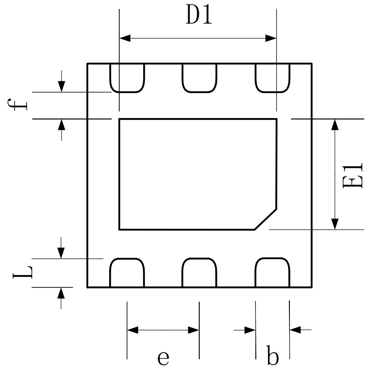
Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors

Packaging Information

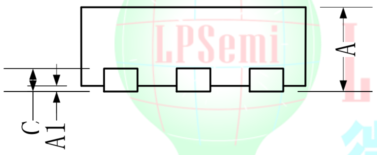
TDFN-6



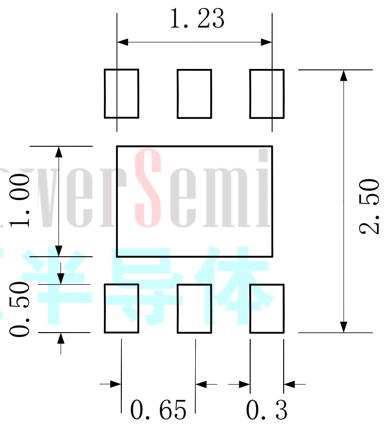
TOP VIEW



BOTTOM VIEW



SIDE VIEW



Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.22	0.30	0.35
c	0.18	0.20	0.25
D	1.90	2.00	2.10
D1	1.00	1.23	1.70
E	1.90	2.00	2.10
E1	0.50	0.70	1.10
e	0.65 BSC		
L1	0.20	0.30	0.40
f	0.20	-	-