





## Functional Pin Description

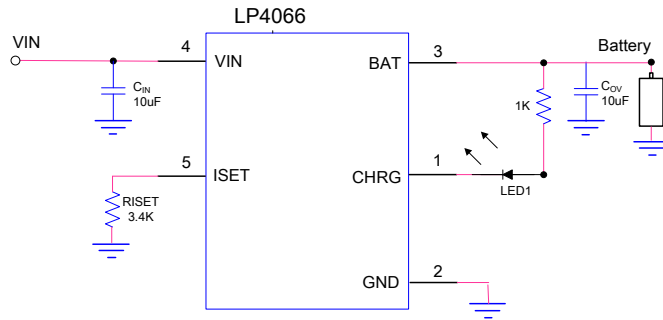
Package Type	Pin Configurations
	LP4066AB6F
SOT23-5	<p style="text-align: center;">SOT23-5 TOP VIEW</p>

## Pin Description

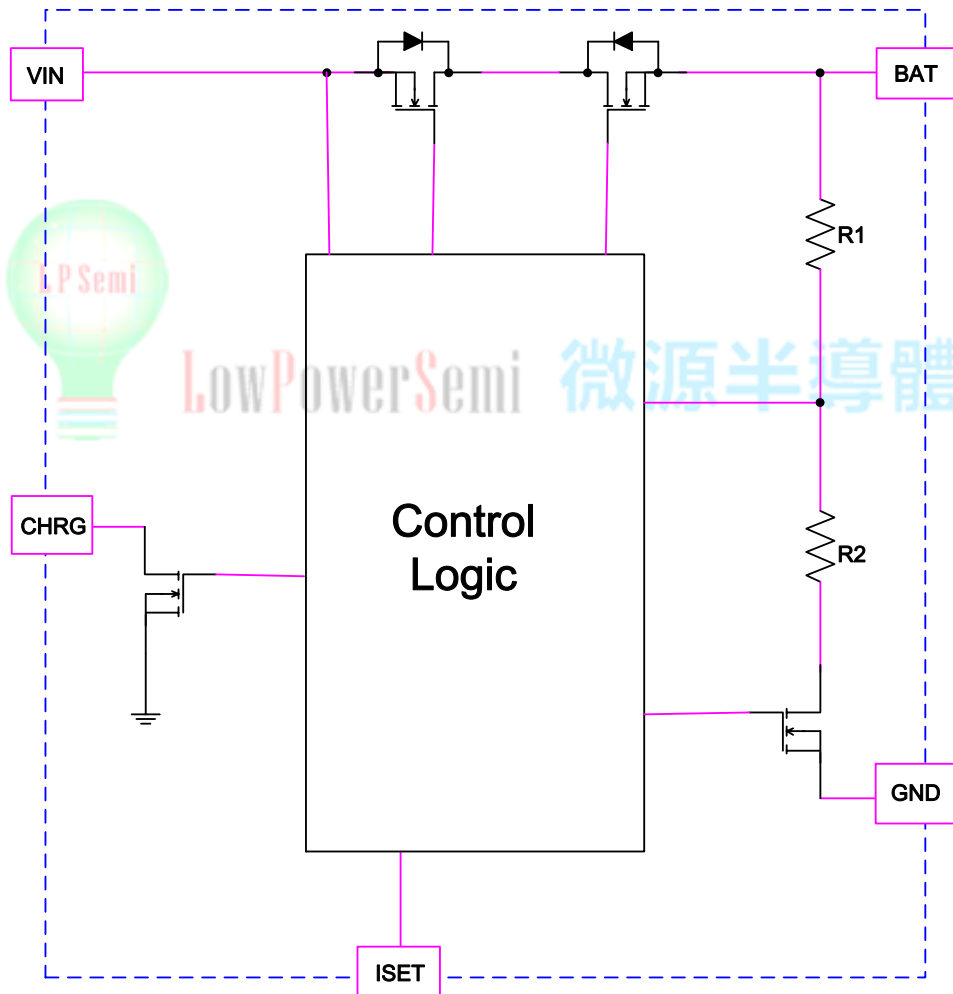
No.	NAME	DESCRIPTION
1	CHRG	Open-Drain Charge Status Output. When the battery is charging, the CHRG pin is pulled low by an internal NMOS. When the charge cycle is completed, the pin could be pulled High by an external pull high resistor.
2	GND	GND is the connection to system ground.
3	BAT	BAT is the connection to the battery. Typically a 10μF Tantalum capacitor is needed for stability when there is no battery attached. When a battery is attached, only a 1uF ceramic capacitor is required.
4	VIN	VIN is the input power source. Connect to a wall adapter.
5	ISET	Charge Current Program. The charge current is programmed by connecting a 1% resistor( $R_{ISET}$ ) to ground. $I_{BAT} = \frac{1700 \times V_{ISET}}{R_{ISET}}$



### Typical Application Circuit



### Function Block Diagram





## Absolute Maximum Ratings <sup>Note 1</sup>

✧ Input Voltage to GND	-----	-0.3V to 28V
✧ BAT Voltage GND	-----	- 5V to 20V
✧ Other pin to GND	-----	-0.3V to 6.5V
✧ Maximum Junction Temperature	-----	125°C
✧ Maximum Soldering Temperature (at leads, 10 sec)	-----	260°C
✧ Operating Junction Temperature Range (T <sub>J</sub> )	-----	-20°C to 85°C
✧ Storage Temperature	-----	-65°C to 165°C

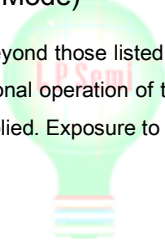
## Thermal Information

✧ Maximum Power Dissipation ( P <sub>D</sub> , T <sub>A</sub> =25°C)	-----	0.6W
✧ Thermal Resistance (θ <sub>JA</sub> )	-----	200°C/W

## ESD Susceptibility

✧ HBM(Human Body Mode)	-----	2KV
✧ MM(Machine Mode)	-----	200V

**Note 1.** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





## Electrical Characteristics

( $T_A=25^{\circ}\text{C}$ ,  $V_{IN}=5\text{V}$ , unless otherwise noted.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
$V_{IN}$	Input Voltage		4.5	5	5.8	V
$I_{IN}$	Input Supply Current	$I_{BAT}=4.2\text{V}$		40		$\mu\text{A}$
$V_{FLOAT}$	Regulated Output (Float) Voltage	$I_{BAT}=40\text{mA}$ ,	4.158	4.2	4.242	V
$V_{UV}$	$V_{IN}$ Under Voltage Lockout Threshold	From $V_{IN}$ Low to High		3.3		V
$V_{OVP}$	Input Voltage OVP	$V_{IN}$ Rising		6.2		V
$V_{OVP\_HYS}$	OVP Hysteresis			150		mV
$I_{BAT}$	BAT Pin Current	$R_{ISET}=3.4\text{k}$ , Current Mode		500		mA
		$R_{ISET}=17\text{k}$ , Current Mode		100		mA
		$V_{BAT}=4.2\text{V}$		1		$\mu\text{A}$
		$V_{IN}=\text{float or }0\text{V}$		1		
$I_{TRIKL}$	Trickle Charge Current	$V_{BAT}<V_{TRIKL}$ , $R_{ISET}=10\text{k}$ , Current Mode		10		$\%I_{BAT}$
$V_{TRIKL}$	Trickle Charge Threshold Voltage	$V_{BAT}$ Rising		2.6		V
$V_{TRHYS}$	Trickle Charge Hysteresis Voltage			150		mV
$I_{TERM}$	Termination Current Threshold			10		$\%I_{BAT}$
$V_{ISET}$	ISET Pin Voltage	$R_{ISET}=10\text{k}$ , Current Mode		1		V
$I_{CHRG}$	CHRG Pin Weak Pull-Down Current	$V_{CHRG}=5\text{V}$			5	$\mu\text{A}$
$V_{CHRG}$	CHRG Pin Output Low Voltage	$I_{CHRG}=5\text{mA}$			0.5	V
$\Delta V_{RECHRG}$	Recharge Battery Threshold Voltage	$V_{FLOAT}-V_{RECHRG}$		150		mV
$T_{LIM}$	Junction Temperature in Constant Temperature Mode			125		$^{\circ}\text{C}$



## Application Information

### Input Voltage Range

The LP4066 has built-in input voltage surge protection as high as +28V. The charger IC will be automatically disabled when the input voltage is lower than 3.3V or higher than 6.2V.

A charge cycle begins when the voltage at the VIN pin rises above the 4.4V level, when a battery is connected to the charger output. If the BAT pin is less than 2.6V, the charger enters trickle charge mode. In this mode, the LP4066 supplies approximately 1/10 the ISET programmed charge current to bring the battery voltage up to a safe level for full current charging. When the BAT pin voltage rises above 2.6V, the charger enters constant-current mode(CC), where the ISET programmed charge current is supplied to the battery. When the BAT pin approaches the final float voltage, the LP4066 enters constant-voltage mode(CV) and the charge current begins to decrease, and the battery full indication is set when the charge current in the CV mode is reduced to the programmed full battery current (1/10).

### Charge Termination

A charge cycle is terminated when the charge current falls to 1/10th the ISET programmed value after the final float voltage is reached. This condition is detected by using an internal, filtered comparator to monitor the ISET pin. When the ISET pin voltage falls below 100mV for longer than t<sub>TERM</sub>(typically 1ms), charging is terminated.

### ISET programming Charge Current

The charge current (I<sub>BAT</sub>) is set by a resistor (R<sub>ISET</sub>) connecting from the ISET pin to GND. The relationship of the charge current and the programming resistance is established by the following equations ( V<sub>ISET</sub>=1V ).

$$I_{BAT} = \frac{1700 \times V_{ISET}}{R_{ISET}}$$

### Automatic Recharge

Once the charge cycle is terminated, the LP4066 continuously monitors the voltage on the BAT pin. A charge cycle restarts when the battery voltage falls below 4.05V (which corresponds to approximately 80% to 90% battery capacity). This ensures that the battery is kept at or near a fully charged condition and eliminates the need for periodic charge cycle initiations.

### Charge Status Indicator(CHRG)

After application of a 5V source, the input voltage rises above the UVLO and sleep thresholds (VIN>VBAT+VDT), but is less than OVP (VIN<VOVP), then the PG turns on and provides a low impedance path to ground.

CHRG has two different states: strong pull-down (~5mA) and high impedance. The strong pull-down state indicates that the LP4066A is in a charge cycle. When the charger is entered CV mode and once the charge current has reduced to the battery full charge current threshold (I<sub>TERM</sub>), the CHRG pin will become high impedance.

Function	CHRG
Charging	High
Charge Finish	Low

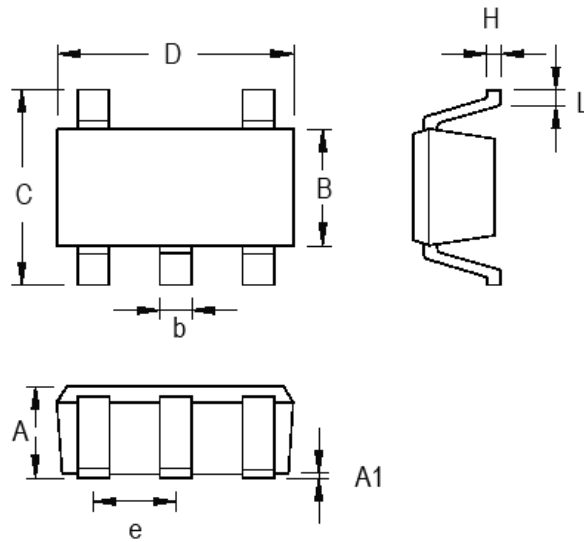
### Thermal Limiting

An internal thermal feedback loop reduces the I<sub>SET</sub> programmed charge current if the die temperature attempts to rise above a preset value of approximately 125°C. This feature protects the LP4066 from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the LP4066. The charge current can be set according to typical (not worst-case) ambient temperature with the assurance that the charger will automatically reduce the current in worst-case conditions.



Packaging Information

SOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-5 Surface Mount Package

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