



Multi-Channel DC-DC Converter for LCD Panel

General Description

The LP6286 includes a high-efficiency boost regulator, a gate pulse modulator (GPM), a voltage detector, a VCOM buffer, and dual charge pump controller for active matrix TFT LCDs.

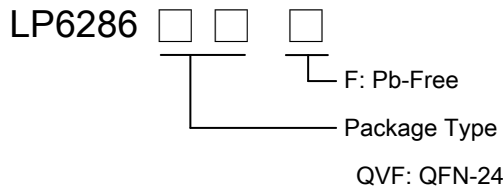
The converter is a high switching frequency current-mode regulator with an integrated N-Channel 0.2Ω MOSFET that allows the use of small inductors and ceramic capacitors.

The OPA can drive the LCD VCOM voltage by Unity-Gain buffer, that features high short-circuit current, fast slew rate and rail-to-rail inputs and outputs.

The charge pump controller provides regulated TFT Gate-On voltage. The regulation of the charge pump is generated by the internal comparator that senses the output voltage and compares it with an internal reference.

Other features include under-voltage protection, short circuit protection, thermal shutdown protection and under-voltage lockout (UVLO). The LP6286 is available in a space saving QFN-24 (0.5mm pitch) package.

Order Information



Features

- ◆ Wide V_{IN} Range: 2.5V to 5.5V
- ◆ 1.2MHz Current-Mode Boost Regulator
 - Fast Transient Response to Pulsed Load
 - Adjustable Output Voltage ($\pm 1\%$)
 - Built-In 3A, 0.2Ω N-MOSFET
 - High Efficiency Up to 90%
 - Internal Soft-Start
- ◆ GPM Controller with Adjustable
 - Power-On Delay and Falling Time
 - Adjustable VGHM Delay
- ◆ Low Voltage Detector
 - Programmable Detecting Voltage
 - Open-Drain Reset Output
- ◆ Operation Amplifier for VCOM Buffer
- ◆ VGH and VGL Charge Pump
- ◆ Under-Voltage Protection
- ◆ Over-Temperature Protection
- ◆ Available in QFN-24 (4x4mm)
- ◆ RoHS Compliant and Halogen Free
- ◆ Pb-Free Package

Applications

- ◆ TFT LCD Panel
- ◆ TFT LCD Monitor

Marking Information

| Device | Marking | Package | Shipping |
|--|----------------------|---------|----------|
| LP6286 | LPS LP6286 YWX | QFN-24 | 3K/REEL |
| Y: Y is year code. W: W is week code. X: X is series number. | | | |





Typical Application Circuit

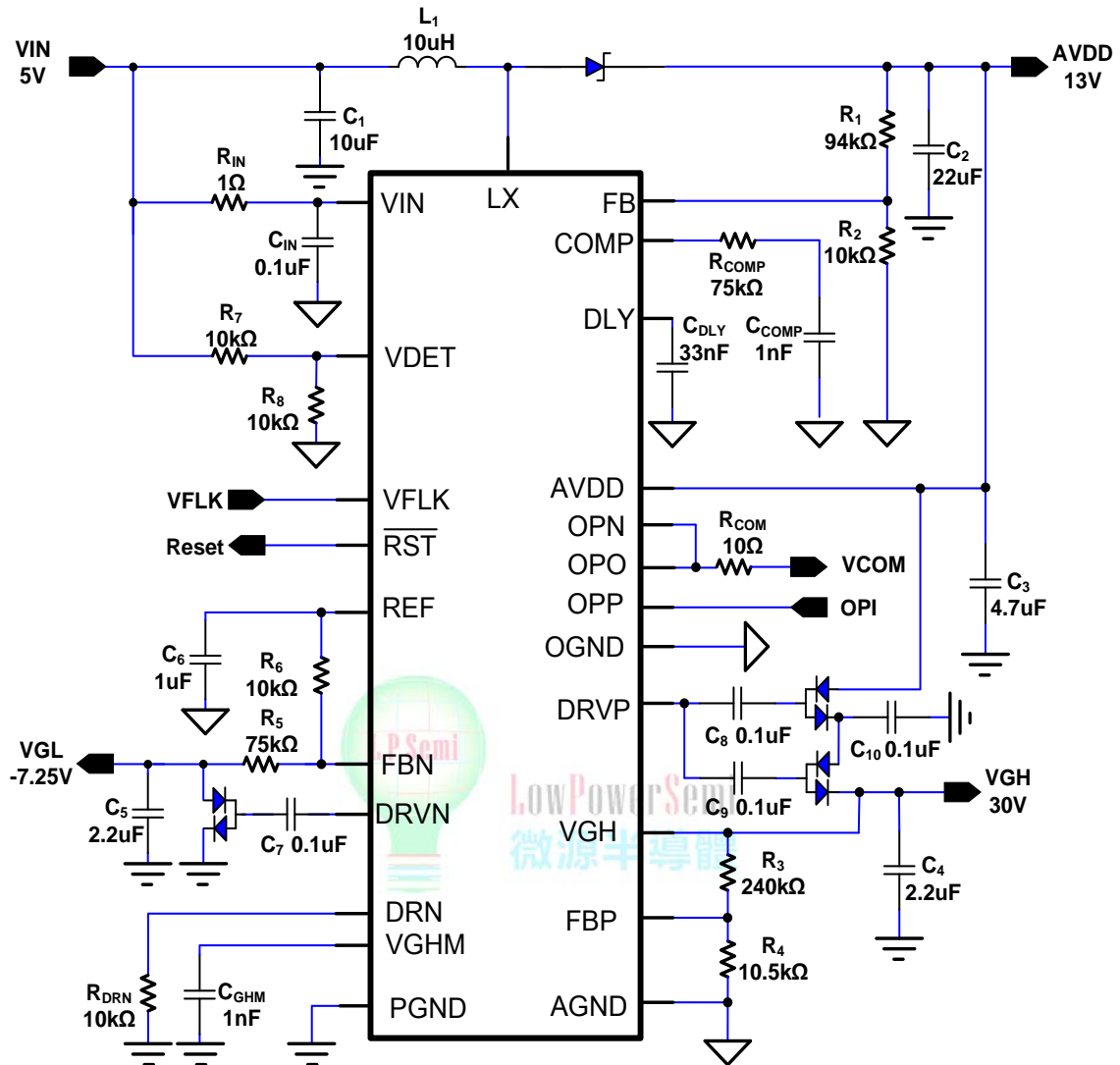


Figure 1. Typical Application Circuit of LP6286



Pin Configuration

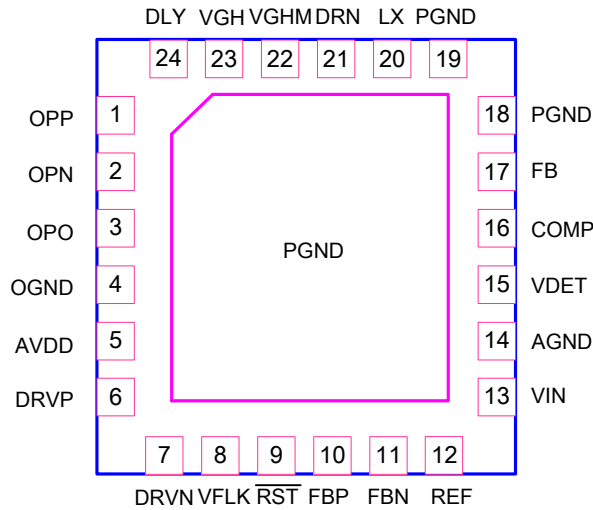


Figure 2. QFN-24 Package (4mm x 4mm) Top View

Function Block Diagram

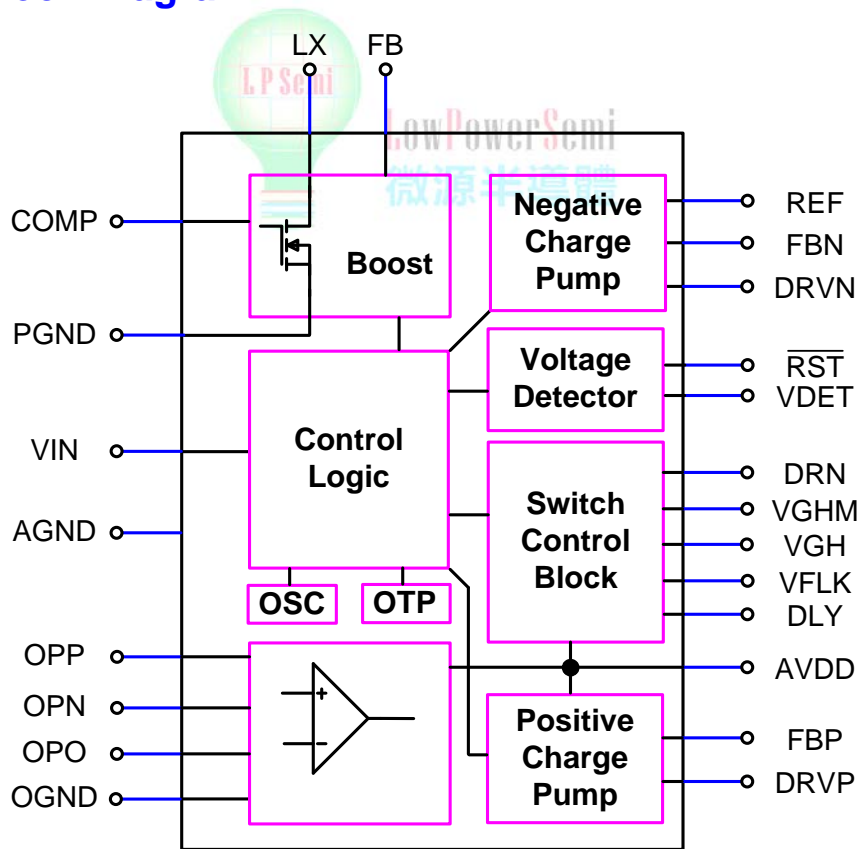


Figure 3. Function Block Diagram



Functional Pin Description

| Pin NO. | Pin Name | Description |
|---------|-------------------------|---|
| 1 | OPP | OPA Non-Inverting Input. |
| 2 | OPN | OPA Inverting Input. |
| 3 | OPO | OPA Output. |
| 4 | OGND | Ground for OPA. Connect this pin to ground. |
| 5 | AVDD | VDD for Source Driver Power. This also supplies the Charge-Pump/OPA power source. |
| 6 | DRVVP | VGH Charge-Pump Regulator Driver Output. |
| 7 | DRVVN | VGL Charge-Pump Regulator Driver Output. |
| 8 | VFLK | VFLK is produced by timing controller for charging or discharging VGHM. |
| 9 | $\overline{\text{RST}}$ | Open-Drain Output for Reset. Active Low. |
| 10 | FBP | VGH Charge-Pump Regulator Feedback Input. Connect to an external resistive voltage divider from the VGH to GND to set the output voltage. |
| 11 | FBN | VGL Charge-Pump Regulator Feedback Input. Connect to an external resistive voltage divider from the VGL to REF to set the output voltage. |
| 12 | REF | Reference Voltage Output. Connect a ceramic capacitor between REF and GND. |
| 13 | VIN | Supply Input. The input voltage range is between 2.5V to 5.5V. Connect a ceramic capacitor between VIN and GND. |
| 14 | AGND | Analog GND. |
| 15 | VDET | Voltage Detector Input. Connect to an external resistive voltage divider from the VIN to AGND. |
| 16 | COMP | Boost Regulator Error Amplifier Compensation Pin. |
| 17 | FB | Boost Regulator Feedback Input. Connect to an external resistive voltage divider from the output to FB to set the output voltage. |
| 18 | PGND | Power Ground. |
| 19 | PGND | Power Ground. |
| 20 | LX | Boost Regulator Switching Node. Connect the inductor and the schottky diode to LX. |
| 21 | DRN | GPM Discharge Pin. Connect a resistor between DRN and GND. |
| 22 | VGHM | GPM Output. |
| 23 | VGH | GPM Input. |
| 24 | DLY | VGHM Delay Discharge Time. Connect a capacitor between DLY and GND. |
| EP | | Exposed pad. Connect this pin to other gnd pin. |



Absolute Maximum Ratings ^{Note 1}

| | | |
|--|-------|------------------------|
| ◇ VIN, RST to GND | ----- | -0.3V to +7V |
| ◇ AVDD, LX to GND | ----- | -0.3V to +20V |
| ◇ VGH to GND | ----- | -0.3V to +36V |
| ◇ FB, FBP, FBN, DLY, VDET, $\overline{\text{RST}}$, COMP, VFLK, REF | ----- | -0.3V to (VIN + 0.3V) |
| ◇ OPP, OPN, OPP, DRVP, DRVN to GND | ----- | -0.3V to (AVDD + 0.3V) |
| ◇ VGHM, VGH, DRN | ----- | -0.3V to +30V |
| ◇ Operating Junction Temperature Range (TJ) | ----- | -40°C to +150°C |
| ◇ Operation Ambient Temperature Range | ----- | -40°C to +85°C |
| ◇ Storage Temperature Range | ----- | -65°C to +150°C |
| ◇ Maximum Soldering Temperature (at leads, 10sec) | ----- | +260°C |
| ◇ Maximum Junction Temperature | ----- | +150°C |

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

| | | |
|---------------------------|-------|--------|
| ◇ Thermal Resistance | | |
| QFN-24 4x4, θ_{JA} | ----- | 78°C/W |
| QFN-24 4x4, θ_{JC} | ----- | 25°C/W |





Electrical Characteristics

($V_{IN}=5V$, $V_{AVDD}=13V$, $T_A=25^\circ C$, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|-------------------------------------|----------------------|---------------------------|-------|------|-------|------------|
| General | | | | | | |
| V_{IN} Input Supply Voltage | V_{IN} | | 2.5 | | 5.5 | V |
| AVDD | AVDD | | 6 | | 18 | V |
| AVDD Over Voltage Protect | V_{OVP} | | | 18 | 20 | V |
| Boost Switching Frequency | F_{LX} | | 1 | 1.2 | 1.4 | MHz |
| Charge Pump Frequency | F_{CP} | | 500 | 600 | 700 | kHz |
| V_{IN} Supply Current | I_Q | VFB=1.5V, LX no Switching | | 0.4 | 0.8 | mA |
| | | VFB=1.2V, LX Switching | | 2.3 | 5 | mA |
| AVDD Operation Current | I_{AVDD} | $V_{OPP}=5V$ | | 1.2 | 3 | mA |
| Input UVLO Threshold | $V_{UVLO(VTH)}$ | V_{IN} Rising | 2.15 | 2.25 | 2.35 | V |
| UVLO Threshold Hysteresis | $V_{UVLO(HYS)}$ | Falling Hysteresis | | 100 | | mV |
| Reference Voltage | V_{REF} | | 1.238 | 1.25 | 1.262 | V |
| Thermal Shutdown Threshold | T_{SD} | | | 160 | | $^\circ C$ |
| Thermal Shutdown Hysteresis | | | | 30 | | $^\circ C$ |
| Boost Regulator | | | | | | |
| Maximum Duty-Cycle | D_{MAX} | | 86 | 90 | 94 | % |
| Feedback Voltage | V_{FB} | | 1.238 | 1.25 | 1.262 | V |
| Transconductance of Error Amplifier | G_m | $\Delta I_{COMP}=5\mu A$ | | 85 | | $\mu A/V$ |
| Voltage Gain | A_V | | | 1500 | | V/V |
| Switch-ON Resistance | $R_{DS(ON)}$ | | | 200 | | m Ω |
| Current Limit | I_{Limit} | | 2.5 | 3 | | A |
| LX Leak Current | I_{Leak} | LX Off. | | 0.01 | 20 | μA |
| Internal Soft Start Time | T_{SS} | | | 10 | | ms |
| UVP Fault Protection Voltage | V_{UVP} | V_{FB} Falling | 0.95 | 1 | 1.05 | V |
| UVP Fault Delay | T_{UVP} | | | 55 | | ms |
| Short Circuit Protection Voltage | V_{SCP} | | | 100 | | mV |
| Voltage Detector | | | | | | |
| Detecting Voltage Adjustment | V_{DET} | HYS=50mV | | 1.25 | | V |
| \overline{RST} Pull Low Voltage | $V_{\overline{RST}}$ | $I_{RST}=5mA$ | | | 0.2 | V |
| \overline{RST} Blanking Time | $T_{\overline{RST}}$ | | 140 | 160 | 180 | ms |



Electrical Characteristics (Continued)

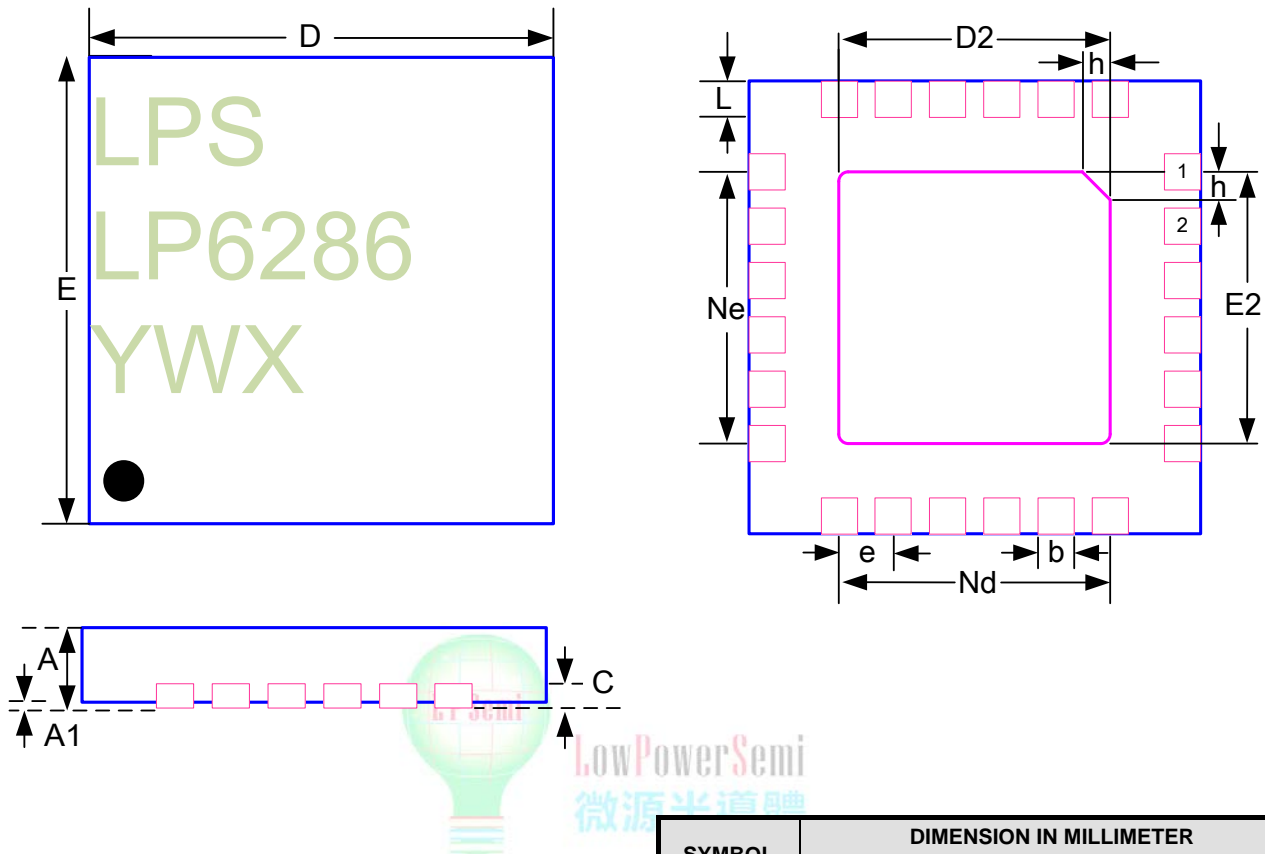
($V_{IN} = 5V$, $V_{AVDD} = 13V$, $T_A = 25^\circ C$, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|--------------------------------|-----------------|---|------|-----------|------|------------|
| Gate Pulse Modulator | | | | | | |
| DLY Source Current | I_{DLY} | | 4 | 5 | 6 | μA |
| DLY Threshold Voltage | V_{DLY} | | 1.22 | 1.25 | 1.28 | V |
| DLY Discharge Resistor | R_{DLY} | | | 10 | | Ω |
| VFLK Input High Voltage | V_{FLK_H} | | 2 | | | V |
| VFLK Input Low Voltage | V_{FLK_L} | | | | 0.5 | V |
| Propagation Delay VFLY to VGHM | T_{PP} | $V_{GH} = 30V$ | | 200 | | ns |
| VGH Switch ON Resistance | R_{DS_GH} | $V_{DLY} = 1.5V$, $V_{FLK} = V_{IN}$ | | 15 | 30 | Ω |
| DRN Switch ON Resistor | R_{DS_DRN} | $V_{DLY} = 1.5V$, $V_{FLK} = GND$ | | 30 | 60 | Ω |
| VGHM Discharge Resistor | R_{DS_VGHM} | $V_{DLY} = 1V$ | 1.5 | 2.5 | 3.5 | k Ω |
| Charge Pump | | | | | | |
| Charge Pump Soft Start Time | T_{SS_CP} | | | 3.4 | | ms |
| Positive Feedback Voltage | V_{FBP} | | 1.23 | 1.25 | 1.27 | V |
| DRVP Switch ON Resistance | R_{DS_DRVP1} | | | 3 | 20 | Ω |
| | R_{DS_DRVP2} | | | 3 | 20 | Ω |
| Negative Feedback Voltage | V_{FBN} | | 235 | 250 | 265 | mV |
| DRVN Switch ON Resistance | R_{DS_DRVN1} | | | 3 | 20 | Ω |
| | R_{DS_DRVN2} | | | 3 | 20 | Ω |
| Operation Amplifier | | | | | | |
| Input Offset Voltage | V_{OS} | $V_{OPO} = V_{AVDD}/2$ | | 2 | 15 | mV |
| Output Voltage Swing High | V_{OH} | $V_{OPP} = V_{AVDD}/2$, $I_{Load} = -50mA$ | | 5.03 | 5.06 | V |
| | | $V_{OPP} = V_{AVDD}$, $I_{Load} = 5mA$ | 9.85 | 9.92 | | |
| Output Voltage Swing Low | V_{OL} | $V_{OPP} = V_{AVDD}/2$, $I_{Load} = 50mA$ | 4.94 | 4.97 | | |
| | | $V_{OPP} = 0V$, $I_{Load} = -5mA$ | | 0.08 | 0.15 | |
| Short Circuit Current | V_{OP_Short} | Unity-Gain, $V_{OPO} = V_{AVDD}/2$ | | ± 200 | | mA |
| Slew Rate | SR | $V_{OPP} = 2V$ to $8V$, $8V$ to $2V$, 20% to 80% | | 40 | | V/ μs |



Outline Information

QFN-24 Package (4x4) pitch 0.5 (Unit: mm)



| SYMBOL | DIMENSION IN MILLIMETER | | |
|--------|-------------------------|-------|-------|
| | MIN | NOM | MAX |
| A | 0.700 | 0.750 | 0.800 |
| A1 | --- | 0.020 | 0.050 |
| b | 0.180 | 0.250 | 0.300 |
| C | 0.180 | 0.200 | 0.250 |
| D | 3.900 | 4.000 | 4.100 |
| D2 | 2.400 | 2.500 | 2.600 |
| E | 3.900 | 4.000 | 4.100 |
| E2 | 2.400 | 2.500 | 2.600 |
| e | 0.500 BSC | | |
| Nd | 2.500 BSC | | |
| Ne | 2.500 BSC | | |
| L | 0.350 | 0.400 | 0.450 |
| h | 0.300 | 0.350 | 0.400 |

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