



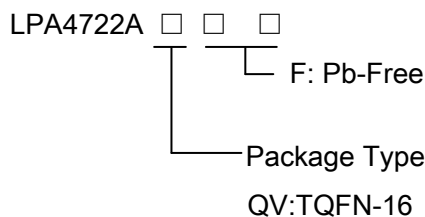
## 5V, Differential Input, DirectDrive, 215mW Stereo Headphone Amplifiers with Shutdown

### General Description

The LPA4722A stereo headphone amplifiers are designed for portable equipment where board space is at a premium. The LPA4722A deliver up to 215mW per channel into a 16Ω load or 200mW into a 32Ω load and have low 0.005% THD+N. An 80dB at 217Hz power-supply rejection ratio (PSRR) allows these devices to operate from noisy digital supplies without an additional linear regulator. Comprehensive anticlick-and-pop circuitry suppresses audible clicks and pops on startup and shutdown. A low-power shutdown mode reduces the supply current to 0.1μA.

The LPA4722A operates from a single 2.5V to 5.5V supply, consumes only 5mA supply current, and is specified over the extended -40 °C to +85 °C temperature range. The devices are available in tiny 16-pin TQFN (3mm× 3mm×0.8mm) packages.

### Order Information



### Applications

- ✧ MP3 Players
- ✧ Smart/Cellular Phones
- ✧ PDAs
- ✧ Portable Audio
- ✧ Notebook and Desktop PCs
- ✧ Flat-Panel Monitors

### Features

- ◆ 2.5V to 5.5V Single-Supply Operation
- ◆ High PSRR (80dB at 217Hz) Eliminates LDO
- ◆ No Bulky DC-Blocking Capacitors Required
- ◆ Ground-Referenced Outputs Eliminate DC Bias Voltage on Headphone Ground Pin
- ◆ No Degradation of Low-Frequency Response Due to Output Capacitors
- ◆ Differential Inputs for Enhanced Noise Cancellation
- ◆ 194mW into 32Ω Load from 5V Power Supply at THD+N = 0.1% (TYP, per Channel)
- ◆ Low 0.008% THD+N
- ◆ Short-Circuit and Thermal-Overload Protection
- ◆ Integrated Click-and-Pop Suppression
- ◆ Low Quiescent Current (3mA at VDD = 5V)
- ◆ Shutdown Control
- ◆ Under-Voltage Lockout Function
- ◆ -40°C to +85°C Operating Temperature Range
- ◆ Available in a Space-Saving 16-Pin TQFN (3mm× 3mm× 0.8mm) Package

### Marking Information

Device	Marking	Package	Shipping
LPA4722A	LPS LPA4722A XXX	TQFN-16	3K/REEL



## Functional Pin Description

Package Type	Pin Configurations
TQFN	

**Figure 1. The Pin Configurations**

## Pin Description

PIN	NAME	DESCRIPTION
1	PVDD	Charge-Pump Power Supply. Powers charge-pump inverter, charge-pump logic, and oscillator. Connect to positive supply (2.5V to 5.5V). Bypass with a 1μF capacitor to PGND as close to the pin as possible.
2	C1P	Flying Capacitor Positive Terminal. Connect C1P and C1N with 1uF capacitor.
3	PGND	Power Ground. Connect PGND and SGND together at the system ground plane.
4	C1N	Flying Capacitor Negative Terminal.
5	PVSS	Charge-Pump Output. Connect to PGND with 1uF capacitor.
6	SGND	Signal Ground. Connect PGND and SGND together at the system ground plane.
7	INR+	Noninverting Right-Channel Audio Input.
8	INR-	Inverting Right-Channel Audio Input.
9,13	SVDD	Amplifier Positive Power Supply. Connect to positive supply (2.5V to 5.5V). Bypass with a 1μF capacitor to SGND as close to the pin as possible.
10	OUTR	Right-Channel Output.
11	BIAS	Amplifier Negative Power Supply. Connect to PVSS.
12	OUTL	Left-Channel Output.
14	INL-	Inverting Left-Channel Audio Input.
15	INL+	Noninverting Left-Channel Audio Input.
16	SHDN	Active-Low Shutdown Input.
-	EP	Exposed Paddle. Electrically connect to PGND or leave unconnected.



### Typical Application Circuit

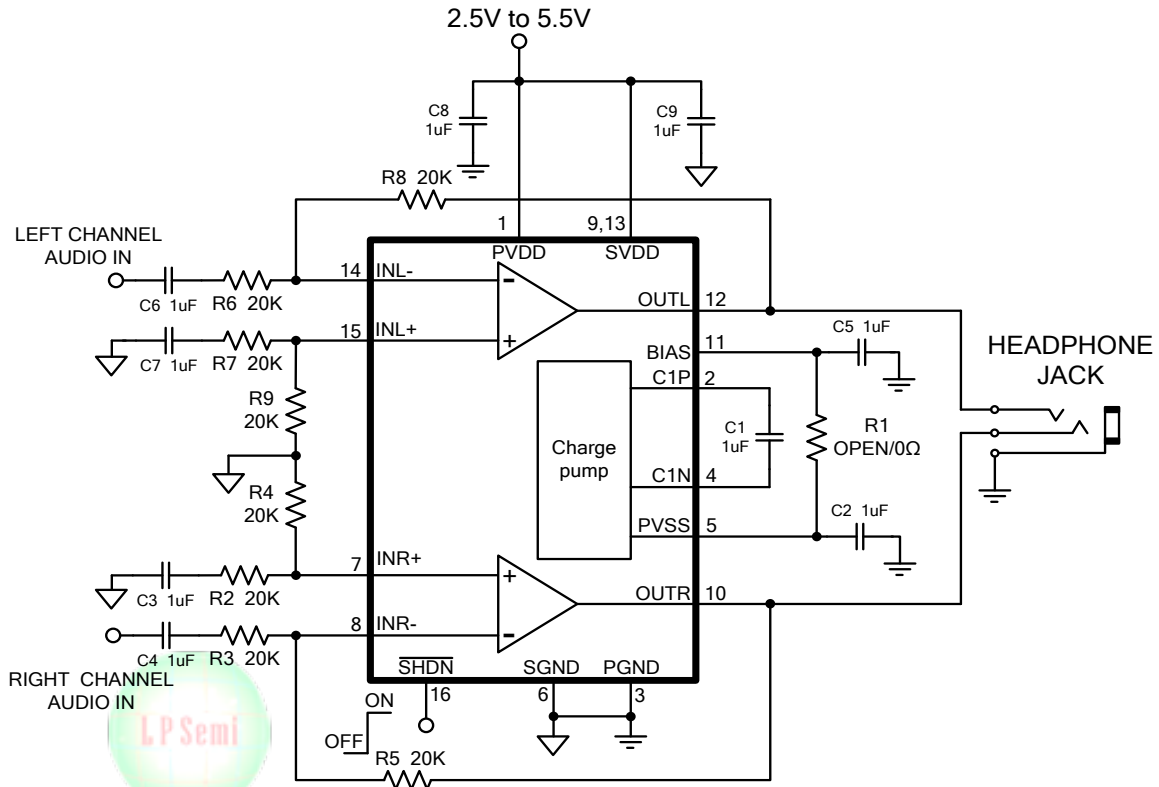


Figure 2. Typical Single-Ended Input Application Circuit

**NOTES:**

1. To ensure the normal operation of the device, decoupling capacitor (C8,C9) must be placed as close to LPA4722A as possible. The loop length formed by C8 and C9.
2. In order to get good performance, it's important to select the right C1, C2, C3, C5 and C8 in application. All tests are performed with circuit set up with X5R and X7R capacitors. Capacitors having high dissipative loss, such as Y5V capacitor, may cause performance degradation and unexpected system behavior.

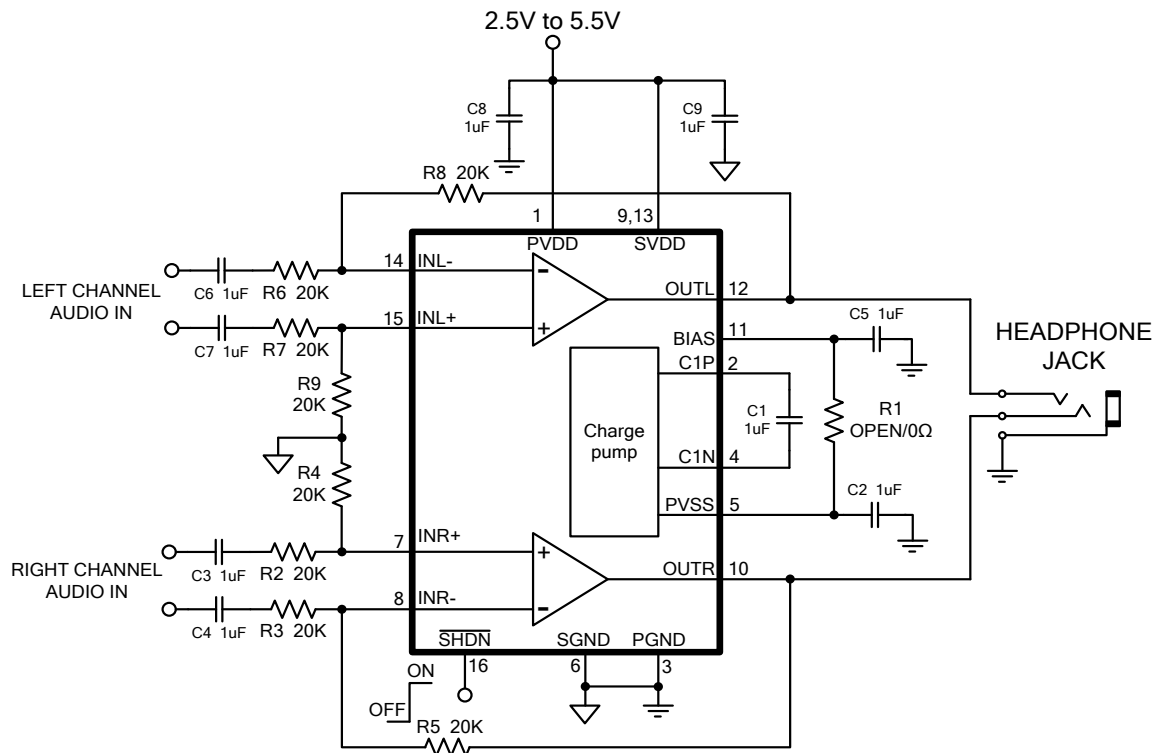


Figure 3. Typical Differential Input Application Circuit

NOTES:

1. To ensure the normal operation of the device, decoupling capacitor (C8,C9) must be placed as close to LPA4722A as possible. The loop length formed by C8 and C9.
2. In order to get good performance, it's important to select the right C1, C2, C3, C5 and C8 in application. All tests are performed with circuit set up with X5R and X7R capacitors. Capacitors having high dissipative loss, such as Y5V capacitor, may cause performance degradation and unexpected system behavior.

### Absolute Maximum Ratings

PGND to SGND .....	-0.3V to +0.3V
PVSS to BIAS .....	0V
PVDD and SVDD to PGND or SGND .....	-0.3V to +6V
PVSS and BIAS to PGND or SGND .....	-6V to +0.3V
IN to SGND .....	(BIAS - 0.3V) to (SVDD + 0.3V)
SHDN to SGND .....	-0.3V to (SVDD + 0.3V)
OUT to SGND .....	(BIAS - 0.3V) to (SVDD + 0.3V)
C1P to PGND .....	-0.3V to (PVDD + 0.3V)
C1N to PGND .....	(PVSS - 0.3V) to + 0.3V
Output Short Circuit to GND or VDD .....	Continuous
Junction Temperature .....	+150°C
Storage Temperature Range .....	-65°C to +150°C
Lead Temperature (Soldering, 10s) .....	+260°C
ESD Susceptibility HBM .....	2000V
HBM (Output pins to Supply and Ground pins) .....	2000V
MM .....	200V

### Recommended Operating Conditions

Supply Voltage Range .....	2.5V to 5.5V
Operating Temperature Range .....	-40°C to +85°C



## Electrical Characteristics

(PVDD = SVDD = +5V, PGND = SGND = 0V,  $\overline{\text{SHDN}}$  = SVDD, C1 = C2 = 1 $\mu$ F, R<sub>L</sub> =  $\infty$ , resistive load referenced to ground, for LPA4722A gain = -1V/V (R<sub>IN</sub> = R<sub>F</sub> = 20k $\Omega$ ), T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C, unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>GENERAL</b>						
Supply Voltage Range	PVDD		2.5		5.5	V
Quiescent Supply Current	I <sub>Q</sub>			3		mA
Shutdown Supply Current	I <sub>SD</sub>	$\overline{\text{SHDN}}$ = SGND = PGND		0.3		$\mu$ A
$\overline{\text{SHDN}}$ Input Logic High	V <sub>IH</sub>		1			V
$\overline{\text{SHDN}}$ Input Logic Low	V <sub>IL</sub>				0.6	V
$\overline{\text{SHDN}}$ to Full Operation Time	t <sub>SON</sub>			0.5		ms
<b>AMPLIFIERS</b>						
Gain Matching	$\Delta A_V$	LPA4722A, between the right and left channels		$\pm 0.2$		%
Output Offset Voltage	V <sub>OS</sub>	Between OUTL(OUTR) and GND, input AC-coupled to ground		0.2		mV
Common Mode Rejection Ratio	CMRR	Input referred, LPA4722A, T <sub>A</sub> = +25°C	-70	-86		dB
Power Supply Rejection Ratio	PSRR	DC, VDD = 2.5V to 5.5V, input referred	-80	-90		dB
		f = 217Hz, 100mV <sub>P-P</sub> ripple, input referred		-80		
		f = 10kHz, 100mV <sub>P-P</sub> ripple, input referred		-60		
Output Power	P <sub>OUT</sub>	R <sub>L</sub> = 16 $\Omega$ , THD+N = 0.1%, T <sub>A</sub> = +25°C		215		mW
		R <sub>L</sub> = 32 $\Omega$ , THD+N = 0.1%, T <sub>A</sub> = +25°C		194		
Output Impedance in Shutdown				10		k $\Omega$
Total Harmonic Distortion Plus Noise	THD+N	R <sub>L</sub> = 16 $\Omega$ , P <sub>OUT</sub> = 55mW, f = 1kHz		0.007		%
		R <sub>L</sub> = 32 $\Omega$ , P <sub>OUT</sub> = 125mW, f = 1kHz		0.005		
Signal-to-Noise Ratio	SNR	R <sub>L</sub> = 32 $\Omega$ , P <sub>OUT</sub> = 20mW, f = 22Hz to 22kHz		100		dB
Noise	V <sub>n</sub>	22Hz to 22kHz bandwidth, input AC grounded		7		$\mu$ V <sub>RMS</sub>
Capacitive Drive	C <sub>L</sub>	No sustained oscillation	47	200		pF
Charge-Pump Oscillator Frequency	f <sub>OSC</sub>			500		kHz
Crosstalk		R <sub>L</sub> = 32 $\Omega$ , V <sub>IN</sub> = 200mV <sub>P-P</sub> , f = 10kHz, A <sub>V</sub> = 1		80		dB
Thermal Shutdown Threshold				145		°C
Thermal Shutdown Hysteresis				5		°C

**Note 1:** All specifications are 100% tested at T<sub>A</sub> = +25°C; temperature limits are guaranteed by design.

**Note 2:** Gain for the LPA4722A is adjustable.

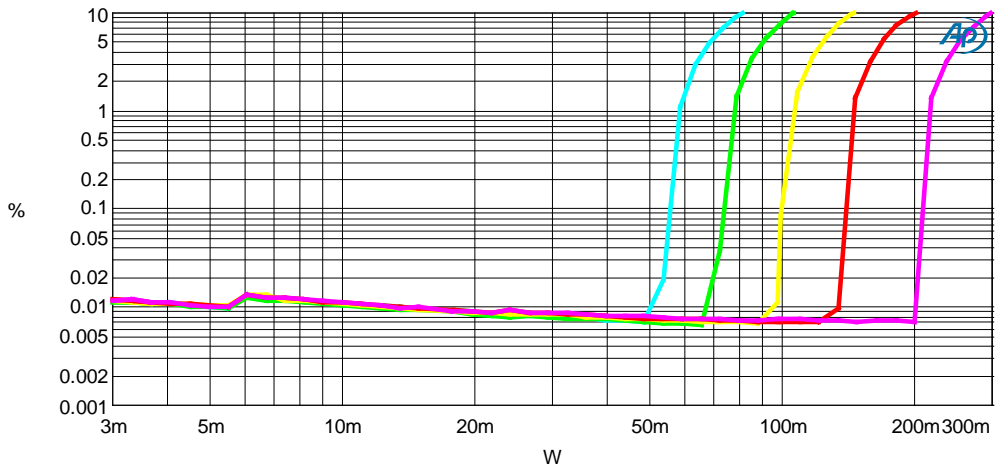
**Note 3:** The amplifier inputs are AC-coupled to ground through CIN<sub>-</sub>.

**Note 4:** Measurement bandwidth is 22Hz to 22kHz.



### Typical Operating Characteristic

Audio Precision

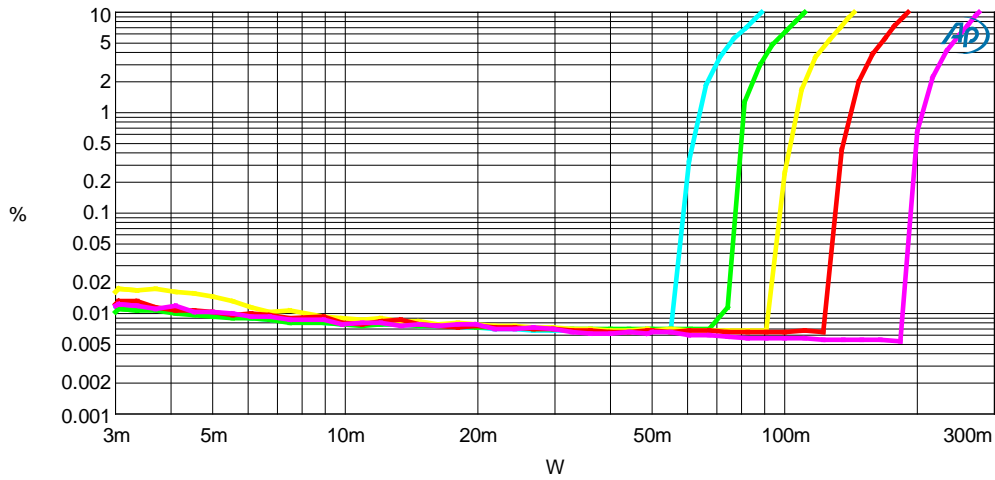


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.THD+N Ratio A	Left	3.0V,16ohm
2	1	Green	Solid	3	Analyzer.THD+N Ratio A	Left	3.3V,16ohm
3	1	Yellow	Solid	3	Analyzer.THD+N Ratio A	Left	3.7V,16ohm
4	1	Red	Solid	3	Analyzer.THD+N Ratio A	Left	4.2V,16ohm
5	1	Magenta	Solid	3	Analyzer.THD+N Ratio A	Left	5.0V,16ohm

Figure 4. THD+N VS Output Power, Freq=1kHz, RL=16Ω



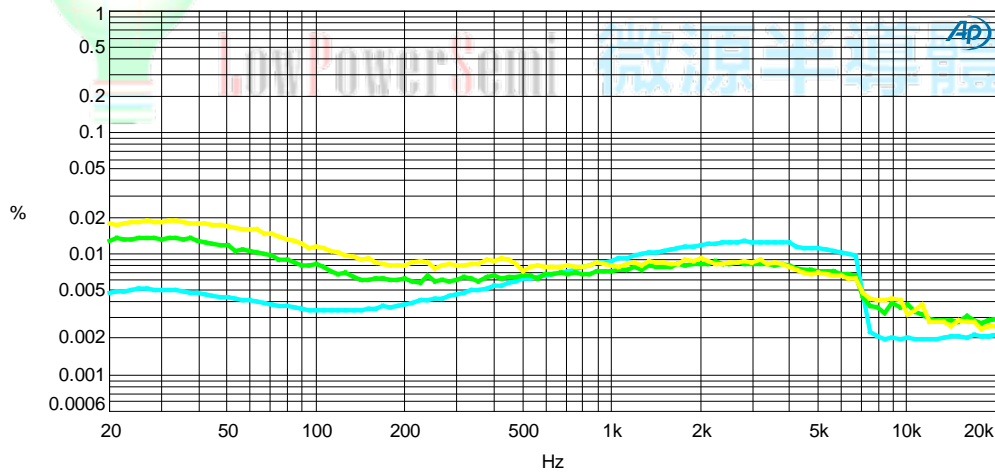
Audio Precision



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.TH+N Ratio A	Left	3.0V,32ohm
2	1	Green	Solid	3	Analyzer.TH+N Ratio A	Left	3.3V,32ohm
3	1	Yellow	Solid	3	Analyzer.TH+N Ratio A	Left	3.7V,32ohm
4	1	Red	Solid	3	Analyzer.TH+N Ratio A	Left	4.2V,32ohm
5	1	Magenta	Solid	3	Analyzer.TH+N Ratio A	Left	5.0V,32ohm

Figure 5. THD+N VS Output Power, Freq=1kHz, RL=32Ω

Audio Precision

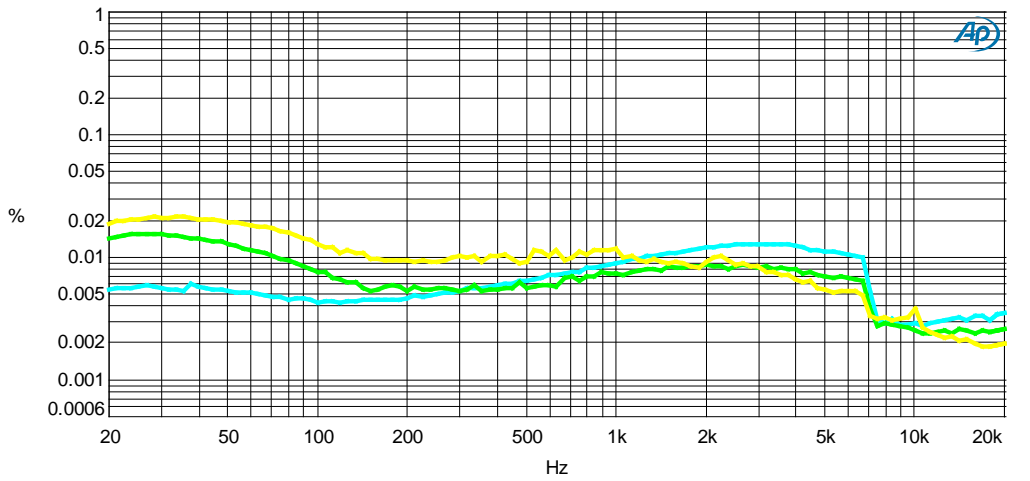


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.TH+N Ratio A	Left	PVDD=3V,RL=16ohm,PO=5mW
2	1	Green	Solid	3	Analyzer.TH+N Ratio A	Left	PVDD=3V,RL=16ohm,PO=20mW
3	1	Yellow	Solid	3	Analyzer.TH+N Ratio A	Left	PVDD=3V,RL=16ohm,PO=40mW

Figure 6. THD VS Frequency, PVDD=SVDD=3V, RL=16Ω



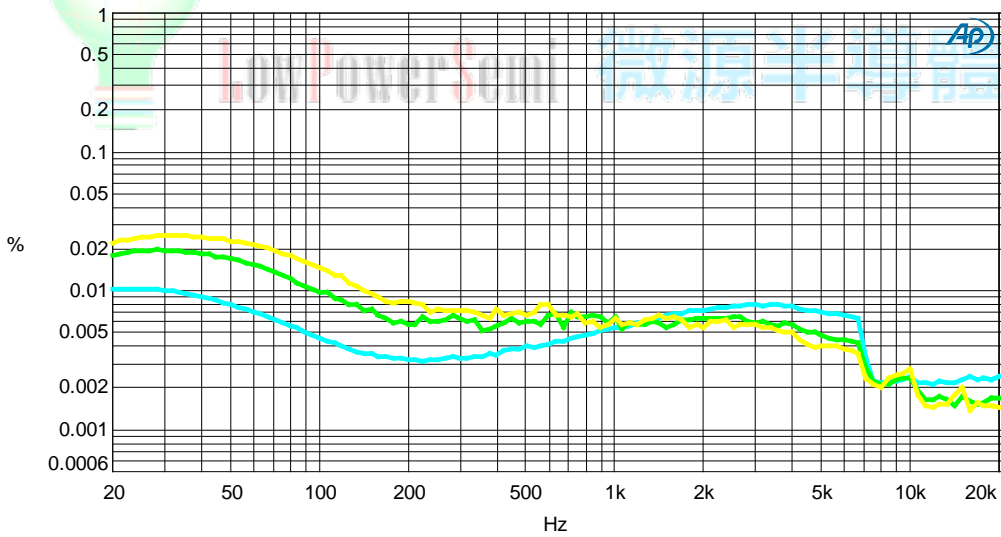
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Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.TH+N Ratio A	Left	PVDD=5V,RL=16ohm,PO=5mW
2	1	Green	Solid	3	Analyzer.TH+N Ratio A	Left	PVDD=5V,RL=16ohm,PO=20mW
3	1	Yellow	Solid	3	Analyzer.TH+N Ratio A	Left	PVDD=5V,RL=16ohm,PO=80mW

Figure 7. THD VS Frequency, PVDD=SVDD=5V, RL=16Ω

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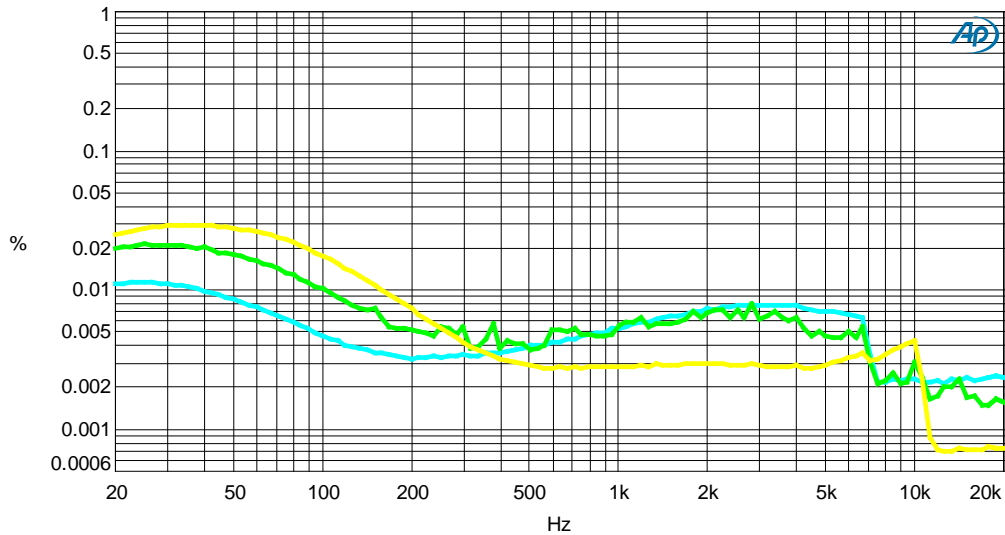
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.TH+N Ratio A	Left	3V,32ohm,5mW
2	1	Green	Solid	3	Analyzer.TH+N Ratio A	Left	3V,32ohm,20mW
3	1	Yellow	Solid	3	Analyzer.TH+N Ratio A	Left	3V,32ohm,40mW

Figure 8. THD VS Frequency, PVDD=SVDD=3V, RL=32Ω





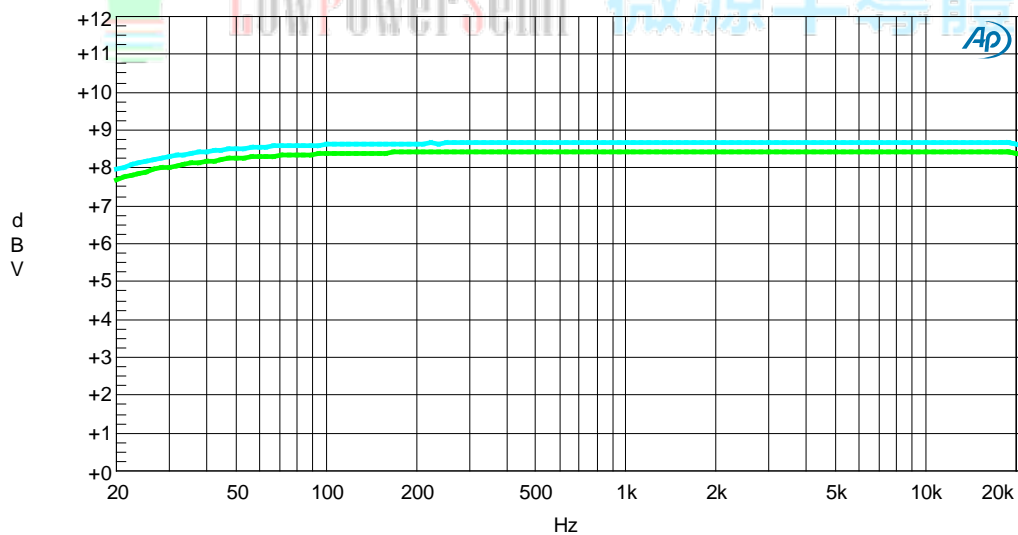
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Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.TH+N Ratio A	Left	5V,32ohm,5mW
2	1	Green	Solid	3	Analyzer.TH+N Ratio A	Left	5V,32ohm,20mW
3	1	Yellow	Solid	3	Analyzer.TH+N Ratio A	Left	5V,32ohm,80mW

Figure 9. THD VS Frequency, PVDD=SVDD=5V, RL=32Ω

Audio Precision



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	3	Analyzer.Level A	Left	PVDD=5V,RL=32ohm,THD=1%
2	1	Green	Solid	3	Analyzer.Level A	Left	PVDD=5V,RL=32ohm,THD=0.1%

Figure 10. Output Amplitude VS Frequency, PVDD=SVDD=5V, RL=32 Ω



## Application Information

The LPA4722A stereo headphone amplifiers feature Maxim’s patented DirectDrive architecture, eliminating the large output-coupling capacitors required by conventional single-supply headphone amplifiers. The devices consist of two class AB headphone amplifiers, undervoltage lockout (UVLO)/shutdown control, charge pump, and comprehensive click-and-pop suppression circuitry (see Typical Application Circuit). The charge pump inverts the positive supply (PVDD), creating a negative supply (PVSS). The headphone amplifiers operate from these bipolar supplies with their outputs biased about GND. The benefit of this GND bias is that the amplifier outputs do not have a DC component, typically  $VDD/2$ . The large DC-blocking capacitors required with conventional headphone amplifiers are unnecessary, thus conserving board space, reducing system cost, and improving frequency response. The device features an undervoltage lockout that prevents operation from an insufficient power supply and clickand-pop suppression that eliminates audible transients on startup and shutdown. Additionally, the LPA4722A feature thermal-overload and short-circuit protection and can withstand  $\pm 2kV$  ESD strikes at the output pins.

### Differential Input

The LPA4722A can be configured as a differential input amplifier(Figure 11), making it compatible with many CODECs. A differential input offers improved noise immunity over a single-ended input. In devices such as cellular phones, high-frequency signals from the RF transmitter can couple into the amplifier’s

input traces. The signals appear at the amplifier’s inputs as common-mode noise. A differential input amplifier amplifies the difference of the two inputs, and signals common to both inputs are cancelled. Configured differentially, the gain of the LPA4722A is set by:

$$A_V = R_{F1} / R_{IN1}$$

$R_{IN1}$  and  $R_{F1}$  must be equal to  $R_{IN2}$  and  $R_{F2}$ .

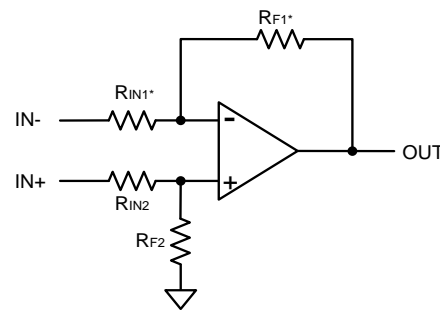


Figure 11. Differential Input Configuration

The common-mode rejection ratio (CMRR) is limited by the external resistor matching. For example, the worstcase variation of 1% tolerant resistors results in 40dB CMRR, while 0.1% resistors result in 60dB CMRR. For best matching, use resistor arrays.

### Shutdown

The LP4772 feature shutdown control allowing audio signals to be shut down or muted. Driving  $\overline{SHDN}$  low disables the amplifiers and the charge pump, sets the amplifier output impedance to  $10k\Omega$ , and reduces the supply current. In shutdown mode, the supply current is reduced to  $0.1\mu A$ . The charge pump is enabled once  $\overline{SHDN}$  is driven high.



## Low-Frequency Response

In addition to the cost and size disadvantages of the DC-blocking capacitors required by conventional head-phone amplifiers, these capacitors limit the amplifier's low-frequency response and can distort the audio signal:

1) The impedance of the headphone load and the DC-blocking capacitor form a highpass filter with the -3dB point set by:

$$f_{-3dB} = \frac{1}{2\pi R_L C_{OUT}}$$

where  $R_L$  is the impedance of the headphone and  $C_{OUT}$  is the value of the DC-blocking capacitor.

The highpass filter is required by conventional singleended, single power-supply headphone amplifiers to block the midrail DC-bias component of the audio signal from the headphones. The drawback to the filter is that it can attenuate low-frequency signals. Larger values of  $C_{OUT}$  reduce this effect but result in physically larger, more expensive capacitors.

2) The voltage coefficient of the DC-blocking capacitor contributes distortion to the reproduced audio signal as the capacitance value varies and the function of the voltage across the capacitor changes. The reactance of the capacitor dominates at frequencies below the -3dB point and the voltage coefficient appears as frequency-dependent distortion. The combination of low-frequency attenuation and frequency-dependent distortion compromises audio reproduction in portable audio equipment that emphasizes low-frequency effects such as in multimedia laptops, MP3, CD, and DVD

players. By eliminating the DC-blocking capacitors through DirectDrive technology, these capacitor-related deficiencies are eliminated.

## Charge Pump

The LPA4722A feature a low-noise charge pump. The 450kHz switching frequency is well beyond the audio range and, thus, does not interfere with the audio signals. Also, the 500kHz switching frequency does not interfere with the 450kHz AM transceivers. The switch drivers feature a controlled switching speed that minimizes noise generated by turn-on and turn-off transients. By limiting the switching speed of the charge pump, the di/dt noise caused by the parasitic bond wire and trace inductance is minimized. Although not typically required, additional high-frequency noise attenuation can be achieved by increasing the value of C2 (see Typical Application Circuit).

## Click-and-Pop Suppression

In conventional single-supply audio amplifiers, the output-coupling capacitor is a major contributor of audible clicks and pops. Upon startup, the amplifier charges the coupling capacitor to its bias voltage, typically half the supply. Likewise, on shutdown, the capacitor is discharged to GND. This results in a DC shift across the capacitor, which, in turn, appears as an audible transient at the speaker. Since the LPA4722A do not require output-coupling capacitors, this problem does not arise. Additionally, the LPA4722A feature extensive click-and-pop suppression that eliminates any audible transient sources internal to the device. The Power-Up/Down Waveform in the Typical Operating Characteristics



shows that there is minimal DC shift and no spurious transients at the output upon startup or shutdown. In most applications, the output of the preamplifier driving the LPA4722A has a DC bias of typically half the supply. At startup, the input-coupling capacitor is charged to the preamplifier's DC-bias voltage through the feedback resistor of the LPA4722A, resulting in a DC shift across the capacitor and an audible click/pop. Delaying the rise of  $\overline{\text{SHDN}}$  4 to 5 time constants (80ms to 100ms) based on  $R_{IN}$  and  $C_{IN}$ , relative to the startup of the preamplifier, eliminates this click/pop caused by the input filter.

### Power Dissipation

Under normal operating conditions, linear power amplifiers can dissipate a significant amount of power. The maximum power dissipation for each package is given in the Absolute Maximum Ratings section under Continuous Power Dissipation or can be calculated by the following equation:

where  $T_{J(MAX)}$  is  $+145^{\circ}\text{C}$ ,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the reciprocal of the derating factor in  $^{\circ}\text{C}/\text{W}$  as specified in the Absolute Maximum Ratings section. For example,  $\theta_{JA}$  of the thin QFN package is  $+63.8^{\circ}\text{C}/\text{W}$ , and  $99.3^{\circ}\text{C}/\text{W}$  for the TSSOP package. The LPA4722A have two power dissipation sources: the charge pump and two amplifiers. If power dissipation for a given application exceeds the maximum allowed for a particular package, either reduce  $\text{SVDD}$ , increase load impedance, decrease the ambient temperature, or add heatsinking to the device. Large output, supply, and ground traces improve the maximum power dissipation in the package. Thermal-overload protection limits total power dissipation in the LPA4722A. When the

junction temperature exceeds  $+145^{\circ}\text{C}$ , the thermal-protection circuitry disables the amplifier output stage. The amplifiers are enabled once the junction temperature cools by  $5^{\circ}\text{C}$ . This results in a pulsing output under continuous thermal-overload conditions.

### Output Power

The device has been specified for the worst-case scenario—when both inputs are in-phase. Under this condition, the amplifiers simultaneously draw current from the charge pump, leading to a slight loss in  $\text{PVSS}$  headroom. In typical stereo audio applications, the left and right signals have differences in both magnitude and phase, subsequently leading to an increase in the maximum attainable output power.

## Component Selection

### Input Filtering

The input capacitor ( $C_{IN}$ ), in conjunction with the input resistor ( $R_{IN}$ ), forms a highpass filter that removes the DC bias from an incoming signal (see the Typical Application Circuit). The AC-coupling capacitor allows the device to bias the signal to an optimum DC level. Assuming zero source impedance, the  $-3\text{dB}$  point of the highpass filter is given by:

$$f_{-3\text{dB}} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Choose  $C_{IN}$  so  $f_{-3\text{dB}}$  is well below the lowest frequency of interest. For the LPA4722A, use the value of  $R_{IN}$  as given in the DC Electrical Characteristics table. Setting  $f_{-3\text{dB}}$  too high affects the device's low-frequency response. Use capacitors whose dielectrics have low-voltage coefficients, such



as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, can result in increased distortion at low frequencies.

#### Charge-Pump Capacitor Selection

Use capacitors with an ESR less than  $100\text{m}\Omega$  for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. For best performance over the extended temperature range, select capacitors with an X7R dielectric. Table 1 lists suggested manufacturers.

#### Flying Capacitor (C1)

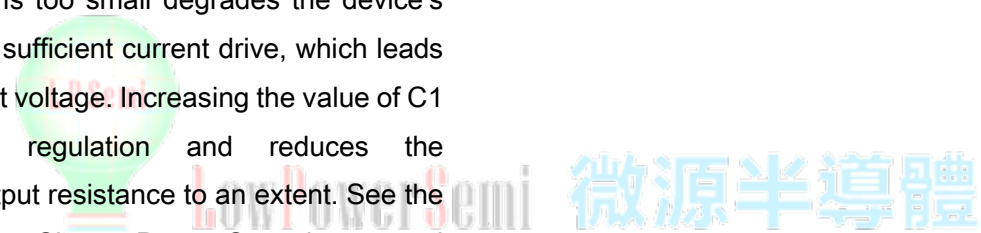
The value of the flying capacitor (C1) affects the charge pump's load regulation and output resistance. A C1 value that is too small degrades the device's ability to provide sufficient current drive, which leads to a loss of output voltage. Increasing the value of C1 improves load regulation and reduces the charge-pump output resistance to an extent. See the Output Power vs. Charge-Pump Capacitance and Load Resistance graph in the Typical Operating Characteristics. Above  $1\mu\text{F}$ , the on-resistance of the switches and the ESR of C1 and C2 dominate.

#### Hold Capacitor (C2)

The hold capacitor value and ESR directly affect the ripple at PVSS. Increasing the value of C2 reduces output ripple. Likewise, decreasing the ESR of C2 reduces both ripple and output resistance. Lower capacitance values can be used in systems with low maximum output power levels. See the Output Power vs. Charge-Pump Capacitance and Load Resistance graph in the Typical Operating Characteristics.

#### Power-Supply Bypass Capacitor

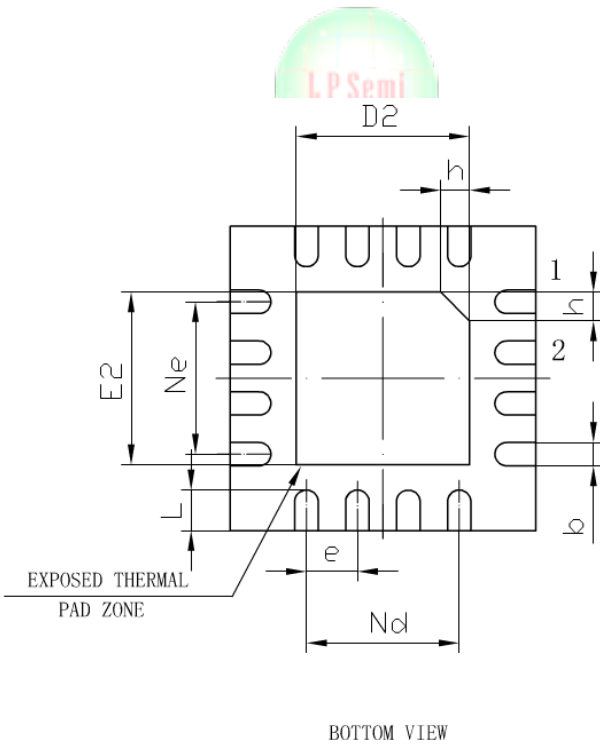
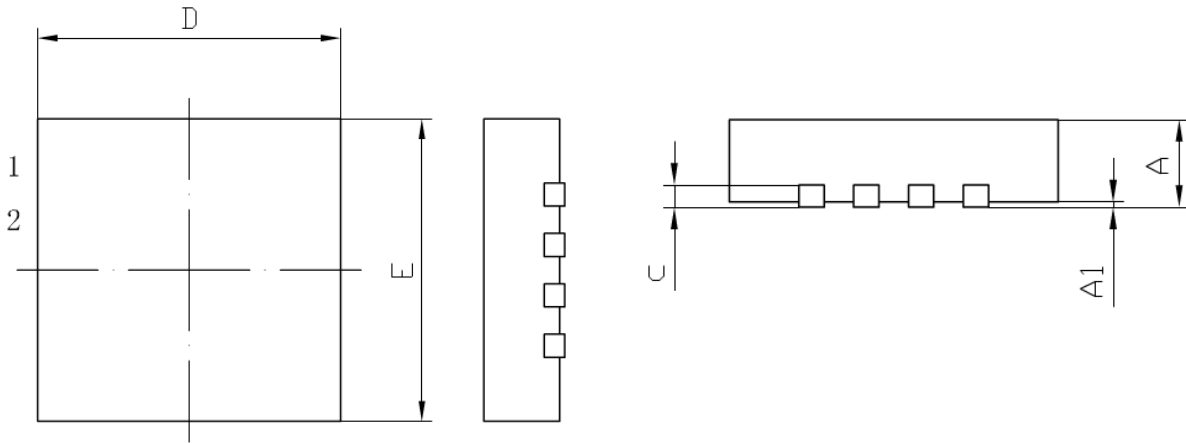
The power-supply bypass capacitor (C8 , C9) lowers the output impedance of the power supply and reduces the impact of the LPA4722A's charge-pump switching transients. Bypass PVDD with C8 and C9, the same value as C1, and place it physically close to the PVDD and PGND pins.





## Packaging Information

### TQFN-16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.50BSC		
Ne	1.50BSC		
Nd	1.50BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30

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