



3-Walts Mono Filter-free Audio Power Amplifier

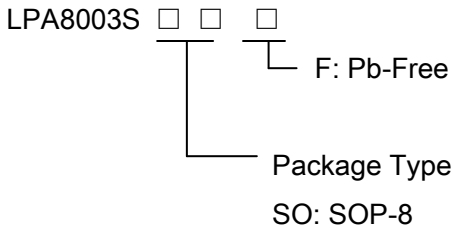
General Description

The LPA8003S is an audio power amplifier designed for portable communication device applications such as mobile phone applications. The LPA8003S is capable of delivering 3W of continuous average power to an 4Ω BTL and with less than 10% distortion (THD+N) from a 5.0V power supply. The LPA8003S provides high quality audio while requiring few external components and minimal power consumption. It features a low-power shutdown mode, which is achieved by driving the SHUTDOWN pin with logic low.

The LPA8003S contains circuitry to prevent from “pop and click” noise that would otherwise occur during turn-on and turn-off transitions. For maximum flexibility, the LPA8003S provides an externally controlled gain (with resistors), as well as an externally controlled turn-on and turn-off times (with the bypass capacitor).

The LPA8003S is available in SOP8 package.

Order Information



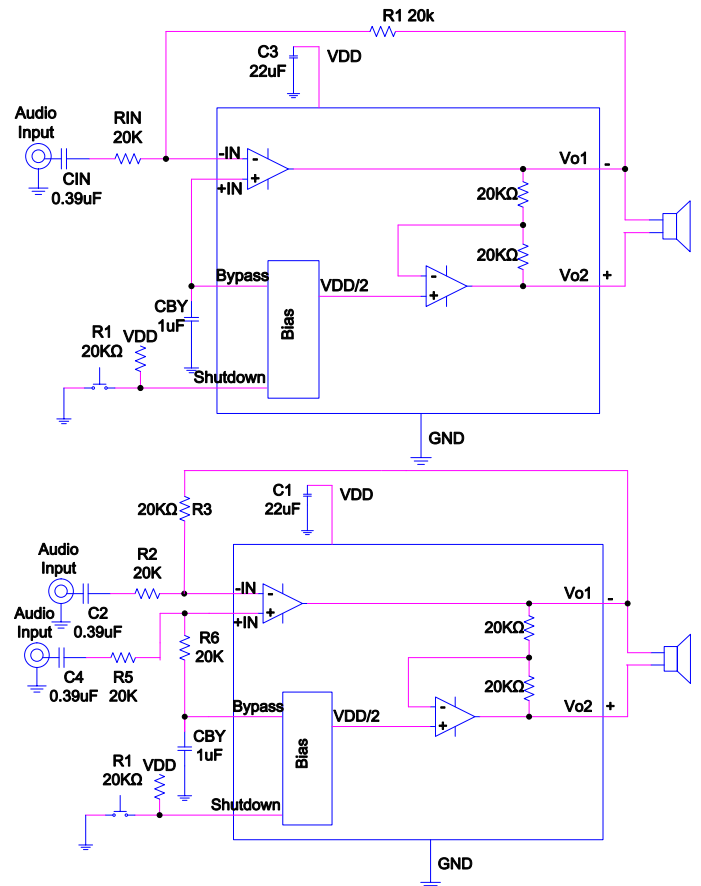
Applications

- ◇ PMP,PSP,Game,Data-Bank
- ◇ Cellular and Smart mobile phone

Features

- ◆ 2.5-5.5V operation
- ◆ 65dB PSRR at 217Hz, VDD=5V
- ◆ 0.1μA ultra low current shutdown mode
- ◆ Improved pop & click circuitry
- ◆ Unique Modulation Scheme Reduces EMI Emissions
- ◆ No output coupling capacitors, snubber networks or bootstrap capacitors required
- ◆ External gain configuration capability
- ◆ Shutdown Pin has 1.8V Compatible Thresholds
- ◆ BTL output can drive capacitive loads
- ◆ RoHS compliant and 100% lead(Pb)-free

Typical Application Circuit





Functional Pin Description

| Package Type | Pin Configurations |
|--------------|---|
| SOP-8 | <p>The diagram shows an SOP-8 package with pins numbered 1 to 8. Pin 1 is labeled SHUTDOWN, Pin 2 is BYPASS, Pin 3 is +IN, and Pin 4 is -IN. On the opposite side, Pin 5 is V_{O1}, Pin 6 is V_{DD}, Pin 7 is GND, and Pin 8 is V_{O2}.</p> |

Pin Description

| Pin No. | Pin Name | DESCRIPTION |
|---------|-----------------|---|
| 1 | SHUTDOWN | The device enters in shutdown mode when a high level is applied on this pin. |
| 2 | BYPASS | Bypass capacitor pin which provides the common mode voltage. |
| 3 | +IN | Positive input of the first amplifier, receives the common mode voltage. |
| 4 | -IN | Negative input of the first amplifier, receives the audio input signal. Connected to the feedback resistor R _f and to the input resistor R _{in} . |
| 5 | V _{O1} | Negative output of the LPA8003S. Connected to the load and to the feedback resistor R _f . |
| 6 | V _{DD} | Analog VDD input supply. |
| 7 | GND | Ground connection for circuitry. |
| 8 | V _{O2} | Positive output of the LPA8003S. |



Absolute Maximum Ratings

| | |
|---|--------------------------------|
| ◇ Input Voltage to GND (V_{INA}, V_{INB}) | -----6V |
| ◇ Adapter Voltage to GND (V_{ADP}) | ----- -0.3V to 6V |
| ◇ Supply Voltage, V_{DD} | ----- -0.3 V to 6V |
| ◇ Voltage at Any Input Pin | ----- -0.3 V to $V_{DD} + 0.3$ |
| ◇ Junction Temperature, T_{JMAX} | ----- 150°C |
| ◇ Storage Temperature Rang, T_{stg} | ----- -65°C to 150°C |
| ◇ ESD Susceptibility | ----- 2 kV |
| ◇ Lead temperature from case for 10 seconds | ----- 260°C |
| ◇ Thermal Resistance | ----- 57°C/W |

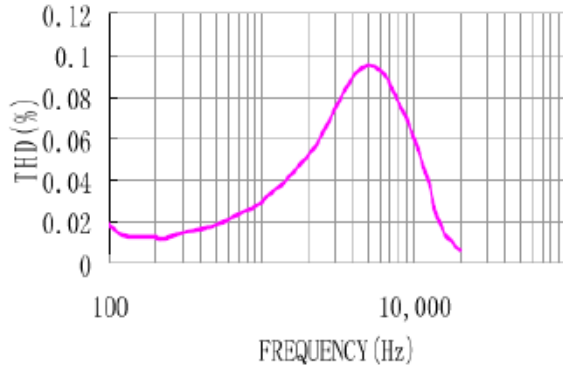
Electrical Characteristics

| Symbol | Parameter | Conditions | LPA8003S | | | Unit | |
|--------------|--|--|---------------------------------------|-------|------|------------|----|
| | | | Min. | Typ. | Max. | | |
| V_{OS} | Output offset voltage (measured differentially) | $V_i=0V, A_v=2V/V, V_{DD}=2.5V$ to 5.5V | | 5 | 25 | mV | |
| I_Q | Quiescent current | $V_{DD}=5.5V$, no load | | 5 | | mA | |
| | | $V_{DD}=3.6V$, no load | | 4 | | | |
| | | $V_{DD}=2.5V$, no load | | 3 | | | |
| I_{SHDN} | Shutdown Current | $V_{SHDN}=0.35V, V_{DD}=2.5V$ to 5.5V | 0.1 | 2.0 | | μA | |
| P_O | Output Power | $V_{DD}=5V, THD=1\%, F=1KHz, R_L=4\Omega$ | | 2.4 | | W | |
| | | $V_{DD}=5V, THD=1\%, F=1KHz, R_L=8\Omega$ | | 1.8 | | | |
| | | $V_{DD}=5V, THD=10\%, F=1KHz, R_L=4\Omega$ | | 3.0 | | | |
| | | $V_{DD}=5V, THD=10\%, F=1KHz, R_L=8\Omega$ | | 2.1 | | | |
| I_{LIM} | P-Channel Current Limit | | 1.2 | | | A | |
| $R_{DS(ON)}$ | Static drain-source on-state resistance | $V_{DD}=5.5V$, no load | | 400 | | m Ω | |
| | | $V_{DD}=3.6V$, no load | | 500 | | | |
| | | $V_{DD}=2.5V$, no load | | 700 | | | |
| THD+N | Total harmonic distortion plus noise | $V_{DD}=5V, P_o=1W, R_L=8\Omega, f=1KHz$ | | 0.123 | | % | |
| | | $V_{DD}=3.6V, P_o=0.5W, R_L=8\Omega, f=1KHz$ | | 0.130 | | | |
| | | $V_{DD}=2.5V, P_o=0.2W, R_L=8\Omega, f=1KHz$ | | 0.163 | | | |
| PSRR | Supply ripple rejection ratio | $V_{DD}=5V$, Inputs ac-grounded with $C_i=2\mu F$ | $F=217Hz,$ $V_{ripple}=200mV_{pp}$ | | -68 | | dB |
| CMRR | Common mode rejection ratio | $V_{DD}=3.6V,$ $V_{ic}=1V_{pp}$ | $F=217Hz$ | | -58 | | dB |
| Z_t | Start-up time from shutdown | $V_{DD}=3.6V$ | | 45 | | | mS |

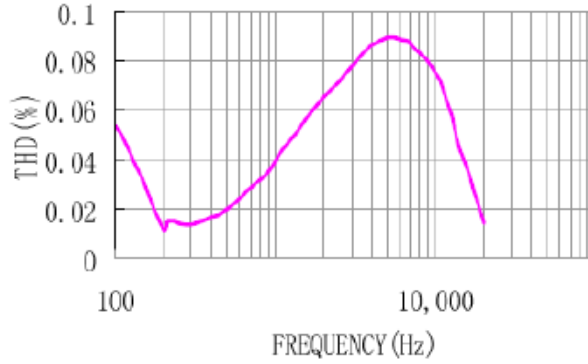


Typical Operating Characteristics

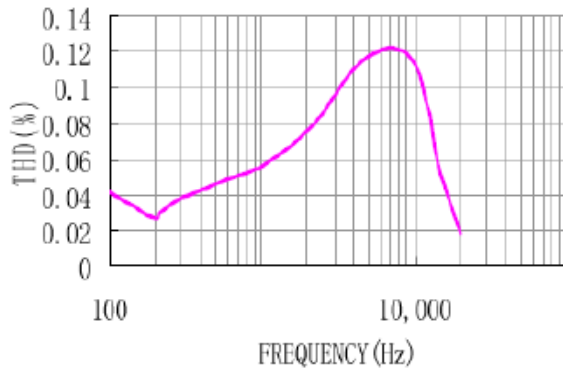
THD vs Frequency
T=25°C, Vdd=5V, RL=8Ω, and Po=500mW



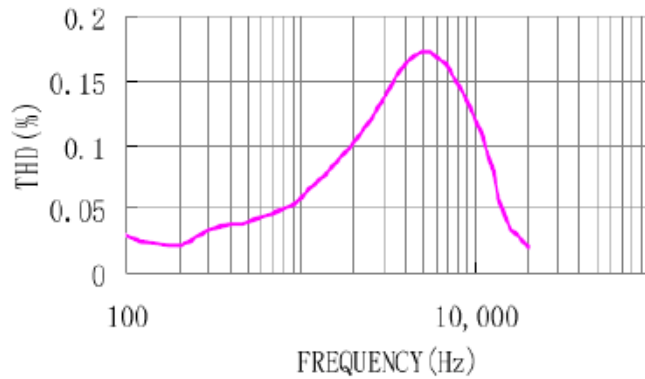
THD vs Frequency
T=25°C, Vdd=3.3V, RL=8Ω, and Po=425mW



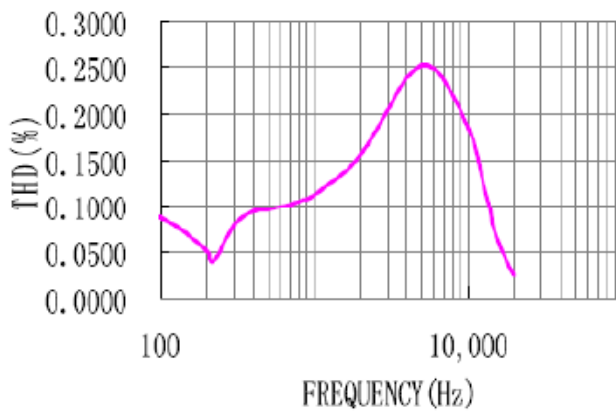
THD vs Frequency
T=25°C, Vdd=2.5V, RL=8Ω, and Po=150mW



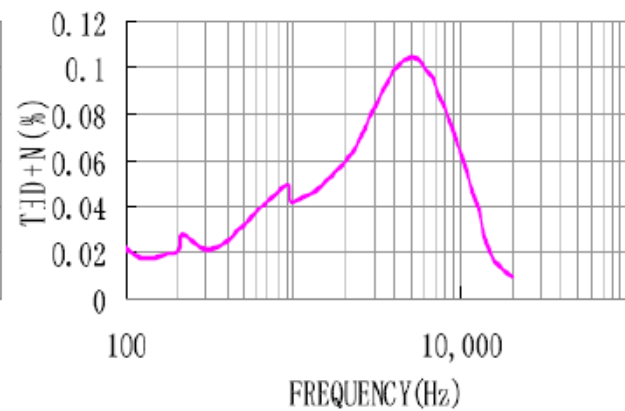
THD vs Frequency
T=25°C, Vdd=3.3V, RL=4Ω, and Po=425mW



THD vs Frequency
T=25°C, Vdd=2.5V, RL=4Ω, and Po=150mW



THD+N vs Frequency
T=25°C, Vdd=5V, RL=8Ω, and Po=500mW





Layout Considerations

As output power increases, interconnect resistance (PCB traces and wires) between the amplifier, load and power supply create a voltage drop. The voltage loss on the traces between the LPA8003S and the load results in lower output power and decreased efficiency. Higher trace resistance between the supply and the LPA8003S has the same effect as a poorly regulated supply, increase ripple on the supply line also reducing the peak output power. The effects of residual trace resistance increases as output current increases due to higher output power, decreased load impedance or both. To maintain the highest output voltage swing and corresponding peak output power, the PCB traces that connect the output pins to the load and the supply pins to the power supply should be as wide as possible to minimize trace resistance.

The use of power and ground planes will give the best THD+N performance. While reducing trace resistance, the use of power planes also creates parasitic capacitors that help to filter the power supply line.

The inductive nature of the transducer load can also result in overshoot on one or both edges, clamped by the parasitic diodes to GND and V_{DD} in each case. From an EMI stand- point, this is an aggressive waveform that can radiate or conduct to other components in the system and cause interference. It is essential to keep the power and output traces short and well shielded if possible. Use of ground planes, beads, and micro-strip layout techniques are all useful in preventing unwanted interference.

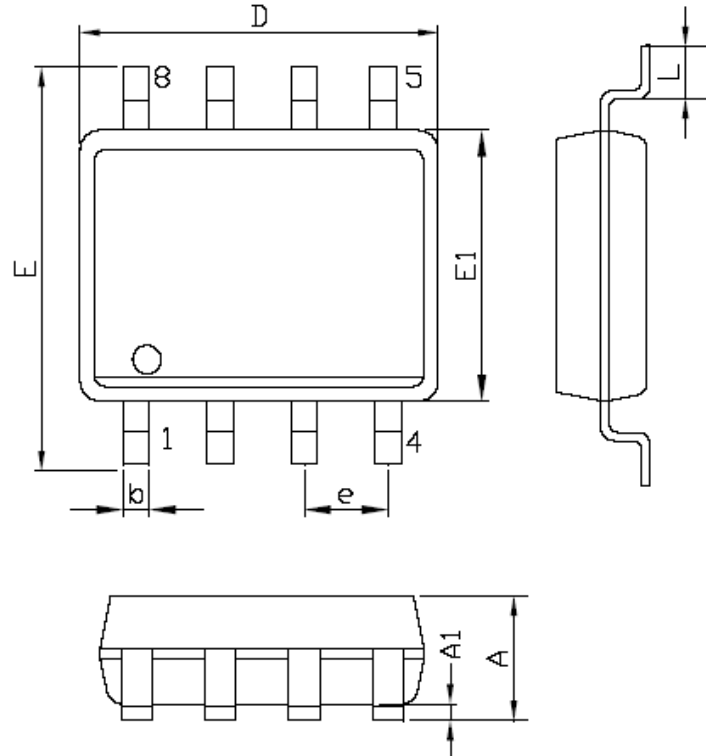
As the distance from the LPA8003S and the speaker increase, the amount of EMI radiation will increase since the output wires or traces acting as antenna become more efficient with length. What is acceptable EMI is highly application specific.

Ferrite chip inductors placed close to the LPA8003S may be needed to reduce EMI radiation. The value of the ferrite chip is very application specific.

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Packaging Information



| SYMBOLS | MILLIMETERS | | INCHES | |
|---------|-------------|------|--------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| D | 4.90 | | 0.193 | |
| E | 5.80 | 6.20 | 0.228 | 0.244 |
| E1 | 3.90 | | 0.153 | |
| L | 0.40 | 1.27 | 0.016 | 0.050 |
| b | 0.31 | 0.51 | 0.012 | 0.020 |
| e | 1.27 | | 0.050 | |

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