Dual P -Channel Enhancement Power MOSFET

General Description

The LPM4953 integrates two P-Channel enhancement MOSFET Transistor. It uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for using in DC-DC conversion, power switch and charging circuit. Standard Product LPM4953 is Pb-free and Halogen-free.

Features

- Trench Technology
- PMOS: V_{DS}=-15V
  $R_{DS(ON)}$ < 65mΩ, I_D=3.6A @ V_{GS}=-4.5V
  $R_{DS(ON)}$ < 42mΩ, I_D=5A @ V_{GS}=-10V
- Super high density cell design
- Extremely Low Threshold Voltage
- Small package SOP-8

Order Information

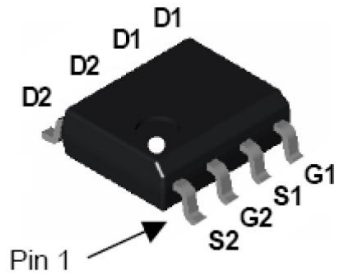
LPM4593 □ □ □
- F: Pb-Free
- Package Type
  SO: SOP-8

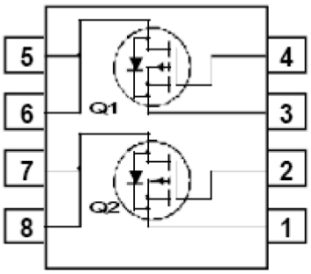
Applications

- Driver for Relay, Solenoid, Motor, LED etc.
- DC-DC converter circuit
- Power Switch
- Load Switch
- Charging

Pin Configurations

SO-8





Marking Information

Device	Marking	Package	Shipping
LPM4953		SOP-8	3K/REEL

Pin Description

Pin Number	Pin Description
1	Source Of PMOS2
2	Gate Of PMOS2
3	Source Of PMOS1
4	Gate Of PMOS1
5,6	Drain Of PMOS1
7,8	Drain Of PMOS2

Absolute Maximum Ratings

Parameter		Symbol	LPM4953	Unit
Drain-Source Voltage		V_{DS}	-15	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain Current	TA=25°C		-5.3	A
Maximum Power Dissipation	TA=25°C		2	W
Operating Junction Temperature		T_J	-40 to 150	°C
Lead Temperature		T_L	260	°C
Storage Temperature Range		T_{stg}	-55 to 150	°C

Thermal resistance ratings

Parameter		Symbol	LPM4953	Unit
Maximum Junction-to-Ambient	Steady State	$R_{\theta JC}$	50	℃/W

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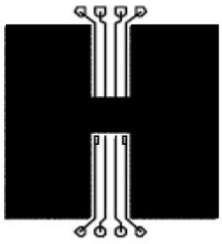
Electrical Characteristics

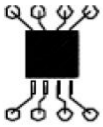
Parameter	Symbol	Test Condition	Min	Typ.	Max	Units
OFF CHARACTERISTICS						
Source-to-Drain Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D =-250uA		-15		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =0V, V_{GS} = 15V			100	nA
Gate-to-source Leakage Current	I_{GSS}	V_{DS} =0V, V_{GS} =-12V			-100	nA
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D=-250uA	-1	-1.7	-3	V
Drain-to-source On-resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D=-5.3A		42	50	mΩ
		V_{GS} = -4.5V, I_D=-4A		65	80	
Forward Transconductance	g_{FS}	V_{DS} =-5V, I_D=-5.3A	10			S
CAPACITANCES, CHARGES						
Input Capacitance	C_{ISS}	V_{GS} = 0V, f =1.0MHz V_{DS} =-15V		528		pF
Output Capacitance	C_{OSS}			132		
Reverse Transfer Capacitance	C_{RSS}			70		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} =-10V, V_{DS} =-15V, I_D =-4A		10	14	nC
Gate-to-Source Charge	Q_{GS}			2.2		
Gate-to-Drain Charge	Q_{GD}			2		
SWITCHING CHARACTERISTICS (Note 2)						
Turn-On Delay Time	$t_{d(ON)}$	V_{GS} =-10V, V_{DD} =-15V, I_D=-1.0A, R_G=6Ω		7	14	ns
Rise Time	t_r			13	24	
Turn-Off Delay Time	$t_{d(OFF)}$			14	25	
Fall Time	t_f			9	17	
Total gate charge	Qg	V_{GS} =-10V, V_{DD} =-15V, I_D=-4.0A		10	14	nC
Gate-Source charge	Qgs			2.2		
Gate-Drain charge	Qgd			2		
BODY DIODE CHARACTERISTICS						
Forward Voltage(Note 2)	V_{SD}	V_{GS} = 0 V, I_S =-2.1A		-0.8	-1.2	V

Notes:

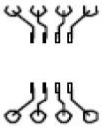
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1in² pad of 2 oz copper



b) 105°C/W when mounted on a .04 in² pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

Typical Characteristics

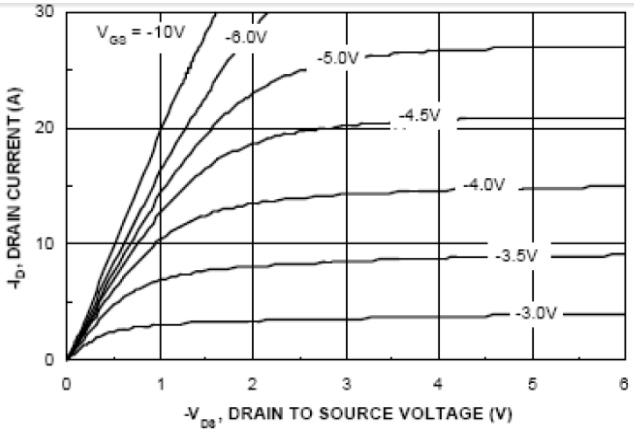


Figure 1. On-Region Characteristics.

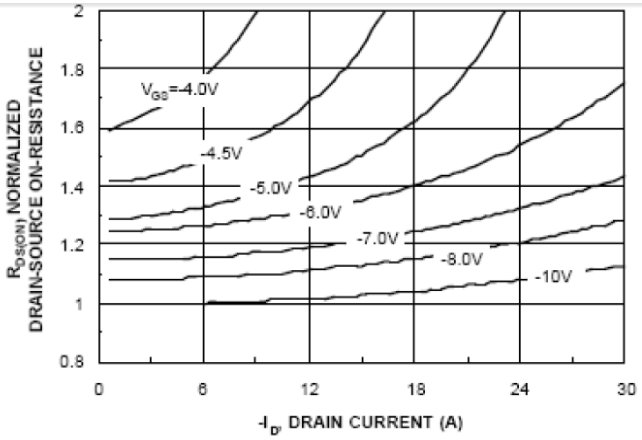


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

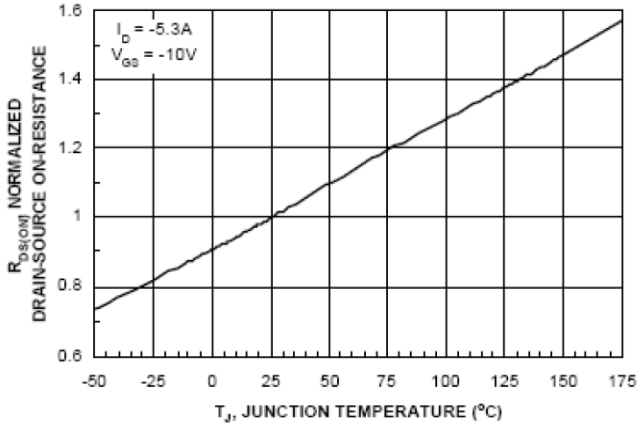


Figure 3. On-Resistance Variation with Temperature.

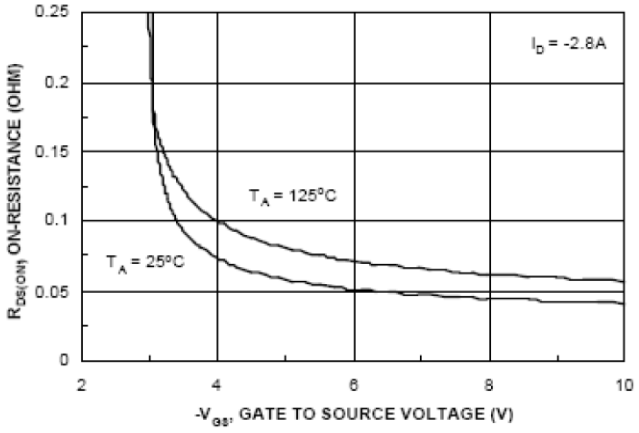


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

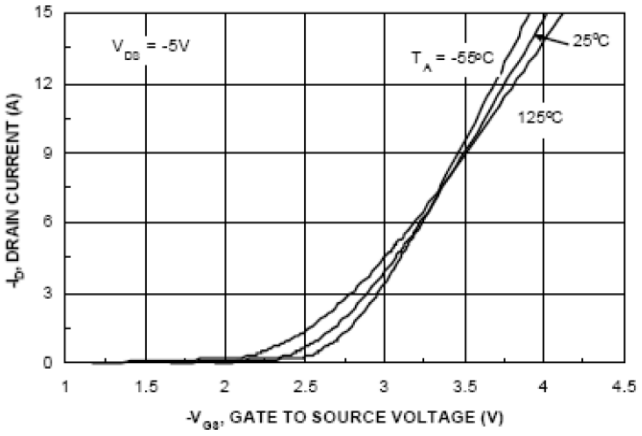


Figure 5. Transfer Characteristics.

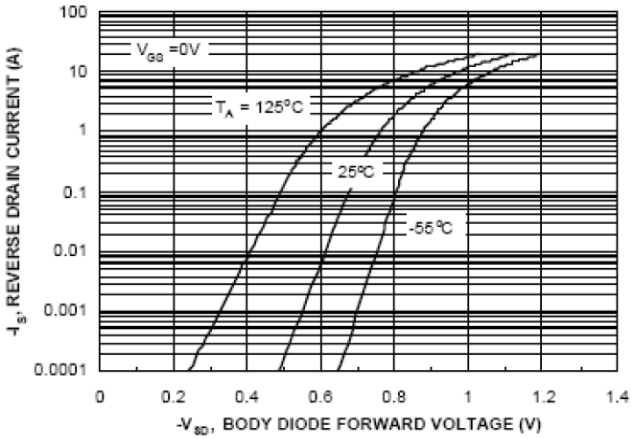


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

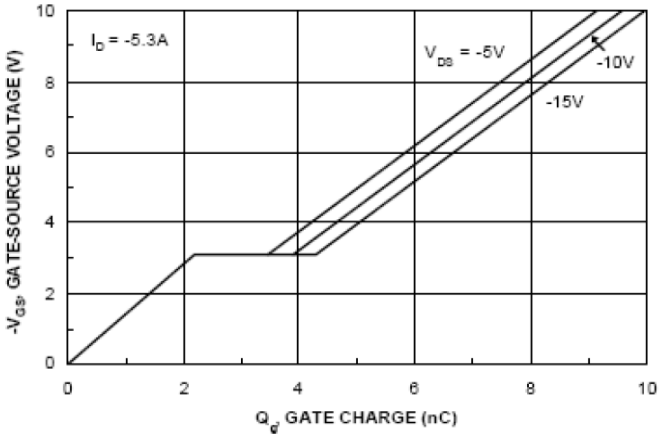
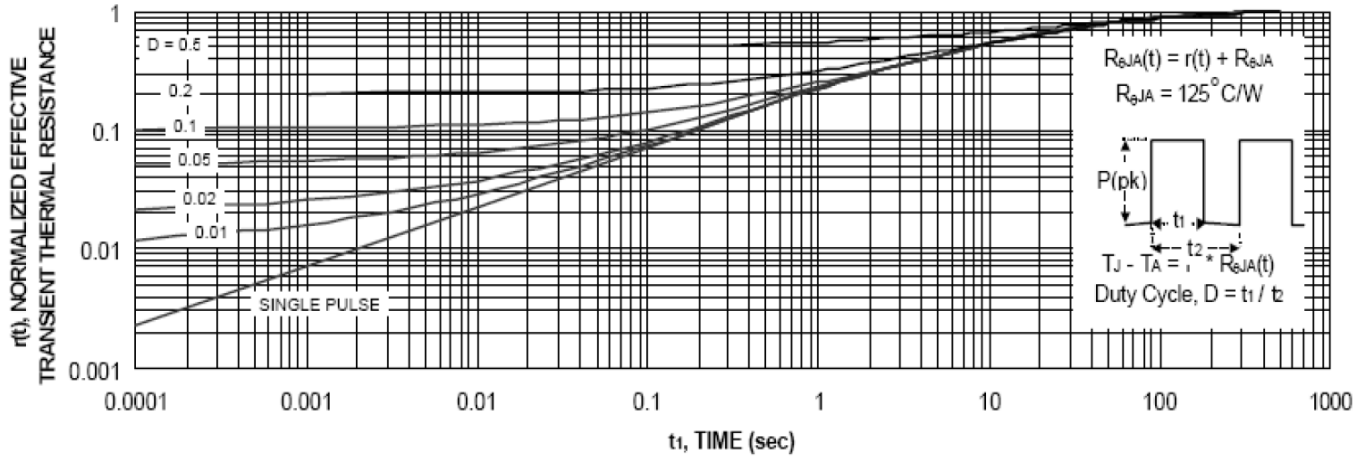


Figure 7. Gate Charge Characteristics.

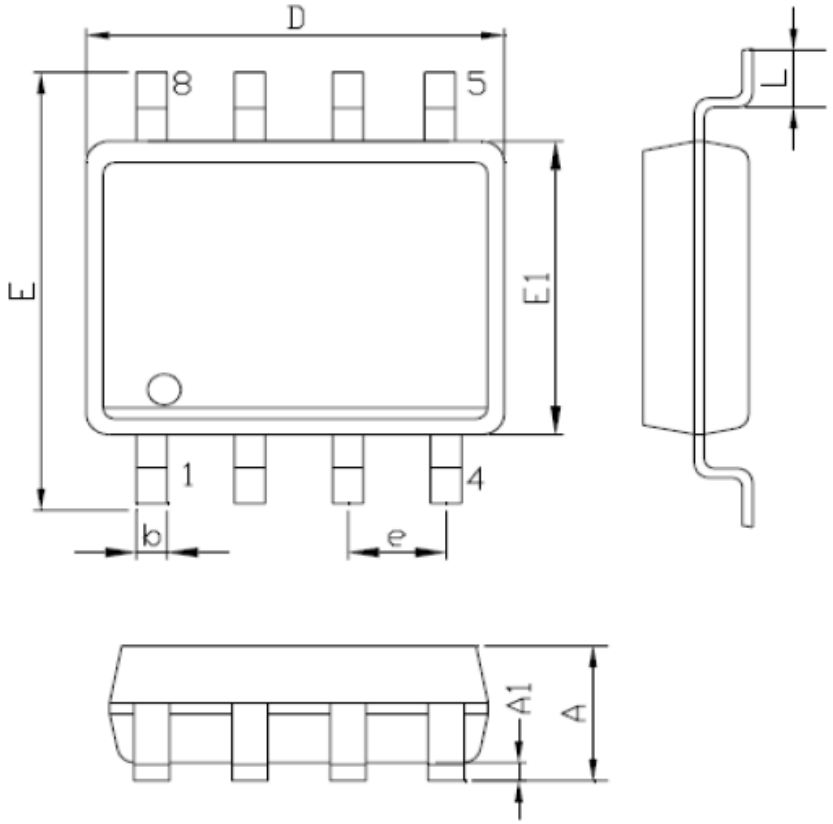


Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

Packaging Information

SOP-8



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.90		0.193	
E	5.80	6.20	0.228	0.244
E1	3.90		0.153	
L	0.40	1.27	0.016	0.050
b	0.31	0.51	0.012	0.020
e	1.27		0.050	

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