



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Jul.12.2012
Rev. 1.1	Revised TEST CONDITION of Average Operating Power Supply Current(I _{CC1}) on page 3, "CE# ≥ V _{CC} - 0.2V" revised as "CE# ≤ 0.2V"	Jul.19.2012
Rev. 1.2	Add " Green package available " on page 1	Nov.02.2012
Rev. 1.3	1.Revised TEST CONDITION of V _{OH} , V _{OL} on page 4 I _{OH} = -8mA revised as -4mA I _{OL} =4mA revised as 8mA 2. Revised V _{IH(max)} & V _{IL(min)} Notes on page 4 V _{IH(max)} = V _{CC} + 2.0V for pulse width less than 6ns. V _{IL(min)} = V _{SS} - 2.0V for pulse width less than 6ns.	Jun.04.2013
Rev. 1.4	Revised the address pin sequence of TSOP-II pin configuration on page 2 to be compatible with industrial convention. (No function specifications and applications changed and all characteristics kept same as Rev 1.3)	Oct.30.2013
Rev. 1.5	Deleted Commercial Grade Added PKG type : 36-ball 6mm x 8mm TFBGA Deleted WRITE CYCLE Notes : 1.WE#,CE# must be high during all address transitions. In page 6.	Jun.22.2016

FEATURES

- Fast access time : 8/10/12ns
- **Low power consumption:**
 Operating current:
 50/40/35mA(TYP.)
 Standby current:
 2mA(TYP.)
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- **Green package available**
- Data retention voltage : 1.5V (MIN.)
- Package : 44-pin 400 mil TSOP-II
 36-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

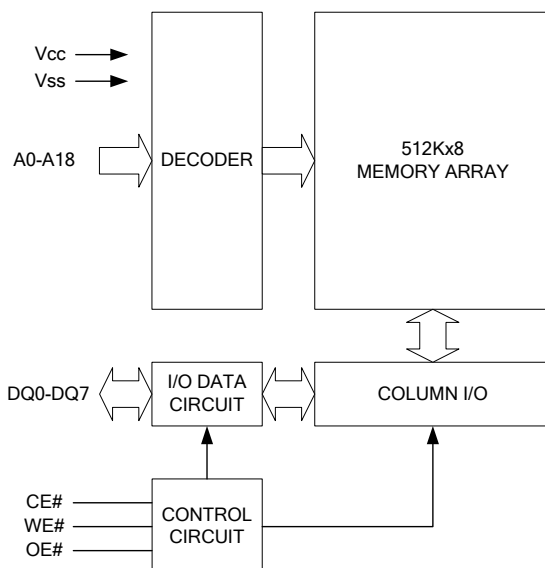
The LY61L5128A is a 4,194,304-bit high speed CMOS static random access memory organized as 524,288 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The LY61L5128A operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	V _{CC} Range	Speed	Power Dissipation	
				Standby(I _{SB1} , TYP.)	Operating(I _{CC1} , TYP.)
LY61L5128A(I)	-40 ~ 85°C	2.7 ~ 3.6V	10/12ns	2mA	40/35mA
		3.0 ~ 3.6V	8ns	2mA	50mA

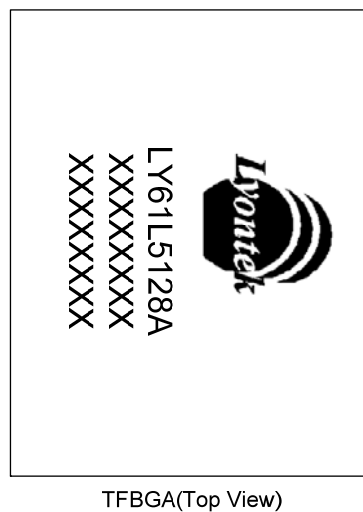
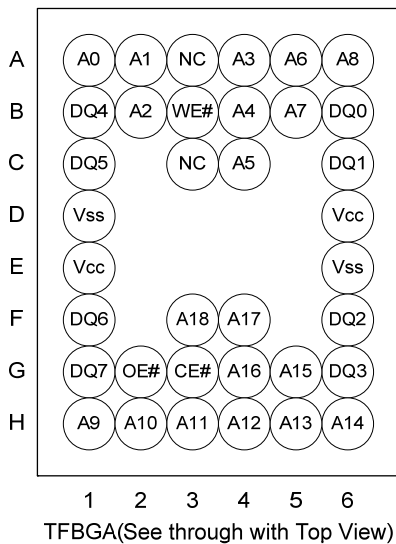
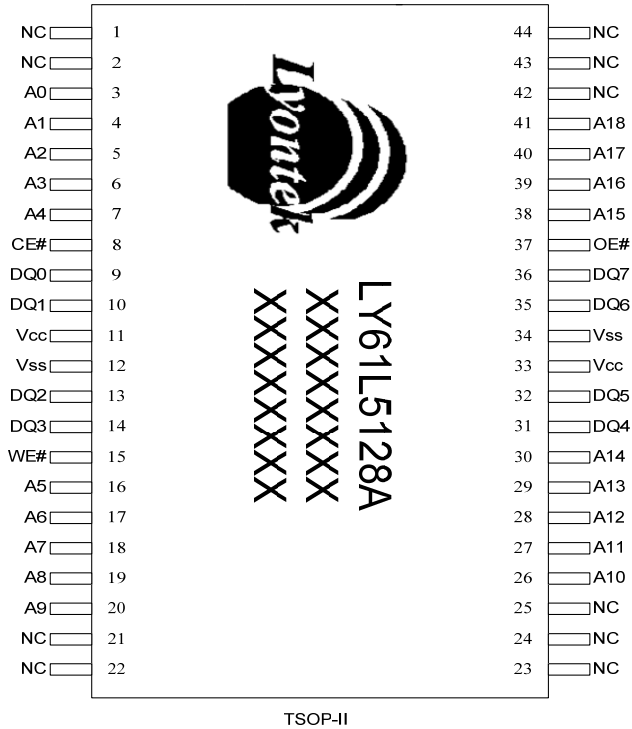
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
DQ0 - D7	Data Inputs/Outputs
CE#	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
V _{CC}	Power Supply
V _{SS}	Ground
NC	No Connection

PIN CONFIGURATION





ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V _{CC} relative to V _{SS}	V _{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V _{SS}	V _{T2}	-0.5 to V _{CC} +0.5	V
Operating Temperature	T _A	-40 to 85(I grade)	°C
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I _{SB} , I _{SB1}
Output Disable	L	H	H	High-Z	I _{CC} , I _{CC1}
Read	L	L	H	D _{OUT}	I _{CC} , I _{CC1}
Write	L	X	L	D _{IN}	I _{CC} , I _{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ⁴	MAX.	UNIT	
Supply Voltage	V _{CC}		-8	3.0	3.3	3.6	V
			-10/-12	2.7	3.3	3.6	V
Input High Voltage	V _{IH} ¹		2.2	-	V _{CC} +0.3	V	
Input Low Voltage	V _{IL} ²		-0.3	-	0.8	V	
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	-1	-	1	μA	
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	-1	-	1	μA	
Output High Voltage	V _{OH}	I _{OH} = -4mA	2.4	-	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 8mA	-	-	0.4	V	
Average Operating Power Supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} , I _{I/O} = 0mA, Others at V _{IL} or V _{IH}	-8	-	65	80	mA
			-10	-	50	70	mA
			-12	-	45	60	mA
	I _{CC1}	CE# ≤ 0.2, Others at 0.2V or V _{CC} -0.2V I _{I/O} = 0mA; f = max	-8	-	50	60	mA
			-10	-	40	55	mA
			-12	-	35	50	mA
Standby Power Supply Current	I _{SB}	CE# = V _{IH} , Others at V _{IL} or V _{IH}	-	-	30	mA	
	I _{SB1}	CE# ≥ V _{CC} - 0.2V, Others at 0.2V or V _{CC} - 0.2V	-	2	10	mA	

Notes:

- V_{IH(max)} = V_{CC} + 2.0V for pulse width less than 6ns.
- V_{IL(min)} = V_{SS} - 2.0V for pulse width less than 6ns.
- Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC(TYP.)} and T_A = 25°C

**CAPACITANCE** ($T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Speed	8/10/12ns
Input Pulse Levels	0.2V to $V_{CC} - 0.2\text{V}$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30\text{pF} + 1\text{TTL}$, $I_{OH}/I_{OL} = -4\text{mA}/8\text{mA}$

AC ELECTRICAL CHARACTERISTICS**(1) READ CYCLE**

PARAMETER	SYM.	LY61L5128A-8		LY61L5128A-10		LY61L5128A-12		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	8	-	10	-	12	-	ns
Address Access Time	t_{AA}	-	8	-	10	-	12	ns
Chip Enable Access Time	t_{ACE}	-	8	-	10	-	12	ns
Output Enable Access Time	t_{OE}	-	4.5	-	4.5	-	5	ns
Chip Enable to Output in Low-Z	t_{CLZ}^*	2	-	2	-	3	-	ns
Output Enable to Output in Low-Z	t_{OLZ}^*	0	-	0	-	0	-	ns
Chip Disable to Output in High-Z	t_{CHZ}^*	-	3	-	4	-	5	ns
Output Disable to Output in High-Z	t_{OHZ}^*	-	3	-	4	-	5	ns
Output Hold from Address Change	t_{OH}	2	-	2	-	2	-	ns

(2) WRITE CYCLE

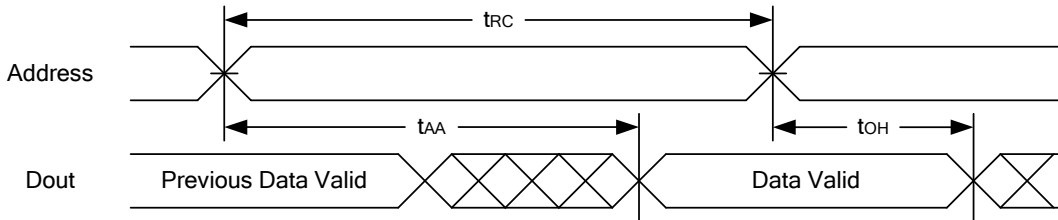
PARAMETER	SYM.	LY61L5128A-8		LY61L5128A-10		LY61L5128A-12		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	8	-	10	-	12	-	ns
Address Valid to End of Write	t_{AW}	6.5	-	8	-	10	-	ns
Chip Enable to End of Write	t_{CW}	6.5	-	8	-	10	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	6.5	-	8	-	10	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	5	-	6	-	7	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}^*	2	-	2	-	2	-	ns
Write to Output in High-Z	t_{WHZ}^*	-	3	-	4	-	5	ns

*These parameters are guaranteed by device characterization, but not production tested.

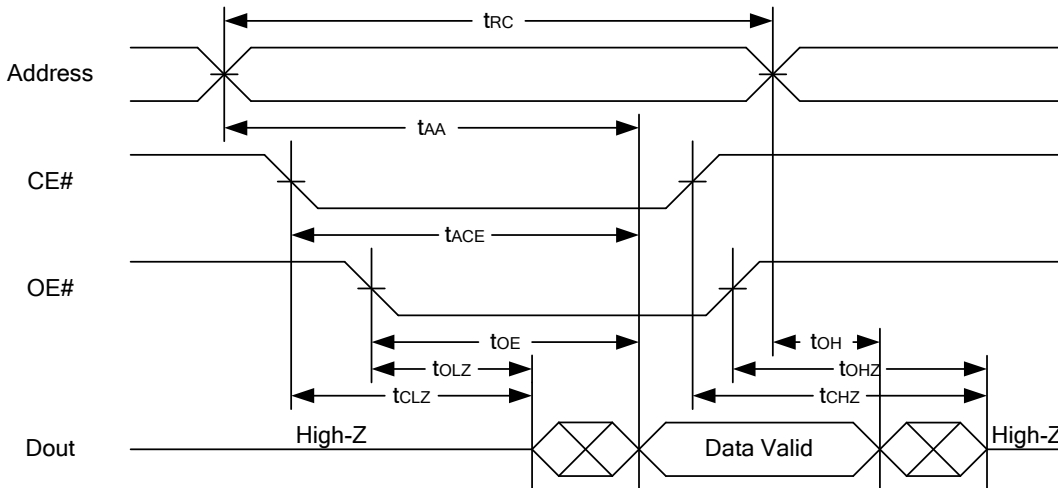


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)

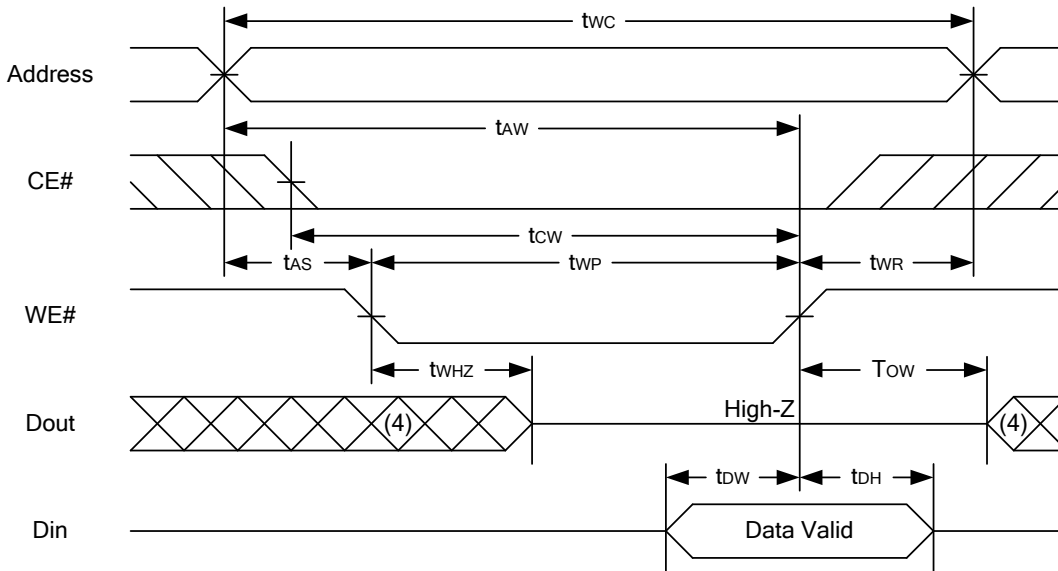


Notes :

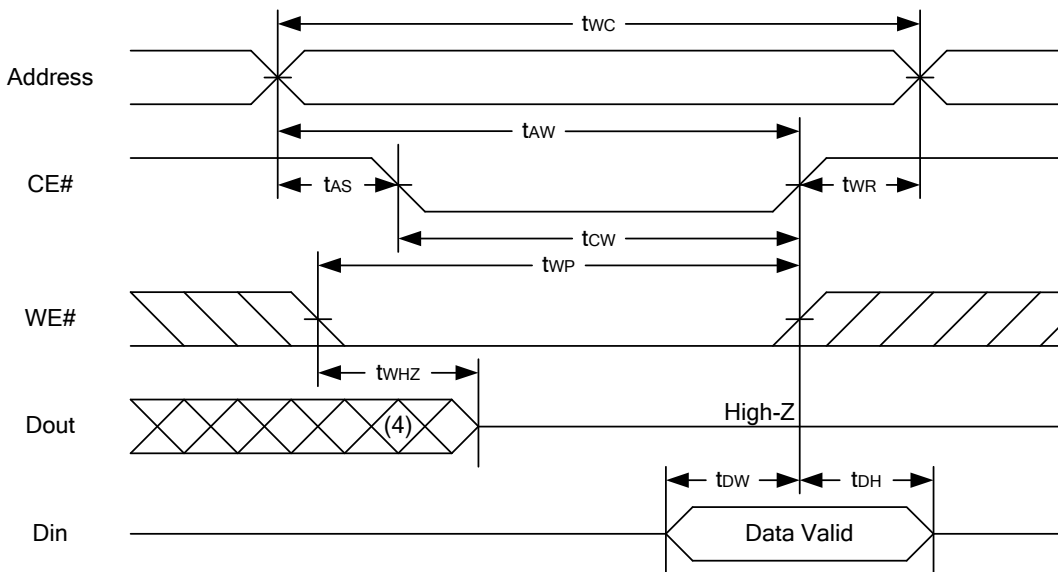
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low.; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{TOLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



WRITE CYCLE 2 (CE# Controlled) (1,4,5)



Notes :

1. A write occurs during the overlap of a low CE#, low WE#.
2. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. t_{ow} and t_{whz} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.

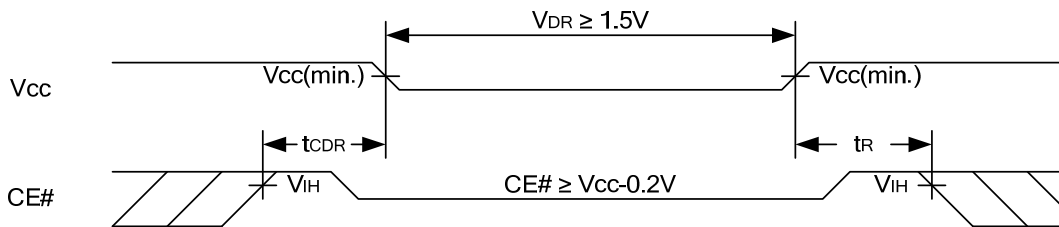


DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VCC for Data Retention	V_{DR}	$CE\# \geq V_{CC} - 0.2V$	1.5	-	3.6	V
Data Retention Current	I_{DR}	$V_{CC} = 1.5V$ $CE\# \geq V_{CC} - 0.2V$ Others at 0.2V or $V_{CC} - 0.2V$	-	2	10	mA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t_R		t_{RC}^*	-	-	ns

t_{RC}^* = Read Cycle Time

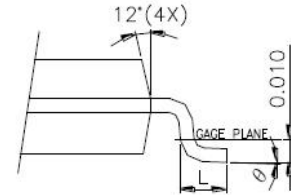
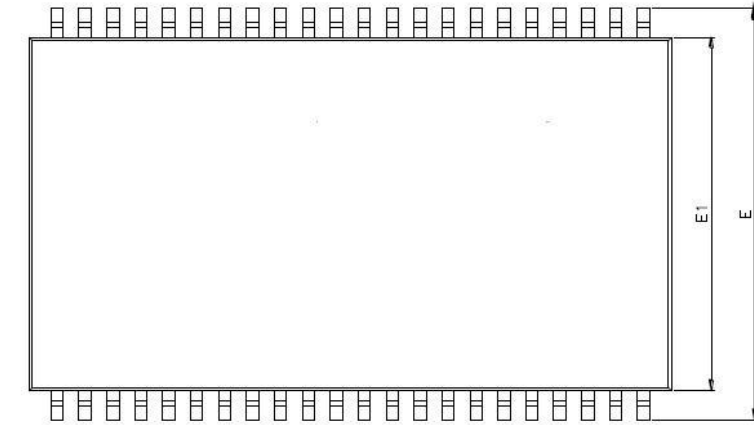
DATA RETENTION WAVEFORM



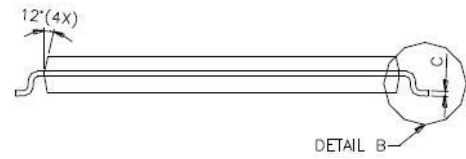
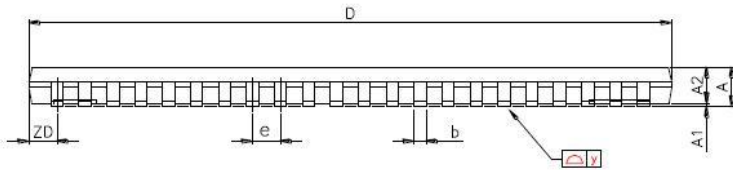


PACKAGE OUTLINE DIMENSION

44-pin 400mil TSOP-II Package Outline Dimension



DETAIL B

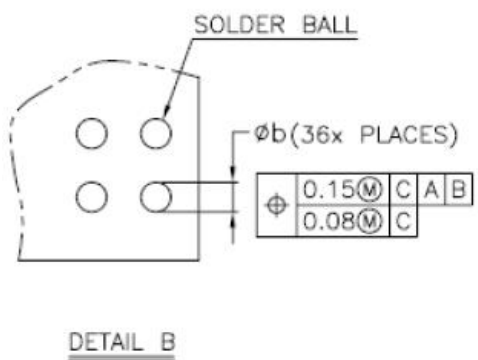
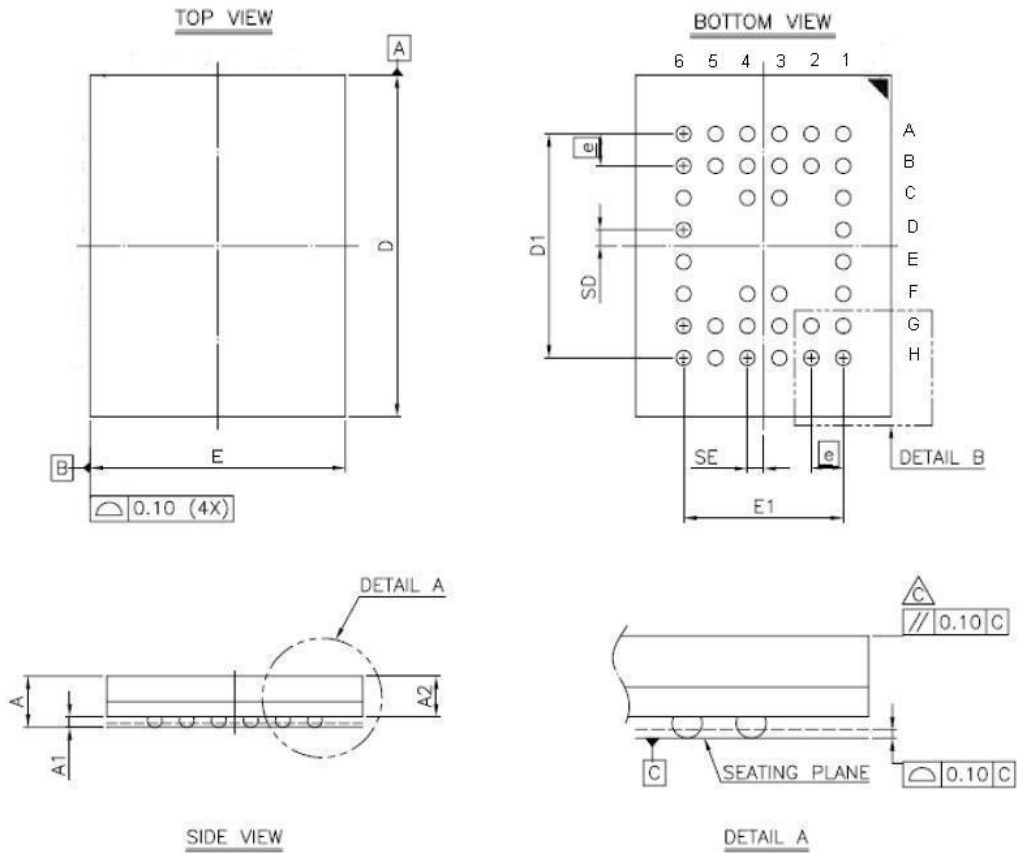


DETAIL B

SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°



36 ball 6mm × 8mm TFBGA Package Outline Dimension



SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	—	—	0.94	—	—	0.037
b	0.30	0.35	0.40	0.012	0.014	0.016
D	7.95	8.00	8.05	0.313	0.315	0.317
D1	5.25 BSC			0.207 BSC		
E	5.95	6.00	6.05	0.234	0.236	0.238
E1	3.75 BSC			0.148 BSC		
SE	0.375 TYP			0.015 TYP		
SD	0.375 TYP			0.015 TYP		
e	0.75 BSC			0.030 BSC		

NOTE:
 1. CONTROLLING DIMENSION : MILLIMETER.
 2. REFERENCE DOCUMENT : JEDEC MO-207.



ORDERING INFORMATION

Package Type	Access Time (Speed/ns)	Temperature Range(°C)	Packing Type	Lyontek Item No.
44Pin 400mil TSOP-II	8	-40°C~85°C	Tray	LY61L5128AML-8I
			Tape Reel	LY61L5128AML-8IT
	10	-40°C~85°C	Tray	LY61L5128AML-10I
			Tape Reel	LY61L5128AML-10IT
36Ball 6mm x 8mm TFBGA	8	-40°C~85°C	Tray	LY61L5128AGL-8I
			Tape Reel	LY61L5128AGL-8IT
	10	-40°C~85°C	Tray	LY61L5128AGL-10I
			Tape Reel	LY61L5128AGL-10IT



Lyontek Inc.

LY61L5128A

Rev. 1.5

512K X 8 BIT HIGH SPEED CMOS SRAM

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