23V/2A High Efficiency Synchronous Rectified Step-Down DC/DC Converter

DESCRIPTION

The IT76620M is a high efficiency synchronous step-down DC/DC converter series with 2A continuous output current supplied. Included on the substrate with the features listed is a high performance trans-conductance error amplifier that provides tight voltage regulation and accuracy under transient conditions. A built-in Under Voltage Lockout (UVLO) circuit is provided to prevent start-up until the input voltage reaches to 4.5V. In addition, it features over-current protection and thermal shutdown. To improve the light load efficiency, it is designed as the power saving mode (PSM) to minimize the switching loss by reducing the switching frequency. The IT76620M is available in SOP8 package.

FEATURES

- Input Voltage Supply Range from 4.5V to 23V
- Power Saving Mode (PSM) during the light Load Operation
- High Efficiency up to 93%
- Adjustable Output Voltage from 0.925V to 15V
- 2A Continuous Output Current
- 330KHz Constant Frequency Operation
- Current Mode Operation
- Programmable Soft-Start
- Over-temperature Protection
- Over-current Protection
- Input Under Voltage Lockout (UVLO)
- 10μA Shutdown Current
- SOP8 Package
- RoHS Compliant (100% Green Available)

APPLICATIONS

- Data comm. xDSL CPE Graphics Cards
- Set-Top-Box, DVD
- Servers/Networking
- DSP and FPGA Power Supply
- Telecomm Equipments
- DC-DC Regulator Modules
- LCD Monitor and LCD TV

TYPICAL APPLICATION

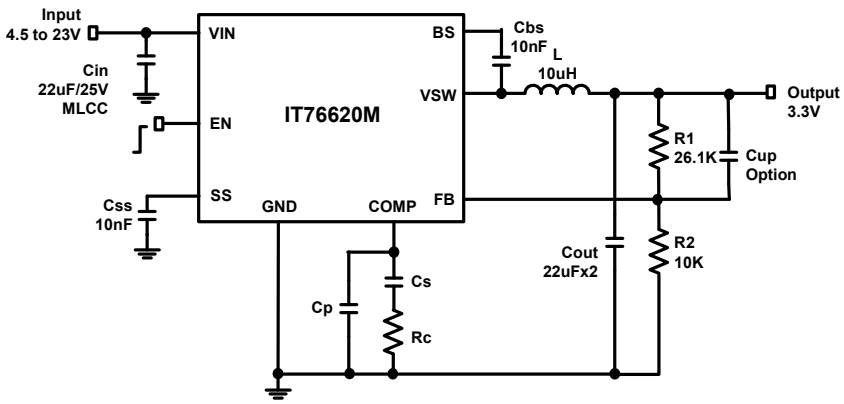


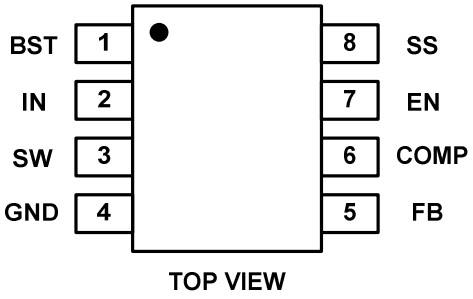
Figure 1. IT76620M Typical Operating Circuit

Ordering Information

Part No.	Marking	Temp. Range	Package	MOQ
IT76620M	IT76620M YYWW-XXX XXXXXX	-40°C ~+85°C	SOP8	2500/Tape&Reel

Note: YY:Year WW:Week

Pin Configuration



TOP VIEW

Pin Description

Pin No.	Symbol	Description
1	BST	**High Side Gate Drive Boost Input** It is required to connect SW and BST by a capacitor, which is able to boost the gate drive to the internal NMOS above VIN to fully turn it ON.
2	VIN	**Power Supply** The input voltage for the power supply is connected to this pin.
3	SW	**Power Switch Output** This is the output of a power MOSFET switch.
4	GND	**Ground** This is the reference of the ground connection for all components in the power Supply.
5	FB	**Voltage Feedback** This is the input to an error amplifier, which drives the PWM controller. It is necessary to connect this pin to the actual output of power supply to set the DC output voltage.
6	COMP	**Compensation** This pin is to compensate the regulation control loop by connecting a series of RC network from COMP pin to GND pin.
7	EN	**Enable (floating of this pin not recommended)** This input provides an electrical ON/OFF control of the power supply. If the EN pin is open, it will be pulled to high by the internal circuit.
8	SS	**Soft-Start** This pin is connected to an external capacitor, which is between the SS pin and GND to control soft-start time. This externally connected 0.1μF capacitor is able to set the soft-start period to 28ms.

Absolute Maximum Rating (Note1)

Input Supply Voltage …… +26V
SW Voltage …….... - 1V to 27V
<10nS ..... (-5V to 30V)
EN Voltage ……..... - 0.3 to VIN+0.3V
Other Pins …… - 0.3V to +6V
Boost Voltage ……..... Vsw+6V

ESD Classification …..…….. Class 2
Junction Temperature Range …...…… -40ºC to 150°C
Storage Temperature Range ……..… -65ºC to 150°C
Lead Temperature (Soldering10s) ……..... 260°C

Thermal information (Note3,4)

Maximum Power Dissipation(TA=+25°C) …… 1.098W

Thermal resistance(θJA) …….. 91°C/W
Thermal resistance(θJC) …….. 43°C/W

Recommend Operating Conditions (Note2)

Input Voltage (V_{IN}) ……..…… +4.5V to +23V

Operating Temperature Range ……-40°C to +85°C

Junction Temperature Range …...…….. 135°C

Note (1): Stress exceeding those listed “Absolute Maximum Ratings” may damage the device.
Note (2): The device is not guaranteed to function outside of the recommended operating conditions.
Note (3): Measured on JESD51-7, 4-Layer PCB.
Note (4): The maximum allowable power dissipation is a function of the maximum junction temperature T_{J_MAX}, the junction to ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D\_MAX}= (T_{J\_MAX}-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

Electrical Characteristics

T_A = +25°C, V_{IN} = 12V, unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage		4.5		23	V
Shutdown Supply Current	VEN = 0V		10		μA
Regulated Feedback Voltage	4.5V≦VIN≦23V	0.9	0.925	0.95	V
Error Amplifier Transconductance	△ICOMP = ±10μA		700		μA/V
Current Sense to COMP Transconductance			2.2		A/V
Current Limit			3.6		A
SW Leakage Current	VEN = 0V, VSW = 0V			10	μA
High Side On Resistance			0.15		Ω
Low Side On Resistance			0.12		Ω
Oscillation Frequency		260	330	400	KHz
Short Circuit Oscillation Frequency	VFB=0V		82.5		kHz
Maximum Duty Cycle	VFB=0.7V		90		%

Parameter	Conditions	Min.	Typ.	Max.	Unit
Minimum Duty Cycle	VFB=1.1V			0	%
Minimum On Time			100		ns
Under Voltage Lockout Threshold	VIN Rising	3.85	4.1	4.35	V
Under Voltage Lockout Threshold Hysteresis			250		mV
Thermal Shutdown Threshold			155		℃
EN High Level		2.8			V
EN Low Level				0.6	V
EN Input Current	VEN = 0V		3	3.6	μA
Soft-Start Current	VSS=0V		5.3		uA
Soft-Start Period	Css=0.1uF		28		mS

Functional Block Diagram

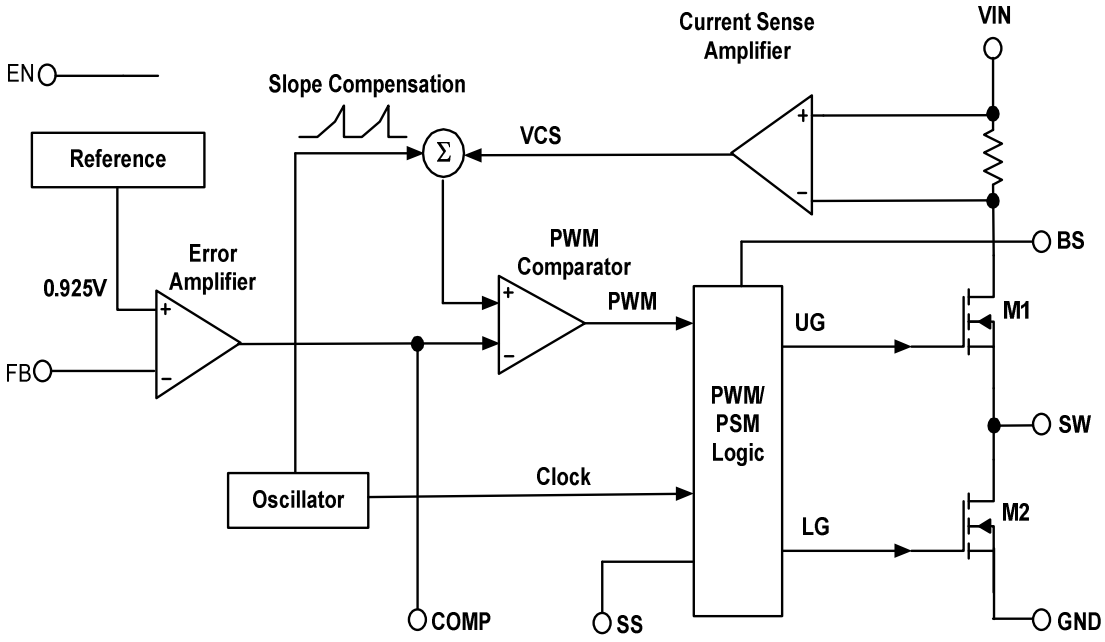
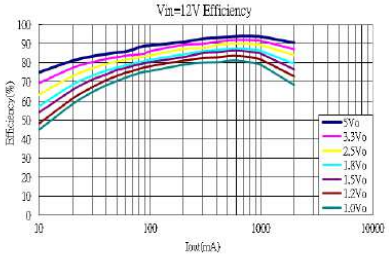


Figure 2. IT76620M Functional Block Diagram

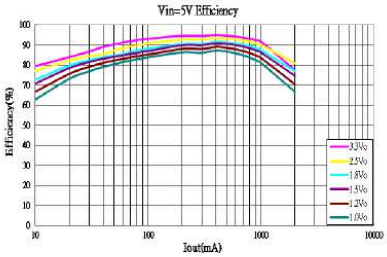
TYPICAL PERFORMANCE CHARACTERISTICS

IT76620M application circuit (Figure 1.), TA = +25°C, unless otherwise noted.

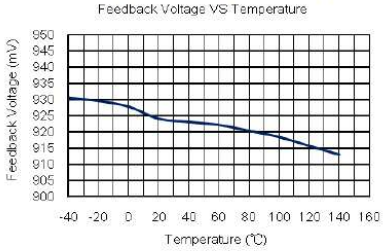
Efficiency vs. Load Current



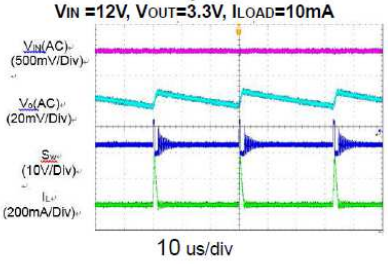
Efficiency vs. Load Current



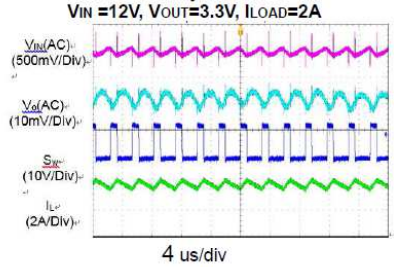
VIN =12V, VOUT=3.3V, ILOAD=0.5A



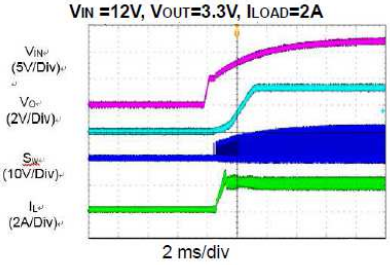
Steady State
VIN =12V, VOUT=3.3V, ILOAD=10mA



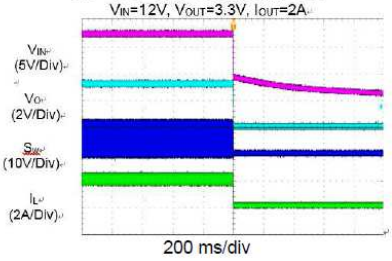
Steady State
VIN =12V, VOUT=3.3V, ILOAD=2A



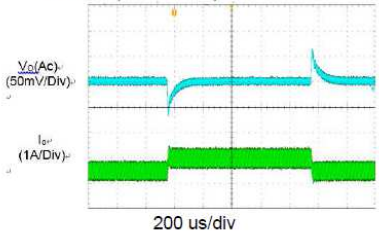
Power On
VIN =12V, VOUT=3.3V, ILOAD=2A



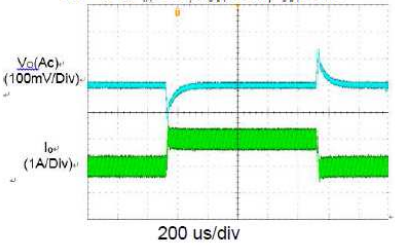
Power OFF
VIN =12V, VOUT=3.3V, ILOAD=2A



Load Transient
VIN =12V, VOUT=3.3V,ILOAD=0.5A~1A



Load Transient
VIN =12V, VOUT=3.3V,ILOAD=1A~2A



Detailed Description

The part is a current mode PWM synchronous step-down converter with a constant switching frequency. It regulates the input voltage from 4.5V to 23V and a low output voltage of 0.925V.The supplied load current is up to 2A.

Power Saving Mode

The switching losses resulted from the Miller capacitance of the MOSFET are the dominant power dissipation parameters at light load. The power saving mode at light load can minimize the switching loss by reducing the switching frequency. Therefore, the part is designed as the power saving mode for high efficiency at light load.

Oscillator Frequency

Slope compensated current mode PWM control provides not only stable switching and cycle-by-cycle current limit for superior load and line response but also protection of the internal main switch and synchronous rectifier. The part switches at a constant frequency (F_{SW}) and regulates the output voltage. The PWM comparator modulates the power transferred to the load by changing the inductor's peak current based on the feedback error voltage during each cycle. The main switch is turned on for a certain period to ramp the inductor's current at each rising edge of the internal oscillator under normal operation whereas off when the inductor's peak current is above the error voltage. After the main switch is turned off, the low side MOS will be turned on immediately and stay on until the next cycle starts.

Short Circuit Protection

The part provides short circuit protection. When the output is shorted to ground, the oscillator's frequency is reduced to prevent the inductor's current from increasing beyond the NMOS current limit. The NMOS current limit is also reduced to lower the short circuit current. The frequency and current limit will return to the normal values once the short circuit condition is removed and the feedback voltage reaches V_{FB}.

Maximum Load current

The part can operate down to 4.5V input voltage; however the maximum load current decreases at lower input due to large IR voltage drop on the main switch and low side switch. The slope compensation signal reduces the inductor's peak current as a function of the duty cycle to prevent sub-harmonic oscillations at duty cycles greater than 50%.

Enable

The EN pin provides electrical on/off control of the regulator. Once the voltage of the EN pin exceeds the threshold voltage, the regulator starts operation and the internal slow start begins to ramp. If the voltage of the EN pin is pulled below the threshold, the regulator will stop switching and the internal slow start reset. If the EN pin is open, it will be pulled to high by the internal circuit.

Under Voltage Lockout

The part incorporates an under voltage lockout circuit to keep the device disabled when VIN is below the UVLO start threshold. During power-up, the internal circuit is held inactive until VIN exceeds the UVLO start threshold voltage. Once this threshold voltage is reached, device start-up begins. The device operates until VIN falls below the UVLO stop threshold voltage. The typical hysteretic in the UVLO comparator is 250mV.

Soft-Start

The built-in soft-start function is to gradually raise the output voltage after power-on. The soft-start period can be set by the external capacitor, which is between the SS pin and GND.

Css	Tss
10nF	2.8ms
100nF	28ms

Boost Capacitor

The BST pin and SW pin can be connected by a 10nF low ESR ceramic capacitor, providing the gate drive voltage for the high side MOSFET.

Thermal Shutdown

The part protects itself from overheating with an internal thermal shutdown circuit. If the junction temperature exceeds the thermal shutdown threshold, the voltage reference will be grounded and high side MOSFET turned off.

Compensation

The system stability is controlled through COMP pin. It will present a general design procedure to ensure a stable and operational circuit. The design in this data sheet is optimized for particular requirements. Some components may need to be changed to ensure stability if there are different requirements. First of all, the power components and their corresponding effects need to be determined. Following are the compensation components, which are to produce stability.

The compensation steps for the converter are listed below:

(1). Choose an appropriate inductor and output capacitance based on the allowed output voltage ripple and load transient.

(2). Placing F_C as high as possible can respond quickly to the load transient. Considering the output capacitor's tolerances and temperature effects, typically place F_C approximately 1/10 of F_S for the multi-layer ceramic output capacitor (X5R, X7R). However, if the type of the output capacitor is the aluminum electrolytic or that largely variable with the temperature, place F_C approximately 1/20 of F_S .

(3). Set the compensation R_C to zero to cancel the R_{LOAD} C_{OUT} pole.

$$R_C = \frac{2\pi \times F_C \times C_{OUT} \times V_{OUT}}{G_M \times G_{CS} \times V_{REF}}$$

$$C_C = \frac{C_{OUT} \times R_{LOAD}}{R_C}$$

G_M: error amp transconductance
G_{CS}: current sense transconductance

(4). Determine C_P if required.
If Z_{ESR} (zero occurs by output capacitor ESR) is less than F_C, it should be cancelled with a pole set by capacitor C_P connected between C_C to GND.

$$C_P = C_{OUT} \times \frac{R_{ESR}}{R_C}$$

Application Information

Input Capacitor Selection

It is necessary for the input capacitor to sustain the ripple current produced during the period of “on” state of the upper MOSFET, so a low ESR is required to minimize the loss. The RMS value of this ripple can be obtained by the following:

$$I_{IN}RMS = I_{OUT}\sqrt{D\times(1-D)}$$

Where D is the duty cycle, I_{INRMS} is the input RMS current, and I_{OUT} is the load current. The equation reaches its maximum value with D = 0.5. The loss of the input capacitor can be calculated by the following equation:

$$P_{CIN} = ESR_{CIN}\times I_{IN}RMS^{2}$$

Where P_{CIN} is the power loss of the input capacitor and ESR_{CIN} is the effective series resistance of the input capacitance. Due to large di/dt through the input capacitor, electrolytic or ceramics should be used. If a tantalum must be used, it must be surge-protected. Otherwise, capacitor failure could occur.

Output Inductor Selection

The output inductor selection is to meet the requirements of the output voltage ripple and affects the load transient response. The higher inductance can reduce the inductor's ripple current and induce the lower output ripple voltage. The ripple voltage and current can be approximately calculated approximated by the following equations:

$$\Delta I = \frac{V_{in} - V_{out}}{F_S \times L} \bullet \frac{V_{out}}{Vin}$$

$$\Delta V_{out} = \Delta I \times ESR$$

Although the increase of the inductance reduces the ripple current and voltage, it contributes to the decrease of the response time for the regulator to load transient as well. Increasing the switching frequency (Fs) for a given inductor also can reduce the ripple current and voltage but it will increase the switching loss of the power MOS.

The way to set a proper inductor value is to have the ripple current (ΔI) be approximately 10%~50% of the maximum output current. Once the value has been determined, select an inductor capable of carrying the required peak current without going into saturation. It is also important to have the inductance tolerance specified to keep the accuracy of the system controlled. Using 20% for the inductance (at room temperature) is reasonable tolerance able to be met by most manufacturers. For some types of inductors, especially those with core made of ferrite, the ripple current will increase abruptly when it saturates, resulting in a larger output ripple voltage.

Output Capacitors Selection

An output capacitor is required to filter the output and supply the load transient current. The high capacitor value and low ESR will reduce the output ripple and the load transient drop. These requirements can be met by a mix of capacitors and careful layout.

In typical switching regulator design, the ESR of the output capacitor bank dominates the transient response. The number of output capacitors can be determined by the following equations:

$$ESR_{MAX} = \frac{\Delta V_{ESR}}{\Delta I_{OUT}}$$

$$\text{Number Of Capacitors} = \frac{ESR_{CAP}}{ESR_{MAX}}$$

ΔV_{ESR} = change in output voltage due to ESR
ΔI_{OUT} = load transient.
ESR_{CAP} = maximum ESR per capacitor (specified in manufacturer's data sheet).
ESR_{MAX} = maximum allowable ESR.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. For the decoupling requirements, please consult the capacitor manufacturers for confirmation.

Output Voltage

The output voltage is set using the FB pin and a resistor divider connected to the output as shown in the following AP Circuit. The output voltage (V_{out}) can be calculated according to the voltage of the FB pin (V_{FB}) and ratio of the feedback resistors by the following equation, where (V_{FB}) is 0.925V:

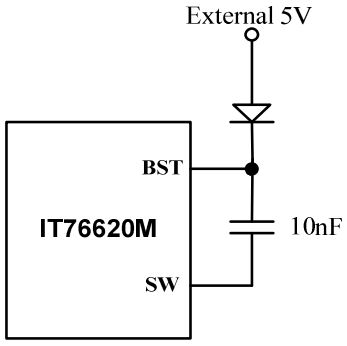
$$V_{FB} = V_{out} \times \frac{R_2}{(R_1 + R_2)}$$

Thus the output voltage is:

$$V_{out} = 0.925 \times \frac{(R_1 + R_2)}{R_2}$$

External Bootstrap Diode

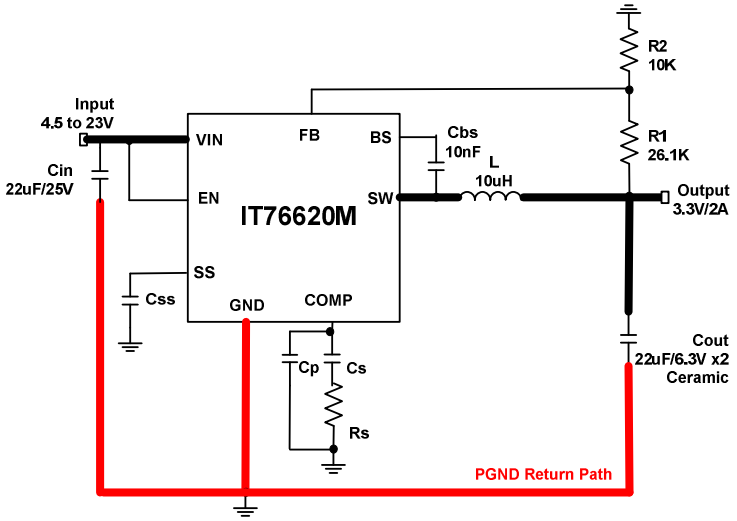
When the condition of Duty Cycle>65% occurs, it is strongly recommended to add an external bootstrap diode (such as IN4148 or BAT54) between an external 5V and BST pin for efficiency improvement.



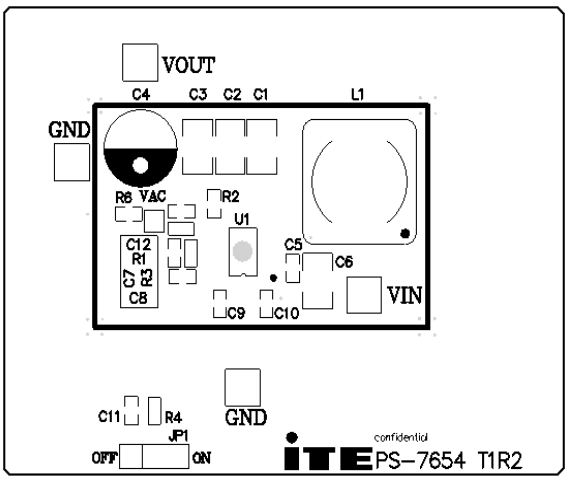
Layout Consideration

For proper operation of the converter, some layout rules should be followed. It is necessary to understand which pin of IT76620M is sensitive and which is insensitive. Please refer the following for the location where noise comes from on the circuit and where the clear ground is for the small signal ground.

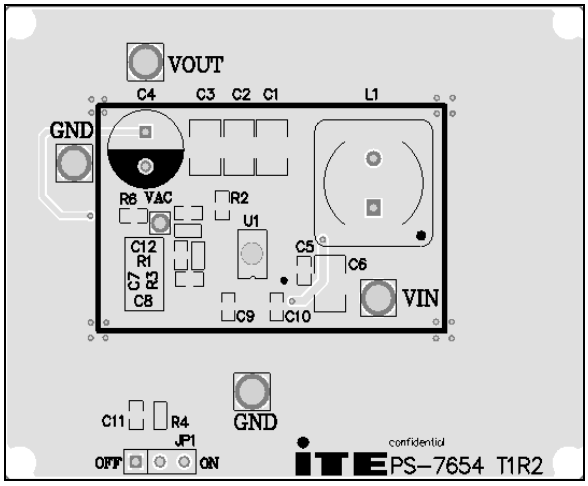
1.) First, put the input capacitor (C_{IN}) as close as possible to the VIN pin.
2.) Secondly, place the Cs, Rs, Cp, Css and R2 as close as IT76620M and connect these analog grounds (Clear AGND) to IT76620M's GND pin. It is recommended to use a dot short for these AGND pins or connect the GND pin via contact.
3.) The large current loop shown in bold lines in the above figure circuit should be routed as short and wide as possible and the switch node is a high dv/dt. It easily couples noise to other traces by the capacitive path. Therefore the sensitive signals like FB, COMP and AGND should be routed away with this noise source.
4.) The feedback network resistors (R1 & R2) should be routed away from the inductor and switch node to minimize noise and EMI issue. And the R1 resistor should be sensed the output capacitor or device loading, not the inductor's output node.



Top Layer

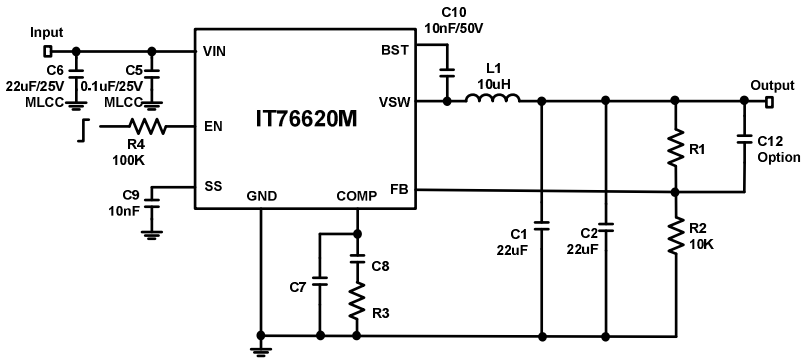


Bottom Layer



IT76620M EVB Schematic

Application: Typical Application Circuit



EVB BOM List

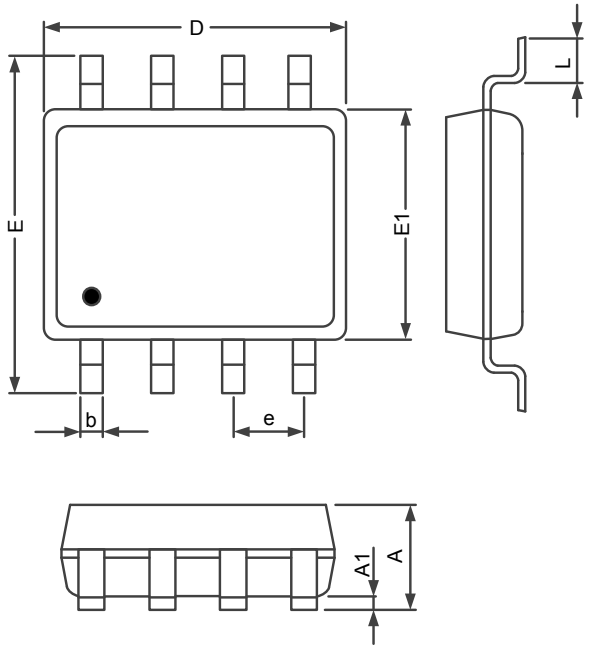
Qty	Ref	Description	Package
3	C1, C2	Ceramic Capacitor X5R 16V Murata-part number:GRM32ER61C226KE20L	1206
1	C6	Ceramic Capacitor X5R 25V Murata-part number:GRM32ER61E226ME15L	1206
1	C5	Ceramic Capacitor	0603
1	L1	Inductor, Rated Current 3.5A WE-part number: 744 066 100---10uH	SMD
4	R1, R2, R3, R4	Resistor, ±1%	0603
4	C8, C9, C10, C11	Ceramic Capacitor	0603
1	C7	C7 value is adjustable for the ESR of Cout	0603
1	U1(IT76620M)	Step-Down DC/DC Converter	SOP8

V_{OUT} (V)	R1(KΩ)	R3(KΩ)	C8(nF)	C7(pF)	C12(pF)	L (μH)	C_{OUT} (μF)
12	120	60.4	3.3	18	NC	10	22 x 2 (X5R 16V)
5	44.2	30.9	3.3	33	NC	10	22 x 2 (X5R 16V)
3.3	26.1	21	3.3	47	NC	10	22 x 2 (X5R 16V)
2.5	17.4	16	3.3	68	NC	10	22 x 2 (X5R 16V)
1.8	9.53	4.7	8.2	100	NC	10	22 x 2 (X5R 16V)
1.2	3	3.9	8.2	150	NC	10	22 x 2 (X5R 16V)
1	0.82	3	8.2	180	NC	10	22 x 2 (X5R 16V)

PACKAGING INFORMATION

Package Outline Dimensions

SOP 8L Package Outline Dimensions

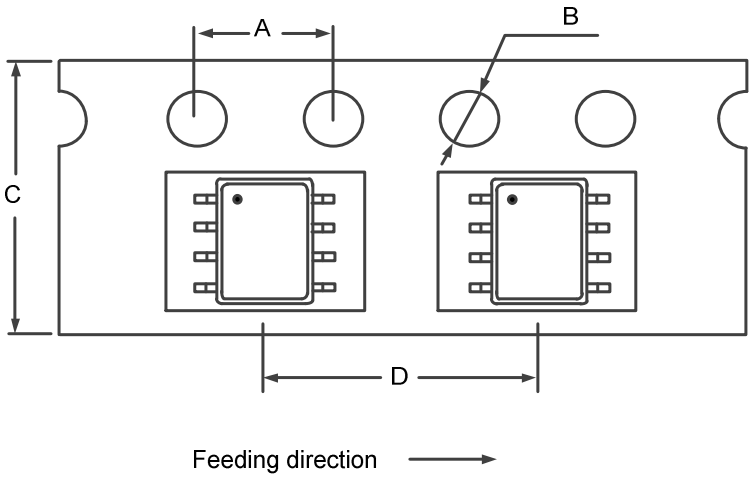


SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MIN.
A	1.35	1.75	0.053	0.069
A1	0.00	0.25	0.000	0.010
D	4.7	5.1	0.185	0.200
E1	3.7	4.1	0.145	0.161
E	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
b	0.31	0.51	0.012	0.020
e	1.16	1.37	0.046	0.054

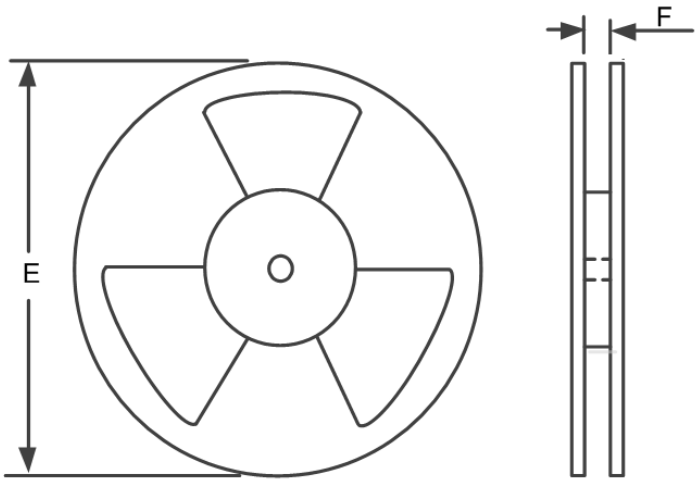
Tape & Reel Carrier Dimensions

SOP 8L

1. Orientation / Carrier Tape Information :



2. Rokreel Information :



3. Dimension Details :

PKG Type	A	B	C	D	E	F	Q'ty/Reel
SOP 8L	4.0 mm	1.5 mm	12.0 mm	8.0 mm	13 inches	13.0 mm	2,500

Reflow Profile

Classification Of IR Reflow Profile

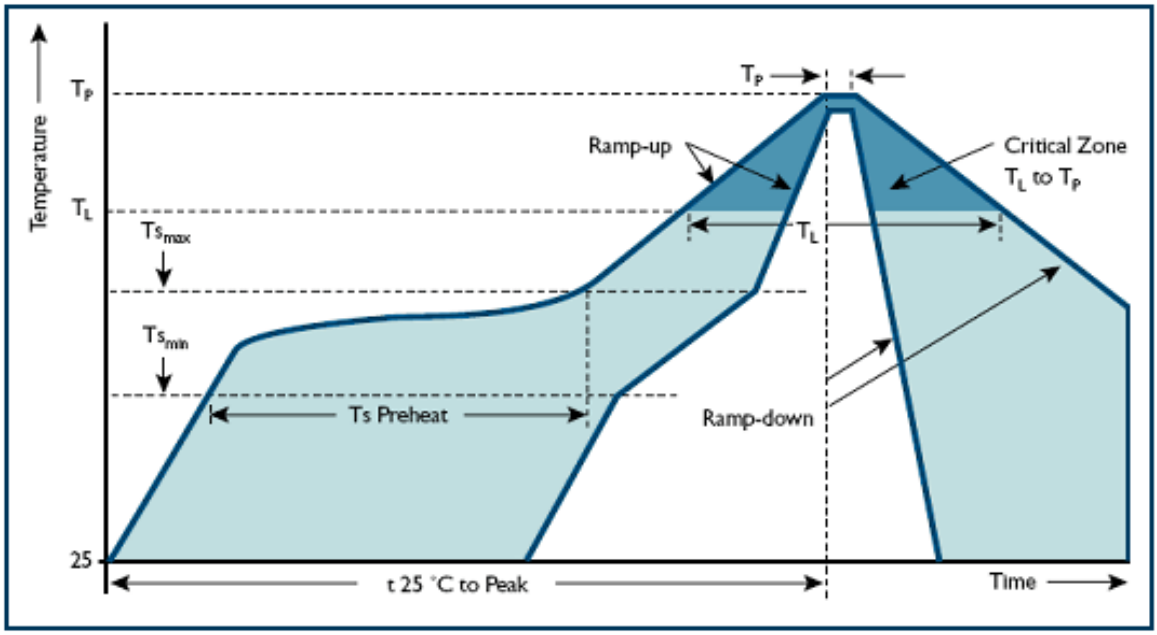
Reflow Profile	Green Assembly
Average Ramp-Up Rate (Ts_{min} to Tp)	1~2℃/second, 3℃/second max.
Preheat & Soak -Temperature Min(Ts_{min}) -Temperature Max(Ts_{max}) -Time(ts_{min} to ts ts_{max})	 150℃ 200℃ 60~120 seconds
Time maintained above: -Temperature(T_L) -Time(t_L)	 217℃ 60~150 seconds
Peak Temperature(Tp)	See Classification Temp in table 1
Time within 5℃ of actual Peak Temperature(tp)	30 seconds max.
Ramp-Down Rate	6℃/second max.
Time 25℃ to Peak Temperature	8 minutes max.

* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Table 1. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 ℃	260 ℃	260 ℃
1.6 mm – 2.5 mm	260 ℃	250 ℃	245 ℃
≥2.5 mm	250 ℃	245 ℃	245 ℃

Note: For all temperature information, please refer to topside of the package, measured on the package body surface.



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