

MC2007-3

3.3 V PIN Pre-Amplifier with AGC for Applications to 200 Mbps

The MC2007-3 is a low-noise, transimpedance amplifier with AGC, manufactured in an advanced, low-cost, sub-micron CMOS process. Its wide dynamic range, differential output and high PIN bias make it well suited to high-performance telecommunications, especially OC-3/STM-1. However, due to its low cost, the MC2007-3 also meets the needs of datacom applications.

The MC2007-3 is available in die form. For optimum system performance die should be mounted in close proximity with the photodetector.

The MC2007-3 is designed to be used with the MC2045 or M02095 post amplifier IC. When combined with a photodiode, the chip set forms a high performance, low cost 3.3V receiver.

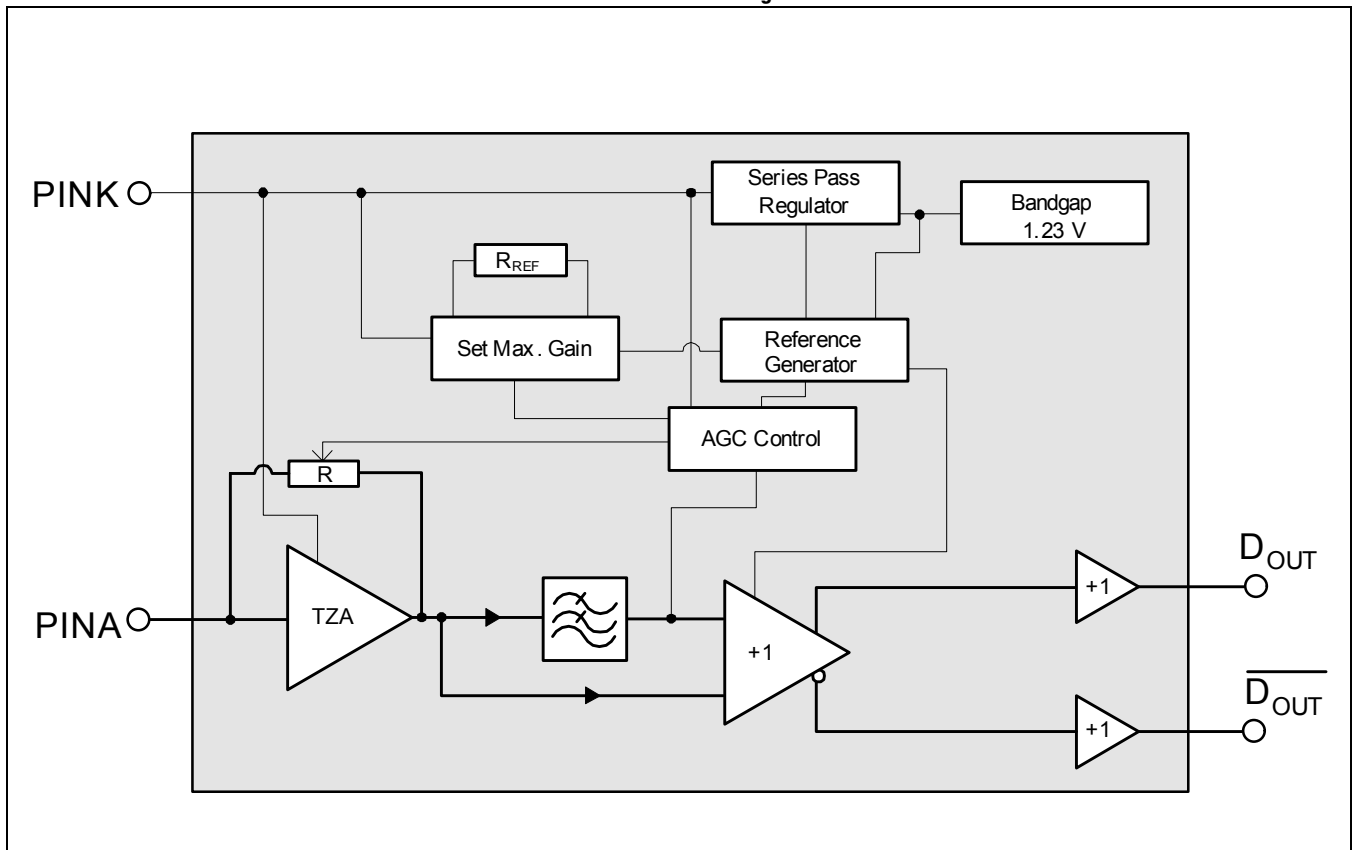
Applications

- Optical Receivers (Up to 200 Mbps Operation)
- SDH / SONET / ATM
- Fast Ethernet
- ESCON
- Passive Optical Networks (PONs)
- SFP/SFF Transceivers
- BiDi Transceivers

Features

- Low-cost, CMOS process
- Receiver sensitivity typically -39 dBm at 155 Mbps, when integrated into a module with suitable photodiode and post-amplifier
- 140 MHz bandwidth allows wide range of operation: 100, 125, 155, and 200 Mbps
- Typical differential gain of 62 k Ω at low signal levels
- AGC gives continuous operation to +3 dBm
- 65 mW power consumption at +3.3 V supply
- > 35 dB Power-supply noise rejection
- Available as die only

Functional Block Diagram



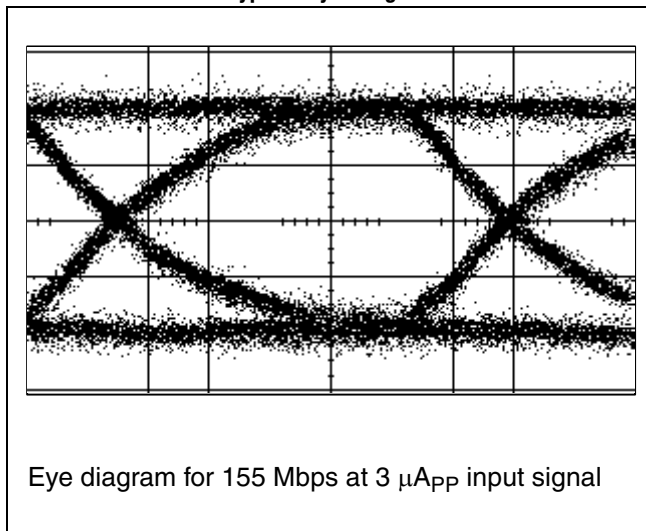
Ordering Information

Part Number	Package	Operating Temperature
MC2007-XX	Waffle pack	-40 °C to 85 °C
MC2007-XX	Expanded whole wafer on a ring	-40 °C to 85 °C
MC2007-EVM	MC2007 evaluation board with MC2045 post amp	-40 °C to 85 °C

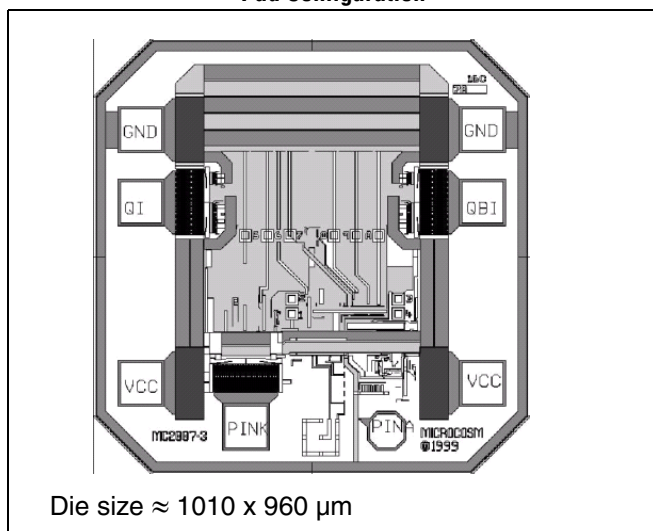
Revision History

Revision	Level	Date	Description
E	Preliminary	November 2007	Correct PinK absolute maximum information. Update format.
D	Preliminary	June 2006	Updated format. Updated Absolute Maximum Ratings. Added TIA Use with Externally Biased Detectors section.
C	Preliminary	June 2004	Added Note 7 to Table 2-4.
B	Preliminary	June 2003	Added externally biases diode maximum to Absolute Maximum Ratings table.
A	Preliminary	December 2000	Initial Release.

Typical Eye Diagram



Pad Configuration





1.0 Product Specification

1.1 Absolute Maximum Ratings

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{CC}	Power supply (V_{CC} - GND)	-0.4 to +4.5	V
T_J	Die Junction temperature	+150	°C
T_{STG}	Storage temperature	-65 to +150	°C
I_{PINA}	PinA maximum input current	4.5 ^(1, 2, 3)	mApp
V_{PINA}	Input voltage at PINA	-0.4 to +3.6 ⁽²⁾	V
I_{PINK}	Maximum average current sourced out of PINK	10	mA
V_{PINK}	Maximum input voltage at PINK and MON	-0.4 to V_{CC} +0.4	V
I_{Dout}	Maximum average current sourced out of Dout and DoutB	10.0 ⁽⁴⁾	mA
V_{Dout}	Maximum input voltage at Dout and DoutB	0.0 to V_{CC} +0.4 ⁽⁴⁾	V

NOTES:

1. Equivalent to 2.8 mA average current.
2. Do not exceed either the I_{PINA} or V_{PINA} rating. PINA damage will result in performance degradation which is difficult to detect.
3. Part must be powered up for PinA to accept this current. With the part unpowered, no current should be sourced into PinA.
4. Do not exceed either the I_{Dout} or V_{Dout} rating. Output device damage could occur.

1.2 Recommended Operating Conditions

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Rating	Units
V_{CC}	Power supply (V_{CC} - GND)	3.3 ± 10%	V
C_{PD}	Max. Photodiode capacitance ($V_{PD} = 1.8$ V), for 155 Mbps data rate	1.0	pF
T_A	Operating ambient temperature	-40 to +85	°C

1.3 DC Characteristics

Table 1-3. DC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{PD}	PIN PD bias voltage (PINK - PINA)	1.5	1.7	2.0	V
V_{CM}	Common mode output voltage	-	$V_{CC}/2$	-	V
I_{CC}	Supply current	12	22	32	mA
V_A	PINA bias voltage with respect to GND	0.9	1.04	1.1	V

1.4 AC Characteristics

Table 1-4. AC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
R_{OUT}	Output impedance (single ended)	25	40	100	Ω
I_{NOISE}	Input noise current ^{(1), (2), (3)}	1.0	1.5	2.6	pA/(rt(Hz))
Pin(mean), Min.	Optical sensitivity ^{(1), (2)}	-	-39	-	dBm
Pin(mean), Max.	Optical saturation ⁽²⁾	+1	+3	-	dBm
G	Small signal transimpedance ^{(3), (4)} Single ended: Differential:	26 52	31 62	35 70	k Ω
V_D	Differential output voltage ⁽³⁾	-	-	800	mV
BW	Bandwidth to -3 dB point (electrical) ⁽⁷⁾	110	140	-	MHz
T_r, T_f	Data out rise/fall times (20% - 80% points)	-	-	2	ns
T_{PWD}	Pulse width distortion	-	-	10	%
OS_{PULSE}	Pulse overshoot	-	-	10	%
T_{AGC}	AGC setting time	-	-	100	μ s
OS_{AGC}	AGC overshoot	-	-	12	%
PSRR	Power supply rejection ratio (<4 MHz)	35	-	-	dB
Z_{IN}	Input impedance ⁽⁵⁾	30	-	3000	Ω

NOTES:

1. Measured with input capacitance, $C_{IN} = 0.7$ pF
2. Assuming photodiode response of 0.9 A/W, extinction ratio of 10 dB and BER of 10^{-10}
3. The 2007 is designed to drive a load $>500 \Omega$. Measurements are taken into high Z.
4. Measured at 100 kHz with a test current of 0.5 μ A mean (1 μ A_{pp}).
5. Data input amplitude dependant Z_{IN} is inversely proportional to input photo diode current and measured between 20 kHz and 100 MHz.
6. All die are tested and guaranteed at 25°C \pm 5°C. Die are characterized and designed to operate from -40 to +85°C. Optical sensitivity is characterized in an optical assembly as an example of what can be achieved, and is not guaranteed. Consult factory for configuration details.
7. Measured electrically using a 50 Ω source with a 480 Ω resistor and 100 nF capacitor in series with the input to PINA pad and a 0.7 pF capacitor to ground with mean input current = 0.5 μ A.

Figure 1-1. Typical Performance

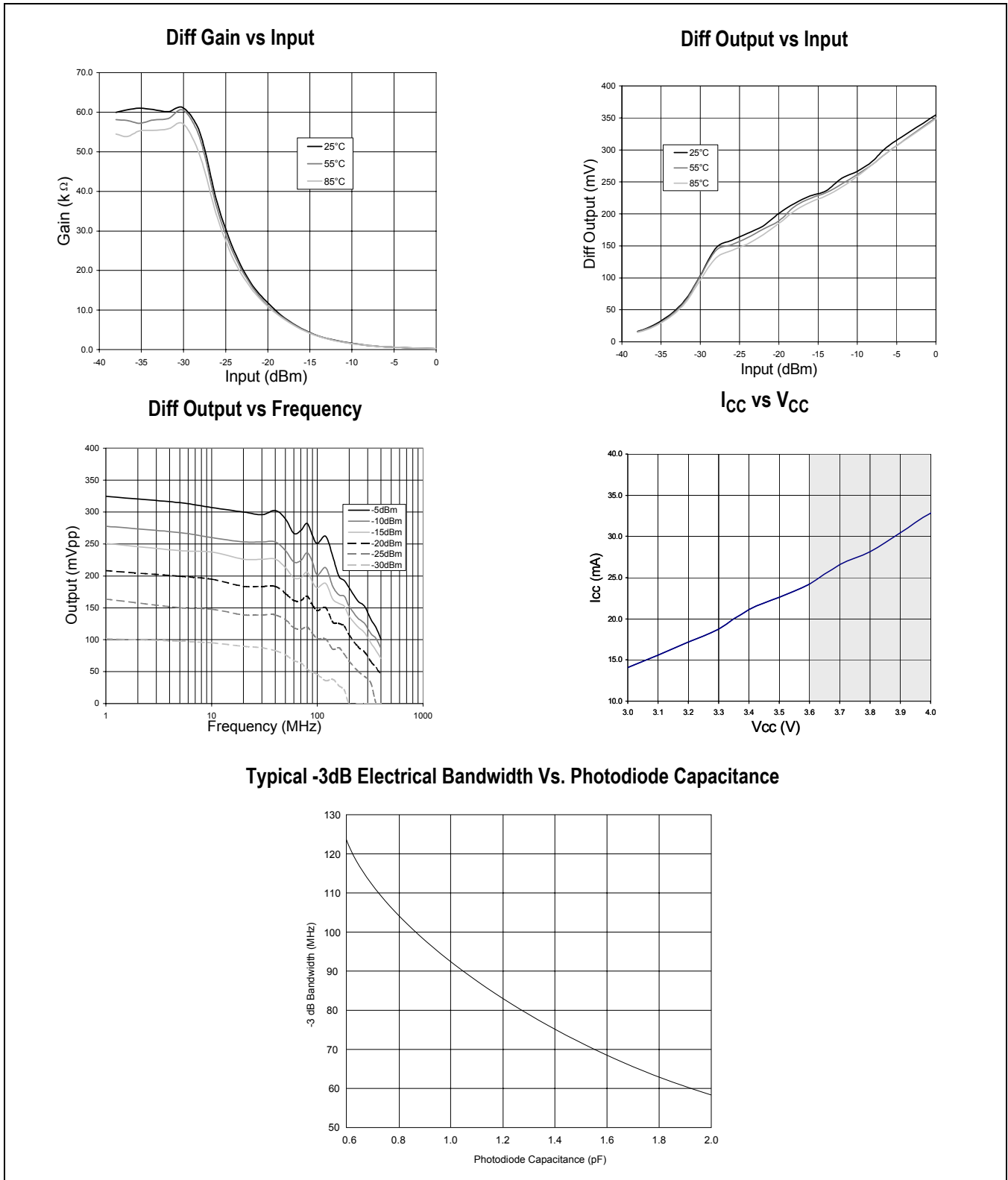
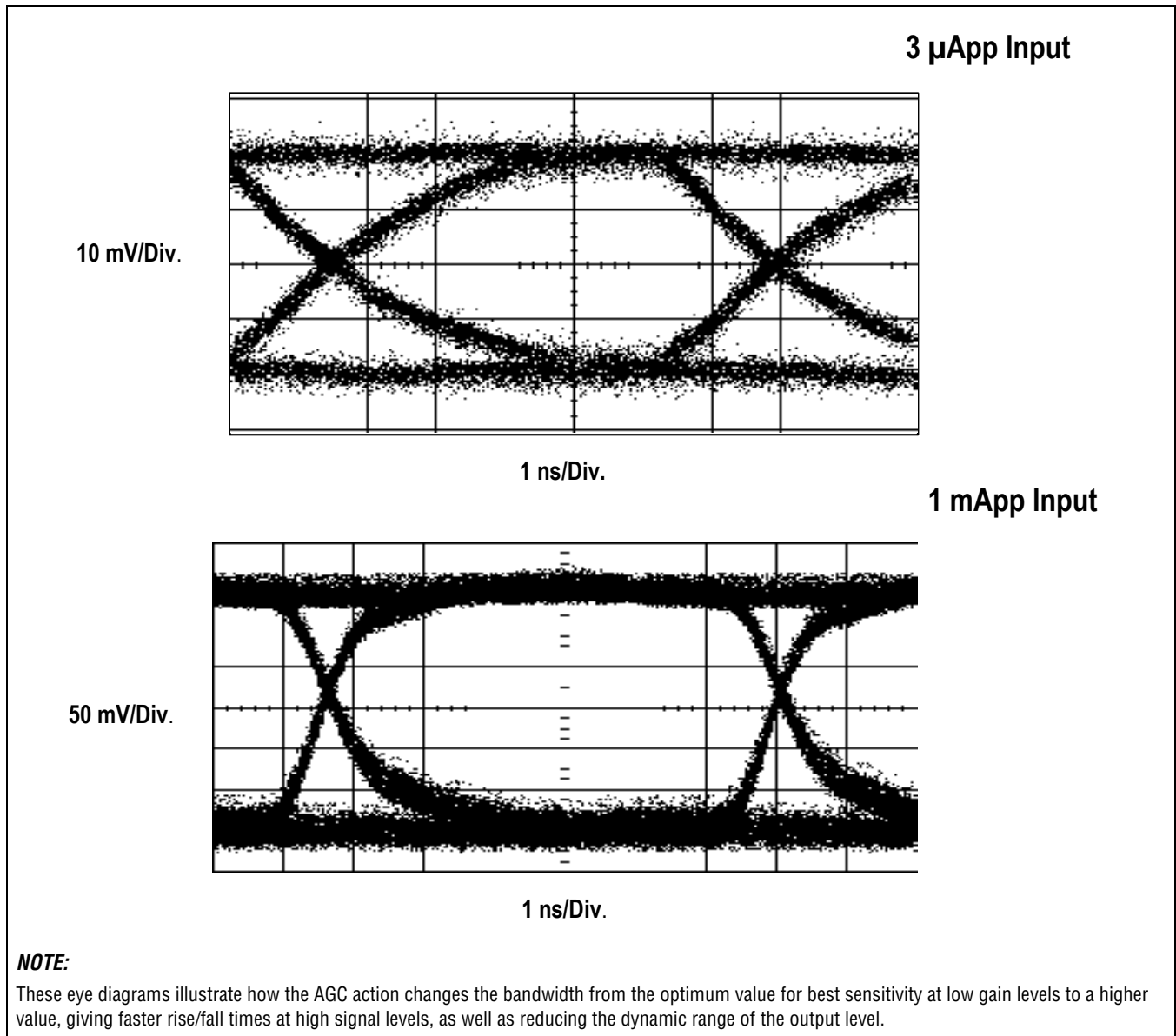


Figure 1-2. Eye Diagrams





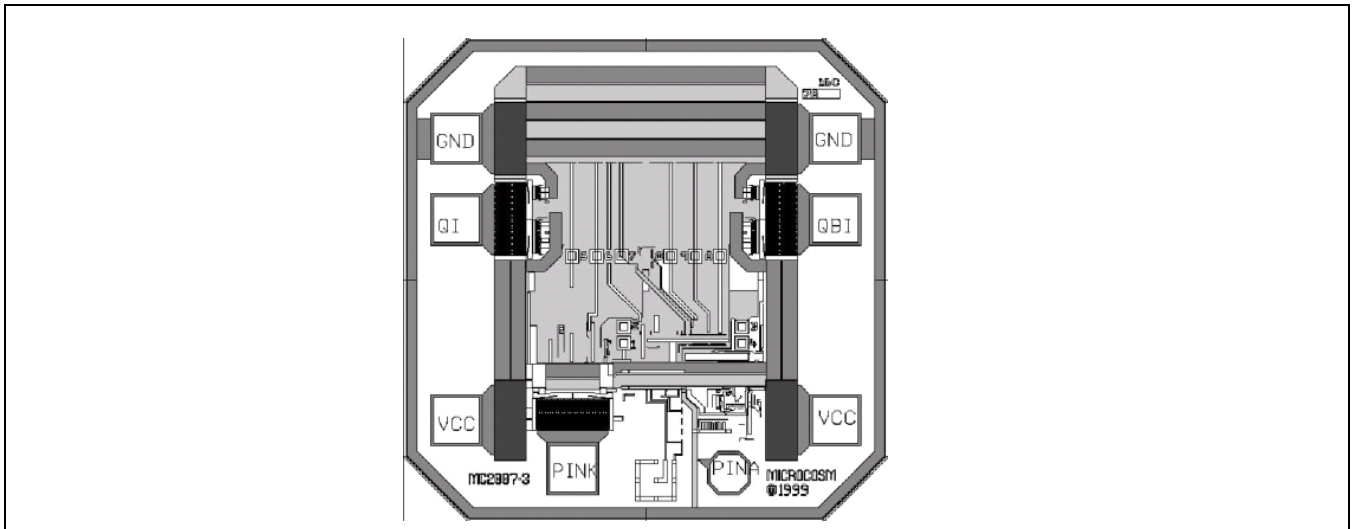
2.0 Pin Description

2.1 Pin Description

Table 2-1. Pin Description

Die Pad No	Name	Function
1, 8	GND	Ground pin. Connect to the most negative supply. Both pins should be used
2	D _{OUT}	Non-inverted data output. Differential output with D _{OUT}
3, 6	V _{CC}	Power pin. Connect to most positive supply. Either or both pins may be used
4	PINK	PIN cathode connection. Connect photodiode between this pin and PINA
5	PINA	PIN anode connection. Connect photodiode between this pin and PINK
7	D _{OUT}	Inverted data output. Differential output with D _{OUT}

Figure 2-1. Bare Die Layout





3.0 Functional Description

3.1 Overview

The MC2007-3 is a low-noise, transimpedance amplifier with AGC, manufactured in an advanced, low-cost, sub-micron CMOS process. Its wide dynamic range, differential output and high PIN bias make it well suited to high-performance telecommunications, especially OC-3/STM-1. However, due to its low cost, the MC2007-3 also meets the needs of Datacom applications.

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Figure 3-1. Block Diagram

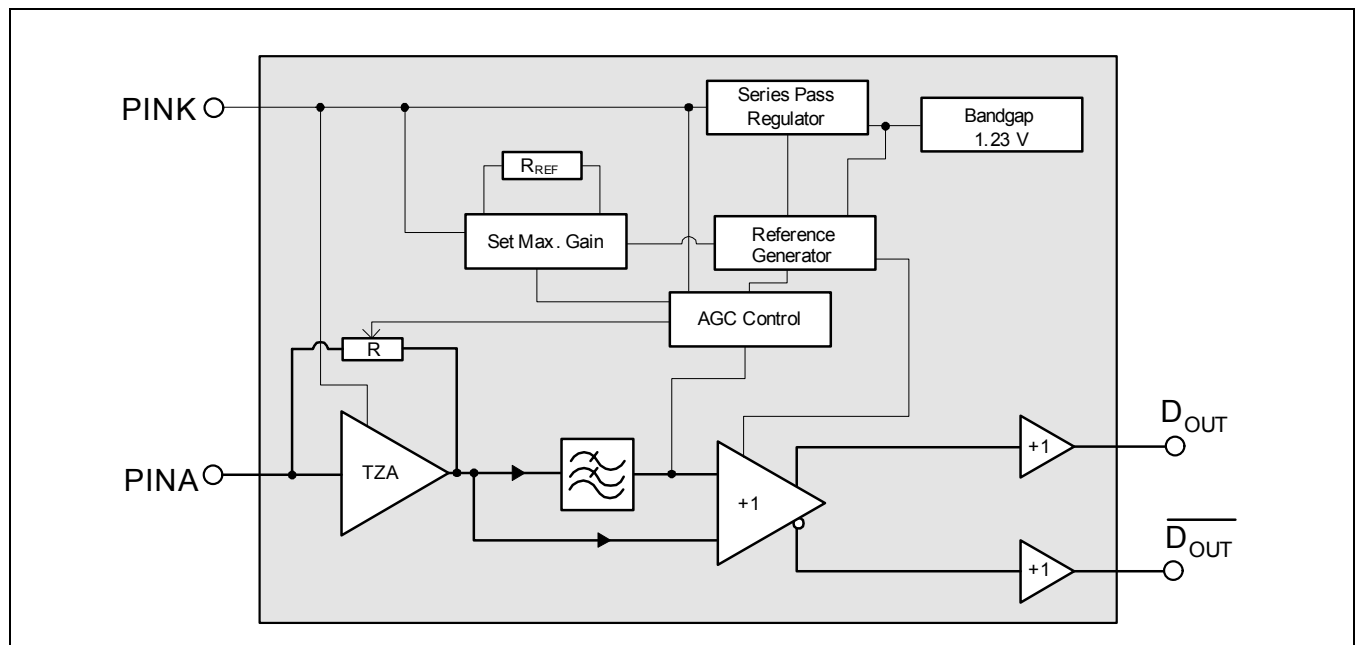
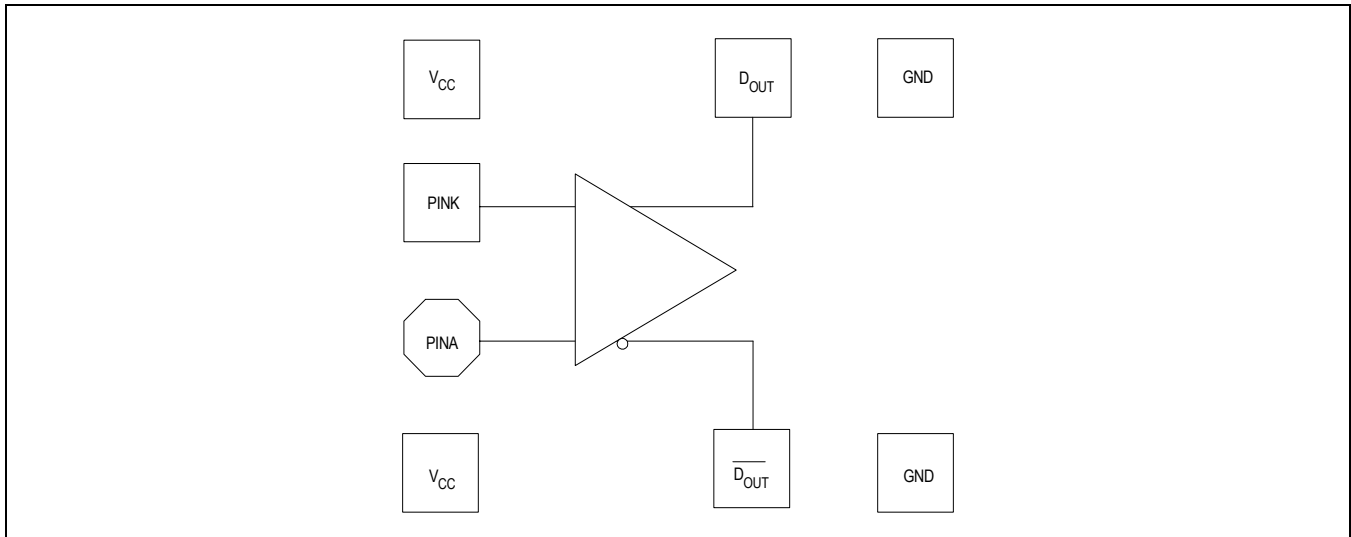


Figure 3-2. Top Level Diagram

3.2 Features

- Low-cost, CMOS process
- Receiver sensitivity typically -39 dBm at 155 Mbps, when integrated into a module with suitable photodiode and post-amplifier
- 140 MHz bandwidth allows wide range of operation: 100, 125, 155, and 200 Mbps
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- > 35 dB Power-supply noise rejection
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3.3 General Description

3.3.1 TIA

The transimpedance amplifier consists of a high gain single-ended CMOS amplifier (TIA), with a feedback resistor. The feedback creates a low impedance at the input and virtually all of the input current passes through the feedback resistor, defining the voltage at the output. Advanced CMOS design techniques are employed to maintain the stability of this stage across all input conditions.

Single-ended amplifiers have inherently poor power supply noise rejection. For this reason, an on-chip, low dropout, linear regulator has been incorporated into the design to give excellent noise rejection up to several MHz. Higher frequency power supply noise must be removed by external decoupling.

The circuit is designed for PIN photodiodes in the grounded cathode configuration, with the anode connected to the input of the TIA and the cathode connected to the PIN K input. The PIN K pad supplies ~1.7V to reverse bias the pin diode to reduce capacitance. If a higher reverse voltage is required, the user may supply their own low impedance bias supply.

3.3.2 AGC

The MC2007-3 has been designed to operate over the input range of +3 dBm to -39 dBm at long wavelengths. To do so, the AGC achieves a dynamic range compression of 50:1 in transimpedance.

The AGC only operates on signals greater than -30 dBm (@ 0.9 A/W). This knee in the gain response is important when setting signal detect functions in the following post amplifier. It also aids in active photodiode alignment.

3.3.3 Output Stage

The signal from the TIA enters a phase splitter and a pair of voltage follower outputs. These are designed to drive a high impedance (>500 Ω) load. They are stable for driving capacitive loads, such as interstage filters.

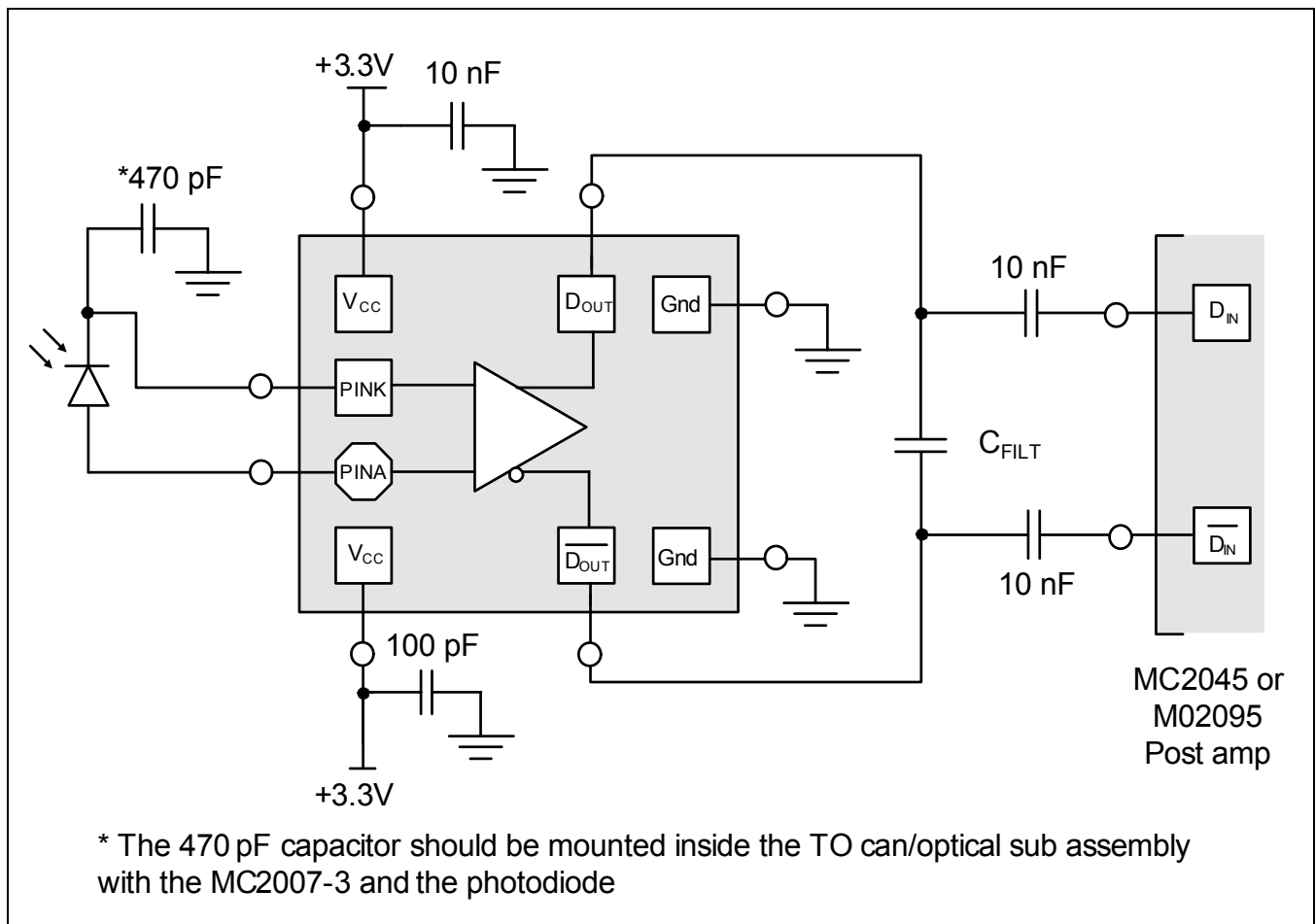


4.0 Applications Information

4.1 Filter Design

The achievable sensitivity of the MC2007-3 is dependant on the noise bandwidth of the amplifier, which varies with temperature and process. The bandwidth should therefore be limited by an interstage filter for maximum performance. This will typically be a one pole filter, using a capacitor across the outputs. For maximum sensitivity, a filter with steeper roll-off and better transient response can be implemented with inductors and capacitors. If the module is intended to be used at several rates, interstage filtering should not be employed. Typical application circuit shown in [Figure 4-1](#).

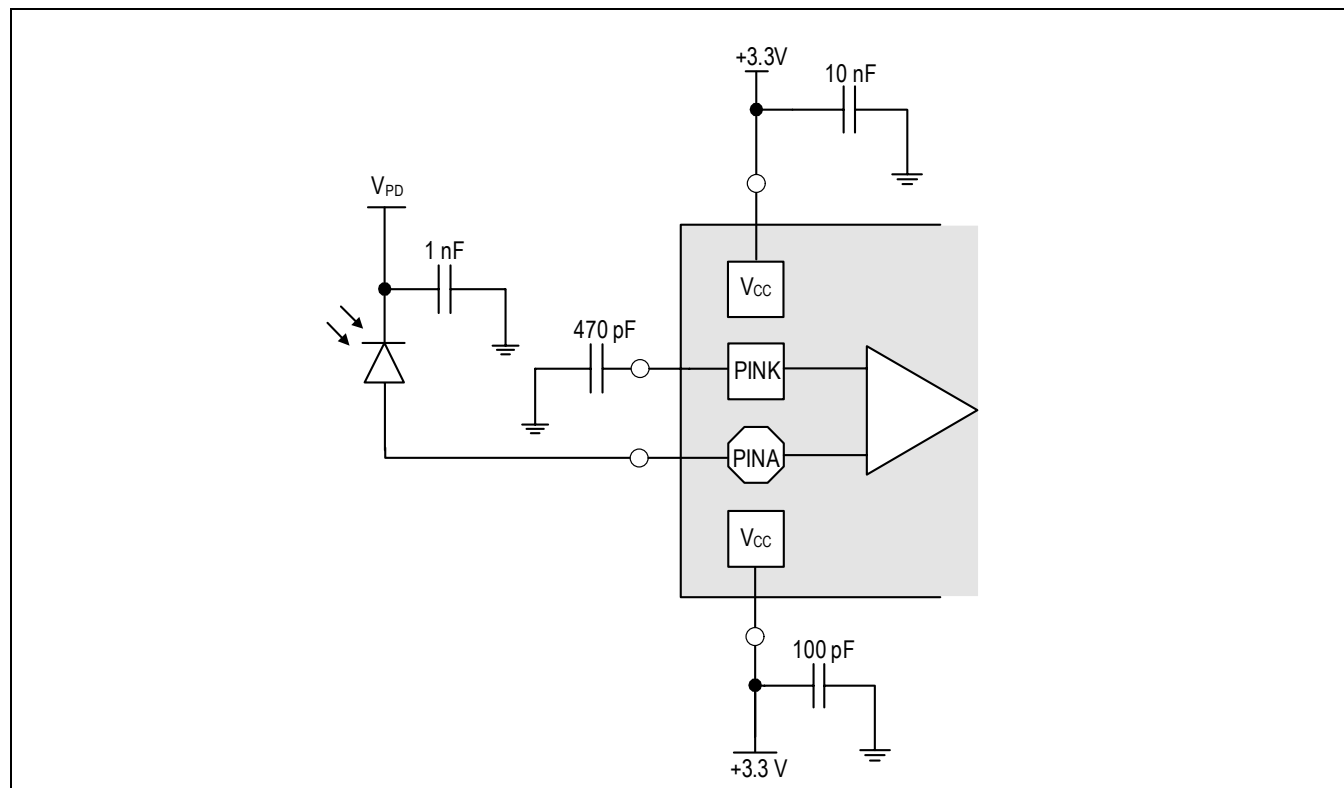
Figure 4-1. Typical Applications Circuit



4.2 Alternative Input Arrangement

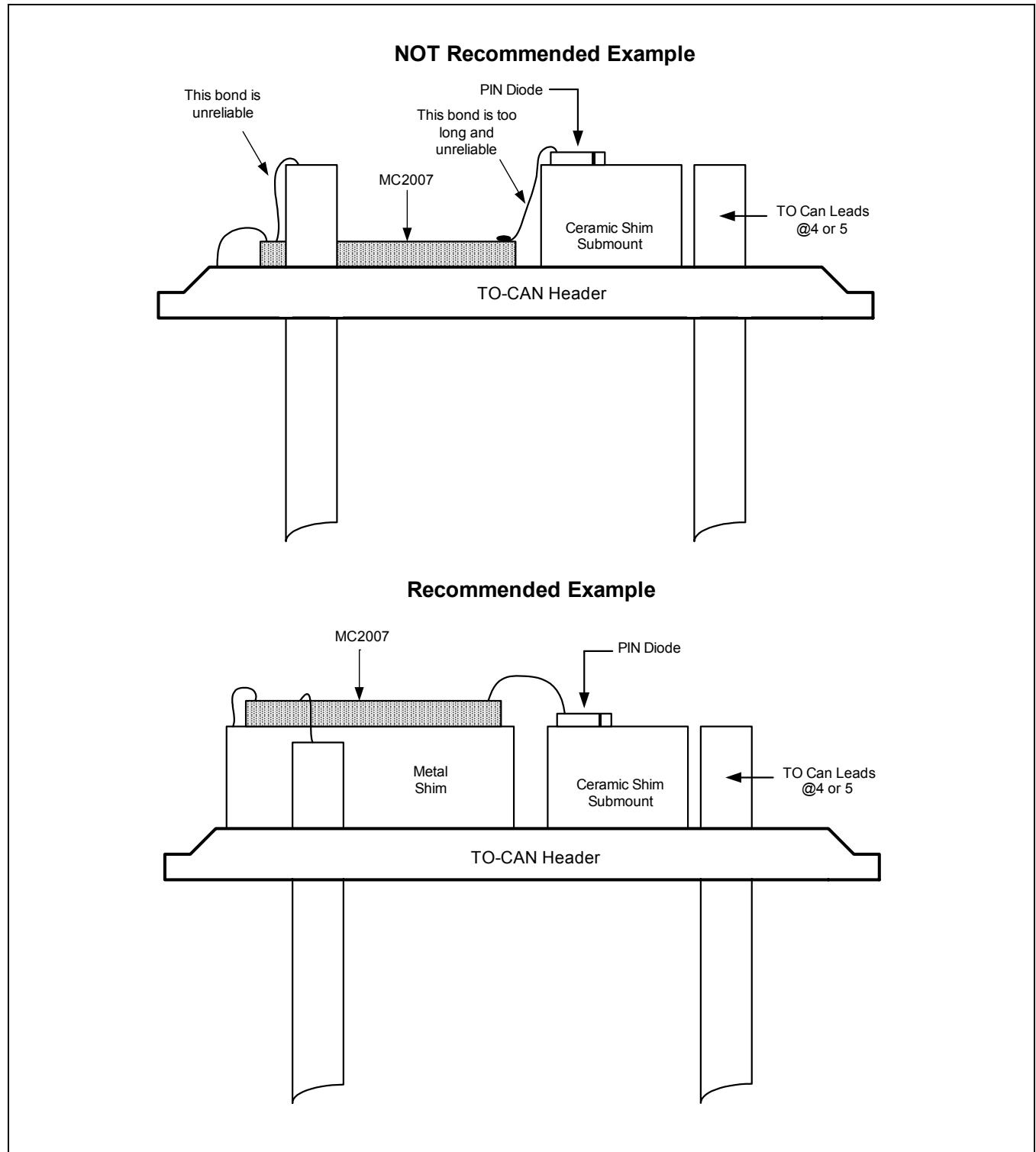
An alternative arrangement can be used to connect the photodiode, with the photodiode cathode being connected directly to V_{CC} (see Figure 4-2). This requires two decoupling capacitors, one connecting V_{CC} to ground, and the other from PIN K to ground. This arrangement reverse biases the photodiode more, but will have inferior low frequency noise performance.

Figure 4-2. Alternative Application Arrangement



4.3 TO-Can Assembly Recommendations

Figure 4-3. Typical TO-Can Assembly



4.3.1 Assembly

The MC2007 is designed to work with a wirebond inductance of $1 \text{ nH} \pm 0.25 \text{ nH}$. Many existing TO-Can configurations will not allow wirebond lengths that short, since the PIN diode submount and the TIA die are more than 1 mm away in the vertical direction, due to the need to have the PIN diode in the correct focal plane. This can be remedied by raising up the TIA die with a conductive metal shim. This will effectively reduce the bond wire length. Refer to [Figure 4-3](#) above for details.

Mindspeed recommends ball bonding with a 1 mil (25.4 μm) gold wire. For performance reasons the PINA pad is smaller than the others and also has less via material connected to it. It therefore requires more care in setting of the bonding parameters. **For the same reason PINA has no ESD protection.**

In addition, please refer to the Mindspeed Product Bulletin (document number 0201X-PBD-002). Care must be taken when selecting chip capacitors, since they must have good low ESR characteristics up to several hundred MHz. It is also important that the termination materials of the capacitor be compatible with the attach method used.

For example, Tin/Lead (Pb/Sn) solder finish capacitors are incompatible with silver-filled epoxies. Palladium/Silver (Pd/Ag) terminations are compatible with silver filled epoxies. Solder can be used only if the substrate thick-film inks are compatible with Pb/Sn solders.

4.3.2 Recommended Assembly Procedures

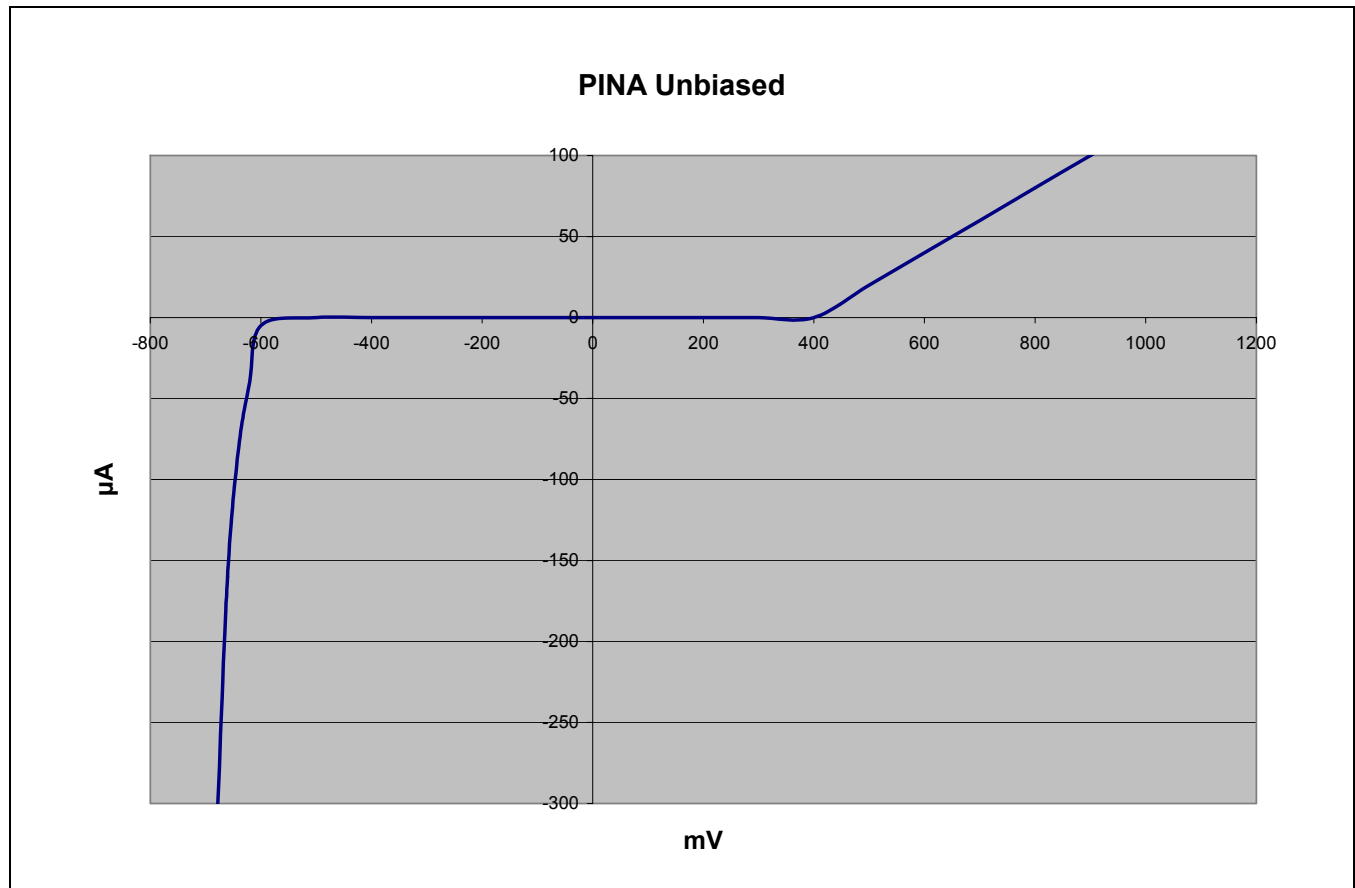
For ESD protection the following steps are recommended for TO-Can assembly:

- a. Ensure good humidity control in the environment (to help minimize ESD).
- b. Consider using additional ionization of the air (also helps minimize ESD).
- c. As a minimum, it is best to ensure that the body of the TO-can header or the ground lead of the header is grounded through the wire-bonding fixture for the following steps. The best solution also ensures that the V_{CC} lead of the TO-Can is also grounded. When this is done and the procedure below is followed, any positive charge on the wire bonder when bonding to PINA (the very last bond placed) will have the PD acting as an ESD diode into PinK of the device. Internally, PinK has an ESD diode between it and VCC that will turn on if V_{CC} is at ground minimizing the ESD event at PINA.
- d. The wire bonder (including the spool, clamp, etc.) must also be grounded.
 1. Wire-bond the ground pad(s) of the die first.
 2. Then wire bond the V_{CC} pad to the TO-Can lead.
 3. Then wire bond any other pads going to the TO-Can leads (such as DOUT, DOUT and possibly MON).
 4. Next wire-bond any capacitors inside the TO-Can.
 5. Inside the TO-Can, wire bond PINK.
 6. The final step is to wire bond PINA.

4.4 TIA Use with Externally Biased Detectors

In some applications, Mindspeed TIAs are used with detectors biased at a voltage greater than available from TIA PIN cathode supply. This works well if some basic cautions are observed. When turned off, the input to the TIA exhibits the following I/V characteristic:

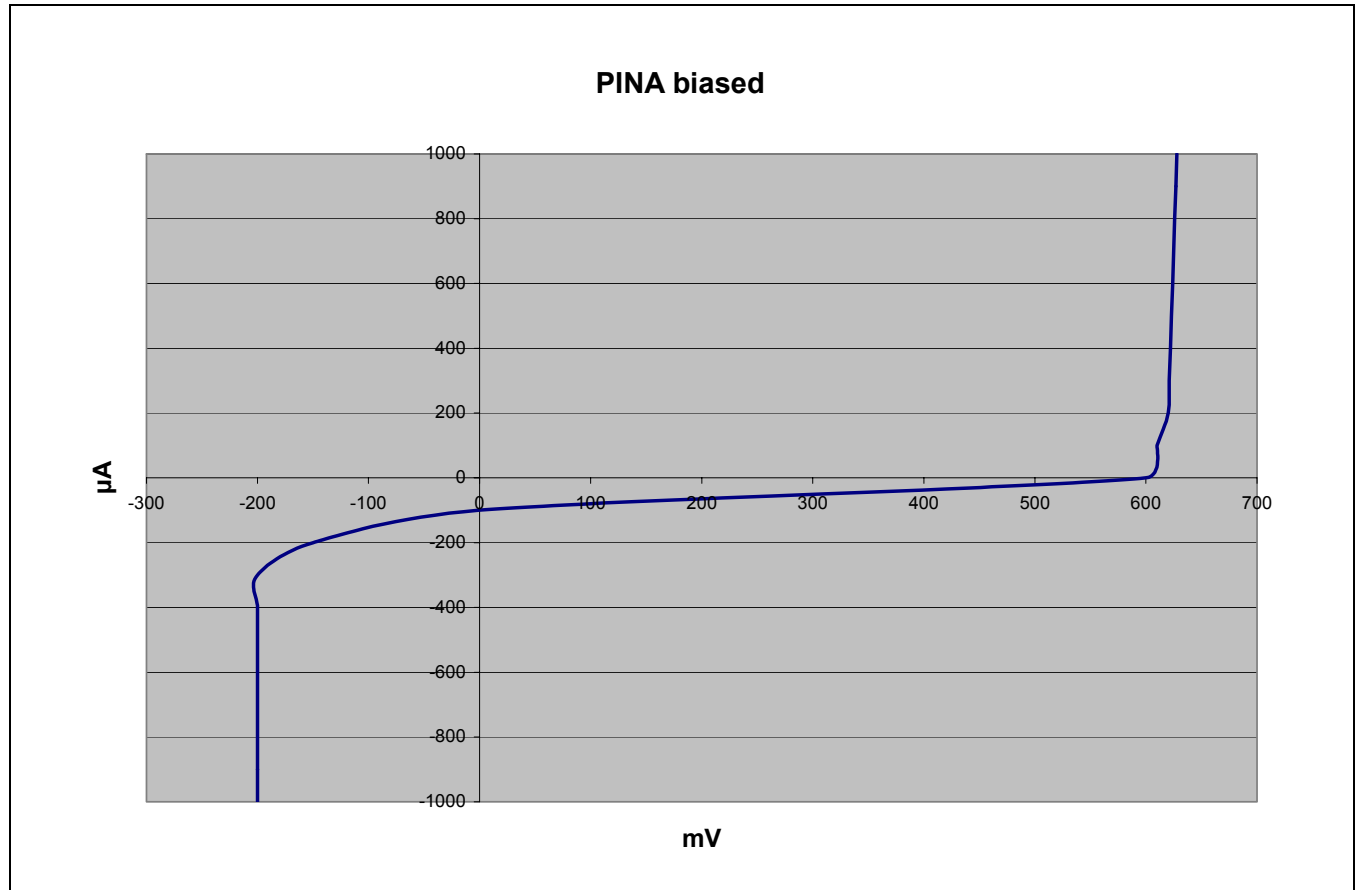
Figure 4-4. TIA Use with Externally Biased Detectors, Powered Off



The impedance of the input is relatively high and can be easily damaged by ESD or EOS.

After the TIA is turned on, the DC servo and AGC circuits attempt to null any input currents (up to the absolute maximum stated in [Table 1-1](#)) as shown by the I/V curve in [Figure 4-5](#).

Figure 4-5. TIA Use with Externally Biased Detectors, Powered On



It can be seen that any negative voltage below 200 mV is nulled and that any positive going voltage above the PINA standing voltage is nulled by the DC servo. The DC servo upper bandwidth varies from part to part, but is generally at least 10 kHz.

When externally biasing a detector such as an APD where the supply voltage of the APD exceeds that for PINA [Table 1-1](#), care should be taken to power up the TIA first and to keep the TIA powered up until after the power supply voltage of the APD is removed. Failure to do this with the TIA unpowered may result in damage to the input FET gate at PINA. In some cases the damage may be very subtle, in that nearly normal operation may be experienced with the damage causing slight reductions in bandwidth and corresponding reductions in input sensitivity.

4.4.1 Treatment of PINK

PINK still requires bypassing to ground with a high quality 220-1000 pF (470 pF recommended) capacitor, even with no other connection to it. The capacitor stabilizes the internal voltage regulator of the TIA.



5.0 Packaging Specification

5.1 Die Details

Table 5-1. Bare Die Information

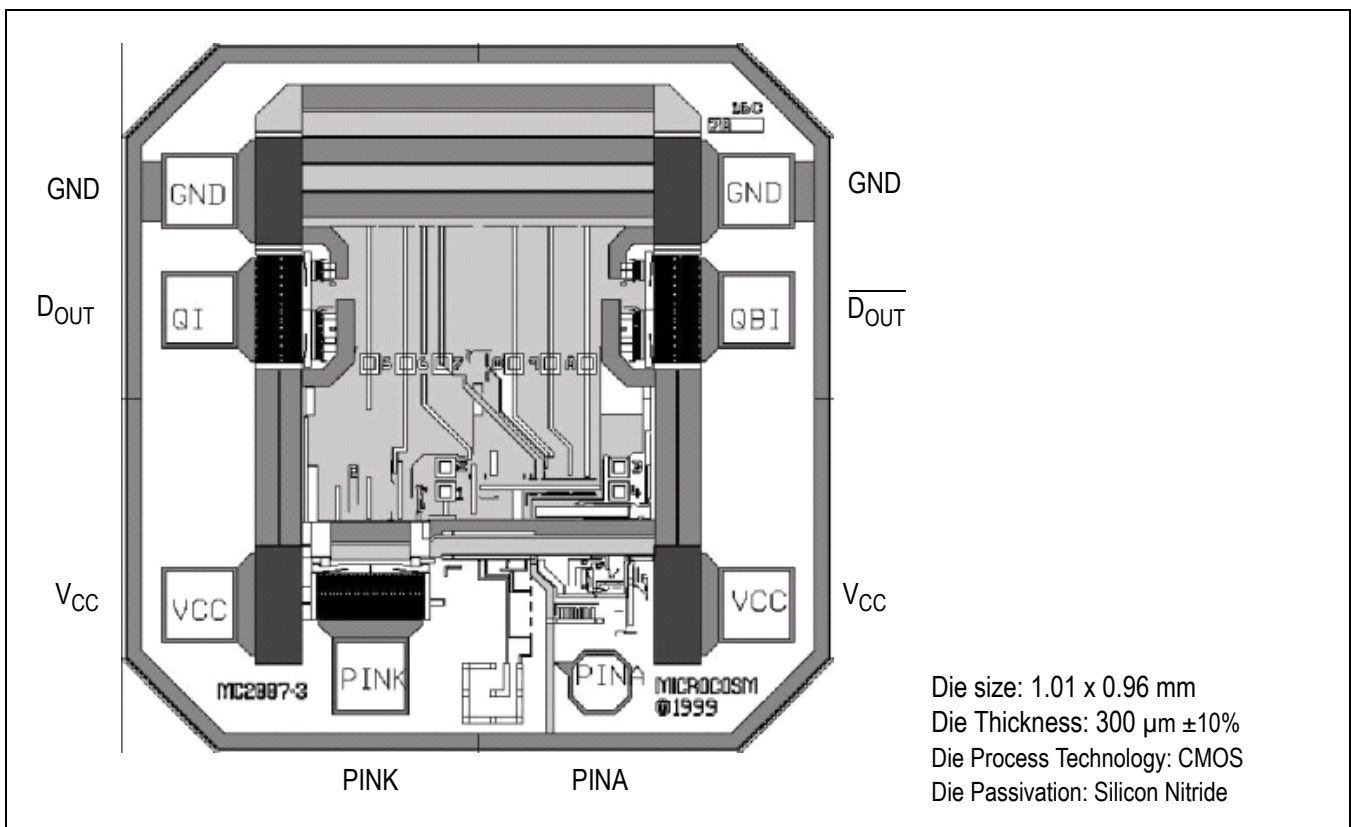


Table 5-2. Pad Coordinates

Pad No.	Description	X (μm)	Y (μm)	Pad No.	Description	X (μm)	Y (μm)
1	GND	-352.	216.7	5	PINA	153.95	-360.
2	D _{OUT}	-352.	111.7	6	V _{CC}	352.	-261.7
3	V _{CC}	-352.	-261.7	7	D _{OUT}	352.	111.7
4	PINK	-135.95	-352.	8	GND	352.	216.7

www.mindspeed.com

General Information:
Telephone: (949) 579-3000
Headquarters - Newport Beach
4000 MacArthur Blvd., East Tower
Newport Beach, CA 92660

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