M02040-14

3.3V Limiting Amplifier for Applications to 2.125 Gbps

The M02040-14 is an integrated high-gain limiting amplifier. Featuring PECL outputs, the M02040-14 is useable in applications to 2.125 Gbps. Full output swing is achieved even at minimum input sensitivity. The M02040-14 operates with a 3.3V supply.

$\overline{DC\_Servo}$ supports applications requiring instantaneous output response.

The M02040-14 also includes two analog RSSI outputs proportional to either the average or peak to peak input signal and a programmable signal-level detector allowing the user to set thresholds at which the logic outputs are enabled.

Other available solutions: M02050-14 3.3V Limiting Amplifier for Applications to 2.5 Gbps (PECL outputs)
        M02049-14 3.3V Limiting Amplifier for Applications to 4.3 Gbps (CML outputs)
        M02043-14 3.3V Limiting Amplifier for Applications to 4.3 Gbps (CML outputs)

1.25 Gbps and 4.25 Gbps SFP reference designs available on Mindspeed.com

Applications

- 1.0625 and 2.125 Gbps Fibre Channel
- 1.25 Gbps Ethernet
- 1.25 Gbps SDH/SONET

Features

- Operates with a 3.3V supply
- 2 mV typical input sensitivity at 1.25 Gbps
- PECL outputs
- Average Receive power monitor output ($RSSI_{AVG}$)
- Peak-to-peak Receive power monitor output ($RSSI_{PP}$)
- On-chip DC offset cancellation circuit
- Offset cancellation circuit can be disabled for Burst mode applications
- Low power (170 mW)
- Output Jam function
- 16-pin 3x3 mm QFN package

## Typical Applications Diagram
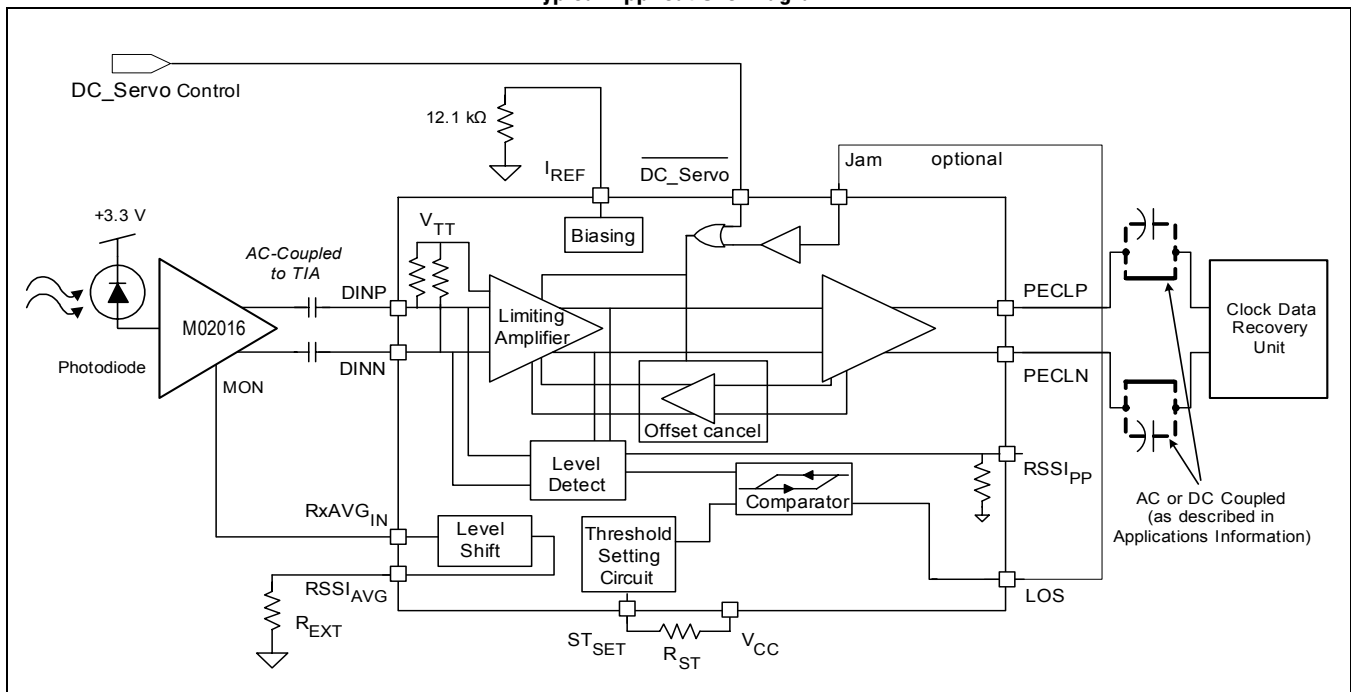
Ordering Information

| Part Number	Package	Operating Temperature
M02040-14 *	M02040-14 in QFN16 package	−40 °C to 85 °C
M02040-14EVM	Evaluation board with M02040-14	−40 °C to 85 °C
* The letter "G" designator after the part number indicates that the device is RoHS-compliant. Refer to www.mindspeed.com for additional information.		

Revision History

Revision	Level	Date	ASIC Revision	Description
H	Final	December 2005	-14	Clarify comments on the use of the $\overline{\text{DC\_Servo}}$ pin in the pin definitions and applications information.
G	Final	August 2005	-14	Correct Jam connection in block diagram and typical applications figures. Correct I_{REF} figure (reference current generation).
F	Final	June 2005	-14	In the DC specifications, update $R_{IN}DIFF$ and RSSIavg; added note 1; moved RSSIavg from ac specifications. In the ac specifications update $V_{IN(MIN)}$, V_{LOS}, DJ and tr/tf; add specifications for LOS assert and deassert. Updated R_{ST} values and the typical LOS curve (Figure 4-3 - Figure 4-5). Added typical hysteresis curve (Figure 4-6).
E	Preliminary	March 2005	-14	Update the DC specification V_{OH}. Update the ac specifications $V_{IN(MIN)}$, v_n, T_{LOS_ON}, and T_{LOS_OFF}. Corrected the EVM ordering number.
D	Preliminary	December 2004	-14	Update the DC specifications $R_{IN}DIFF$ and V_{IH}. Update R_{ST} values, update RSSI information. Remove peaking circuit applications information as this is not necessary for the -14 revision. Note that the -14 is for 3.3V only.

Typical Eye Diagram

10 mV$_{PP}$ differential input
1.25 Gbps

160 mV/div
140 ps/div
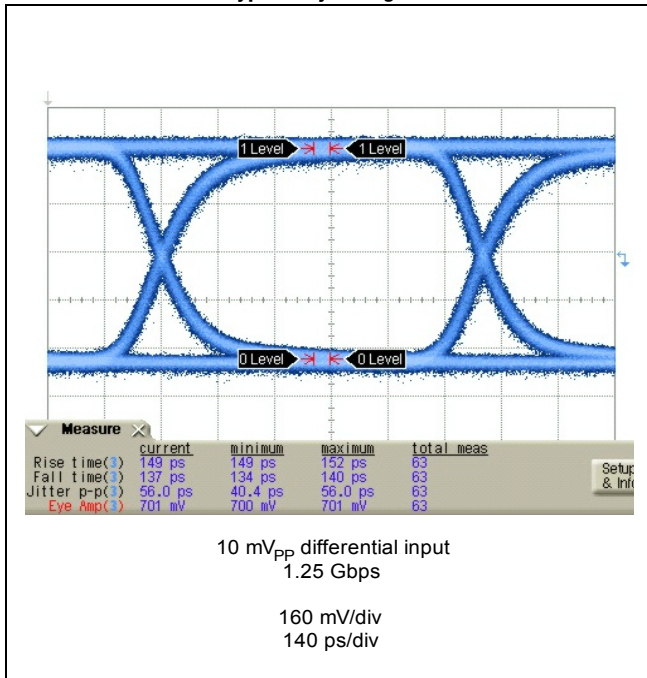
Pin Configuration
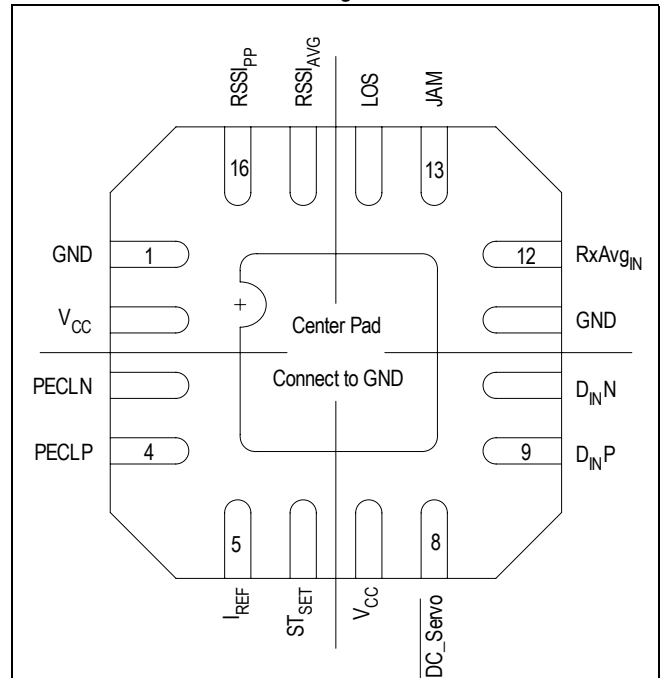
1.0 Product Specification

1.1 Absolute Maximum Ratings

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

NOTE: The package bottom should be adequately grounded to ensure correct thermal performance, and it is recommended that vias are inserted through to a lower ground plane.

Table 1-1. *Absolute Maximum Ratings*

Symbol	Parameter	Rating	Units
V_{CC}	Power supply voltage (V_{CC}-GND)	-0.5 to +4	V
T_{STG}	Storage temperature	-65 to +150	°C
PECLP, PECLN	PECL Output pins voltage	V_{CC} - 2 to V_{CC} + 0.4	V
I(PECLP), I(PECLN)	PECL Output pins maximum continuous current (delivered to load)	30	mA
|DINP - DINN|	Data input pins differential voltage	0.80	V
DINP, DINN	Data input pins voltage meeting |DINP - DINN| requirement	GND to V_{CC} + 0.4	V
ST_{SET}	Signal detect threshold setting pin voltage	GND to V_{CC} + 0.4	V
JAM	Output enable pin voltage	GND to V_{CC} + 0.4	V
LOS	Status Output pins voltage	GND to V_{CC} + 0.4	V
$\overline{DC\_Servo}$	DC_Servo disable input pin voltage	GND to V_{CC} + 0.4	V
I_{REF}	Current into Reference input	+0 to -120	µA
I($RSSI_{AVG}$)	Current into RSSIavg input	+0 to -3	mA
$RSSI_{PP}$	$RSSI_{PP}$ pin voltage	GND to +3.6	V
I(LOS)	Current into Loss of Signal pin	+3000 to -100	µA

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1.2 Recommended Operating Conditions

Table 1-2.   Recommended Operating Conditions

Parameter	Rating	Units
Power supply: (V_{CC}-GND)	+3.3V ± 7.5%	V
Junction temperature	-40 to +110	°C
Operating ambient	-40 to +85	°C

1.3 DC Characteristics

V_{CC} = +3.3V ± 7.5%, T_A = -40°C to +85°C, unless otherwise noted.
Typical specifications are for V_{CC} = 3.3V, T_A = 25°C, unless otherwise noted.

Table 1-3.   DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current	Outputs terminated into 50 Ω to V_{CC} (includes PECL load)	–	52	61	mA
$V_{OUTLpecl}$	PECL Output Low Voltage [1] (PECLP, PECLN)	Single ended; 50 Ω load to V_{CC}-2V	V_{CC}-1.81	V_{CC}-1.71	V_{CC}-1.62	V
$V_{OUTHpecl}$	PECL Output High Voltage [1] (PECLP, PECLN)	Single ended; 50 Ω load to V_{CC}-2V	V_{CC}-1.025	V_{CC}-0.952	V_{CC}-0.88	V
$R_{IN}DIFF$	Differential Input Resistance	Measured between DINP and DINN	90	110	130	Ω
V_{OH_CMOS}	LOS Output High Voltage	External 4.7-10 kΩ pull up to V_{CC}	2.75	V_{CC}	–	V
V_{OL_CMOS}	LOS Output Low Voltage	External 4.7-10 kΩ pull up to V_{CC}	0	–	0.4	V
V_{IH}	Logic Input High Voltage JAM, $\overline{DC\_Servo}$		2.7	–	V_{CC}	V
V_{IL}	Logic Input Low Voltage JAM, $\overline{DC\_Servo}$		–	–	0.8	V
RSSIavg	Average received signal strength indicator range	± 15% accuracy	5	–	2000	µA

Notes:
1. Limits apply between 0°C to +85°C. Below 0 °C the minimum decreases by up to 40 mV.

1.4 AC Characteristics

V_{CC} = +3.3V ± 7.5%, T_A = -40°C to +85°C, input bit rate = 1.25 Gbps 2^{23}-1 PRBS unless otherwise noted. Typical specifications are for V_{CC} = 3.3V, T_A = 25°C, unless otherwise noted.

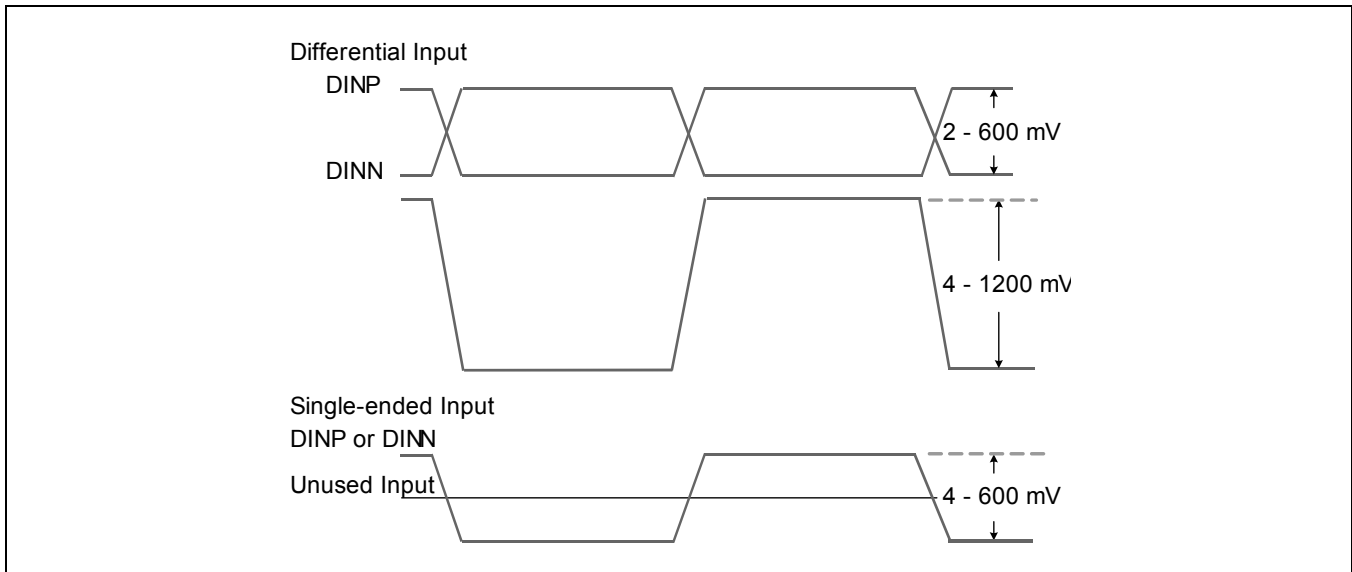*Table 1-4.   AC Characteristics*

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN(MIN)}$	Differential Input Sensitivity	1.25 Gbps, BER < 10^{-12}	–	2	2.75	mV
		2.125 Gbps, BER < 10^{-12}	–	3.5	5	mV
$V_{I(MAX)}$	Input Overload	BER < 10^{-12}, differential input 1.25 Gbps	1200	–	–	mV
		BER < 10^{-12}, single-ended input, 1.25 Gbps	600	–	–	mV
v_n	RMS Input Referred Noise		–	140	–	μV_{RMS}
RSSIpp	Peak-to-peak received signal strength indicator range		4	–	100	mV
BW_{LF}	Small-Signal –3dB Low Frequency Cutoff	Excluding AC coupling capacitors	–	25	–	kHz
DJ	Deterministic Jitter (includes DCD)	K28.5 pattern at 1.25 Gbps, 10 mV_{PP} input	–	14	60	ps
RJ	Random Jitter	10 mV_{PP} input	–	5		ps_{RMS}
t_r / t_f	Data Output Rise and Fall Times	20% to 80%; outputs terminated into 50 Ω; 10 mV_{PP} input	–	145	180	ps
V_{LOS}	LOS Programmable Range	Differential inputs	5	–	55	mV
HYS	Signal Detect Hysteresis	electrical; across LOS programmable range	2	3.5	5.5	dB
$ASSERT_{LOW}$	Low Input LOS Assert threshold	R_{ST} = 7.50 kΩ, differential input	3.5	4.9	–	mV_{PP}
$DEASSERT_{LOW}$	Low Input LOS De-Assert threshold	R_{ST} = 7.50 kΩ, differential input	–	7.8	11.3	mV_{PP}
$ASSERT_{MED}$	Medium Input LOS Assert threshold	R_{ST} = 6.81 kΩ, differential input	8.4	11.7	–	mV_{PP}
$DEASSERT_{MED}$	Medium Input LOS De-Assert threshold	R_{ST} = 6.81 kΩ, differential input	–	17.0	24.6	mV_{PP}
$ASSERT_{HI}$	High Input LOS Assert threshold	R_{ST} = 6.19 kΩ, differential input	16.6	23.2	–	mV_{PP}
$DEASSERT_{HI}$	High Input LOS De-Assert threshold	R_{ST} = 6.19 kΩ, differential input	–	33.4	48.4	mV_{PP}
T_{LOS_ON}	Time from LOS state until LOS output is asserted [1]	LOS assert time after 1 V_{PP} input signal is turned off; signal detect level set to 10 mV	2.3	–	80	μs
T_{LOS_OFF}	Time from non-LOS state until LOS is deasserted [2]	LOS deassert time after input crosses signal detect level; signal detect set to 10 mV with applied input signal of 20 mV_{PP}	2.3	–	80	μs

Notes:
1. With V_{IN_DIFF} = 1 V_{PP}, typical times decrease as V_{IN_DIFF} decreases.
2. With V_{IN_DIFF} = 20 mVpp, typical times decrease as V_{IN_DIFF} increases.

Figure 1-1.   Data Input Requirements

Differential Input
DINP
DINN
2 - 600 mV
4 - 1200 mV

Single-ended Input
DINP or DINN
Unused Input
4 - 600 mV

NOTE: For single-ended input connections.
When connecting to the used input with AC-coupling, the unused input should be AC-coupled through 50Ω to the supply voltage of the TIA;

When connecting to the used input with DC-coupling, the unused input should be DC-coupled through 50Ω to a voltage equal to the common mode level of the used input.

1.5   Typical Eye Diagrams

Figure 1-2.   M02040 1.25 Gbps

10 mV$_{PP}$ differential input
1.25 Gbps

160 mV/div
140 ps/div
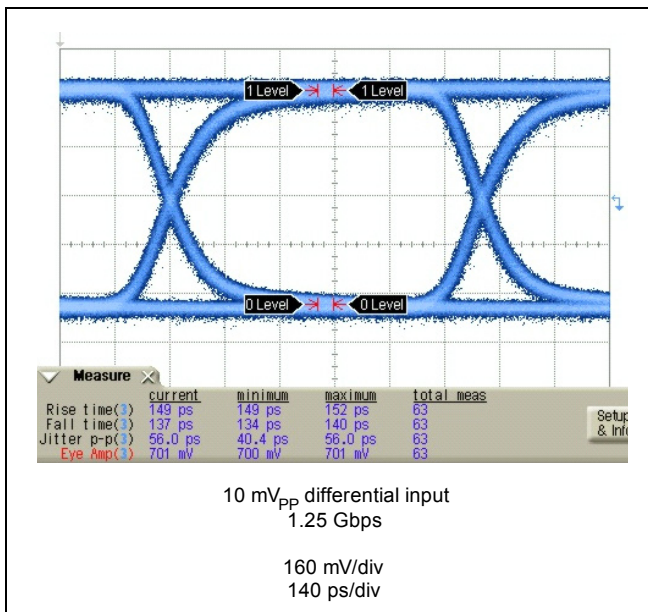
Figure 1-3.   M02040 2.125 Gbps
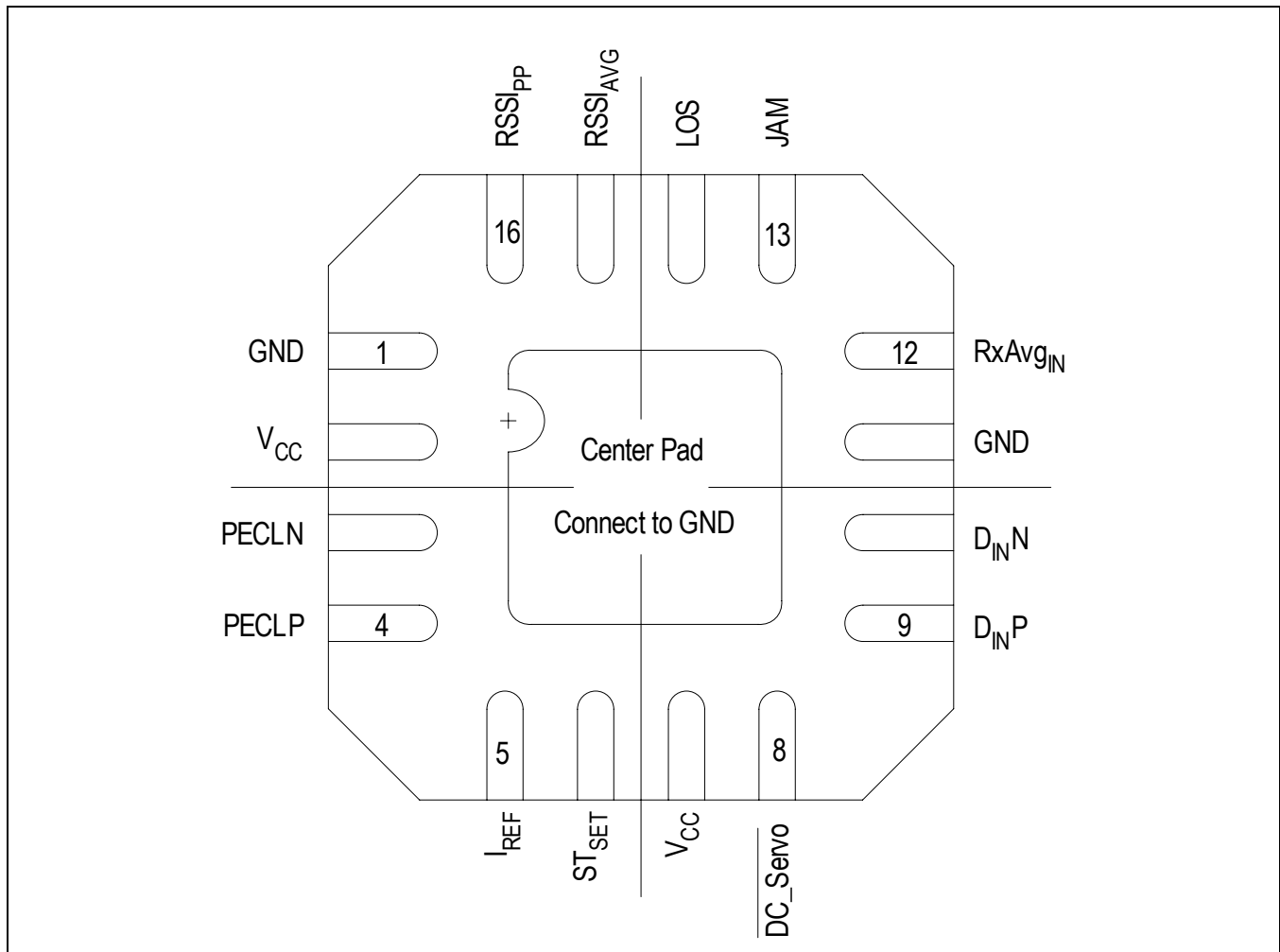

10 mV$_{PP}$ differential input
2.125 Gbps

160 mV/div
80 ps/div
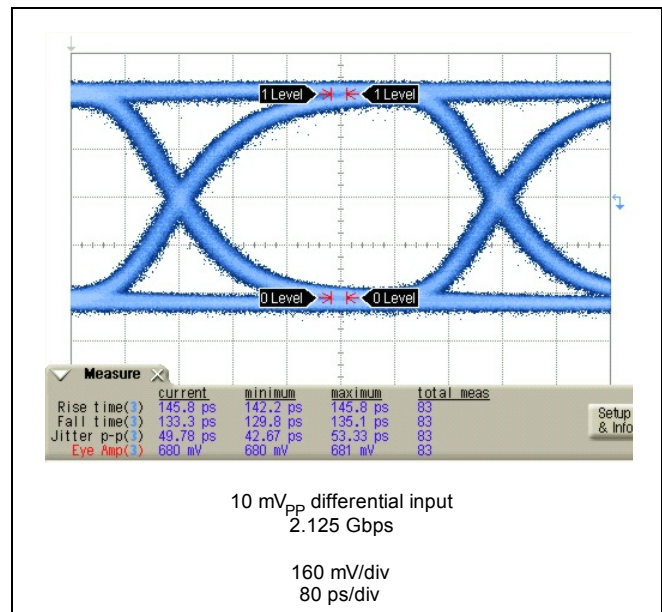
2.0   Pin Definitions

Table 2-1.   Pin Descriptions

QFN Pin#	Name	Function
1	GND	Ground.
2	V_{CC}	Power supply. Both V_{CC} pins must be connected to +3.3V.
3	PECLN	Inverting data output (PECL).
4	PECLP	Non-inverting data output (PECL).
5	I_{REF}	Internal LOS reference current. Must be connected to ground through a 12.1 kΩ 1% resistor.
6	ST_{SET}	Loss of signal threshold setting input. Connect a 1% resistor between this pin and V_{CC} to set loss of signal threshold.
7	V_{CC}	Power supply. Both V_{CC} pins must be connected to +3.3V.
8	$\overline{DC\_Servo}$	DC Servo disable. When high, the DC servo circuit is disabled, allowing the limiting amplifier to be used with data that has changes quickly in amplitude and phase. Also useful for data containing significant low-speed or DC signals. When low or floating, DC servo is enabled. Internal 80 kΩ resistor to ground. It is recommended that this pin be grounded if the DC servo is to be continuously enabled.
9	DINP	Non-inverting data input. Internally terminated with 50 Ω to V_{TT} (see Figure 3-2).
10	DINN	Inverting data input. Internally terminated with 50 Ω to V_{TT} (see Figure 3-2).
11	GND	Ground.
12	$RxAVG_{IN}$	Average power monitor input. Connect to monitor output of TIAs that produce a current (sink) mirror replica of the photodiode current. Leave floating if not used.
13	JAM	Output disable. When high, data outputs are disabled (with non-inverting output held high and inverting output held low). Connect to LOS output to disable outputs with loss of signal. Outputs are enabled when JAM is low or floating. Internal 150 kΩ resistor to ground.
14	LOS	Loss of signal output. Goes high when input signal falls below threshold set by ST_{SET}. Open collector TTL with internal 80 kΩ pull-up resistor to V_{CC}.
15	$RSSI_{AVG}$	Receiver average input power monitor. Provides a current source mirror of the current at $RxAVG_{IN}$. Connect a resistor to ground to set the full scale voltage to the desired level at maximum average input power.
16	$RSSI_{PP}$	Receiver peak-to-peak input voltage monitor. Provides a DC voltage (ground referenced) proportional to the peak-to-peak input voltage swing.
17	Center Pad	Ground to PCB for thermal dissipation.

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Figure 2-1.   M02040-14 Pinout

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3.0 Functional Description

3.1 Overview

The M02040-14 is a high-gain limiting amplifier for applications up to 2.125 Gbps and incorporates a limiting amplifier, an input signal level detection circuit and also a fully integrated DC-offset cancellation loop that does not require any external components. The M02040-14 features PECL data outputs.

The M02040-14 provides the user with the flexibility to set the signal detect threshold. Optional output buffer disable (squelch/jam) can be implemented using the JAM input.

Figure 3-1.   M02040-14 Block Diagram

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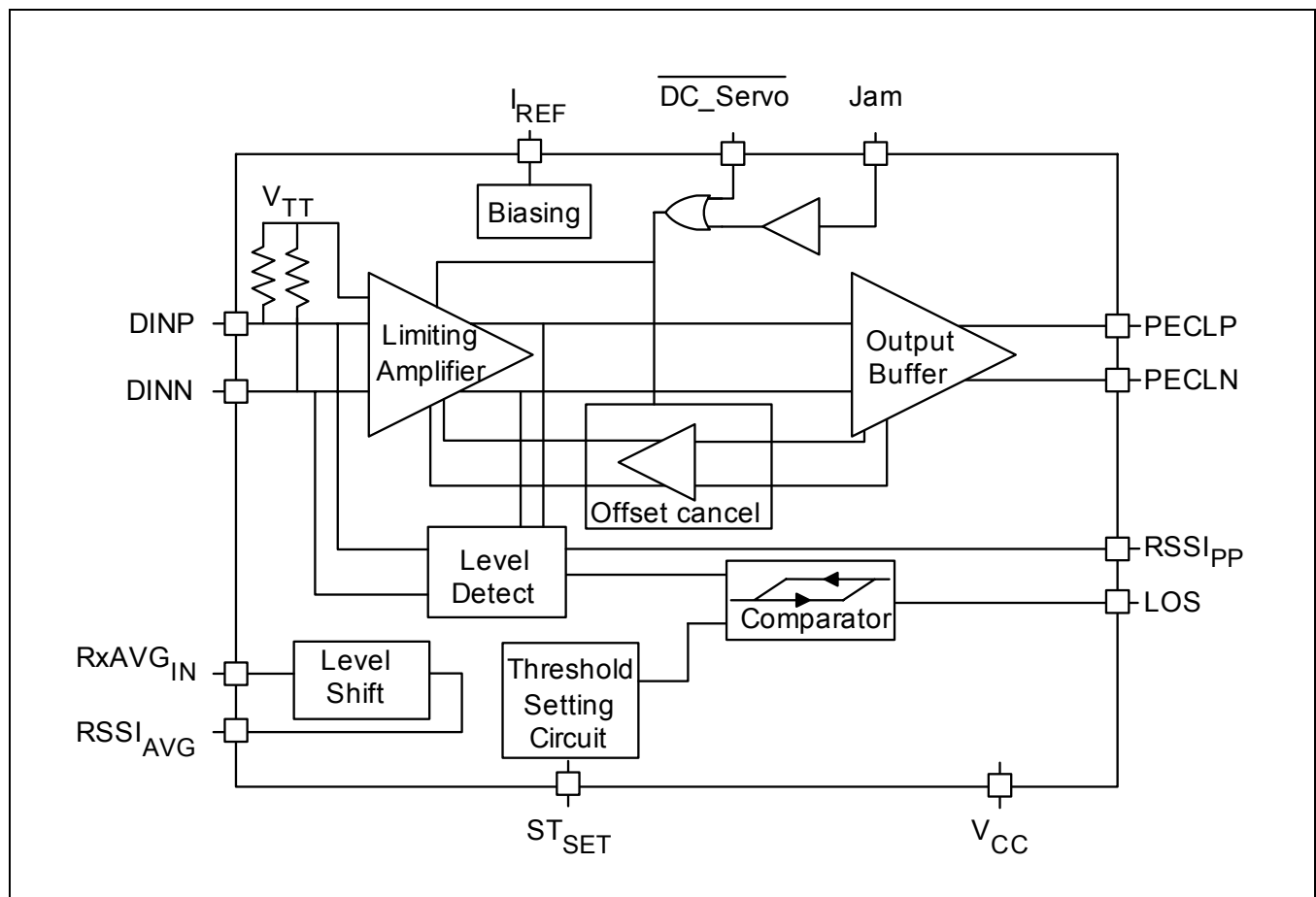
3.2   Features

- Operates with a 3.3V supply
- 2 mV typical input sensitivity at 1.25 Gbps
- PECL outputs
- Average Receive power monitor output (RSSI$_{AVG}$)
- Peak-to-peak Receive power monitor output (RSSI$_{PP}$)
- On-chip DC offset cancellation circuit
- Offset cancellation circuit can be disabled for Burst mode applications
- Low power (170 mW)
- Output Jam function
- 16-pin 3x3 mm QFN package

3.3   General Description

The M02040-14 is an integrated high-gain limiting amplifier. Featuring PECL outputs, the M02040-14 is useable in applications to 2.125 Gbps. Full output swing is achieved even at minimum input sensitivity. The M02040-14 operates with a 3.3V supply.

$\overline{\text{DC\_Servo}}$ supports applications requiring instantaneous output response.

The M02040-14 also includes two analog RSSI outputs proportional to either the average or peak to peak input signal and a programmable signal-level detector allowing the user to set thresholds at which the logic outputs are enabled.

3.3.1   Inputs

The data inputs are internally connected to V_{TT} via 50 Ω resistors, and generally need to be AC coupled. Referring to Figure 3-2, the nominal V_{TT} voltage is 2.85V because of the internal resistor divider to V_{CC}, which means this is the DC potential on the data inputs. See the applications information section for further details on choosing the AC-coupling capacitor.

Figure 3-2.   CML Data Inputs
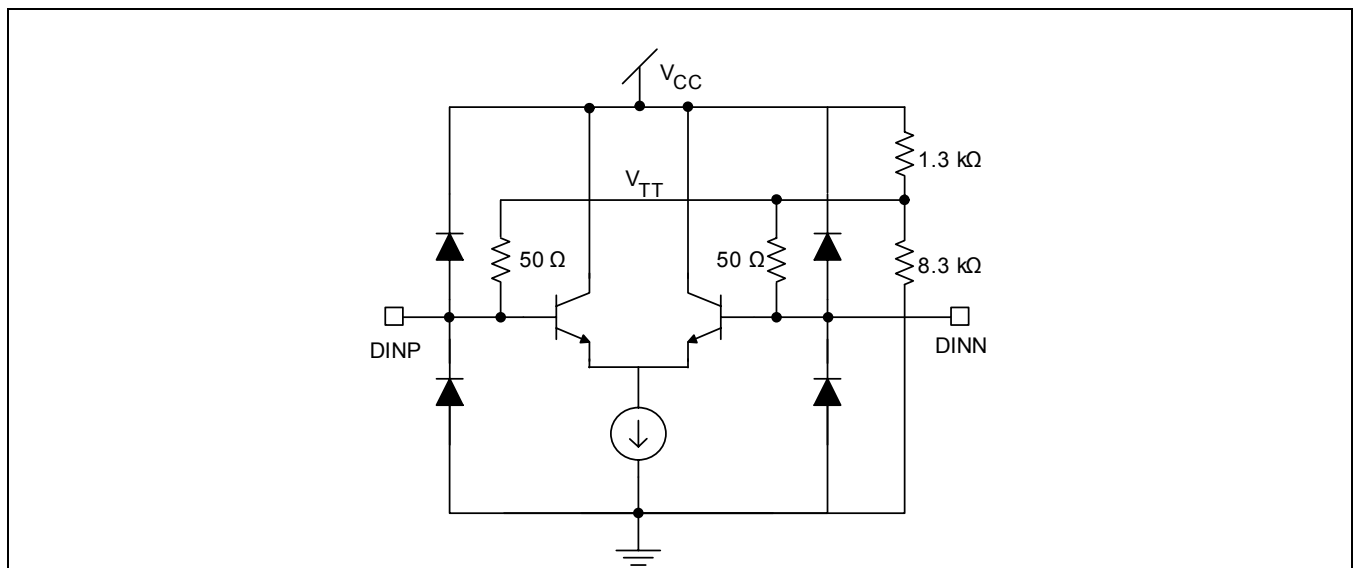
3.3.2 DC Offset Compensation

The M02040-14 contain an internal DC autozero circuit that can remove the effect of DC offsets without using external components. This circuit is configured such that the feedback is effective only at frequencies well below the lowest frequency of interest. The low frequency cut off is typically 25 kHz.

3.3.3 Data Outputs

The M02040-14 features 100k/300k PECL compliant outputs as shown in Figure 3-3. The outputs may be terminated using any standard AC or DC-coupling PECL termination technique. AC-coupling is used in applications where the average DC content of the data is zero. The advantage of this approach is lower power consumption, no susceptibility to DC drive and compatibility with non-PECL interfaces.

Figure 3-3.   PECL Data Outputs
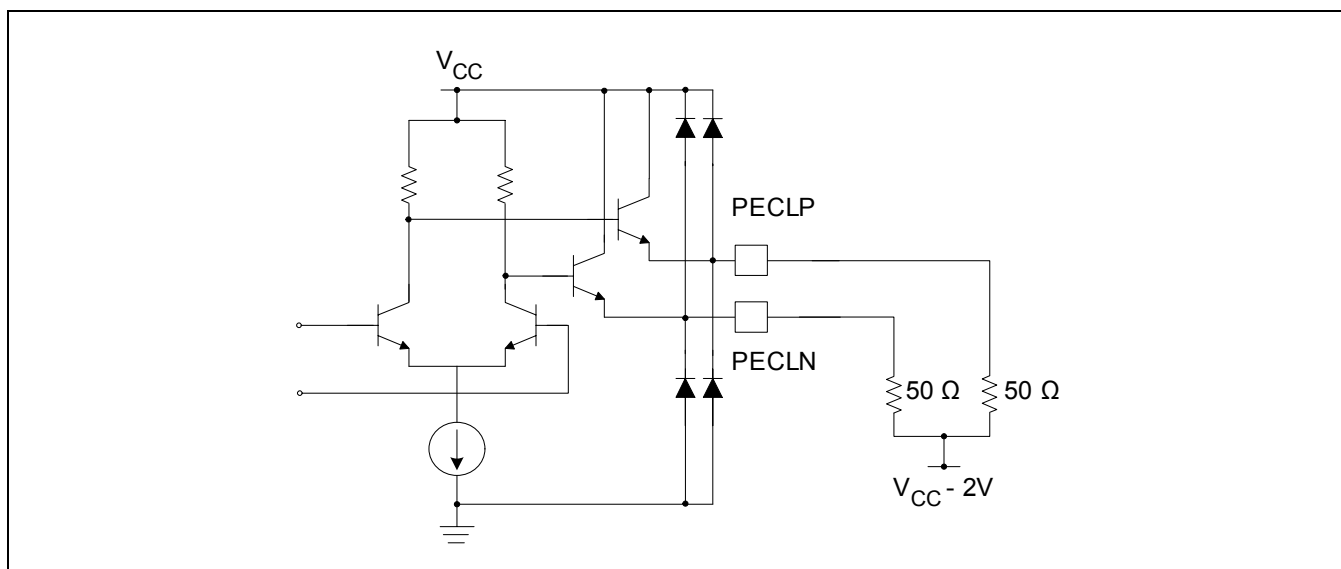
3.3.4   Loss of Signal (LOS)

The M02040-14 features input signal level detection over an extended range. Using an external resistor, R_{ST}, between pin ST_{SET} and V_{CC} (Figure 3-5) the user can program the input signal threshold. The signal detect status is indicated on the LOS output pin shown in Figure 3-4. The LOS signal is active when the signal is below the threshold value. The signal detection circuitry has the equivalent of 3.5 dB (typical) electrical hysteresis.

Figure 3-4.   LOS Output
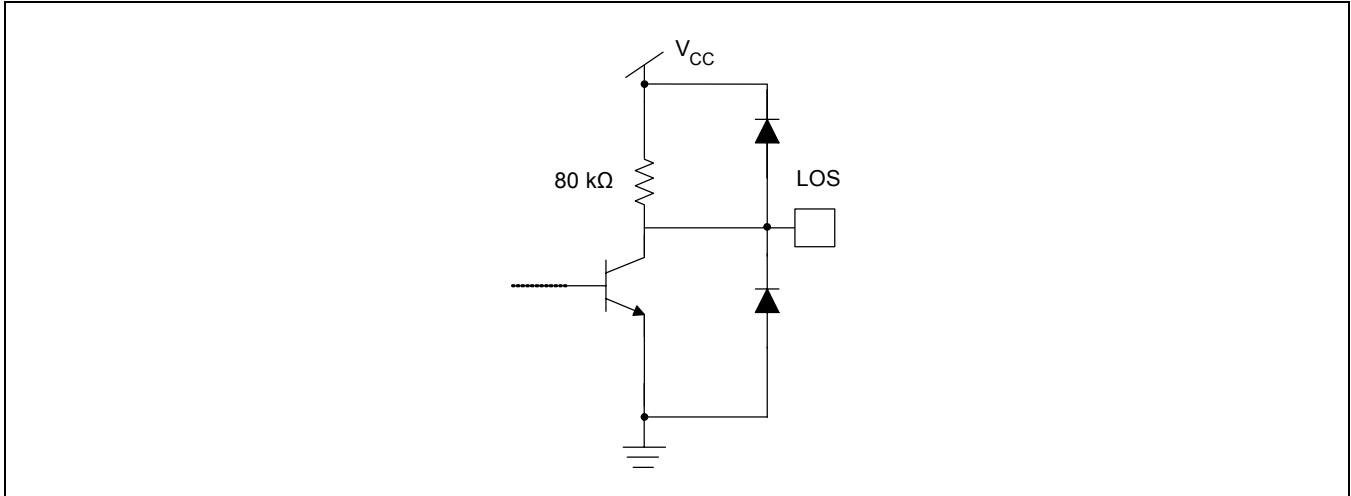
R_{ST} establishes a threshold voltage at the ST_{SET} pin as shown in Figure 3-5. Internally, the input signal level is monitored by the Level Detector (which also outputs the $RSSI_{PP}$ voltage). As described in the $RSSI_{PP}$ section, this voltage is proportional to the input signal peak to peak value. The voltage at ST_{SET} is internally compared to the signal level from the Level Detector. When the Level Detect voltage is less than $V_{(STSET)}$, LOS is asserted and will stay asserted until the input signal level increases by a predefined amount of hysteresis. When the input level increases by more than this hysteresis above $V_{(STSET)}$, LOS is deasserted. See the applications information section for the selection of R_{ST}.

Note that ST_{SET} can be left open if the loss of signal detector function is not required. In this case LOS would be low.

Figure 3-5. ST_{SET} Input

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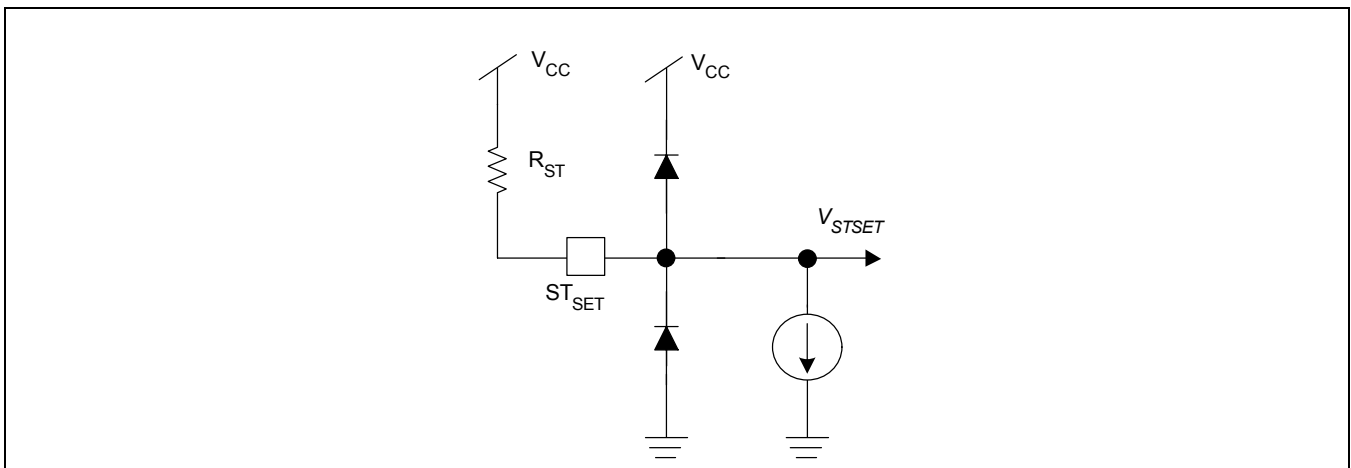
3.3.5 Peak to Peak Received Signal Strength Indicator (RSSI$_{PP}$)

The RSSI$_{PP}$ output voltage is logarithmically proportional to the peak to peak level of the input signal. It is not necessary to connect an external capacitor to this output. Internally, the RSSI voltage is compared with a user selectable reference to determine loss of signal as described in the previous section.
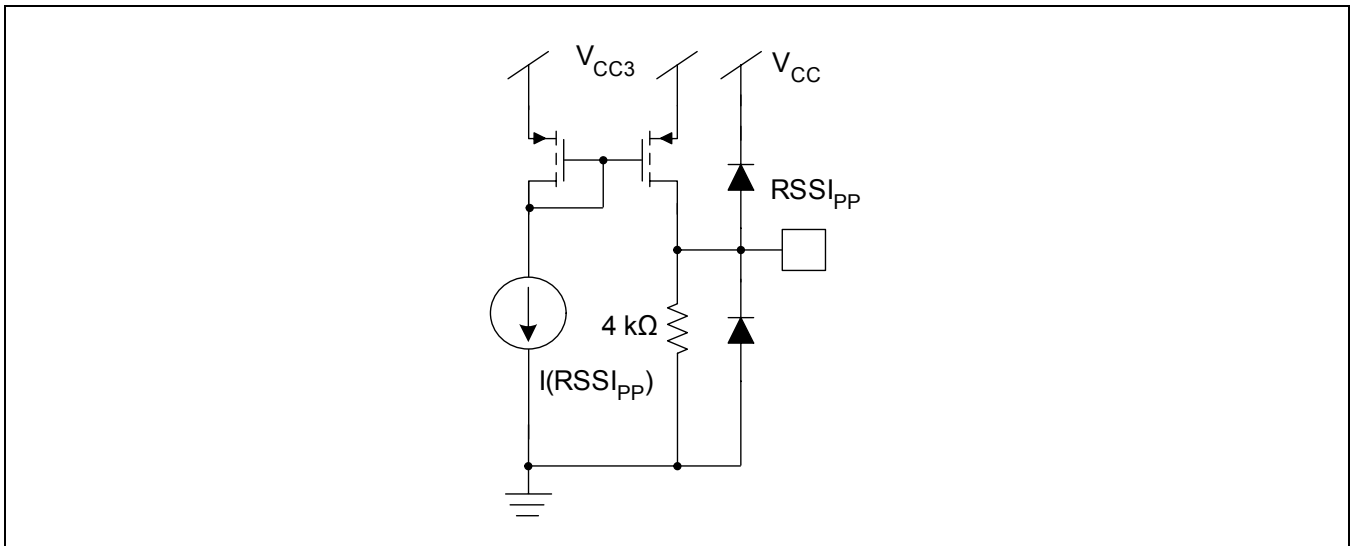
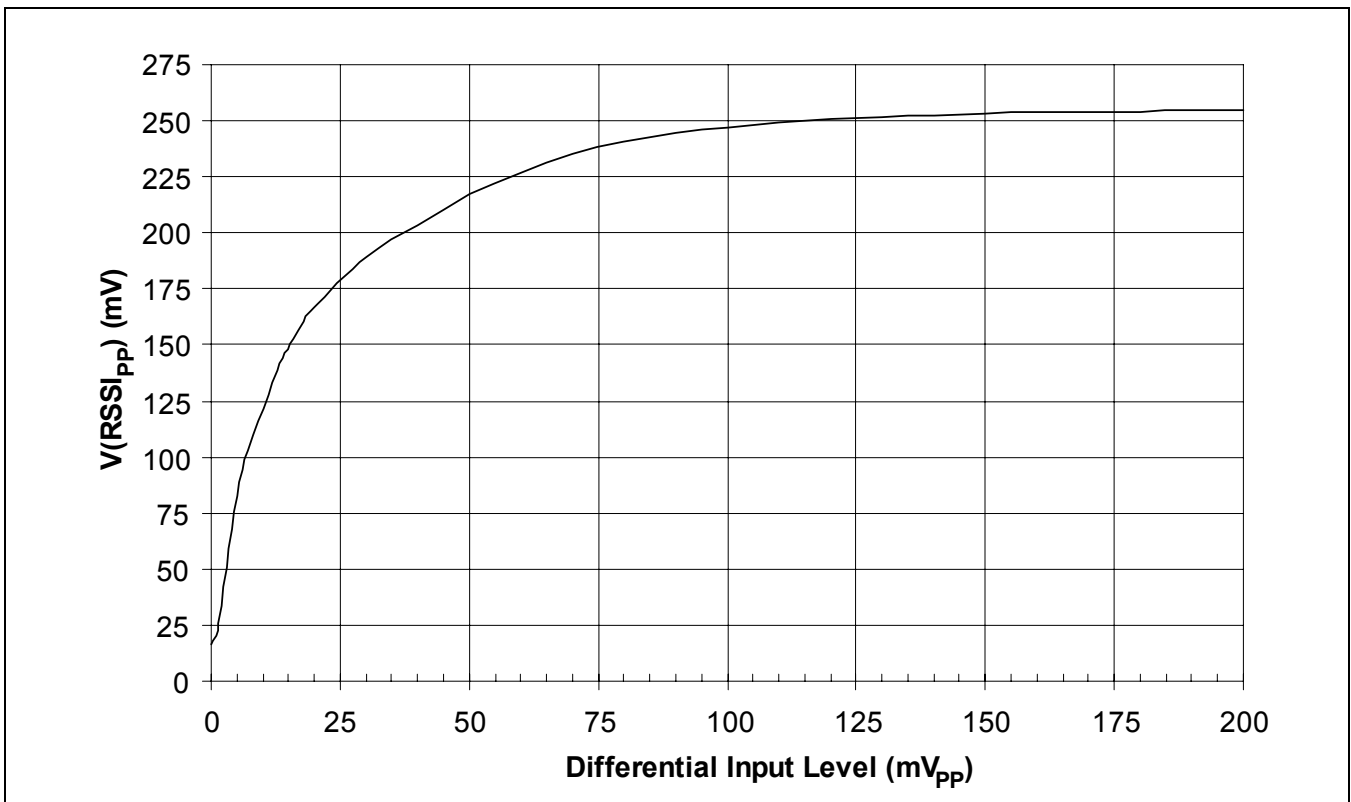*Figure 3-6.   RSSI$_{PP}$ Output*

Figure 3-7.   Typical RSSI$_{PP}$ Transfer Function

Figure 3-8.   Typical RSSI$_{PP}$ Transfer Function (Low Input Level Range)
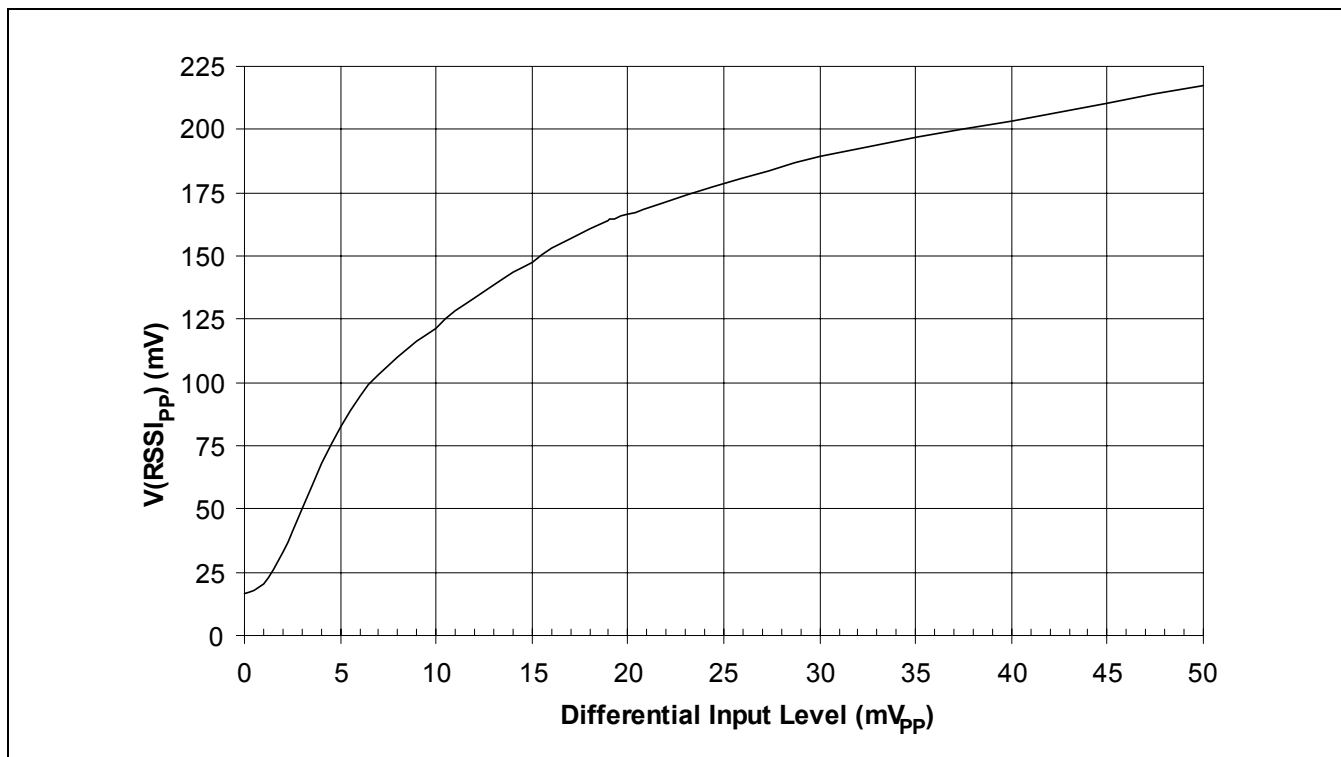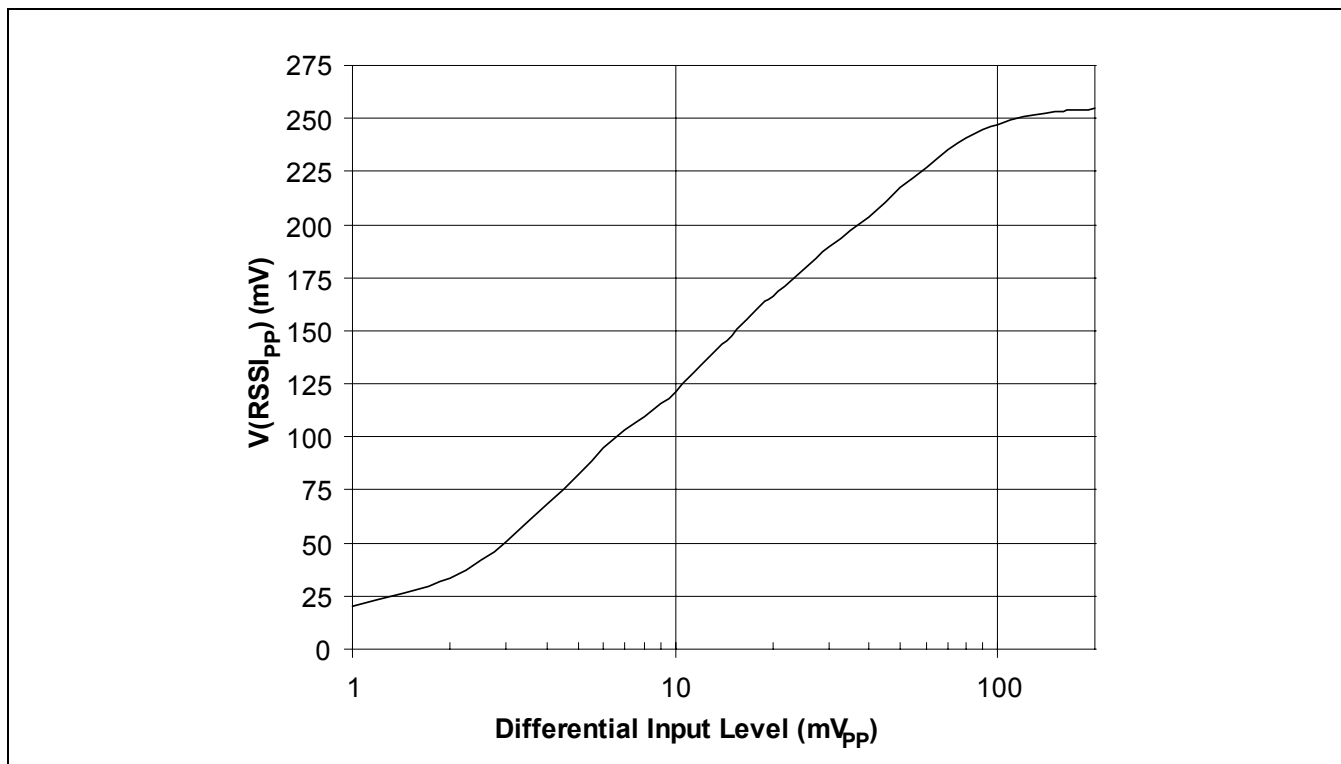

Figure 3-9.   Typical RSSI$_{PP}$ Transfer Function (Log Scale)
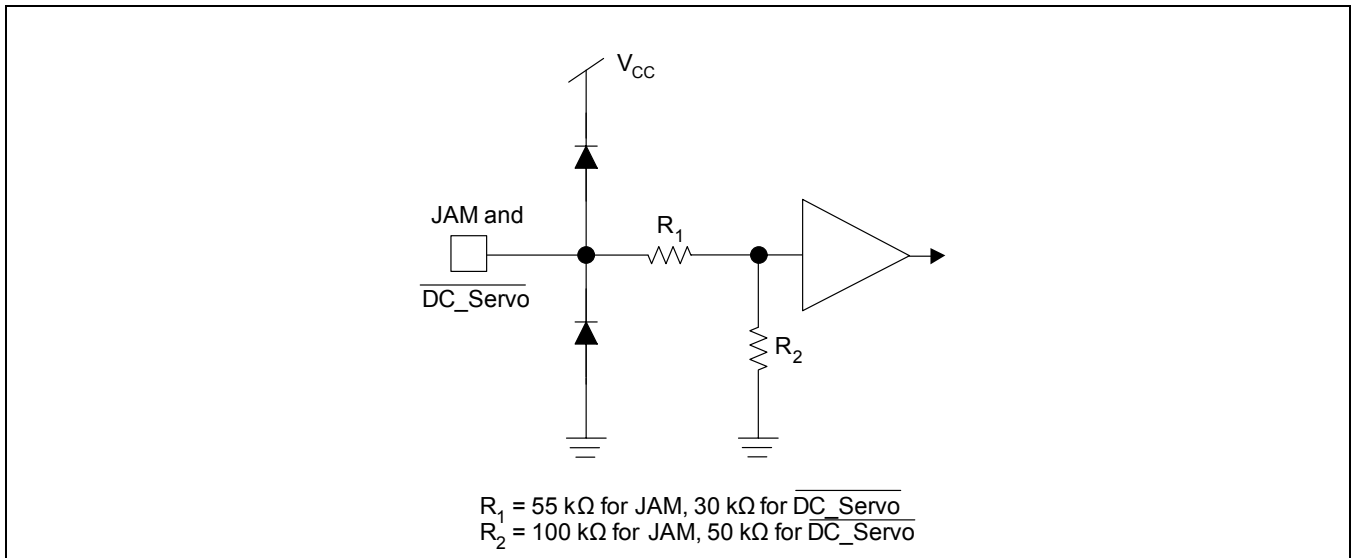
3.3.6   JAM Function

When asserted, the active high power down (JAM) pin forces the outputs to a logic "one" state. This ensures that no data is propagated through the system. The loss of signal detection circuit can be used to automatically force the data outputs to a high state when the input signal falls below the threshold. The function is normally used to allow data to propagate only when the signal is above the user's bit-error-rate requirement. It therefore inhibits the data outputs toggling due to noise when there is no signal present ("squelch").

In order to implement this function, LOS should be connected to the JAM pin shown in Figure 3-10, thus forcing the data outputs to a logic "one" state when the signal falls below the threshold.

3.3.7 $\overline{\text{DC Servo}}$ Function

When the $\overline{\text{DC\_Servo}}$ pin (shown in Figure 3-10) is driven high, the M02040-14 internal DC servo loop (described in Section 3.3.2) is disabled and the part will pass DC signals. This is useful when using signals with an unequal mark and space ratio, when the signal contains significant low speed or DC information, or when the input to the part must be DC coupled to a TIA that will change its common mode output voltage very quickly. Note that when the servo loop is disabled, any offset from the TIA or within the M02040-14 will cause DCD at the output which is a function of the offset and the input PP amplitude (large offsets and low amplitude input signals create the largest output DCD). When this pin is tied low or floating the 2040-14 servo loop operates as described in Section 3.3.2.
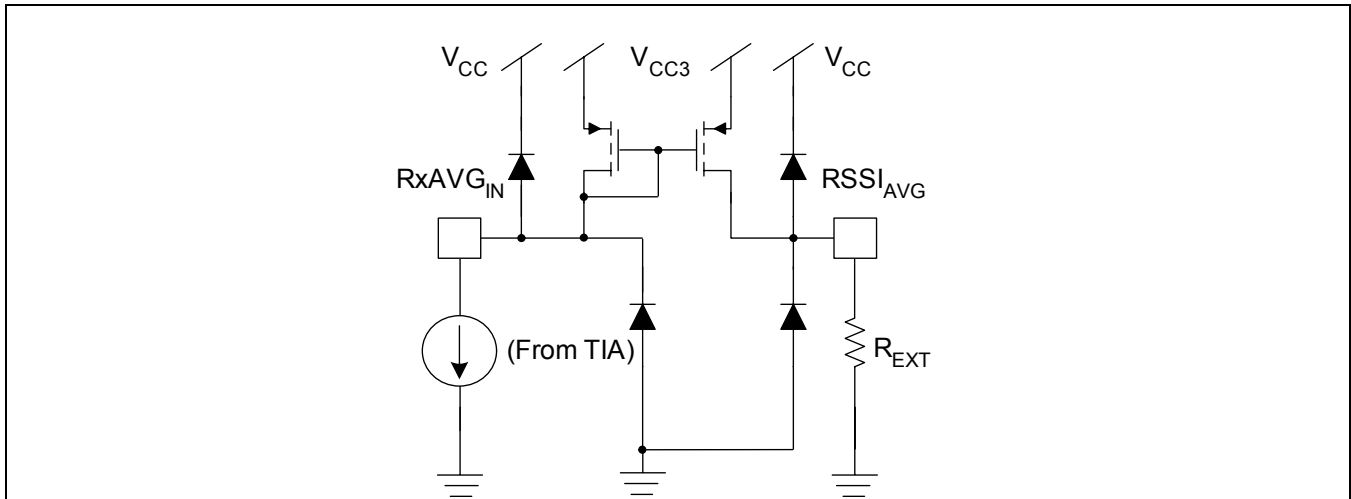
Figure 3-10.   JAM and $\overline{DC\_Servo}$ Input

R_1 = 55 kΩ for JAM, 30 kΩ for $\overline{\text{DC\_Servo}}$
R_2 = 100 kΩ for JAM, 50 kΩ for $\overline{\text{DC\_Servo}}$

3.3.8　　　Average Received Signal Strength Indicator (RSSI$_{AVG}$)

The RSSI$_{AVG}$ output current is a mirrored version of the RxAVG$_{IN}$ current from compatible TIAs. It sources rather than sinks the current making it compatible with DDMI type interfaces.

Figure 3-11.　RSSI$_{AVG}$ Output

4.0   Applications Information

4.1   Applications

- 1.0625 and 2.125 Gbps Fibre Channel
- 1.25 Gbps Ethernet
- 1.25 Gbps SDH/SONET

Figure 4-1.   Typical Applications Circuit

![MINDSPEED logo]

4.1.1 Reference Current Generation

The M02040-14 contain an accurate on-chip bias circuit that requires an external 12.1 kΩ 1% resistor, R_{REF} from pin I_{REF} to ground to set the LOS threshold voltage at ST_{SET} precisely.

Figure 4-2.   Reference Current Connection
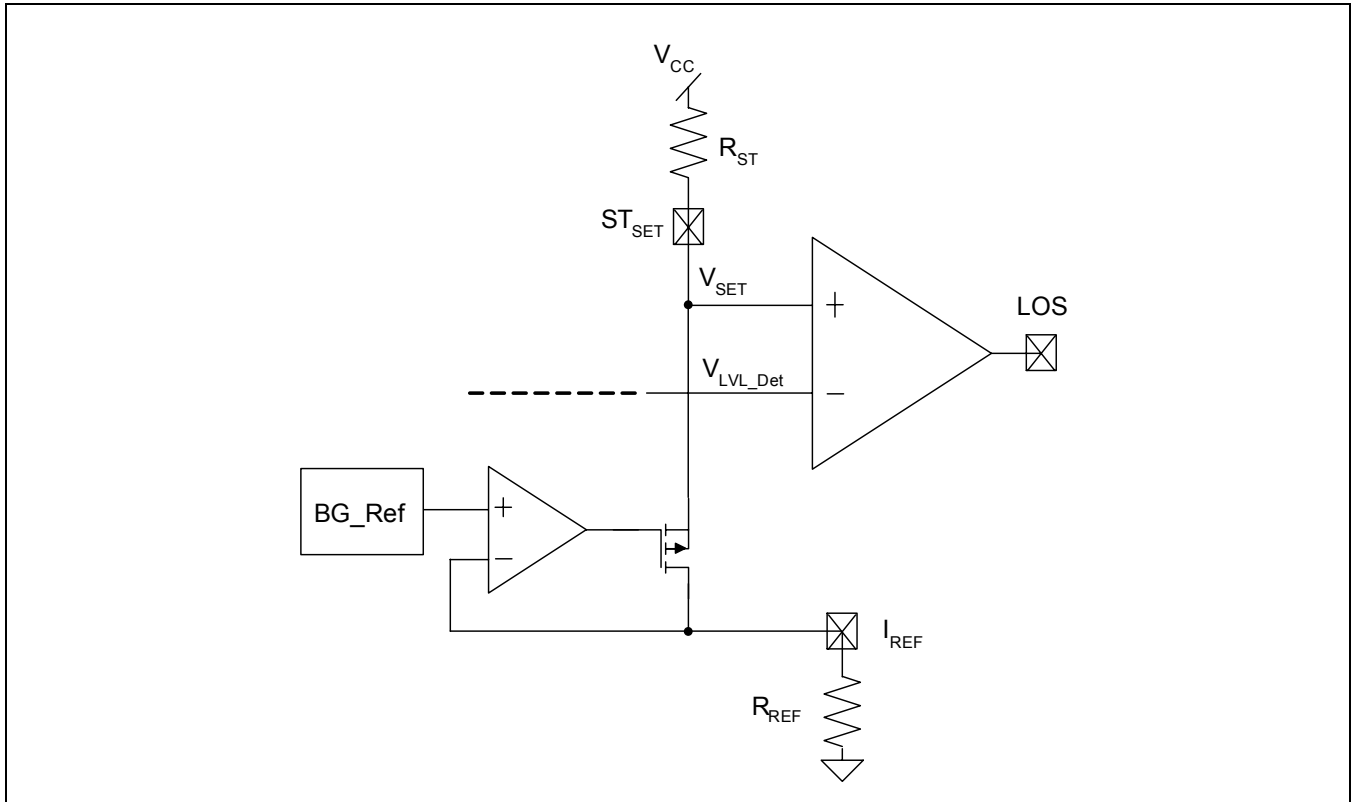
4.1.2 Choosing an Input AC-Coupling Capacitor

When AC-coupling the input the coupling capacitor should be of sufficient value to pass the lowest frequencies of interest, bearing in mind the number of consecutive identical bits, and the input resistance of the part. For Ethernet or Fibre Channel data, a good rule of thumb is to chose a coupling capacitor that has a cut-off frequency less than 1/(1,000) of the input data rate. For example, for 1.25 Gbps data, the coupling capacitor should be chosen as:

$f_{CUTOFF} \leq (1.25 \times 10^9 / 1 \times 10^3) = 1.25 \times 10^6$

The -3 dB cutoff frequency of the low pass filter at the 50 Ω input is found as:

$f_{3dB} = 1/ (2 * \pi * 50 \, \Omega * C_{AC})$
so solving for C where $f_{3dB} = f_{CUTOFF}$

$C_{AC} = 1/ (2 * \pi * 50 \, \Omega * f_{CUTOFF})$ EQ.1

and in this case the minimum capacitor is 2.5 nF.

For 2.125 Gbps Fibre Channel, this results in a minimum capacitor of 1.5 nF.

4.1.2.1 Multirate applications down to 155 Mbps

In this case, the input coupling capacitor needs to be large enough to pass 15 kHz ($155 \times 10^6/10,000$) which results in a capacitor value of 0.2 μF. However, because this low pass frequency is close to the 25 kHz low pass frequency of the internal DC servo loop, it is preferable to use a larger input coupling capacitor such as 1 μF which provides an input cutoff frequency of 3.1 kHz. This separates the two poles sufficiently to allow them to be considered independent. This capacitor should also have a 10 nF capacitor in parallel to pass the higher frequency data (in the multirate application) without distortion.

In all cases, a high quality coupling capacitor should be used as to pass the high frequency content of the input data stream.

4.1.3 Using $\overline{DC\_Servo}$

When the $\overline{DC\_Servo}$ pin (shown in Figure 3-10) is tied high, the M02040-14 disables the internal servo loop which allows the device to pass signals with DC content resulting in instantaneous response to changes in the input data stream (e.g. data amplitude and phase). However, there is no correction for limit amp offset when the servo loop is disabled which results in degraded sensitivity and increased duty cycle distortion. For normal operation the $\overline{DC\_Servo}$ pin should be tied low.

4.1.4 Using RSSI$_{AVG}$

As shown in the typical applications circuit (front page), when interfacing to a TIA that features a "MON" output such as the M02010 or M02016, the M02040-14 can reference the current sunk into the TIA "MON" output and produce a proportional current at the 2040 RSSI$_{AVG}$ output. The current is sourced into resistor R$_{EXT}$ to ground creating a voltage suitable for DDMI applications. R$_{EXT}$ should be chosen as:

$$R_{EXT} = 1/(\text{maximum current into RSSI}_{AVG}) \hspace{3cm} EQ.2$$

This keeps the voltage at RSSI$_{AVG}$ between 0 and 1 V.

4.1.5 Setting the Signal Detect Level

Using Figure 4-3, the value for R$_{ST}$ is chosen to set the LOS threshold at the desired value. The resulting hysteresis is also shown in Figure 4-3.

From Figure 4-3, it is apparent that small variations in R$_{ST}$ cause significant variation in the LOS threshold level, particularly for low input signal levels. This is because of the logarithmic relationship between the RSSI voltage and the input signal level. It is recommended that a 1% resistor be used for R$_{ST}$ and that allowance is provided for LOS variation, particularly when the LOS threshold is near the sensitivity limit of the M02040-14.

Example R$_{ST}$ resistor values are given in Table 4-1.

Table 4-1.   Typical LOS Assert and De-assert Levels for Various 1% R$_{ST}$ Resistor Values

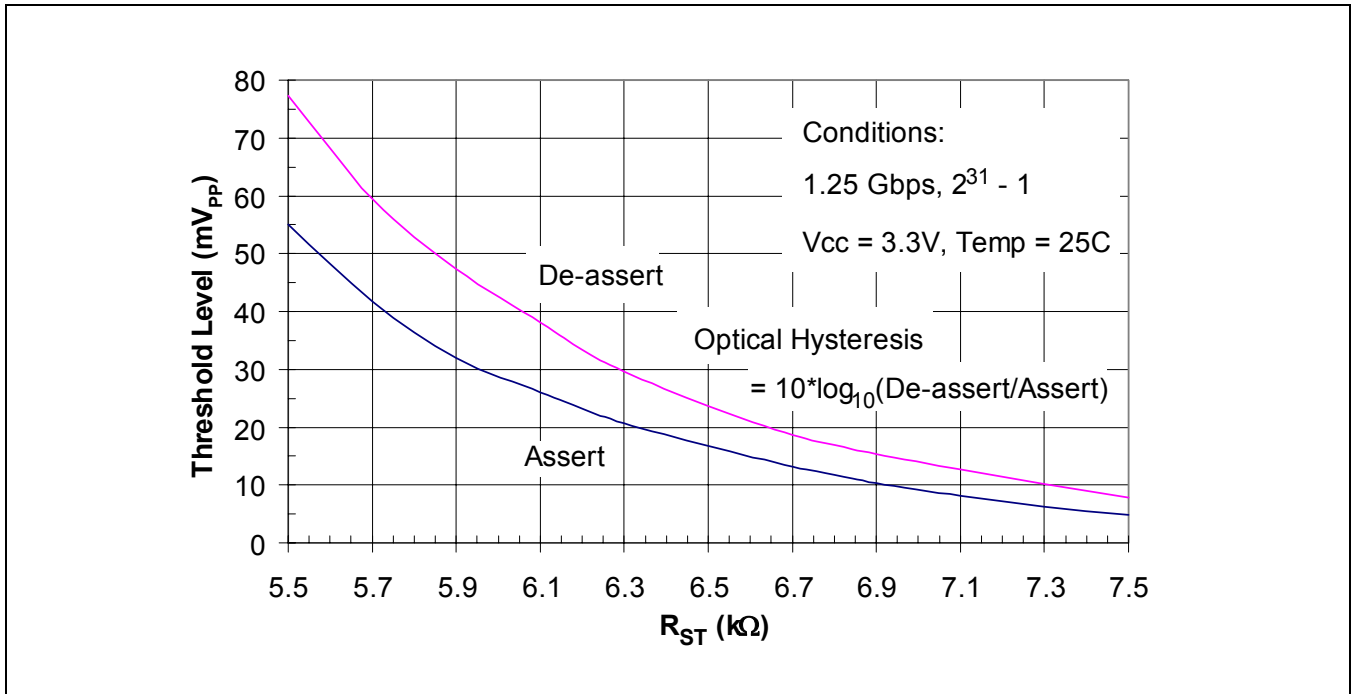| R$_{ST}$ (kΩ)	VIN (mV pp) differential	
	LOS Assert	LOS De-Assert
7.50	4.9	7.8
6.81	11.7	17.0
6.19	23.2	33.4
5.49	55.0	77.3

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Figure 4-3. *Typical Loss of Signal Characteristic (Full Input Signal Range)*

Figure 4-4. *Typical Loss of Signal Characteristic (Low Input Signal Range)*

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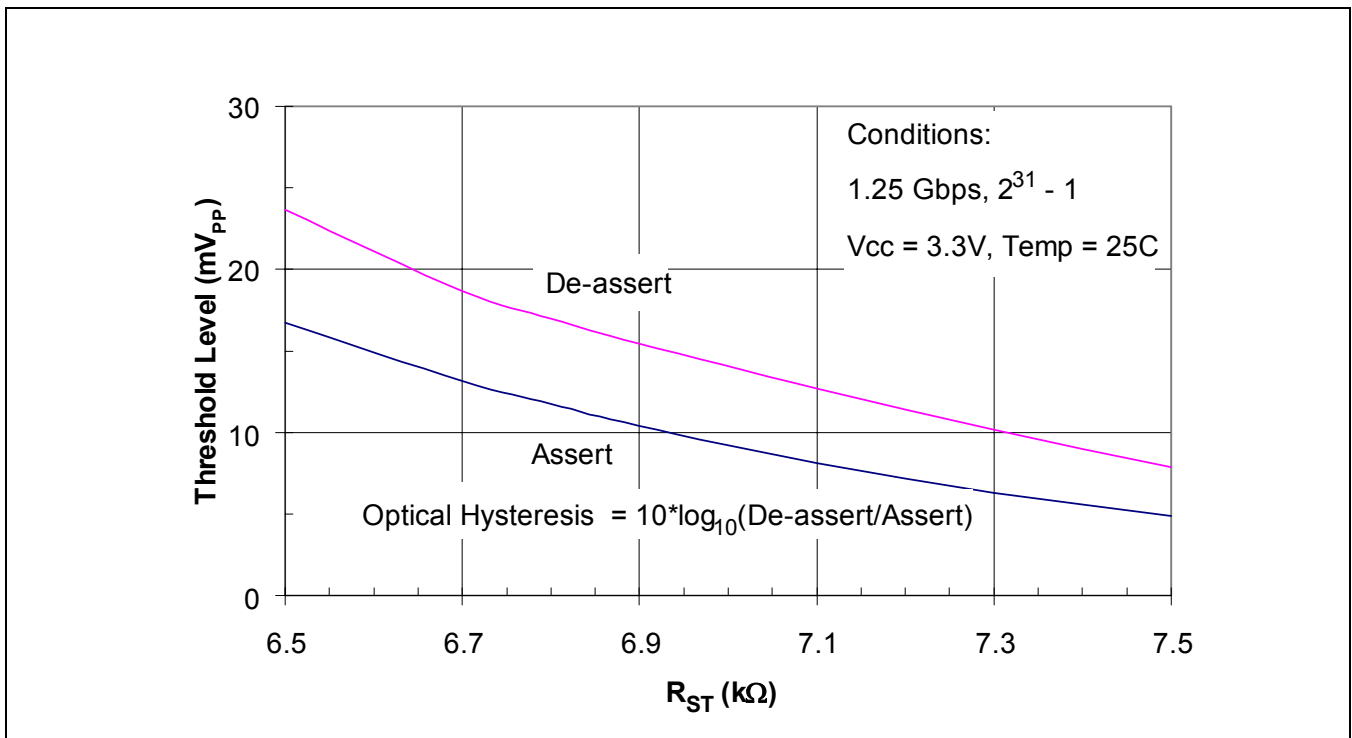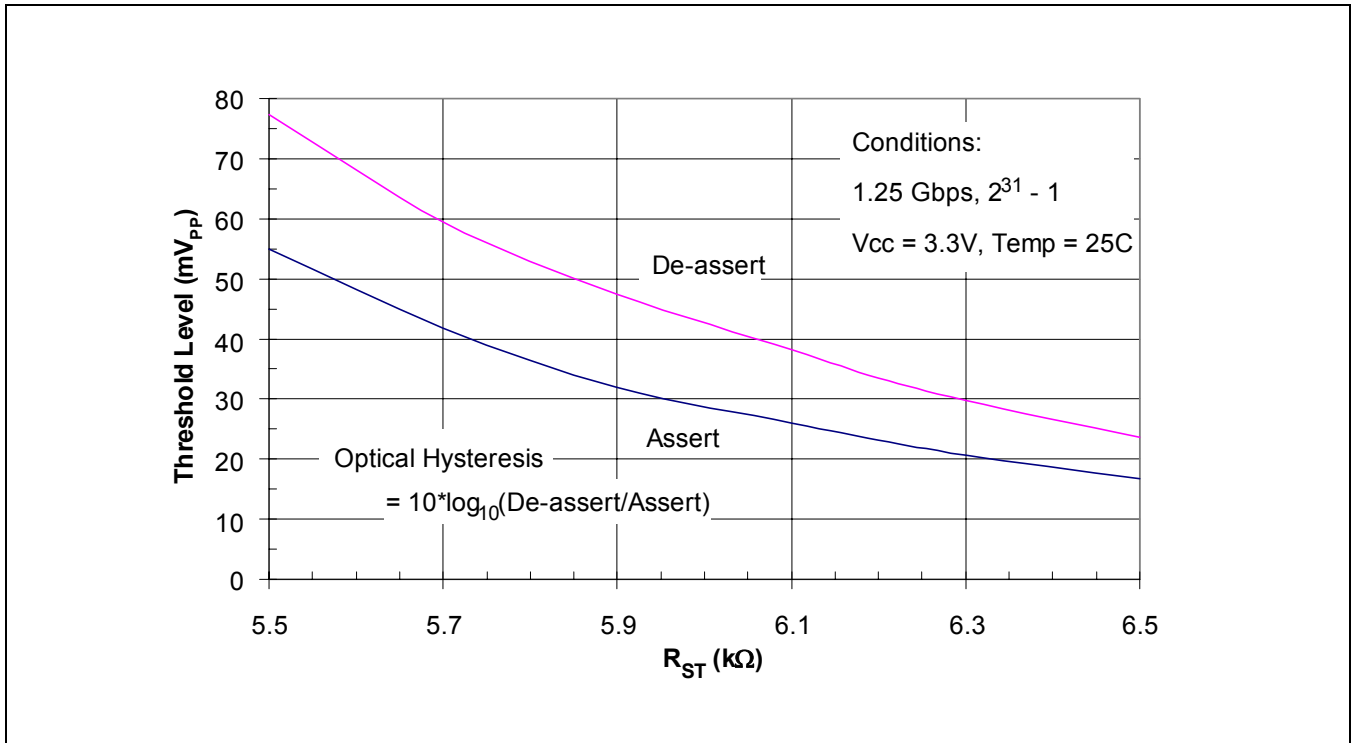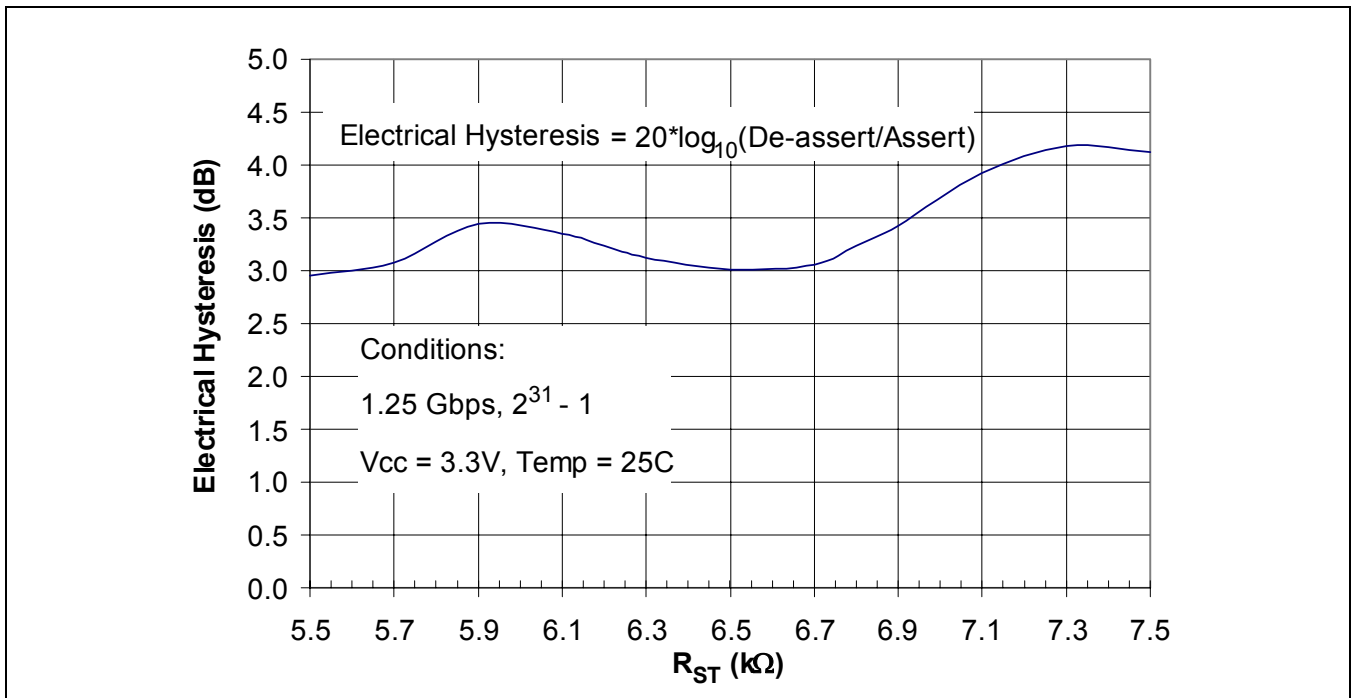**Mindspeed Proprietary and Confidential**

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Figure 4-5. *Typical Loss of Signal Characteristic (High Input Signal Range)*

Figure 4-6. *Typical Loss of Signal Hysteresis Characteristic (Full Input Signal Range)*

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4.1.6 PECLP and PECLN Termination

The outputs of the M02040-14 are PECL compatible and any standard AC or DC-coupling termination technique can be used. Figure 4-7 and Figure 4-8 illustrate typical AC and DC terminations.

AC-coupling is used in applications where the average DC content of the data is zero e.g. SONET. The advantage of this approach is lower power consumption, no susceptibility to DC drift and compatibility with non-PECL interfaces. Figure 4-7 shows the circuit configuration and Table 4-2 lists the resistor values. If using transmission lines other than 50 Ω, the shunt terminating resistance Z_T should equal twice the impedance of the transmission line (Z_O).

DC-coupling can be used when driving PECL interfaces and has the advantage of a reduced component count. A Thevenin termination is used at the receive end to give a 50 Ω load and the correct DC bias. Figure 4-8 shows the circuit configuration and Table 4-2 the resistor values.

Alternatively, if available, terminating to V_{CC} - 2V as shown in Figure 4-9 has performance advantages at high data rates.

Table 4-2.   PECL Termination Resistor Values

Supply	Output Impedance	$R_{PULL-DOWN}$	Z_T	R_{TA} / R_{TB}	R_T / R_B
3.3V	50 Ω	150 Ω	100 Ω	2.7 kΩ / 4.3 kΩ	130 Ω / 82 Ω

Figure 4-7.   AC-Coupled PECL Termination
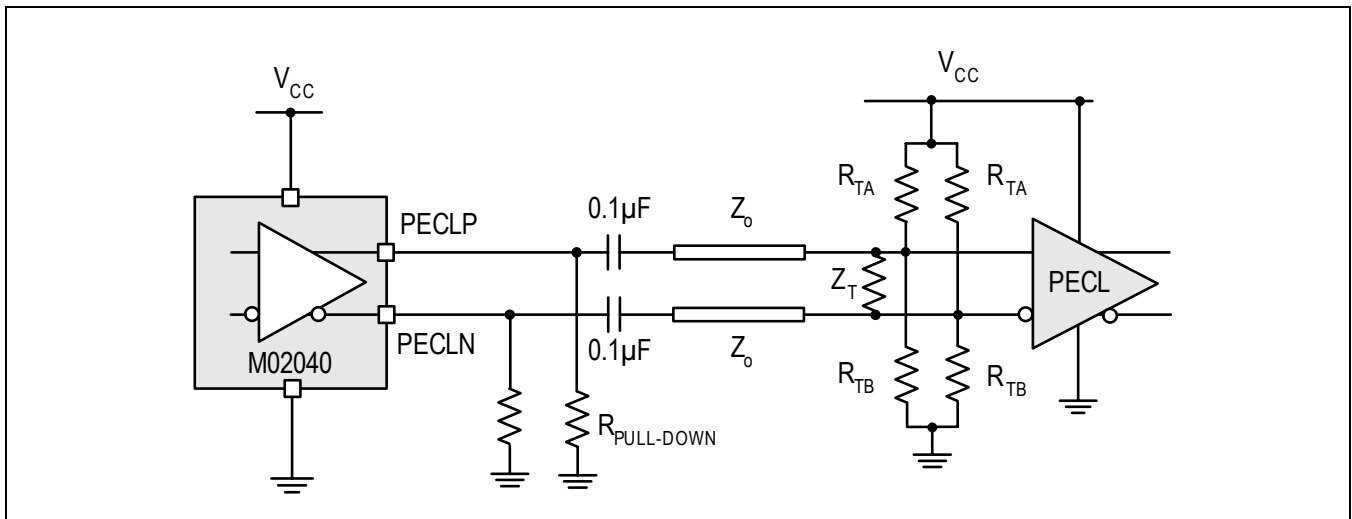
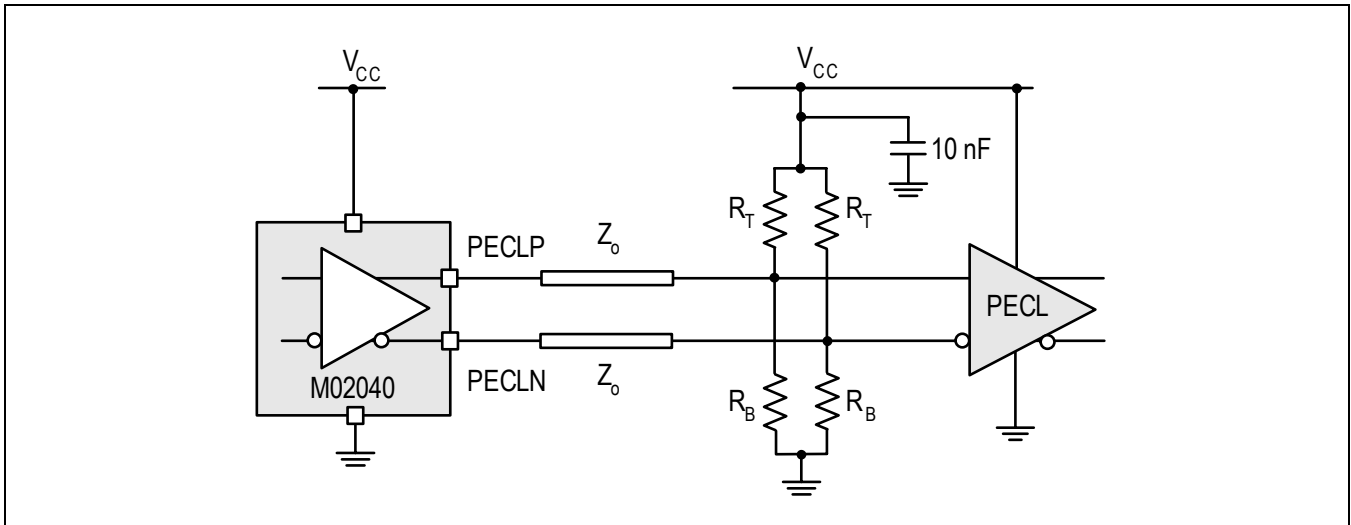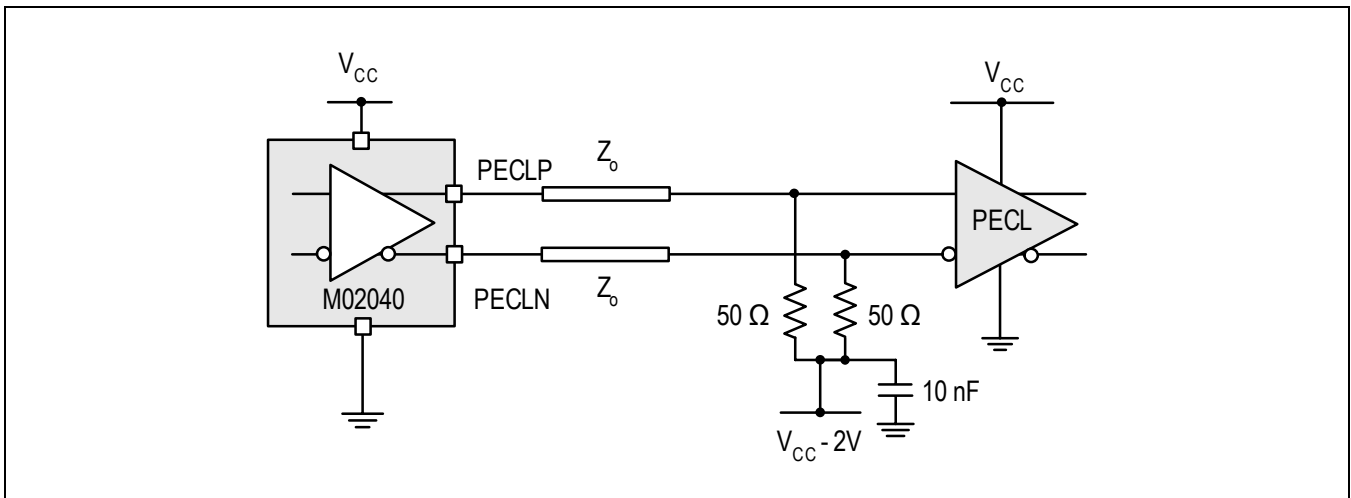*Figure 4-8.   DC-Coupled PECL Termination*

Figure 4-9.   Alternative PECL Termination
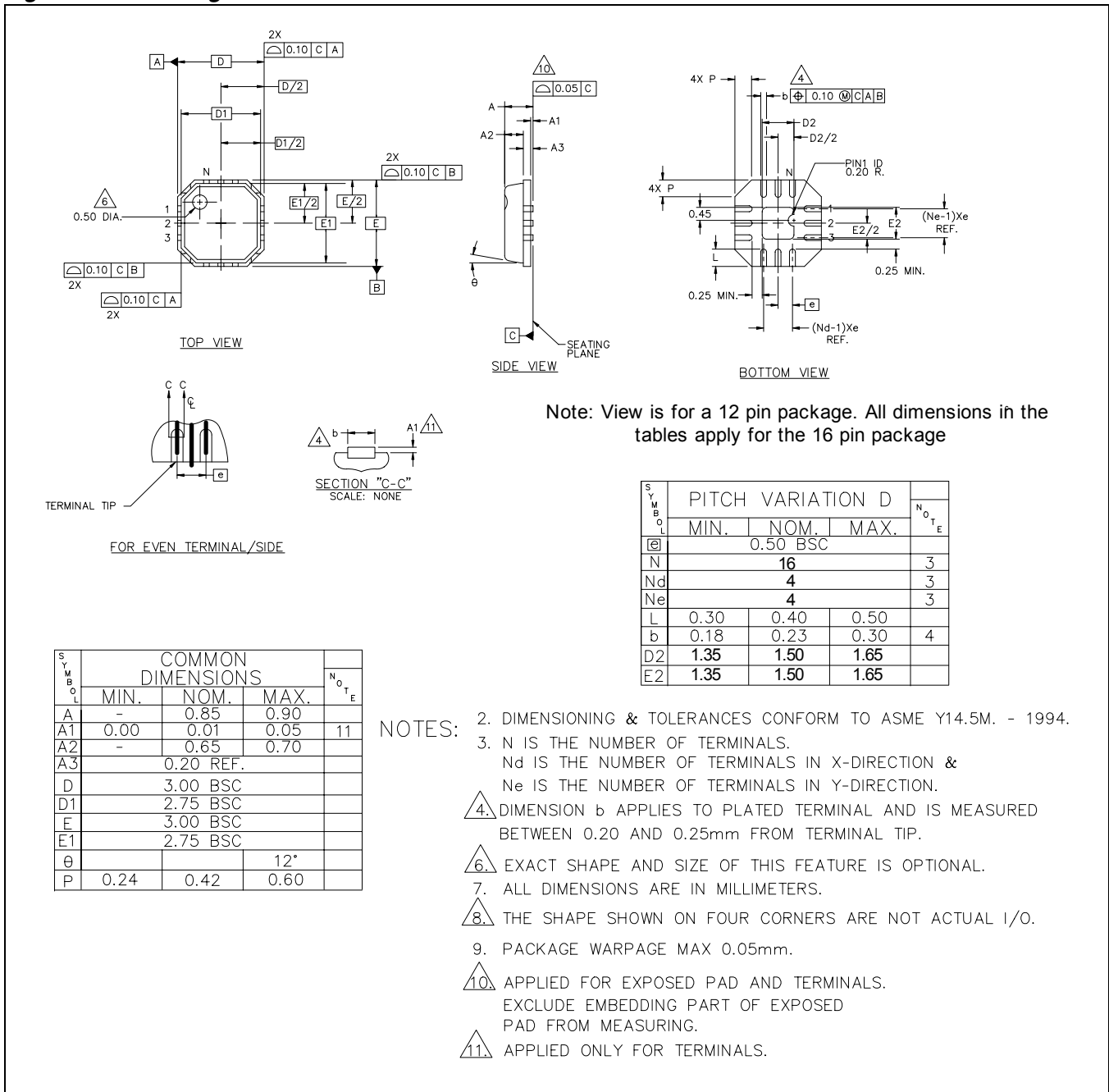

4.1.7   Using JAM

As shown in the typical applications circuit (Figure 1-2), the LOS output pin can optionally be connected to the Jam input pin. When LOS asserts the Jam function sets the data outputs to a fixed "one" state (PECLP is held high and PECLN is held low). This is normally used to allow data to propagate only when the signal is above the users' bit error rate (BER) requirement. It prevents the outputs from toggling due to noise when no signal is present.

From the LOS assert and deassert figures above (Figure 4-2 - Figure 4-4), when an input signal is below the LOS assert threshold, LOS asserts (LOS high) causing Jam to assert. When Jam asserts, the data outputs and the internal servo loop of the M02040-14 are disabled. If the input signal reaches or exceeds the LOS deassert threshold, LOS deasserts (LOS low) causing Jam to deassert, and hence enables the data outputs and the internal servo loop. If, however, the input signal is slowly increasing to a level that does not exceed the LOS deassert threshold (operating in the hysteresis region), the internal servo loop may not be fully established and this may cause partial enabling of the data outputs. To avoid this the input signal needs to fully reach or exceed the LOS deassert level to fully enable the data outputs.

Figure 5-1.   Package Information

TOP VIEW

SIDE VIEW

BOTTOM VIEW

SECTION "C-C"
SCALE: NONE

FOR EVEN TERMINAL/SIDE

TERMINAL TIP

Note: View is for a 12 pin package. All dimensions in the tables apply for the 16 pin package

S Y M B O L	PITCH VARIATION D			N O T E
	MIN.	NOM.	MAX.	
e	0.50 BSC			
N	16			3
Nd	4			3
Ne	4			3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
D2	1.35	1.50	1.65	
E2	1.35	1.50	1.65	

S Y M B O L	COMMON DIMENSIONS			N O T E
	MIN.	NOM.	MAX.	
A	–	0.85	0.90	
A1	0.00	0.01	0.05	11
A2	–	0.65	0.70	
A3	0.20 REF.			
D	3.00 BSC			
D1	2.75 BSC			
E	3.00 BSC			
E1	2.75 BSC			
θ			12°	
P	0.24	0.42	0.60	

NOTES:

2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.

3. N IS THE NUMBER OF TERMINALS.
Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.

4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED
BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.

6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.

7. ALL DIMENSIONS ARE IN MILLIMETERS.

8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.

9. PACKAGE WARPAGE MAX 0.05mm.

10. APPLIED FOR EXPOSED PAD AND TERMINALS.
EXCLUDE EMBEDDING PART OF EXPOSED
PAD FROM MEASURING.

11. APPLIED ONLY FOR TERMINALS.

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