M21170

3.2 Gbps 288x288 Asynchronous Crosspoint Switch

The M21170 is a high-performance, 288x288, asynchronous non-blocking crosspoint switch featuring 82,944 unique switching paths. It is ideally suited for high-speed data switching in datacom, telecom, and video applications.

Each switching path can operate independently at any data rate of up to 3.2 Gbps, allowing for multi-rate routing and switching in one single device. The M21170 includes per lane, programmable, input equalization and output de-emphasis, enabling optimal compensation for board trace losses and making the device ideal for designs in very large systems.

To alleviate the power consumption and heat dissipation challenges in such systems, the output swing level for each lane may be set individually, providing flexibility and optimization of power dissipation without compromised performance. All unused output drivers, in addition to all paths not exercised within the device, are automatically disabled for maximum power savings.

The device is configurable through standard 2-wire (I^2C compatible) and 4-wire serial interfaces, as well as a 9-bit parallel interface.

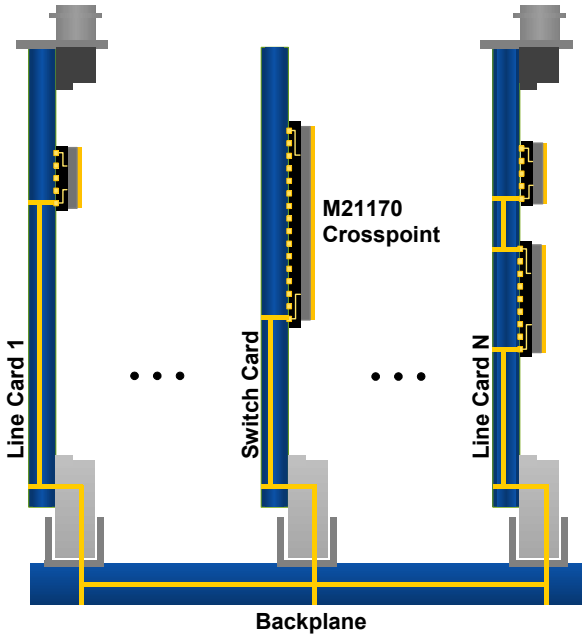
Applications

- Digital video switchers/routers
- DWDM routers
- Backplane switching and signal conditioning

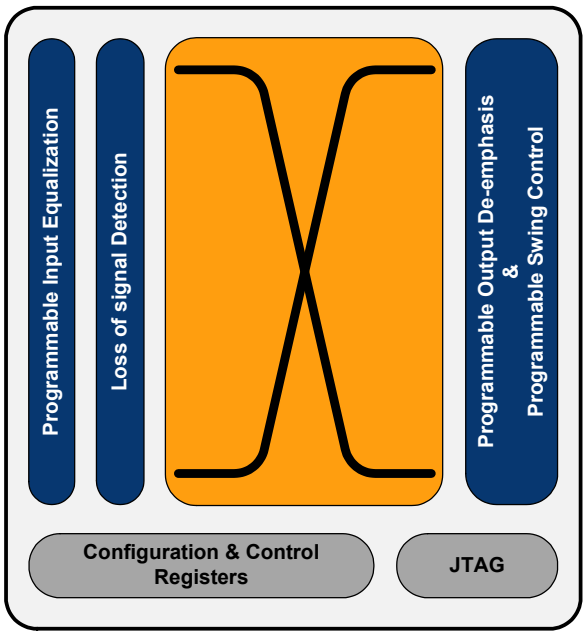
Features

- Fully non-blocking matrix array
- Protocol agnostic
- Global or individual programmable input equalization and output de-emphasis
- Global or individual programmable output swing level
- Individual input termination control (High-Z or 50 Ω)
- Support for multiple switch points
- Loss of signal alarm per input
- Flexible configuration through standard 2-wire and 4-wire serial interfaces, as well as parallel interface
- 1.2 V core, 1.2 V output, and optional 1.2 V/1.8 V/2.5 V input supply voltages
- DC and AC coupling support at input/output
- Electrically independent input and output supply voltage rails for increased flexibility
- JTAG boundary scan

Routing Switcher Application Diagram



M21170 Device Architecture



Ordering Information

Part Number	Package	Operating Temperature
M21170G-12*	2389-pin, 50 mm x 50 mm BGA	-40 °C to 85 °C
* The letter “G” designator after the part number indicates that the device is RoHS compliant. Refer to www.mindspeed.com for additional information.		

Revision History

Revision	Level	Date	Description
E	Release	September 2011	Figure 4-20, Figure 4-21, and Figure 4-22: t_{DD} and t_{DRIVER} labels were inverted in the timing diagrams. Updated the data sheet format to reflect new register naming convention.
D	Release	December 2010	Limited AV_{DD0} voltage to 1.2 V only. Removed 1.8 V support, once 1.8 V lifetime reliability testing is completed, support for AV_{DD0} at 1.8 V will be restored. Updated Table 1-2 junction to case thermal resistance from TBD to 0.55 °C/W. Updated Table 1-4 power consumption specifications, tightened maximum power and current consumption limits. Section 4.10, Page21h temperature monitoring, register 041h, removed the 1 sigma value = 1.6 °C. Figure 4-11 updated to include Read and Write I^2C description. Figure 4-21 and Figure 4-22 updated to show the correct Tdd and Tdriver definition for the parallel interface timing specifications. Section 4.5 juntion temperature monitor. Removed the uncalibrated accuracy of the sensors. Updated Figure 2-1 and Figure 2-2 to show point blank operation at 3.2 Gbps. Added Figure 2-6, Agilent BERT N4903A Backplan FR4 traces used to measure input Equalization performance on Figure 2-5.

Revision History

Revision	Level	Date	Description
C	Advance	November 2010	Table 1-1: - Updated AV_{DDO} Absolute Maximum Rating. - Updated ESD HBM and CDM maximum ratings based on qualification test results. Added the following new sections: Section 4.2.3.1 LOS Monitoring Feature1, Hardware Pin xAlarm. Section 4.2.3.2 Using xAlarm to Monitor LOS for ALL Input Channels, Application Example. Section 4.2.3.3 Using xAlarm to Monitor LOS for Individual Input Channels, Application Example. Section 4.2.3.4 LOS Monitoring Feature 2, Registers LOS ALARM and STAT ALARM. Section 4.2.3.5 Using Register LOS ALARM to Monitor LOS for Input Channels, Application Example. Section 4.2.3.6 - Using Register STAT ALARM to Monitor LOS for Individual Input Channels, Application Example. Updated typical and maximum current consumption for AV_{DDI}, AV_{DD}, AV_{DDO}, DV_{DDIO} and total power consumption in Table 1-3. In Table 1-5, updated minimum data rate supported. Updated minimum, typical and maximum values for the differential output swing, rise and fall times as well as additive deterministic jitter. Updated pinout diagram to show the do-not-connect pins in Figure 3-1. Added Section 4.2.3.2. Updated Package Drawing, Figure 3-10, Figure 3-11. Removed the specific swings and replaced them with minimum, intermediate and maximum values in Section 4.2, Section 4.9, and Section 4.10. Table 1-4, Updated values based on characterization. Table 1-4, Changed DR min to be 10 kbps, added Note 1 to stipulate LOS disable. Table 1-4, Updated output voltage differential and separated to two rows for AV_{DDO}=1.2 V and 1.8 V. Table 1-4, Updated notes for t_R/t_F. Section 4.4, revised sub-section headings. Added Figure 4-21, Parallel Interface Multiple Single Read Timing Configuration. Added Figure 4-22, Parallel Interface Single Read, Single Write Timing Configuration. Updated the following register default values: - Product Revision Code: M21170-12. Page 00h, register 02h, from 00h, to 01h. - Auxiliary Input Channel: Enabled 50 Ω input termination. Pages 21h, registers 80h, 81h from 78h to 58h. - Enabled Global LOS hysteresis: Page 21h, register 0Ch, from 01h to 00h. Added Figure 2-1 through Figure 2-5 to show Typical performance characteristics.
B	Advance	March 2010	Changed Operating Case Temperature. Updated Table 1-2, Table 1-3, and Table 1-4. Add Figure 4-2 through 4-8. Updated Section 4.2.3, 4.6.1, 4.6.3, Table 4-3, Table 4-5.
A	Advance	December 2009	Initial release.

Marking Diagram

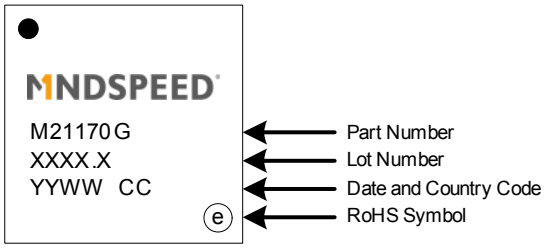


Table of Contents

List of Figures

List of Tables

1.0 Electrical Characteristics

Unless noted otherwise, specifications in this section are valid with DV_{DDIO} = 3.3 V, AV_{DDI} = AV_{DDO} = 1.2 V, AV_{DD} = 1.2 V power supplies, 25 °C ambient temperature, 800 mV_{PPD} differential input data swing, minimum output data swing, PRBS 2^{15} - 1 test pattern at 3.2 Gbps, R_{LOAD} = 50 Ω.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Note	Minimum	Maximum	Unit
DV_{DDIO}	Digital I/Os supply voltage	1, 3	-0.5	3.6	V
AV_{DD}	Analog core supply voltage	1, 3	-0.5	1.5	V
AV_{DDO}	Analog output supply voltage	1, 3	-0.5	2.0	V
AV_{DDI}	Analog input supply voltage	1, 3	-0.5	2.8	V
V_{IN}	DC input voltage (PCML)	1, 3	V_{SS} - 0.5	AV_{DD} + 0.5	V
$V_{IN, CMOS}$	DC input voltage (CMOS)	1, 3	V_{SS} - 0.5	DV_{DDIO} + 0.5	V
T_{STORE}	Storage temperature	1, 3	-65	+150	°C
T_{JUNC}	Junction temperature	1, 3	-20	+125	°C
$V_{ESD, HBM}$	Electrostatic discharge voltage (HBM)	1, 2, 3	-2000	+2000	V
$V_{ESD, CDM}$	Electrostatic discharge voltage (CDM)	1, 2, 3	-500	+500	V
LU	Latch up @ 85 °C	1, 3	-150	+150	mA

NOTES:

1. Exposure of the device beyond the minimum/maximum limits may cause permanent damage.
2. HBM and CDM per JEDEC Class 2 (JESD22-A114-B).
3. Limits listed in the above table are stress limits only and do not imply functional operation within these limits.

Table 1-2. Recommended Operation Conditions

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
DV_{DDIO}	Digital I/Os supply voltage		1.14	1.2 / 2.5 / 3.3	3.47	V
AV_{DD}	Analog core supply voltage		1.14	1.2	1.26	V
AV_{DDO}	Analog output supply voltage		1.14	1.2	1.26	V
AV_{DDI}	Analog input supply voltage		1.14	1.2 / 1.8 / 2.5	2.63	V
T_{JUNC}	Junction temperature		—	—	110	°C
θ_{JC}	Junction to case thermal resistance	1, 2	0.55			°C/W

NOTES:

1. Without heat sink and without air flow.
2. Thermal resistance value is calculated using a 5% increase on the supply voltage, with all 288 inputs and 288 outputs enabled, and includes all temperature variations.

NOTE: A bolted-down heat sink is recommended for this product. Mindspeed strongly recommends against the use of adhesively mounted heat sinks. Please refer to Mindspeed's M21170 thermal application note (document number 21170-APP-001).

Table 1-3. Power Consumption Specifications

Symbol	Parameter			Typical	Maximum	Unit
DI_{DDIO}, Digital IO Current Consumption	Average current using the parallel interface in read mode at maximum speed.			10	30	mA
AI_{DDI}, AV_{DDI} Current Consumption	With input termination set in high-Z mode.			0	0.2	mA
	50 Ω input termination enabled AC-coupled on all 288 input channels	AV_{DDI}=1.2 V	Minimum EQ set	0.38	0.50	A
			Intermediate EQ set 1	0.28	0.35	A
			Intermediate EQ set 2	0.19	0.25	A
			Maximum EQ set	0.10	0.15	A
		AV_{DDI}=1.8 V	Minimum EQ set	0.70	0.90	A
			Intermediate EQ set 1	0.50	0.65	A
			Intermediate EQ set 2	0.35	0.45	A
			Maximum EQ set	0.25	0.27	A
		AV_{DDI}=2.5 V	Minimum EQ set	1.1	1.3	A
			Intermediate EQ set 1	0.75	0.95	A
			Intermediate EQ set 2	0.50	0.65	A
			Maximum EQ set	0.35	0.45	A
	50 Ω input termination enabled DC-coupled @ 200 mV_{PPD} of input launch.	AV_{DDI}=1.2 V	Minimum EQ set	0.90	1.00	A
			Intermediate EQ set 1	0.80	0.90	A
			Intermediate EQ set 2	0.72	0.80	A
			Maximum EQ set	0.66	0.70	A
		AV_{DDI}=1.8 V	Minimum EQ set	1.20	1.35	A
			Intermediate EQ set 1	1.00	1.15	A
			Intermediate EQ set 2	0.90	1.00	A
			Maximum EQ set	0.76	0.80	A
		AV_{DDI}=2.5 V	Minimum EQ set	1.50	1.75	A
			Intermediate EQ set 1	1.25	1.45	A
			Intermediate EQ set 2	1.00	1.20	A
			Maximum EQ set	0.90	0.95	A
AI_{DD}, AV_{DD} Current Consumption	AV_{DD} = 1.2 V. Switch configuration sets in 1 to 1 for all 288 channels		Minimum swing	28.0	34.0	A
			Intermediate swing	29.0	35.0	A
			Maximum swing	29.5	35.5	A
AI_{DDO}, AV_{DDO} Current Consumption	AV_{DDO}=1.2 V. Switch configuration sets in 1 to 1 for all 288 output channels with 4.7 µF capacitors		Minimum swing	3.5	4.0	A
			Intermediate swing	5.5	6.5	A
			Maximum swing	5.6	6.8	A

Table 1-3. Power Consumption Specifications

Symbol	Parameter		Typical	Maximum	Unit
P_{TOTAL}, Total Power Consumption	AV_{DDI} = AV_{DDO}=1.2 V. Switch configuration sets in 1 to 1 for all 288 output channels with 4.7 µF capacitors	Minimum swing	38.5	48.5	W
		Intermediate swing	41.5	52.5	W
		Maximum swing	42.5	54.0	W

NOTES:

1. Maximum current and maximum power consumption numbers are calculated using a 5% increase on the supply voltage, with all 288 inputs and 288 outputs enabled, and include all temperature and process variations.
2. In a DC-coupled interface, the DC current is drawn from AV_{DDO} of the upstream transmitting device. When AV_{DDI} is setup to be DC-coupled, the DC current is drawn from the AV_{DDO} of the upstream transmitting device.

Table 1-4. Control/Interface Logic Input/Output Specifications

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
V_{OH}	Output logic high	1	0.80 x DV_{DDIO}	DV_{DDIO}	—	V
V_{OL}	Output logic low	2	—	0	0.20 x DV_{DDIO}	V
V_{IH}	Input logic high	1	0.75 x DV_{DDIO}	—	DV_{DDIO}	V
V_{IL}	Input logic low	1	0	—	0.25 x DV_{DDIO}	V

NOTES:

1. I_{OH} = -1 mA.
2. I_{OL} = 2 mA.

Table 1-5. PCML Input/Output Electrical Characteristics

Symbol	Parameter			Note	Minimum	Typical	Maximum	Unit
DR	NRZ data rate			1	0.01	—	3200	Mbps
V_{IH}	Maximum input high voltage			—	—	—	AV_{DDI} + 0.3	V
V_{IL}	Minimum input high voltage			—	AV_{DDI} - 0.8	—	—	V
V_{IN}	Differential input swing			2, 3	200	—	1600	mV_{PPD}
V_{ICM}	Input common mode			—	AV_{DDI} - 0.5	—	AV_{DDI} + 0.1	V
V_{OUT}	Differential output swing, all outputs are AC coupled (4.7 µF)	AV_{DDO}=1.2 V	Minimum swing	—	330	550	750	mV_{PPD}
			Intermediate swing	—	650	900	1090	mV_{PPD}
			Maximum swing	—	800	1060	1200	mV_{PPD}
R_{IN}	Input termination resistance. 50 Ω, input resistance enabled		AV_{DDI}=1.2 V	—	45	55	70	Ω
			AV_{DDI}=1.8 V	—	40	50	55	Ω
			AV_{DDI}=2.5 V	—	40	45	55	Ω
t_{PD}	Propagation delay (from any input to any output)			2, 4, 5	0.5	—	8	ns
t_R/t_F	Output rise/fall time (20%–80%)		AV_{DDO}=1.2 V	4, 5, 6	—	135	200	ps
t_{DCV}	Output duty cycle			8	0	—	50	ps
t_{DJ}	Additive deterministic jitter (t_{DJ})			5, 6, 7	—	100	250	mUI

NOTES:

1. Minimum data rate is limited by AC coupling capacitor if present. For data rates below 100 Mbps, DC servo and LOS must be disabled.
2. Inputs are AC coupled during testing operation.
3. Value specified at the device pins with minimum EQ setting.
4. Value specified using pattern with minimum pulse width of Consecutive Identical Digit (CID) ≥ 10 at 3.2 Gbps data rate; 800 mV_{PPD} input swing, AC coupled.
5. Value specified with load as follows: Mindspeed Evaluation Module (EVM) with 3 ft. coaxial cables into Agilent DCAJ or equivalent (intermediate output swing).
6. Absolute value specified using 101010 clock-like pattern.
7. Value specified at 3.2 Gbps using PRBS 2^{15}-1 pattern with setup as follows: Mindspeed Evaluation Module with 3 ft. coaxial cables from Agilent JBERT or equivalent (800 mV_{PPD} input swing, minimum input equalization setting).
8. Value as reported by Agilent DCAJ or equivalent. t_{DJ} measurements includes t_{DCV}.

2.0 Typical Performance Characteristics

Unless noted otherwise, specifications in this section are valid with DV_{DDIO} = 3.3 V, AV_{DDI} = AV_{DDO} = 1.2 V, AV_{DD} = 1.2 V power supplies, 25 °C ambient temperature, 800 mV_{PPD} differential input data swing, intermediate output data swing, PRBS 2^{15} - 1 test pattern at 3.2 Gbps, R_{LOAD} = 50 Ω.

Figure 2-1. 3.2G Typical Eye Diagram, 3.5 Inches of Backplane in Front and Back of the M21170

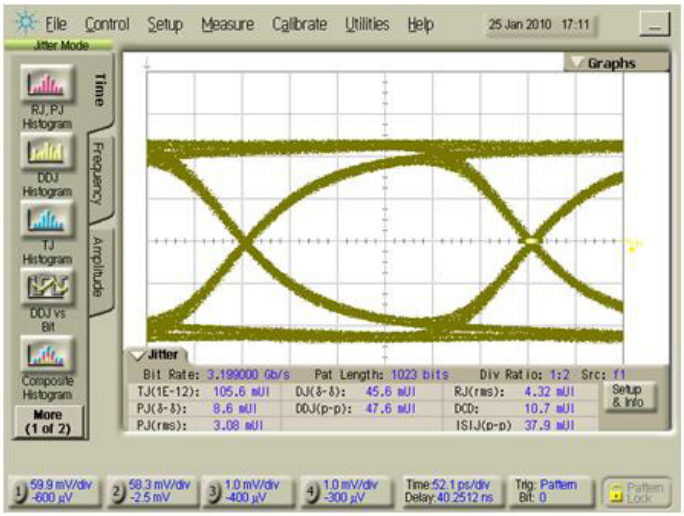


Figure 2-2. 3.2G Typical Eye Diagram, 3.5 inches of Backplane in Front and Back of the M21170, 2 dB of De-emphasis Enabled

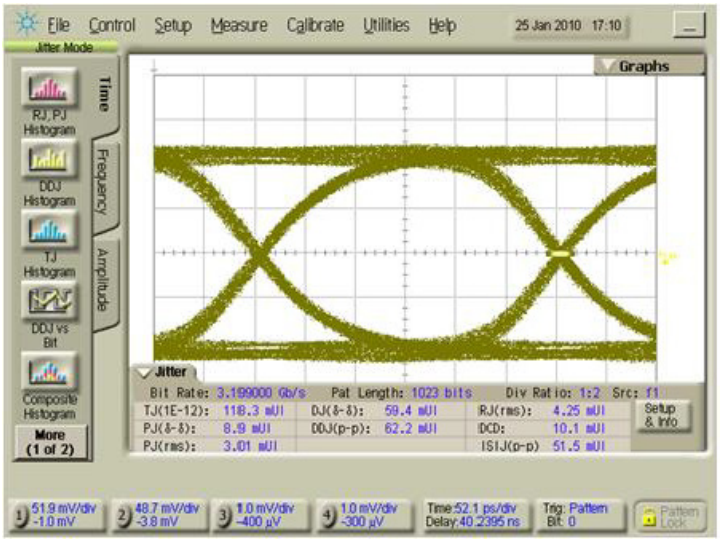


Figure 2-3. Typical Power Consumption for AV_{DD} Vs Number of Channels ON

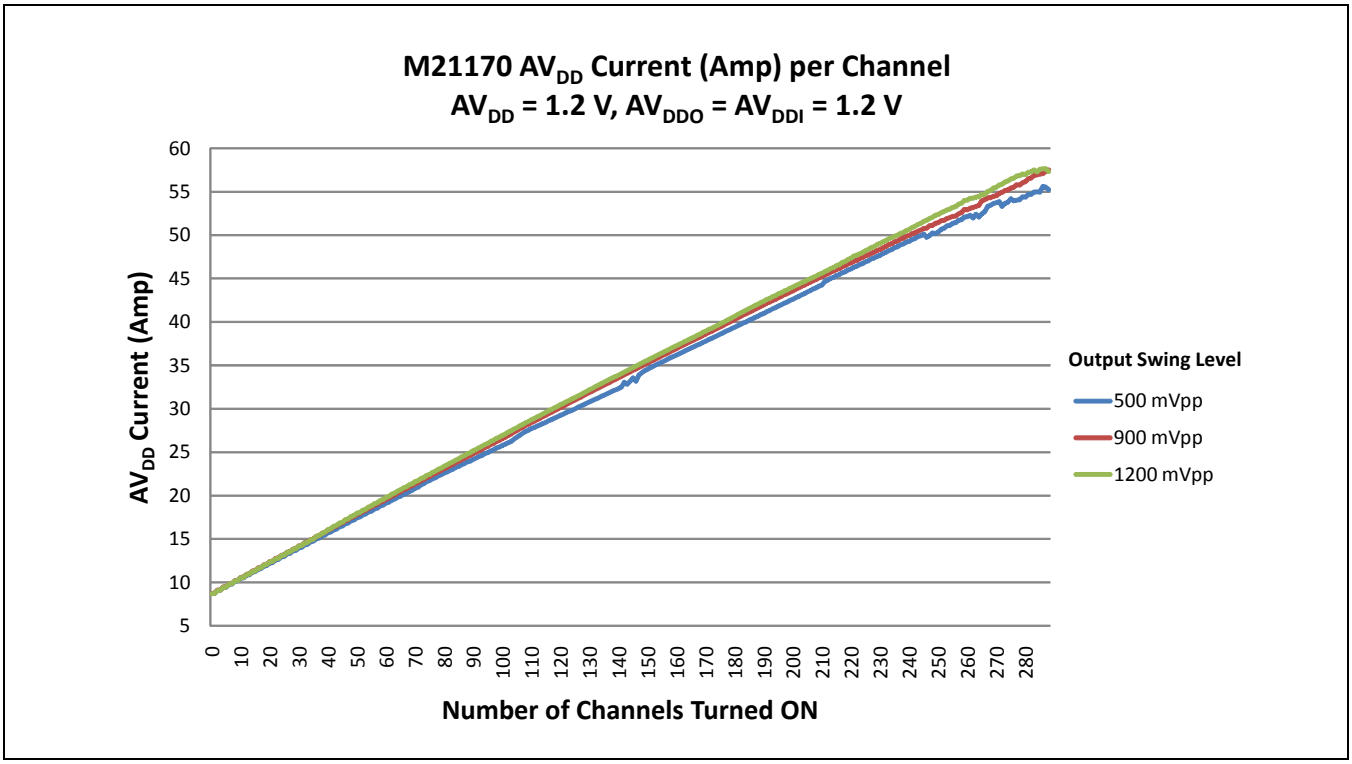


Figure 2-4. Typical Power Consumption for AV_{DDO} (1.2 V) Vs Number of Channels ON

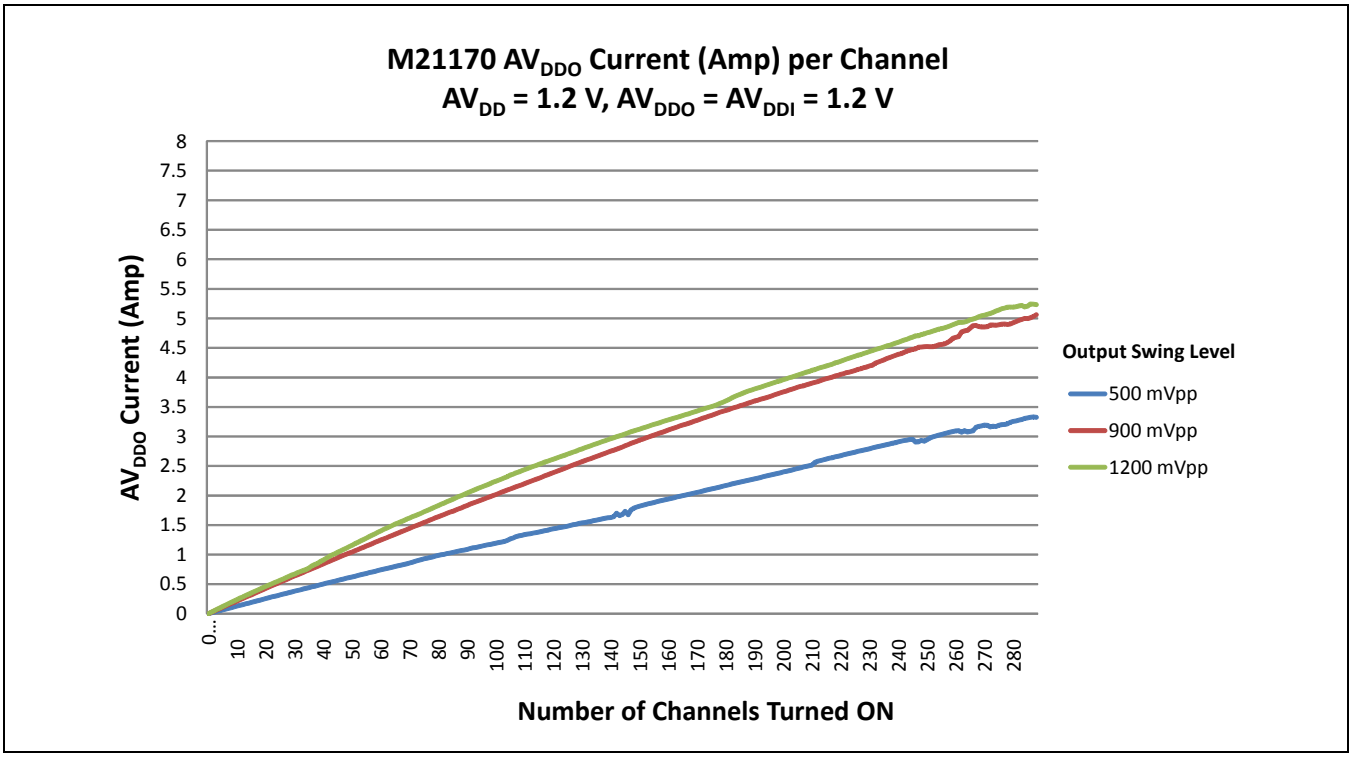


Figure 2-5. Input Equalization Level Vs Trace Length in Front of the M21170

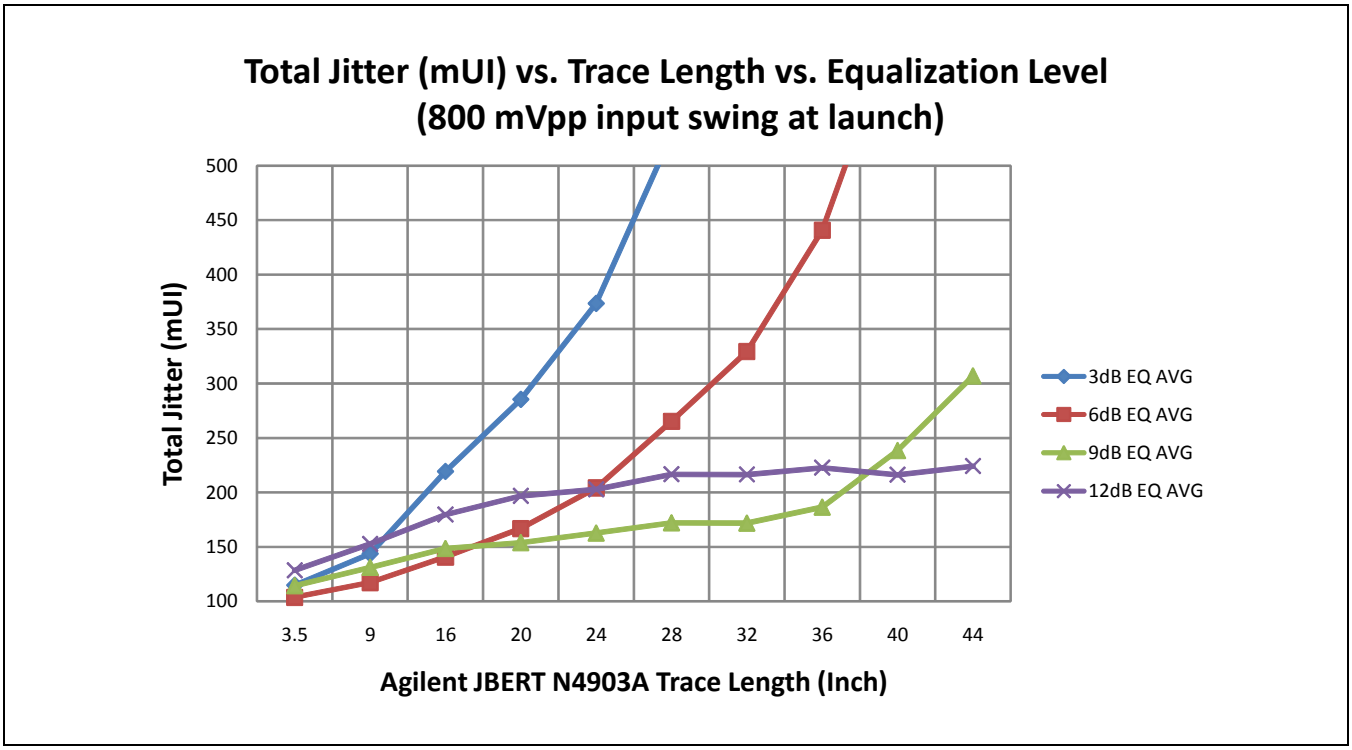
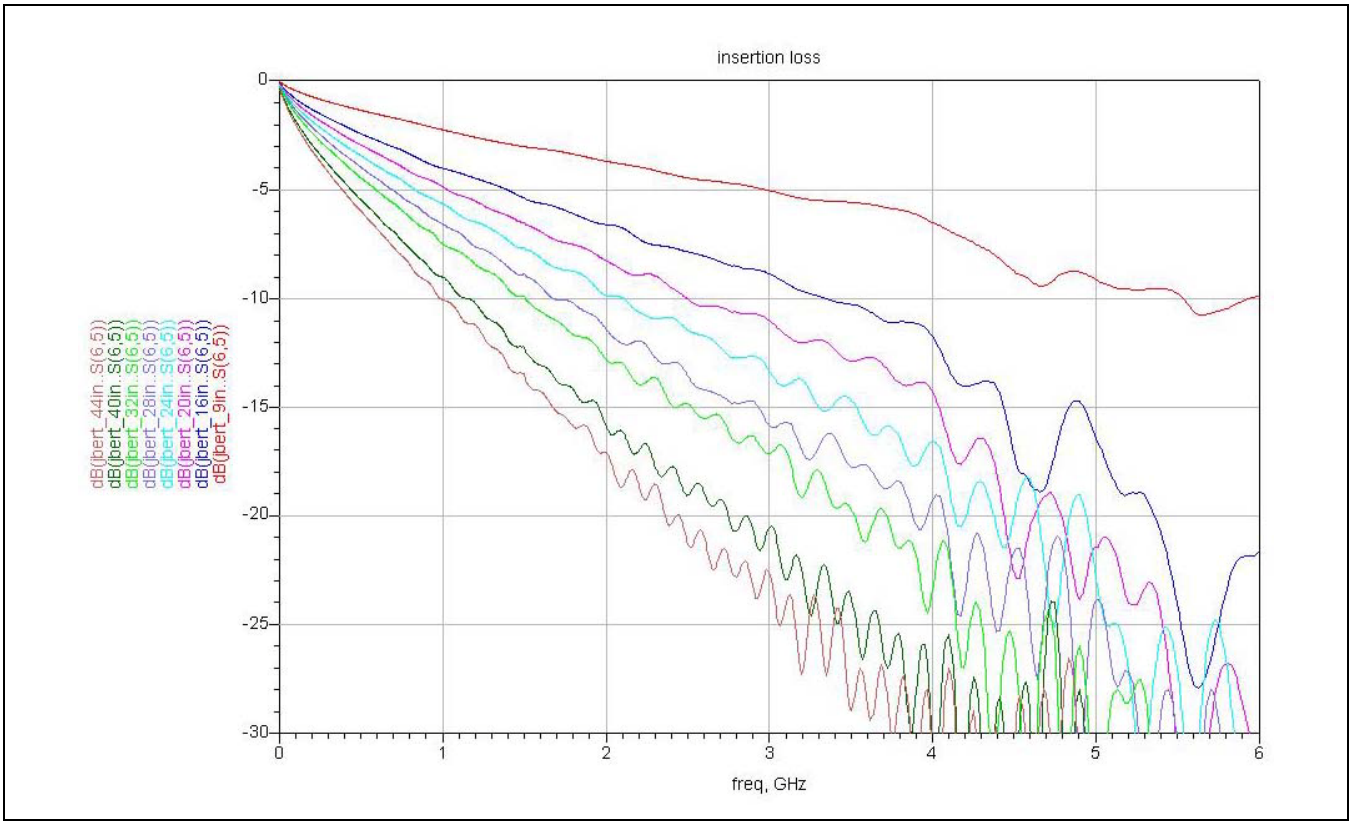


Figure 2-6. Agilent BERT N4903A FR4 Backplane Insertion Loss
These backplane traces were used to measure Input EQ on Figure 2-5



3.0 Pin Descriptions, Pinout Diagrams, and Package Outline Drawing

3.1 M21170 Pin Descriptions

Table 3-1. M21170 Power Pin Assignments (1 of 4)

Pin Name	Pin Numbers	Type	Description
AV_{DD}	AB16, AB28, AD21, AD33, AF26, AH19, AH31, AK24, Y17, Y29 AB17, AB29, AD22, AD34, AF27, AH20, AH32, AK25, Y18, Y30 AB18, AB30, AD23, AF16, AF28, AH21, AH33, AK26, Y19, Y31 AB19, AB31, AD24, AF17, AF29, AH22, AH34, AK27, Y20, Y32 AB20, AB32, AD25, AF18, AF30, AH23, AK16, AK28, Y21, Y33 AB21, AB33, AD26, AF19, AF31, AH24, AK17, AK29, Y22, Y34 AB22, AB34, AD27, AF20, AF32, AH25, AK18, AK30, Y23, AB23, AD16, AD28, AF21, AF33, AH26, AK19, AK31, Y24, AB24, AD17, AD29, AF22, AF34, AH27, AK20, AK32, Y25, AB25, AD18, AD30, AF23, AH16, AH28, AK21, AK33, Y26, AB26, AD19, AD31, AF24, AH17, AH29, AK22, AK34, Y27, AB27, AD20, AD32, AF25, AH18, AH30, AK23, Y16, Y28	Power	Analog positive supply
AV_{DDI}	AA12, AC12, AE12, AG12, AJ12, AL12, AT47, BF3, P3, W44 AA13, AC13, AE13, AG13, AJ13, AL38, AT9, D47, P41, W6 AA14, AC14, AE14, AG14, AJ14, AL44, AU12, F3, P47, Y3 AA15, AC15, AE15, AG15, AJ15, AL6, AU38, F47, P9, Y41 AA16, AC16, AE16, AG16, AJ16, AM3, AU44, G44, R12, Y47 AA17, AC17, AE17, AG17, AJ17, AM41, AU6, H3, R38, Y9 AA18, AC18, AE18, AG18, AJ18, AM47, AV3, H47, R44, AA19, AC19, AE19, AG19, AJ19, AM9, AV41, J44, R6, AA31, AC31, AE31, AG31, AJ31, AN12, AV47, J6, T3, AA32, AC32, AE32, AG32, AJ32, AN38, AV9, K3, T41, AA33, AC33, AE33, AG33, AJ33, AN44, AW44, K41, T47, AA34, AC34, AE34, AG34, AJ34, AN6, AW6, K47, T9, AA35, AC35, AE35, AG35, AJ35, AP3, AY3, L44, U12, AA36, AC36, AE36, AG36, AJ36, AP41, AY47, L6, U38, AA37, AC37, AE37, AG37, AJ37, AP47, AY9, M3, U44, AA38, AC38, AE38, AG38, AJ38, AP9, BA44, M41, U6, AA44, AC44, AE44, AG44, AJ44, AR12, BA6, M47, V3, AA6, AC6, AE6, AG6, AJ6, AR38, BB3, M9, V41, AB3, AD3, AF3, AH3, AK3, AR44, BB47, N12, V47, AB41, AD41, AF41, AH41, AK41, AR6, BC6, N38, V9, AB47, W12, W38, N44, N6, BD3, BD47, AT3, AT41, AK47, AK9, AH47, AH9, AF47, AF9, AD47, AD9, AB9	Power	Analog positive supply

Table 3-1. M21170 Power Pin Assignments (2 of 4)

Pin Name	Pin Numbers	Type	Description
AV_{DDO}	AM21, AT23, AV37, BD21, BG26, C24, F23, J28, N25, U27 AM23, AT25, BA12, BD23, BG28, C26, F25, J30, N27, U29 AM25, AT27, BA14, BD25, BG30, C28, F27, J32, N29, V21 AM27, AT29, BA16, BD27, BG32, C30, F29, J34, P21, V23 AM29, AU21, BA18, BD29, BG34, C32, F31, J36, P23, V25 AN21, AU23, BA20, BD31, BG36, C34, F33, J38, P25, V27 AN23, AU25, BA22, BD33, BG38, C36, F35, M13, P27, V29 AN25, AU27, BA24, BD35, BG4, C38, F37, M15, P29, AN27, AU29, BA26, BD37, BG40, C4, F39, M17, R21, AN29, AV13, BA28, BD39, BG42, C40, F41, M19, R23, AP21, AV15, BA30, BD41, BG44, C42, F7, M21, R25, AP23, AV17, BA32, BD43, BG46, C44, F9, M23, R27, AP25, AV19, BA34, BD9, BG6, C46, J10, M25, R29, AP27, AV21, BA36, BG10, BG8, C6, J12, M27, T21, AP29, AV23, BA38, BG12, C10, C8, J14, M29, T23, AR21, AV25, BA40, BG14, C12, F11, J16, M31, T25, AR23, AV27, BD11, BG16, C14, F13, J18, M33, T27, AR25, AV29, BD13, BG18, C16, F15, J20, M35, T29, AR27, AV31, BD15, BG20, C18, F17, J22, M37, U21, AR29, AV33, BD17, BG22, C20, F19, J24, N21, U23, AT21, AV35, BD19, BG24, C22, F21, J26, N23, U25	Power	Analog positive supply
DV_{DDIO}	AM18, AM19, V18, V19, V32, W18, W19	Power	Digital positive supply

Table 3-1. M21170 Power Pin Assignments (3 of 4)

Pin Name	Pin Numbers	Type	Description
V_{SS}	A3, AF36, AL30, AP44, AV38, BE6, E47, M30, T6, Y37 A46, AF37, AL31, AP6, AV39, BF47, F10, M32, U16, Y38 A47, AF38, AL32, AR15, AV40, BF48, F12, M34, U17, Y44 AA20, AF44, AL33, AR16, AV44, BF49, F14, M36, U18, Y6 AA21, AF6, AL34, AR17, AV6, BF6, F16, M38, U19, AA22, AG20, AL35, AR18, AW12, BG1, F18, M44, U20, AA23, AG21, AL36, AR19, AW3, BG11, F20, M6, U22, AA24, AG22, AL37, AR20, AW41, BG13, F22, N19, U24, AA25, AG23, AL41, AR22, AW47, BG15, F24, N20, U26, AA26, AG24, AL47, AR24, AW9, BG17, F26, N22, U28, AA27, AG25, AL9, AR26, AY12, BG19, F28, N24, U3, AA28, AG26, AM12, AR28, AY41, BG2, F30, N26, U30, AA29, AG27, AM13, AR3, AY44, BG21, F32, N28, U31, AA3, AG28, AM14, AR30, AY6, BG23, F34, N3, U32, AA30, AG29, AM15, AR31, B2, BG25, F36, N30, U33, AA41, AG3, AM16, AR32, B3, BG27, F38, N31, U34, AA47, AG30, AM17, AR33, B46, BG29, F4, N32, U35, AA9, AG41, AM20, AR34, B47, BG3, F40, N33, U36, AB12, AG47, AM22, AR37, B48, BG31, F42, N34, U37, AB13, AG9, AM24, AR41, BA10, BG33, F43, N41, U41, AB14, AH12, AM26, AR47, AB15, AB35, AB36, AB37, AB38, AB44, AB6, AC20, AC21, AC22, AC23, AC24, AC25, AC26, AC27, AC28, AC29, AC3, AC30, AC41, AC47, AC9, AD12, AD13, AD14, AD15, AD35, AD36, AD37, AD38, AD44, AD6, AE20, AE21, AE22, AE23, AE24, AE25, AE26, AE27, AE28, AE29, AE3, AE30, AE41, AE47, AE9, AF12, AF13, AF14, AF15, AF35, AH13, AH14, AH15, AH35, AH36, AH37, AH38, AH44, AH6, AJ20, AJ21, AJ22, AJ23, AJ24, AJ25, AJ26, AJ27, AJ28, AJ29, AJ3, AJ30, J41, AJ47, AJ9, AK12, AK13, AK14, AK15, AK35, AK36, AK37, AK38, AK44, AK6, AL13, AL14, AL15, AL16, AL17, AL18, AL19, AL20, AL21, AL22, AL23, L24, AL25, AL26, AL27, AL28, AL29, AL3, AM28, AM30, AM31, AM32, AM34, AM35, AM36, AM37, AM38, AM44, AM6, AN13, AN14, AN15, AN16, AN17, AN18, AN19, AN20, AN22, AN24, AN26, AN28, AN3, AN30,	Power	Ground

Table 3-1. M21170 Power Pin Assignments (4 of 4)

Pin Name	Pin Numbers	Type	Description
V_{SS} *(continued)*	AN31, AN32, AN34, AN35, AN36, AN37, AN41, AN47, AN9, AP12, AP14, AP15, AP18, AP19, AP20, AP22, AP24, AP26, AP28, AP30, AP31, AP32, AP33, AP34, AP36, AP37, AP38, AR9, AT12, AT17, AT18, AT19, AT20, AT22, AT24, AT26, AT28, AT30, AT31, AT32, AT33, AT34, AT35, AT37, AT38, AT44, AT6, AU18, AU19, AU20, AU22, AU24, AU26, AU28, AU3, AU30, AU31, AU32, AU33, AU34, AU35, AU36, AU37, AU41, AU47, AU9, AV12, AV14, AV16, AV18, AV20, AV22, AV24, AV26, AV28, AV30, AV32, AV34, AV36, BA11, BA13, BA15, BA17, BA19, BA21, BA23, BA25, BA27, BA29, BA3, BA31, BA33, BA35, BA37, BA39, BA41, BA42, BA43, BA47, BA9, BB44, BB6, BB9, BC3, BC44, BC47, BC9, BD10, BD12, BD14, BD16, BD18, BD20, BD22, BD24, BD26, BD28, BD30, BD32, BD34, BD36, BD38, BD40, BD42, BD44, BD45, BD46, BD6, BD7, BD8, BE3, BE47, BG35, BG37, BG39, BG41, BG43, BG45, BG47, BG48, BG49, BG5, BG7, BG9, BH2, BH3, BH4, BH47, BH48, BJ3, BJ4, BJ47, C1, C11, C13, C15, C17, C19, C2, C21, C23, C25, C27, C29, C3, C31, C33, C35, C37, C39, C41, C43, C45, C47, C48, C49, C5, C7, C9, D1, D2, D3, D44, E3, E44, F44, F5, F6, F8, G3, G41, G47, G6, H41, H44, H6, J11, J13, J15, J17, J19, J21, J23, J25, J27, J29, J3, J31, J33, J35, J37, J39, J40, J41, J47, J7, J8, J9, K38, K44, K6, K9, L3, L38, L41, L47, L9, M10, M11, M12, M14, M16, M18, M20, M22, M24, M26, M28, N47, N9, P12, P18, P19, P20, P22, P24, P26, P28, P30, P31, P32, P33, P34, P36, P38, P44, P6, R18, R19, R20, R22, R24, R26, R28, R3, R30, R31, R32, R33, R34, R36, R41, R47, R9, T12, T16, T17, T18, T19, T20, T22, T24, T26, T28, T30, T31, T32, T35, T36, T38, T44, U47, U9, V12, V16, V17, V20, V22, V24, V26, V28, V30, V31, V33, V34, V35, V36, V37, V38, V44, V6, W13, W14, W15, W16, W17, W20, W21, W22, W23, W24, W25, W26, W27, W28, W29, W3, W30, W31, W32, W33, W34, W35, W36, W37, W41, W47, W9, Y12, Y13, Y14, Y15, Y35, Y36	Power	Ground

Table 3-2. M21170 Data Pin Assignments (1 of 13)

Pin Name	Pin Numbers	Type	Description
INP_0, INN_0	D49, D48	PCML input	Data input lane 0; true/complement
INP_1, INN_1	E1, E2	PCML input	Data input lane 1; true/complement
INP_2, INN_2	D46, D45	PCML input	Data input lane 2; true/complement
INP_3, INN_3	G4, G5	PCML input	Data input lane 3; true/complement
INP_4, INN_4	K40, K39	PCML input	Data input lane 4; true/complement
INP_5, INN_5	K7, K8	PCML input	Data input lane 5; true/complement
INP_6, INN_6	E49, E48	PCML input	Data input lane 6; true/complement
INP_7, INN_7	F1, F2	PCML input	Data input lane 7; true/complement
INP_8, INN_8	E46, E45	PCML input	Data input lane 8; true/complement
INP_9, INN_9	H4, H5	PCML input	Data input lane 9; true/complement
INP_10, INN_10	G43, G42	PCML input	Data input lane 10; true/complement
INP_11, INN_11	N10, N11	PCML input	Data input lane 11; true/complement
INP_12, INN_12	F49, F48	PCML input	Data input lane 12; true/complement
INP_13, INN_13	G1, G2	PCML input	Data input lane 13; true/complement

Table 3-2. M21170 Data Pin Assignments (2 of 13)

Pin Name	Pin Numbers	Type	Description
INP_14, INN_14	F46, F45	PCML input	Data input lane 14; true/complement
INP_15, INN_15	J4, J5	PCML input	Data input lane 15; true/complement
INP_16, INN_16	L40, L39	PCML input	Data input lane 16; true/complement
INP_17, INN_17	L7, L8	PCML input	Data input lane 17; true/complement
INP_18, INN_18	G49, G48	PCML input	Data input lane 18; true/complement
INP_19, INN_19	H1, H2	PCML input	Data input lane 19; true/complement
INP_20, INN_20	G46, G45	PCML input	Data input lane 20; true/complement
INP_21, INN_21	K4, K5	PCML input	Data input lane 21; true/complement
INP_22, INN_22	H43, H42	PCML input	Data input lane 22; true/complement
INP_23, INN_23	P10, P11	PCML input	Data input lane 23; true/complement
INP_24, INN_24	H49, H48	PCML input	Data input lane 24; true/complement
INP_25, INN_25	J1, J2	PCML input	Data input lane 25; true/complement
INP_26, INN_26	H46, H45	PCML input	Data input lane 26; true/complement
INP_27, INN_27	L4, L5	PCML input	Data input lane 27; true/complement
INP_28, INN_28	M40, M39	PCML input	Data input lane 28; true/complement
INP_29, INN_29	M7, M8	PCML input	Data input lane 29; true/complement
INP_30, INN_30	J49, J48	PCML input	Data input lane 30; true/complement
INP_31, INN_31	K1, K2	PCML input	Data input lane 31; true/complement
INP_32, INN_32	J46, J45	PCML input	Data input lane 32; true/complement
INP_33, INN_33	M4, M5	PCML input	Data input lane 33; true/complement
INP_34, INN_34	J43, J42	PCML input	Data input lane 34; true/complement
INP_35, INN_35	R10, R11	PCML input	Data input lane 35; true/complement
INP_36, INN_36	K49, K48	PCML input	Data input lane 36; true/complement
INP_37, INN_37	L1, L2	PCML input	Data input lane 37; true/complement
INP_38, INN_38	K46, K45	PCML input	Data input lane 38; true/complement
INP_39, INN_39	N4, N5	PCML input	Data input lane 39; true/complement
INP_40, INN_40	N40, N39	PCML input	Data input lane 40; true/complement
INP_41, INN_41	N7, N8	PCML input	Data input lane 41; true/complement
INP_42, INN_42	L49, L48	PCML input	Data input lane 42; true/complement
INP_43, INN_43	M1, M2	PCML input	Data input lane 43; true/complement
INP_44, INN_44	L46, L45	PCML input	Data input lane 44; true/complement
INP_45, INN_45	P4, P5	PCML input	Data input lane 45; true/complement
INP_46, INN_46	K43, K42	PCML input	Data input lane 46; true/complement
INP_47, INN_47	T10, T11	PCML input	Data input lane 47; true/complement
INP_48, INN_48	M49, M48	PCML input	Data input lane 48; true/complement
INP_49, INN_49	N1, N2	PCML input	Data input lane 49; true/complement
INP_50, INN_50	M46, M45	PCML input	Data input lane 50; true/complement
INP_51, INN_51	R4, R5	PCML input	Data input lane 51; true/complement
INP_52, INN_52	P40, P39	PCML input	Data input lane 52; true/complement
INP_53, INN_53	P7, P8	PCML input	Data input lane 53; true/complement
INP_54, INN_54	N49, N48	PCML input	Data input lane 54; true/complement
INP_55, INN_55	P1, P2	PCML input	Data input lane 55; true/complement
INP_56, INN_56	N46, N45	PCML input	Data input lane 56; true/complement
INP_57, INN_57	T4, T5	PCML input	Data input lane 57; true/complement
INP_58, INN_58	L43, L42	PCML input	Data input lane 58; true/complement
INP_59, INN_59	U10, U11	PCML input	Data input lane 59; true/complement
INP_60, INN_60	P49, P48	PCML input	Data input lane 60; true/complement
INP_61, INN_61	R1, R2	PCML input	Data input lane 61; true/complement

Table 3-2. M21170 Data Pin Assignments (3 of 13)

Pin Name	Pin Numbers	Type	Description
INP_62, INN_62	P46, P45	PCML input	Data input lane 62; true/complement
INP_63, INN_63	U4, U5	PCML input	Data input lane 63; true/complement
INP_64, INN_64	R40, R39	PCML input	Data input lane 64; true/complement
INP_65, INN_65	R7, R8	PCML input	Data input lane 65; true/complement
INP_66, INN_66	R49, R48	PCML input	Data input lane 66; true/complement
INP_67, INN_67	T1, T2	PCML input	Data input lane 67; true/complement
INP_68, INN_68	R46, R45	PCML input	Data input lane 68; true/complement
INP_69, INN_69	W7, W8	PCML input	Data input lane 69; true/complement
INP_70, INN_70	M43, M42	PCML input	Data input lane 70; true/complement
INP_71, INN_71	V10, V11	PCML input	Data input lane 71; true/complement
INP_72, INN_72	T49, T48	PCML input	Data input lane 72; true/complement
INP_73, INN_73	U1, U2	PCML input	Data input lane 73; true/complement
INP_74, INN_74	V43, V42	PCML input	Data input lane 74; true/complement
INP_75, INN_75	V4, V5	PCML input	Data input lane 75; true/complement
INP_76, INN_76	T40, T39	PCML input	Data input lane 76; true/complement
INP_77, INN_77	T7, T8	PCML input	Data input lane 77; true/complement
INP_78, INN_78	U49, U48	PCML input	Data input lane 78; true/complement
INP_79, INN_79	V1, V2	PCML input	Data input lane 79; true/complement
INP_80, INN_80	T46, T45	PCML input	Data input lane 80; true/complement
INP_81, INN_81	Y7, Y8	PCML input	Data input lane 81; true/complement
INP_82, INN_82	N43, N42	PCML input	Data input lane 82; true/complement
INP_83, INN_83	W10, W11	PCML input	Data input lane 83; true/complement
INP_84, INN_84	V49, V48	PCML input	Data input lane 84; true/complement
INP_85, INN_85	W1, W2	PCML input	Data input lane 85; true/complement
INP_86, INN_86	W43, W42	PCML input	Data input lane 86; true/complement
INP_87, INN_87	W4, W5	PCML input	Data input lane 87; true/complement
INP_88, INN_88	U40, U39	PCML input	Data input lane 88; true/complement
INP_89, INN_89	U7, U8	PCML input	Data input lane 89; true/complement
INP_90, INN_90	W49, W48	PCML input	Data input lane 90; true/complement
INP_91, INN_91	Y1, Y2	PCML input	Data input lane 91; true/complement
INP_92, INN_92	U46, U45	PCML input	Data input lane 92; true/complement
INP_93, INN_93	AA7, AA8	PCML input	Data input lane 93; true/complement
INP_94, INN_94	P43, P42	PCML input	Data input lane 94; true/complement
INP_95, INN_95	Y10, Y11	PCML input	Data input lane 95; true/complement
INP_96, INN_96	Y49, Y48	PCML input	Data input lane 96; true/complement
INP_97, INN_97	AA1, AA2	PCML input	Data input lane 97; true/complement
INP_98, INN_98	Y43, Y42	PCML input	Data input lane 98; true/complement
INP_99, INN_99	Y4, Y5	PCML input	Data input lane 99; true/complement
INP_100, INN_100	V40, V39	PCML input	Data input lane 100; true/complement
INP_101, INN_101	V7, V8	PCML input	Data input lane 101; true/complement
INP_102, INN_102	AA49, AA48	PCML input	Data input lane 102; true/complement
INP_103, INN_103	AB1, AB2	PCML input	Data input lane 103; true/complement
INP_104, INN_104	V46, V45	PCML input	Data input lane 104; true/complement
INP_105, INN_105	AB7, AB8	PCML input	Data input lane 105; true/complement
INP_106, INN_106	R43, R42	PCML input	Data input lane 106; true/complement
INP_107, INN_107	AA10, AA11	PCML input	Data input lane 107; true/complement
INP_108, INN_108	AB46, AB45	PCML input	Data input lane 108; true/complement
INP_109, INN_109	AC1, AC2	PCML input	Data input lane 109; true/complement

Table 3-2. M21170 Data Pin Assignments (4 of 13)

Pin Name	Pin Numbers	Type	Description
INP_110, INN_110	AA43, AA42	PCML input	Data input lane 110; true/complement
INP_111, INN_111	AA4, AA5	PCML input	Data input lane 111; true/complement
INP_112, INN_112	W40, W39	PCML input	Data input lane 112; true/complement
INP_113, INN_113	AB10, AB11	PCML input	Data input lane 113; true/complement
INP_114, INN_114	AB49, AB48	PCML input	Data input lane 114; true/complement
INP_115, INN_115	AC4, AC5	PCML input	Data input lane 115; true/complement
INP_116, INN_116	W46, W45	PCML input	Data input lane 116; true/complement
INP_117, INN_117	AC7, AC8	PCML input	Data input lane 117; true/complement
INP_118, INN_118	T43, T42	PCML input	Data input lane 118; true/complement
INP_119, INN_119	AC10, AC11	PCML input	Data input lane 119; true/complement
INP_120, INN_120	AC46, AC45	PCML input	Data input lane 120; true/complement
INP_121, INN_121	AD1, AD2	PCML input	Data input lane 121; true/complement
INP_122, INN_122	AB43, AB42	PCML input	Data input lane 122; true/complement
INP_123, INN_123	AB4, AB5	PCML input	Data input lane 123; true/complement
INP_124, INN_124	Y40, Y39	PCML input	Data input lane 124; true/complement
INP_125, INN_125	AD10, AD11	PCML input	Data input lane 125; true/complement
INP_126, INN_126	AC49, AC48	PCML input	Data input lane 126; true/complement
INP_127, INN_127	AD4, AD5	PCML input	Data input lane 127; true/complement
INP_128, INN_128	Y46, Y45	PCML input	Data input lane 128; true/complement
INP_129, INN_129	AD7, AD8	PCML input	Data input lane 129; true/complement
INP_130, INN_130	U43, U42	PCML input	Data input lane 130; true/complement
INP_131, INN_131	AE10, AE11	PCML input	Data input lane 131; true/complement
INP_132, INN_132	AD46, AD45	PCML input	Data input lane 132; true/complement
INP_133, INN_133	AE1, AE2	PCML input	Data input lane 133; true/complement
INP_134, INN_134	AC43, AC42	PCML input	Data input lane 134; true/complement
INP_135, INN_135	AE7, AE8	PCML input	Data input lane 135; true/complement
INP_136, INN_136	AA40, AA39	PCML input	Data input lane 136; true/complement
INP_137, INN_137	AF10, AF11	PCML input	Data input lane 137; true/complement
INP_138, INN_138	AD49, AD48	PCML input	Data input lane 138; true/complement
INP_139, INN_139	AE4, AE5	PCML input	Data input lane 139; true/complement
INP_140, INN_140	AA46, AA45	PCML input	Data input lane 140; true/complement
INP_141, INN_141	AF7, AF8	PCML input	Data input lane 141; true/complement
INP_142, INN_142	AB40, AB39	PCML input	Data input lane 142; true/complement
INP_143, INN_143	AG10, AG11	PCML input	Data input lane 143; true/complement
INP_144, INN_144	AE46, AE45	PCML input	Data input lane 144; true/complement
INP_145, INN_145	AF1, AF2	PCML input	Data input lane 145; true/complement
INP_146, INN_146	AD43, AD42	PCML input	Data input lane 146; true/complement
INP_147, INN_147	AJ4, AJ5	PCML input	Data input lane 147; true/complement
INP_148, INN_148	AC40, AC39	PCML input	Data input lane 148; true/complement
INP_149, INN_149	AH10, AH11	PCML input	Data input lane 149; true/complement
INP_150, INN_150	AE49, AE48	PCML input	Data input lane 150; true/complement
INP_151, INN_151	AF4, AF5	PCML input	Data input lane 151; true/complement
INP_152, INN_152	AE43, AE42	PCML input	Data input lane 152; true/complement
INP_153, INN_153	AG7, AG8	PCML input	Data input lane 153; true/complement
INP_154, INN_154	AD40, AD39	PCML input	Data input lane 154; true/complement
INP_155, INN_155	AJ10, AJ11	PCML input	Data input lane 155; true/complement
INP_156, INN_156	AF46, AF45	PCML input	Data input lane 156; true/complement
INP_157, INN_157	AG1, AG2	PCML input	Data input lane 157; true/complement

Table 3-2. M21170 Data Pin Assignments (5 of 13)

Pin Name	Pin Numbers	Type	Description
INP_158, INN_158	AF43, AF42	PCML input	Data input lane 158; true/complement
INP_159, INN_159	AK4, AK5	PCML input	Data input lane 159; true/complement
INP_160, INN_160	AE40, AE39	PCML input	Data input lane 160; true/complement
INP_161, INN_161	AN7, AN8	PCML input	Data input lane 161; true/complement
INP_162, INN_162	AF49, AF48	PCML input	Data input lane 162; true/complement
INP_163, INN_163	AG4, AG5	PCML input	Data input lane 163; true/complement
INP_164, INN_164	AH46, AH45	PCML input	Data input lane 164; true/complement
INP_165, INN_165	AH7, AH8	PCML input	Data input lane 165; true/complement
INP_166, INN_166	AF40, AF39	PCML input	Data input lane 166; true/complement
INP_167, INN_167	AK10, AK11	PCML input	Data input lane 167; true/complement
INP_168, INN_168	AG46, AG45	PCML input	Data input lane 168; true/complement
INP_169, INN_169	AH1, AH2	PCML input	Data input lane 169; true/complement
INP_170, INN_170	AG43, AG42	PCML input	Data input lane 170; true/complement
INP_171, INN_171	AL4, AL5	PCML input	Data input lane 171; true/complement
INP_172, INN_172	AG40, AG39	PCML input	Data input lane 172; true/complement
INP_173, INN_173	AP7, AP8	PCML input	Data input lane 173; true/complement
INP_174, INN_174	AG49, AG48	PCML input	Data input lane 174; true/complement
INP_175, INN_175	AH4, AH5	PCML input	Data input lane 175; true/complement
INP_176, INN_176	AJ46, AJ45	PCML input	Data input lane 176; true/complement
INP_177, INN_177	AJ7, AJ8	PCML input	Data input lane 177; true/complement
INP_178, INN_178	AH40, AH39	PCML input	Data input lane 178; true/complement
INP_179, INN_179	AL10, AL11	PCML input	Data input lane 179; true/complement
INP_180, INN_180	AH49, AH48	PCML input	Data input lane 180; true/complement
INP_181, INN_181	AJ1, AJ2	PCML input	Data input lane 181; true/complement
INP_182, INN_182	AH43, AH42	PCML input	Data input lane 182; true/complement
INP_183, INN_183	AM4, AM5	PCML input	Data input lane 183; true/complement
INP_184, INN_184	AJ40, AJ39	PCML input	Data input lane 184; true/complement
INP_185, INN_185	AR7, AR8	PCML input	Data input lane 185; true/complement
INP_186, INN_186	AJ49, AJ48	PCML input	Data input lane 186; true/complement
INP_187, INN_187	AK1, AK2	PCML input	Data input lane 187; true/complement
INP_188, INN_188	AK46, AK45	PCML input	Data input lane 188; true/complement
INP_189, INN_189	AK7, AK8	PCML input	Data input lane 189; true/complement
INP_190, INN_190	AM43, AM42	PCML input	Data input lane 190; true/complement
INP_191, INN_191	AM10, AM11	PCML input	Data input lane 191; true/complement
INP_192, INN_192	AK49, AK48	PCML input	Data input lane 192; true/complement
INP_193, INN_193	AL1, AL2	PCML input	Data input lane 193; true/complement
INP_194, INN_194	AJ43, AJ42	PCML input	Data input lane 194; true/complement
INP_195, INN_195	AN4, AN5	PCML input	Data input lane 195; true/complement
INP_196, INN_196	AK40, AK39	PCML input	Data input lane 196; true/complement
INP_197, INN_197	AT7, AT8	PCML input	Data input lane 197; true/complement
INP_198, INN_198	AL49, AL48	PCML input	Data input lane 198; true/complement
INP_199, INN_199	AM1, AM2	PCML input	Data input lane 199; true/complement
INP_200, INN_200	AL46, AL45	PCML input	Data input lane 200; true/complement
INP_201, INN_201	AL7, AL8	PCML input	Data input lane 201; true/complement
INP_202, INN_202	AN43, AN42	PCML input	Data input lane 202; true/complement
INP_203, INN_203	AN10, AN11	PCML input	Data input lane 203; true/complement
INP_204, INN_204	AM49, AM48	PCML input	Data input lane 204; true/complement
INP_205, INN_205	AN1, AN2	PCML input	Data input lane 205; true/complement

Table 3-2. M21170 Data Pin Assignments (6 of 13)

Pin Name	Pin Numbers	Type	Description
INP_206, INN_206	AK43, AK42	PCML input	Data input lane 206; true/complement
INP_207, INN_207	AP4, AP5	PCML input	Data input lane 207; true/complement
INP_208, INN_208	AL40, AL39	PCML input	Data input lane 208; true/complement
INP_209, INN_209	AU7, AU8	PCML input	Data input lane 209; true/complement
INP_210, INN_210	AN49, AN48	PCML input	Data input lane 210; true/complement
INP_211, INN_211	AP1, AP2	PCML input	Data input lane 211; true/complement
INP_212, INN_212	AM46, AM45	PCML input	Data input lane 212; true/complement
INP_213, INN_213	AM7, AM8	PCML input	Data input lane 213; true/complement
INP_214, INN_214	AP43, AP42	PCML input	Data input lane 214; true/complement
INP_215, INN_215	AP10, AP11	PCML input	Data input lane 215; true/complement
INP_216, INN_216	AP49, AP48	PCML input	Data input lane 216; true/complement
INP_217, INN_217	AR1, AR2	PCML input	Data input lane 217; true/complement
INP_218, INN_218	AL43, AL42	PCML input	Data input lane 218; true/complement
INP_219, INN_219	AR4, AR5	PCML input	Data input lane 219; true/complement
INP_220, INN_220	AM40, AM39	PCML input	Data input lane 220; true/complement
INP_221, INN_221	AV7, AV8	PCML input	Data input lane 221; true/complement
INP_222, INN_222	AR49, AR48	PCML input	Data input lane 222; true/complement
INP_223, INN_223	AT1, AT2	PCML input	Data input lane 223; true/complement
INP_224, INN_224	AN46, AN45	PCML input	Data input lane 224; true/complement
INP_225, INN_225	AT4, AT5	PCML input	Data input lane 225; true/complement
INP_226, INN_226	AR43, AR42	PCML input	Data input lane 226; true/complement
INP_227, INN_227	AR10, AR11	PCML input	Data input lane 227; true/complement
INP_228, INN_228	AT49, AT48	PCML input	Data input lane 228; true/complement
INP_229, INN_229	AU1, AU2	PCML input	Data input lane 229; true/complement
INP_230, INN_230	AP46, AP45	PCML input	Data input lane 230; true/complement
INP_231, INN_231	AU4, AU5	PCML input	Data input lane 231; true/complement
INP_232, INN_232	AN40, AN39	PCML input	Data input lane 232; true/complement
INP_233, INN_233	AW7, AW8	PCML input	Data input lane 233; true/complement
INP_234, INN_234	AU49, AU48	PCML input	Data input lane 234; true/complement
INP_235, INN_235	AV1, AV2	PCML input	Data input lane 235; true/complement
INP_236, INN_236	AR46, AR45	PCML input	Data input lane 236; true/complement
INP_237, INN_237	AV4, AV5	PCML input	Data input lane 237; true/complement
INP_238, INN_238	AT43, AT42	PCML input	Data input lane 238; true/complement
INP_239, INN_239	AT10, AT11	PCML input	Data input lane 239; true/complement
INP_240, INN_240	AV49, AV48	PCML input	Data input lane 240; true/complement
INP_241, INN_241	AW1, AW2	PCML input	Data input lane 241; true/complement
INP_242, INN_242	AT46, AT45	PCML input	Data input lane 242; true/complement
INP_243, INN_243	AW4, AW5	PCML input	Data input lane 243; true/complement
INP_244, INN_244	AP40, AP39	PCML input	Data input lane 244; true/complement
INP_245, INN_245	AY7, AY8	PCML input	Data input lane 245; true/complement
INP_246, INN_246	AW49, AW48	PCML input	Data input lane 246; true/complement
INP_247, INN_247	AY1, AY2	PCML input	Data input lane 247; true/complement
INP_248, INN_248	AU46, AU45	PCML input	Data input lane 248; true/complement
INP_249, INN_249	AY4, AY5	PCML input	Data input lane 249; true/complement
INP_250, INN_250	AU43, AU42	PCML input	Data input lane 250; true/complement
INP_251, INN_251	AU10, AU11	PCML input	Data input lane 251; true/complement
INP_252, INN_252	AY49, AY48	PCML input	Data input lane 252; true/complement
INP_253, INN_253	BA1, BA2	PCML input	Data input lane 253; true/complement

Table 3-2. M21170 Data Pin Assignments (7 of 13)

Pin Name	Pin Numbers	Type	Description
INP_254, INN_254	AV46, AV45	PCML input	Data input lane 254; true/complement
INP_255, INN_255	BA4, BA5	PCML input	Data input lane 255; true/complement
INP_256, INN_256	AR40, AR39	PCML input	Data input lane 256; true/complement
INP_257, INN_257	BA7, BA8	PCML input	Data input lane 257; true/complement
INP_258, INN_258	BA49, BA48	PCML input	Data input lane 258; true/complement
INP_259, INN_259	BB1, BB2	PCML input	Data input lane 259; true/complement
INP_260, INN_260	AW46, AW45	PCML input	Data input lane 260; true/complement
INP_261, INN_261	BB4, BB5	PCML input	Data input lane 261; true/complement
INP_262, INN_262	AV43, AV42	PCML input	Data input lane 262; true/complement
INP_263, INN_263	AV10, AV11	PCML input	Data input lane 263; true/complement
INP_264, INN_264	BB49, BB48	PCML input	Data input lane 264; true/complement
INP_265, INN_265	BC1, BC2	PCML input	Data input lane 265; true/complement
INP_266, INN_266	AY46, AY45	PCML input	Data input lane 266; true/complement
INP_267, INN_267	BC4, BC5	PCML input	Data input lane 267; true/complement
INP_268, INN_268	AT40, AT39	PCML input	Data input lane 268; true/complement
INP_269, INN_269	BB7, BB8	PCML input	Data input lane 269; true/complement
INP_270, INN_270	BC49, BC48	PCML input	Data input lane 270; true/complement
INP_271, INN_271	BD1, BD2	PCML input	Data input lane 271; true/complement
INP_272, INN_272	BA46, BA45	PCML input	Data input lane 272; true/complement
INP_273, INN_273	BD4, BD5	PCML input	Data input lane 273; true/complement
INP_274, INN_274	AW43, AW42	PCML input	Data input lane 274; true/complement
INP_275, INN_275	AW10, AW11	PCML input	Data input lane 275; true/complement
INP_276, INN_276	BD49, BD48	PCML input	Data input lane 276; true/complement
INP_277, INN_277	BE1, BE2	PCML input	Data input lane 277; true/complement
INP_278, INN_278	BB46, BB45	PCML input	Data input lane 278; true/complement
INP_279, INN_279	BE4, BE5	PCML input	Data input lane 279; true/complement
INP_280, INN_280	AU40, AU39	PCML input	Data input lane 280; true/complement
INP_281, INN_281	BC7, BC8	PCML input	Data input lane 281; true/complement
INP_282, INN_282	BE49, BE48	PCML input	Data input lane 282; true/complement
INP_283, INN_283	BF1, BF2	PCML input	Data input lane 283; true/complement
INP_284, INN_284	BC46, BC45	PCML input	Data input lane 284; true/complement
INP_285, INN_285	BF4, BF5	PCML input	Data input lane 285; true/complement
INP_286, INN_286	AY43, AY42	PCML input	Data input lane 286; true/complement
INP_287, INN_287	AY10, AY11	PCML input	Data input lane 287; true/complement
INP_AUXE, INN_AUXE	AM33, AN33	PCML input	Data input lane AUXE; true/complement
INP_AUXO, INN_AUXO	AP16, AP17	PCML input	Data input lane AUXO; true/complement
OUTP_0, OUTN_0	A45, B45	PCML output	Data output lane 0; true/complement
OUTP_1, OUTN_1	BJ46, BH46	PCML output	Data output lane 1; true/complement
OUTP_2, OUTN_2	D43, E43	PCML output	Data output lane 2; true/complement
OUTP_3, OUTN_3	BF46, BE46	PCML output	Data output lane 3; true/complement
OUTP_4, OUTN_4	G40, H40	PCML output	Data output lane 4; true/complement
OUTP_5, OUTN_5	AY40, AW40	PCML output	Data output lane 5; true/complement
OUTP_6, OUTN_6	A44, B44	PCML output	Data output lane 6; true/complement
OUTP_7, OUTN_7	BJ45, BH45	PCML output	Data output lane 7; true/complement
OUTP_8, OUTN_8	D42, E42	PCML output	Data output lane 8; true/complement
OUTP_9, OUTN_9	BF45, BE45	PCML output	Data output lane 9; true/complement
OUTP_10, OUTN_10	K37, L37	PCML output	Data output lane 10; true/complement
OUTP_11, OUTN_11	BC43, BB43	PCML output	Data output lane 11; true/complement

Table 3-2. M21170 Data Pin Assignments (8 of 13)

Pin Name	Pin Numbers	Type	Description
OUTP_12, OUTN_12	A43, B43	PCML output	Data output lane 12; true/complement
OUTP_13, OUTN_13	BJ44, BH44	PCML output	Data output lane 13; true/complement
OUTP_14, OUTN_14	D41, E41	PCML output	Data output lane 14; true/complement
OUTP_15, OUTN_15	BF44, BE44	PCML output	Data output lane 15; true/complement
OUTP_16, OUTN_16	G39, H39	PCML output	Data output lane 16; true/complement
OUTP_17, OUTN_17	AY39, AW39	PCML output	Data output lane 17; true/complement
OUTP_18, OUTN_18	A42, B42	PCML output	Data output lane 18; true/complement
OUTP_19, OUTN_19	BJ43, BH43	PCML output	Data output lane 19; true/complement
OUTP_20, OUTN_20	D40, E40	PCML output	Data output lane 20; true/complement
OUTP_21, OUTN_21	BF43, BE43	PCML output	Data output lane 21; true/complement
OUTP_22, OUTN_22	K36, L36	PCML output	Data output lane 22; true/complement
OUTP_23, OUTN_23	BC42, BB42	PCML output	Data output lane 23; true/complement
OUTP_24, OUTN_24	A41, B41	PCML output	Data output lane 24; true/complement
OUTP_25, OUTN_25	BJ42, BH42	PCML output	Data output lane 25; true/complement
OUTP_26, OUTN_26	D39, E39	PCML output	Data output lane 26; true/complement
OUTP_27, OUTN_27	BF42, BE42	PCML output	Data output lane 27; true/complement
OUTP_28, OUTN_28	G38, H38	PCML output	Data output lane 28; true/complement
OUTP_29, OUTN_29	AY38, AW38	PCML output	Data output lane 29; true/complement
OUTP_30, OUTN_30	A40, B40	PCML output	Data output lane 30; true/complement
OUTP_31, OUTN_31	BJ41, BH41	PCML output	Data output lane 31; true/complement
OUTP_32, OUTN_32	D38, E38	PCML output	Data output lane 32; true/complement
OUTP_33, OUTN_33	BF41, BE41	PCML output	Data output lane 33; true/complement
OUTP_34, OUTN_34	K35, L35	PCML output	Data output lane 34; true/complement
OUTP_35, OUTN_35	BC41, BB41	PCML output	Data output lane 35; true/complement
OUTP_36, OUTN_36	A39, B39	PCML output	Data output lane 36; true/complement
OUTP_37, OUTN_37	BJ40, BH40	PCML output	Data output lane 37; true/complement
OUTP_38, OUTN_38	D37, E37	PCML output	Data output lane 38; true/complement
OUTP_39, OUTN_39	BF40, BE40	PCML output	Data output lane 39; true/complement
OUTP_40, OUTN_40	G37, H37	PCML output	Data output lane 40; true/complement
OUTP_41, OUTN_41	AY37, AW37	PCML output	Data output lane 41; true/complement
OUTP_42, OUTN_42	A38, B38	PCML output	Data output lane 42; true/complement
OUTP_43, OUTN_43	BJ39, BH39	PCML output	Data output lane 43; true/complement
OUTP_44, OUTN_44	D36, E36	PCML output	Data output lane 44; true/complement
OUTP_45, OUTN_45	BF39, BE39	PCML output	Data output lane 45; true/complement
OUTP_46, OUTN_46	K34, L34	PCML output	Data output lane 46; true/complement
OUTP_47, OUTN_47	BC40, BB40	PCML output	Data output lane 47; true/complement
OUTP_48, OUTN_48	A37, B37	PCML output	Data output lane 48; true/complement
OUTP_49, OUTN_49	BJ38, BH38	PCML output	Data output lane 49; true/complement
OUTP_50, OUTN_50	D35, E35	PCML output	Data output lane 50; true/complement
OUTP_51, OUTN_51	BF38, BE38	PCML output	Data output lane 51; true/complement
OUTP_52, OUTN_52	G36, H36	PCML output	Data output lane 52; true/complement
OUTP_53, OUTN_53	AY36, AW36	PCML output	Data output lane 53; true/complement
OUTP_54, OUTN_54	A36, B36	PCML output	Data output lane 54; true/complement
OUTP_55, OUTN_55	BJ37, BH37	PCML output	Data output lane 55; true/complement
OUTP_56, OUTN_56	D34, E34	PCML output	Data output lane 56; true/complement
OUTP_57, OUTN_57	BF37, BE37	PCML output	Data output lane 57; true/complement
OUTP_58, OUTN_58	K33, L33	PCML output	Data output lane 58; true/complement
OUTP_59, OUTN_59	BC39, BB39	PCML output	Data output lane 59; true/complement

Table 3-2. M21170 Data Pin Assignments (9 of 13)

Pin Name	Pin Numbers	Type	Description
OUTP_60, OUTN_60	A35, B35	PCML output	Data output lane 60; true/complement
OUTP_61, OUTN_61	BJ36, BH36	PCML output	Data output lane 61; true/complement
OUTP_62, OUTN_62	D33, E33	PCML output	Data output lane 62; true/complement
OUTP_63, OUTN_63	BF36, BE36	PCML output	Data output lane 63; true/complement
OUTP_64, OUTN_64	G35, H35	PCML output	Data output lane 64; true/complement
OUTP_65, OUTN_65	AY35, AW35	PCML output	Data output lane 65; true/complement
OUTP_66, OUTN_66	A34, B34	PCML output	Data output lane 66; true/complement
OUTP_67, OUTN_67	BJ35, BH35	PCML output	Data output lane 67; true/complement
OUTP_68, OUTN_68	G31, H31	PCML output	Data output lane 68; true/complement
OUTP_69, OUTN_69	BF35, BE35	PCML output	Data output lane 69; true/complement
OUTP_70, OUTN_70	K32, L32	PCML output	Data output lane 70; true/complement
OUTP_71, OUTN_71	BC38, BB38	PCML output	Data output lane 71; true/complement
OUTP_72, OUTN_72	A33, B33	PCML output	Data output lane 72; true/complement
OUTP_73, OUTN_73	BJ34, BH34	PCML output	Data output lane 73; true/complement
OUTP_74, OUTN_74	D32, E32	PCML output	Data output lane 74; true/complement
OUTP_75, OUTN_75	BC32, BB32	PCML output	Data output lane 75; true/complement
OUTP_76, OUTN_76	G34, H34	PCML output	Data output lane 76; true/complement
OUTP_77, OUTN_77	AY34, AW34	PCML output	Data output lane 77; true/complement
OUTP_78, OUTN_78	A32, B32	PCML output	Data output lane 78; true/complement
OUTP_79, OUTN_79	BJ33, BH33	PCML output	Data output lane 79; true/complement
OUTP_80, OUTN_80	G30, H30	PCML output	Data output lane 80; true/complement
OUTP_81, OUTN_81	BF34, BE34	PCML output	Data output lane 81; true/complement
OUTP_82, OUTN_82	K31, L31	PCML output	Data output lane 82; true/complement
OUTP_83, OUTN_83	BC37, BB37	PCML output	Data output lane 83; true/complement
OUTP_84, OUTN_84	A31, B31	PCML output	Data output lane 84; true/complement
OUTP_85, OUTN_85	BJ32, BH32	PCML output	Data output lane 85; true/complement
OUTP_86, OUTN_86	D31, E31	PCML output	Data output lane 86; true/complement
OUTP_87, OUTN_87	BC31, BB31	PCML output	Data output lane 87; true/complement
OUTP_88, OUTN_88	G33, H33	PCML output	Data output lane 88; true/complement
OUTP_89, OUTN_89	AY33, AW33	PCML output	Data output lane 89; true/complement
OUTP_90, OUTN_90	A30, B30	PCML output	Data output lane 90; true/complement
OUTP_91, OUTN_91	BJ31, BH31	PCML output	Data output lane 91; true/complement
OUTP_92, OUTN_92	G29, H29	PCML output	Data output lane 92; true/complement
OUTP_93, OUTN_93	BF33, BE33	PCML output	Data output lane 93; true/complement
OUTP_94, OUTN_94	K30, L30	PCML output	Data output lane 94; true/complement
OUTP_95, OUTN_95	BC36, BB36	PCML output	Data output lane 95; true/complement
OUTP_96, OUTN_96	A29, B29	PCML output	Data output lane 96; true/complement
OUTP_97, OUTN_97	BJ30, BH30	PCML output	Data output lane 97; true/complement
OUTP_98, OUTN_98	D30, E30	PCML output	Data output lane 98; true/complement
OUTP_99, OUTN_99	BC30, BB30	PCML output	Data output lane 99; true/complement
OUTP_100, OUTN_100	G32, H32	PCML output	Data output lane 100; true/complement
OUTP_101, OUTN_101	AY32, AW32	PCML output	Data output lane 101; true/complement
OUTP_102, OUTN_102	A28, B28	PCML output	Data output lane 102; true/complement
OUTP_103, OUTN_103	BJ29, BH29	PCML output	Data output lane 103; true/complement
OUTP_104, OUTN_104	G28, H28	PCML output	Data output lane 104; true/complement
OUTP_105, OUTN_105	BF32, BE32	PCML output	Data output lane 105; true/complement
OUTP_106, OUTN_106	K29, L29	PCML output	Data output lane 106; true/complement
OUTP_107, OUTN_107	BC35, BB35	PCML output	Data output lane 107; true/complement

Table 3-2. M21170 Data Pin Assignments (10 of 13)

Pin Name	Pin Numbers	Type	Description
OUTP_108, OUTN_108	A27, B27	PCML output	Data output lane 108; true/complement
OUTP_109, OUTN_109	BF28, BE28	PCML output	Data output lane 109; true/complement
OUTP_110, OUTN_110	D29, E29	PCML output	Data output lane 110; true/complement
OUTP_111, OUTN_111	BC29, BB29	PCML output	Data output lane 111; true/complement
OUTP_112, OUTN_112	K28, L28	PCML output	Data output lane 112; true/complement
OUTP_113, OUTN_113	AY31, AW31	PCML output	Data output lane 113; true/complement
OUTP_114, OUTN_114	D27, E27	PCML output	Data output lane 114; true/complement
OUTP_115, OUTN_115	BJ28, BH28	PCML output	Data output lane 115; true/complement
OUTP_116, OUTN_116	G27, H27	PCML output	Data output lane 116; true/complement
OUTP_117, OUTN_117	BF31, BE31	PCML output	Data output lane 117; true/complement
OUTP_118, OUTN_118	K27, L27	PCML output	Data output lane 118; true/complement
OUTP_119, OUTN_119	BC34, BB34	PCML output	Data output lane 119; true/complement
OUTP_120, OUTN_120	A26, B26	PCML output	Data output lane 120; true/complement
OUTP_121, OUTN_121	BF27, BE27	PCML output	Data output lane 121; true/complement
OUTP_122, OUTN_122	D28, E28	PCML output	Data output lane 122; true/complement
OUTP_123, OUTN_123	BC28, BB28	PCML output	Data output lane 123; true/complement
OUTP_124, OUTN_124	K26, L26	PCML output	Data output lane 124; true/complement
OUTP_125, OUTN_125	AY30, AW30	PCML output	Data output lane 125; true/complement
OUTP_126, OUTN_126	D26, E26	PCML output	Data output lane 126; true/complement
OUTP_127, OUTN_127	BJ27, BH27	PCML output	Data output lane 127; true/complement
OUTP_128, OUTN_128	G26, H26	PCML output	Data output lane 128; true/complement
OUTP_129, OUTN_129	BF30, BE30	PCML output	Data output lane 129; true/complement
OUTP_130, OUTN_130	K25, L25	PCML output	Data output lane 130; true/complement
OUTP_131, OUTN_131	BC33, BB33	PCML output	Data output lane 131; true/complement
OUTP_132, OUTN_132	A25, B25	PCML output	Data output lane 132; true/complement
OUTP_133, OUTN_133	BF26, BE26	PCML output	Data output lane 133; true/complement
OUTP_134, OUTN_134	G25, H25	PCML output	Data output lane 134; true/complement
OUTP_135, OUTN_135	BC27, BB27	PCML output	Data output lane 135; true/complement
OUTP_136, OUTN_136	K24, L24	PCML output	Data output lane 136; true/complement
OUTP_137, OUTN_137	AY29, AW29	PCML output	Data output lane 137; true/complement
OUTP_138, OUTN_138	D25, E25	PCML output	Data output lane 138; true/complement
OUTP_139, OUTN_139	BJ26, BH26	PCML output	Data output lane 139; true/complement
OUTP_140, OUTN_140	G24, H24	PCML output	Data output lane 140; true/complement
OUTP_141, OUTN_141	BF29, BE29	PCML output	Data output lane 141; true/complement
OUTP_142, OUTN_142	K23, L23	PCML output	Data output lane 142; true/complement
OUTP_143, OUTN_143	AY28, AW28	PCML output	Data output lane 143; true/complement
OUTP_144, OUTN_144	A24, B24	PCML output	Data output lane 144; true/complement
OUTP_145, OUTN_145	BF25, BE25	PCML output	Data output lane 145; true/complement
OUTP_146, OUTN_146	D21, E21	PCML output	Data output lane 146; true/complement
OUTP_147, OUTN_147	BC26, BB26	PCML output	Data output lane 147; true/complement
OUTP_148, OUTN_148	K22, L22	PCML output	Data output lane 148; true/complement
OUTP_149, OUTN_149	AY27, AW27	PCML output	Data output lane 149; true/complement
OUTP_150, OUTN_150	D24, E24	PCML output	Data output lane 150; true/complement
OUTP_151, OUTN_151	BJ25, BH25	PCML output	Data output lane 151; true/complement
OUTP_152, OUTN_152	G23, H23	PCML output	Data output lane 152; true/complement
OUTP_153, OUTN_153	BC25, BB25	PCML output	Data output lane 153; true/complement
OUTP_154, OUTN_154	K21, L21	PCML output	Data output lane 154; true/complement
OUTP_155, OUTN_155	AY26, AW26	PCML output	Data output lane 155; true/complement

Table 3-2. M21170 Data Pin Assignments (11 of 13)

Pin Name	Pin Numbers	Type	Description
OUTP_156, OUTN_156	A23, B23	PCML output	Data output lane 156; true/complement
OUTP_157, OUTN_157	BF24, BE24	PCML output	Data output lane 157; true/complement
OUTP_158, OUTN_158	D20, E20	PCML output	Data output lane 158; true/complement
OUTP_159, OUTN_159	BC24, BB24	PCML output	Data output lane 159; true/complement
OUTP_160, OUTN_160	G17, H17	PCML output	Data output lane 160; true/complement
OUTP_161, OUTN_161	AY25, AW25	PCML output	Data output lane 161; true/complement
OUTP_162, OUTN_162	D23, E23	PCML output	Data output lane 162; true/complement
OUTP_163, OUTN_163	BJ24, BH24	PCML output	Data output lane 163; true/complement
OUTP_164, OUTN_164	G22, H22	PCML output	Data output lane 164; true/complement
OUTP_165, OUTN_165	BF22, BE22	PCML output	Data output lane 165; true/complement
OUTP_166, OUTN_166	K20, L20	PCML output	Data output lane 166; true/complement
OUTP_167, OUTN_167	AY24, AW24	PCML output	Data output lane 167; true/complement
OUTP_168, OUTN_168	A22, B22	PCML output	Data output lane 168; true/complement
OUTP_169, OUTN_169	BF23, BE23	PCML output	Data output lane 169; true/complement
OUTP_170, OUTN_170	D19, E19	PCML output	Data output lane 170; true/complement
OUTP_171, OUTN_171	BC23, BB23	PCML output	Data output lane 171; true/complement
OUTP_172, OUTN_172	G16, H16	PCML output	Data output lane 172; true/complement
OUTP_173, OUTN_173	AY23, AW23	PCML output	Data output lane 173; true/complement
OUTP_174, OUTN_174	D22, E22	PCML output	Data output lane 174; true/complement
OUTP_175, OUTN_175	BJ23, BH23	PCML output	Data output lane 175; true/complement
OUTP_176, OUTN_176	G21, H21	PCML output	Data output lane 176; true/complement
OUTP_177, OUTN_177	BF21, BE21	PCML output	Data output lane 177; true/complement
OUTP_178, OUTN_178	K19, L19	PCML output	Data output lane 178; true/complement
OUTP_179, OUTN_179	AY22, AW22	PCML output	Data output lane 179; true/complement
OUTP_180, OUTN_180	A21, B21	PCML output	Data output lane 180; true/complement
OUTP_181, OUTN_181	BJ22, BH22	PCML output	Data output lane 181; true/complement
OUTP_182, OUTN_182	D18, E18	PCML output	Data output lane 182; true/complement
OUTP_183, OUTN_183	BC22, BB22	PCML output	Data output lane 183; true/complement
OUTP_184, OUTN_184	G15, H15	PCML output	Data output lane 184; true/complement
OUTP_185, OUTN_185	AY21, AW21	PCML output	Data output lane 185; true/complement
OUTP_186, OUTN_186	A20, B20	PCML output	Data output lane 186; true/complement
OUTP_187, OUTN_187	BJ21, BH21	PCML output	Data output lane 187; true/complement
OUTP_188, OUTN_188	G20, H20	PCML output	Data output lane 188; true/complement
OUTP_189, OUTN_189	BF20, BE20	PCML output	Data output lane 189; true/complement
OUTP_190, OUTN_190	K18, L18	PCML output	Data output lane 190; true/complement
OUTP_191, OUTN_191	BC18, BB18	PCML output	Data output lane 191; true/complement
OUTP_192, OUTN_192	A19, B19	PCML output	Data output lane 192; true/complement
OUTP_193, OUTN_193	BJ20, BH20	PCML output	Data output lane 193; true/complement
OUTP_194, OUTN_194	D17, E17	PCML output	Data output lane 194; true/complement
OUTP_195, OUTN_195	BC21, BB21	PCML output	Data output lane 195; true/complement
OUTP_196, OUTN_196	G14, H14	PCML output	Data output lane 196; true/complement
OUTP_197, OUTN_197	AY20, AW20	PCML output	Data output lane 197; true/complement
OUTP_198, OUTN_198	A18, B18	PCML output	Data output lane 198; true/complement
OUTP_199, OUTN_199	BJ19, BH19	PCML output	Data output lane 199; true/complement
OUTP_200, OUTN_200	G19, H19	PCML output	Data output lane 200; true/complement
OUTP_201, OUTN_201	BF19, BE19	PCML output	Data output lane 201; true/complement
OUTP_202, OUTN_202	K17, L17	PCML output	Data output lane 202; true/complement
OUTP_203, OUTN_203	BC17, BB17	PCML output	Data output lane 203; true/complement

Table 3-2. M21170 Data Pin Assignments (12 of 13)

Pin Name	Pin Numbers	Type	Description
OUTP_204, OUTN_204	A17, B17	PCML output	Data output lane 204; true/complement
OUTP_205, OUTN_205	BJ18, BH18	PCML output	Data output lane 205; true/complement
OUTP_206, OUTN_206	D16, E16	PCML output	Data output lane 206; true/complement
OUTP_207, OUTN_207	BC20, BB20	PCML output	Data output lane 207; true/complement
OUTP_208, OUTN_208	G13, H13	PCML output	Data output lane 208; true/complement
OUTP_209, OUTN_209	AY19, AW19	PCML output	Data output lane 209; true/complement
OUTP_210, OUTN_210	A16, B16	PCML output	Data output lane 210; true/complement
OUTP_211, OUTN_211	BJ17, BH17	PCML output	Data output lane 211; true/complement
OUTP_212, OUTN_212	G18, H18	PCML output	Data output lane 212; true/complement
OUTP_213, OUTN_213	BF18, BE18	PCML output	Data output lane 213; true/complement
OUTP_214, OUTN_214	K16, L16	PCML output	Data output lane 214; true/complement
OUTP_215, OUTN_215	BC16, BB16	PCML output	Data output lane 215; true/complement
OUTP_216, OUTN_216	A15, B15	PCML output	Data output lane 216; true/complement
OUTP_217, OUTN_217	BJ16, BH16	PCML output	Data output lane 217; true/complement
OUTP_218, OUTN_218	D15, E15	PCML output	Data output lane 218; true/complement
OUTP_219, OUTN_219	BC19, BB19	PCML output	Data output lane 219; true/complement
OUTP_220, OUTN_220	G12, H12	PCML output	Data output lane 220; true/complement
OUTP_221, OUTN_221	AY18, AW18	PCML output	Data output lane 221; true/complement
OUTP_222, OUTN_222	A14, B14	PCML output	Data output lane 222; true/complement
OUTP_223, OUTN_223	BJ15, BH15	PCML output	Data output lane 223; true/complement
OUTP_224, OUTN_224	D14, E14	PCML output	Data output lane 224; true/complement
OUTP_225, OUTN_225	BF17, BE17	PCML output	Data output lane 225; true/complement
OUTP_226, OUTN_226	K15, L15	PCML output	Data output lane 226; true/complement
OUTP_227, OUTN_227	BC15, BB15	PCML output	Data output lane 227; true/complement
OUTP_228, OUTN_228	A13, B13	PCML output	Data output lane 228; true/complement
OUTP_229, OUTN_229	BJ14, BH14	PCML output	Data output lane 229; true/complement
OUTP_230, OUTN_230	D13, E13	PCML output	Data output lane 230; true/complement
OUTP_231, OUTN_231	BF16, BE16	PCML output	Data output lane 231; true/complement
OUTP_232, OUTN_232	G11, H11	PCML output	Data output lane 232; true/complement
OUTP_233, OUTN_233	AY17, AW17	PCML output	Data output lane 233; true/complement
OUTP_234, OUTN_234	A12, B12	PCML output	Data output lane 234; true/complement
OUTP_235, OUTN_235	BJ13, BH13	PCML output	Data output lane 235; true/complement
OUTP_236, OUTN_236	D12, E12	PCML output	Data output lane 236; true/complement
OUTP_237, OUTN_237	BF15, BE15	PCML output	Data output lane 237; true/complement
OUTP_238, OUTN_238	K14, L14	PCML output	Data output lane 238; true/complement
OUTP_239, OUTN_239	BC14, BB14	PCML output	Data output lane 239; true/complement
OUTP_240, OUTN_240	A11, B11	PCML output	Data output lane 240; true/complement
OUTP_241, OUTN_241	BJ12, BH12	PCML output	Data output lane 241; true/complement
OUTP_242, OUTN_242	D11, E11	PCML output	Data output lane 242; true/complement
OUTP_243, OUTN_243	BF14, BE14	PCML output	Data output lane 243; true/complement
OUTP_244, OUTN_244	G10, H10	PCML output	Data output lane 244; true/complement
OUTP_245, OUTN_245	AY16, AW16	PCML output	Data output lane 245; true/complement
OUTP_246, OUTN_246	A10, B10	PCML output	Data output lane 246; true/complement
OUTP_247, OUTN_247	BJ11, BH11	PCML output	Data output lane 247; true/complement
OUTP_248, OUTN_248	D10, E10	PCML output	Data output lane 248; true/complement
OUTP_249, OUTN_249	BF13, BE13	PCML output	Data output lane 249; true/complement
OUTP_250, OUTN_250	K13, L13	PCML output	Data output lane 250; true/complement
OUTP_251, OUTN_251	BC13, BB13	PCML output	Data output lane 251; true/complement

Table 3-2. M21170 Data Pin Assignments (13 of 13)

Pin Name	Pin Numbers	Type	Description
OUTP_252, OUTN_252	A9, B9	PCML output	Data output lane 252; true/complement
OUTP_253, OUTN_253	BJ10, BH10	PCML output	Data output lane 253; true/complement
OUTP_254, OUTN_254	D9, E9	PCML output	Data output lane 254; true/complement
OUTP_255, OUTN_255	BF12, BE12	PCML output	Data output lane 255; true/complement
OUTP_256, OUTN_256	G9, H9	PCML output	Data output lane 256; true/complement
OUTP_257, OUTN_257	AY15, AW15	PCML output	Data output lane 257; true/complement
OUTP_258, OUTN_258	A8, B8	PCML output	Data output lane 258; true/complement
OUTP_259, OUTN_259	BJ9, BH9	PCML output	Data output lane 259; true/complement
OUTP_260, OUTN_260	D8, E8	PCML output	Data output lane 260; true/complement
OUTP_261, OUTN_261	BF11, BE11	PCML output	Data output lane 261; true/complement
OUTP_262, OUTN_262	K12, L12	PCML output	Data output lane 262; true/complement
OUTP_263, OUTN_263	BC12, BB12	PCML output	Data output lane 263; true/complement
OUTP_264, OUTN_264	A7, B7	PCML output	Data output lane 264; true/complement
OUTP_265, OUTN_265	BJ8, BH8	PCML output	Data output lane 265; true/complement
OUTP_266, OUTN_266	D7, E7	PCML output	Data output lane 266; true/complement
OUTP_267, OUTN_267	BF10, BE10	PCML output	Data output lane 267; true/complement
OUTP_268, OUTN_268	G8, H8	PCML output	Data output lane 268; true/complement
OUTP_269, OUTN_269	AY14, AW14	PCML output	Data output lane 269; true/complement
OUTP_270, OUTN_270	A6, B6	PCML output	Data output lane 270; true/complement
OUTP_271, OUTN_271	BJ7, BH7	PCML output	Data output lane 271; true/complement
OUTP_272, OUTN_272	D6, E6	PCML output	Data output lane 272; true/complement
OUTP_273, OUTN_273	BF9, BE9	PCML output	Data output lane 273; true/complement
OUTP_274, OUTN_274	K11, L11	PCML output	Data output lane 274; true/complement
OUTP_275, OUTN_275	BC11, BB11	PCML output	Data output lane 275; true/complement
OUTP_276, OUTN_276	A5, B5	PCML output	Data output lane 276; true/complement
OUTP_277, OUTN_277	BJ6, BH6	PCML output	Data output lane 277; true/complement
OUTP_278, OUTN_278	D5, E5	PCML output	Data output lane 278; true/complement
OUTP_279, OUTN_279	BF8, BE8	PCML output	Data output lane 279; true/complement
OUTP_280, OUTN_280	G7, H7	PCML output	Data output lane 280; true/complement
OUTP_281, OUTN_281	AY13, AW13	PCML output	Data output lane 281; true/complement
OUTP_282, OUTN_282	A4, B4	PCML output	Data output lane 282; true/complement
OUTP_283, OUTN_283	BJ5, BH5	PCML output	Data output lane 283; true/complement
OUTP_284, OUTN_284	D4, E4	PCML output	Data output lane 284; true/complement
OUTP_285, OUTN_285	BF7, BE7	PCML output	Data output lane 285; true/complement
OUTP_286, OUTN_286	K10, L10	PCML output	Data output lane 286; true/complement
OUTP_287, OUTN_287	BC10, BB10	PCML output	Data output lane 287; true/complement
OUTP_AUXE, OUTN_AUXE	P35, R35	PCML output	Data output lane AUXE; true/complement
OUTP_AUXO, OUTN_AUXO	AR35, AP35	PCML output	Data output lane AUXO; true/complement

Table 3-3. M21170 Control and Interface Pin Assignments (1 of 2)

Pin Name	Pin Numbers	Type	Description
CONFIGSEL	AR13	CMOS Input	Hardware ISC select. L=ISC#1, H=ISC#2, termination: pull-down[1]
TDI	AT15	CMOS Input	JTAG data input port, termination: pull-up[1]

Table 3-3. M21170 Control and Interface Pin Assignments (2 of 2)

Pin Name	Pin Numbers	Type	Description
TDO	AU15	CMOS Output	JTAG data output port, termination: -
TMS	AT14	CMOS Input	JTAG test mode select input port, termination: pull-up[1]
xRST	AU16	CMOS Input	Hardware reset (active low), termination: pull-up[1]
xALARM	AU13	Output (open drain)	LOS alarm, L=alarm assert, H=alarm de-assert, termination: external pull-up[2]
DISTEMP	AR14	CMOS Input	L: Do not disable the device upon any over-temperature alarm flag and let the overtemp alarm configuration per register.tempmon, address.00h, page.21h., termination: pull-down[1] H: Power-down the entire device upon any over-temperature flag. This setting overrides and forces register.tempmon.bit[7,6,0] to 001b, termination: pull-down[1]
xINPUTEN	AP13	CMOS Input	Power up inputs, H=power down, L=power up, termination: pull-up[1]
xOUTPUTEN	AT16	CMOS Input	Power up outputs, H=power down, L=power up, termination: pull-up[1]
xOVERTEMP	AT13	Output (open drain)	Thermal alarm. , termination: external pull-up[2] L=alarm assert, H=alarm de-assert, if register.tempmon.bit[5]=0b, address.00h, page.21h L=alarm de-assert, H=alarm assert, if register.tempmon.bit[5]=1b, address.00h, page.21h
xSET0	R13	CMOS Input	Hardware switch state update ASC / ISC#1 / ISC#2 (update on H to L transition) , termination: pull-down[1]
xSET1	T13	CMOS Input	Multiple switch point config1, termination: pull-down[1]
xSET2	P14	CMOS Input	Multiple switch point config2, termination: pull-down[1]
xSET3	N16	CMOS Input	Multiple switch point config3, termination: pull-down[1]

NOTES:

1. Pull-up/pull-down resistance is an integrated 100 kΩ to DV_{DDIO} or V_{SS}.
2. External pull-up resistance should be > 10 kΩ.

Table 3-4. M21170 Multi-Function Pin Assignments

Pin Name	Pin Numbers	Type	Description
Do Not Connect	AR36, T33, AT36, T34, AU17, T37	N/A	Do not connect
CONFIG0	P37	CMOS Control Input	Pull-down[1] / Input
CONFIG1	R37	CMOS Control Input	Pull-down[1] / Input
TEN	N35	CMOS Control Input	Pull-down[1] / Input
TEST0	N36	CMOS Control Input	Pull-down[1] / Input
TEST1	N37	CMOS Control Input	Pull-down[1] / Input
TCLK	AU14	CMOS Control Input	Pull-up[1] / Input
MF11	V14	Control	High-Z / Input
MF10	N13	Control	High-Z / Input
MF9	P15	Control	High-Z / I_O
MF8	T14	Control	High-Z / I_O
MF7	U14	Control	High-Z / I_O
MF6	N18	Control	High-Z / I_O
MF5	R17	Control	High-Z / I_O
MF4	T15	Control	High-Z / I_O
MF3	R14	Control	High-Z / I_O
MF2	P17	Control	High-Z / I_O
MF1	R16	Control	High-Z / I_O
A8	N14	Control	High-Z / Input
A7	V15	Control	High-Z / Input
A6	V13	Control	High-Z / Input
A5	N17	Control	High-Z / Input
A4	U13	Control	High-Z / Input
A3	U15	Control	High-Z / Input
A2	N15	Control	High-Z / Input
A1	P13	Control	High-Z / Input
A0	P16	Control	High-Z / Input
MF0	R15	Control	High-Z / Input

NOTES:

1. Pull-up/pull-down resistance is an integrated 100 kΩ to DV_{DDIO} or V_{SS}.

Table 3-5. M21170 No-Connect Pin Assignments

Pin Name	Pin Numbers	Type	Description
Do Not Connect	AR36, T33, AT36, T34, AU17, T37	N/A	Do not connect

3.2 M21170 Pinout Diagrams

Figure 3-1. M21170 Pinout Diagram (Top View of Package)

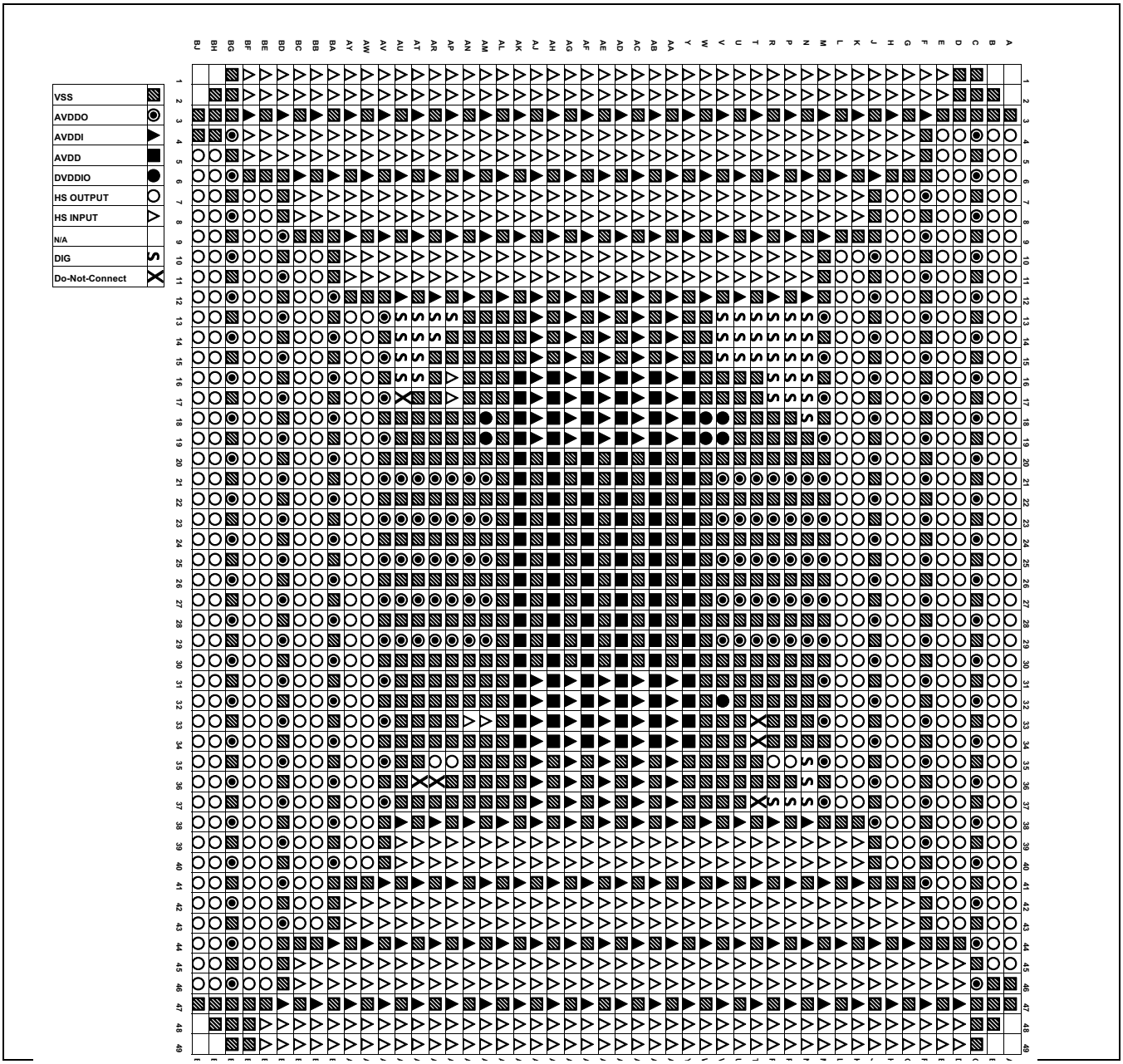


Figure 3-2. M21170 Pinout Diagram (1 of 8)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A			VSS	OUTP_282	OUTP_276	OUTP_270	OUTP_264	OUTP_258	OUTP_252	OUTP_246	OUTP_240	OUTP_234	OUTP_228
B		VSS	VSS	OUTN_282	OUTN_276	OUTN_270	OUTN_264	OUTN_258	OUTN_252	OUTN_246	OUTN_240	OUTN_234	OUTN_228
C	VSS	VSS	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS
D	VSS	VSS	VSS	OUTP_284	OUTP_278	OUTP_272	OUTP_266	OUTP_260	OUTP_254	OUTP_248	OUTP_242	OUTP_236	OUTP_230
E	INP_1	INN_1	VSS	OUTN_284	OUTN_278	OUTN_272	OUTN_266	OUTN_260	OUTN_254	OUTN_248	OUTN_242	OUTN_236	OUTN_230
F	INP_7	INN_7	AVDDI	VSS	VSS	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO
G	INP_13	INN_13	VSS	INP_3	INN_3	VSS	OUTP_280	OUTP_268	OUTP_256	OUTP_244	OUTP_232	OUTP_220	OUTP_208
H	INP_19	INN_19	AVDDI	INP_9	INN_9	VSS	OUTN_280	OUTN_268	OUTN_256	OUTN_244	OUTN_232	OUTN_220	OUTN_208
J	INP_25	INN_25	VSS	INP_15	INN_15	AVDDI	VSS	VSS	VSS	AVDDO	VSS	AVDDO	VSS
K	INP_31	INN_31	AVDDI	INP_21	INN_21	VSS	INP_5	INN_5	VSS	OUTP_286	OUTP_274	OUTP_262	OUTP_250
L	INP_37	INN_37	VSS	INP_27	INN_27	AVDDI	INP_17	INN_17	VSS	OUTN_286	OUTN_274	OUTN_262	OUTN_250
M	INP_43	INN_43	AVDDI	INP_33	INN_33	VSS	INP_29	INN_29	AVDDI	VSS	VSS	VSS	AVDDO
N	INP_49	INN_49	VSS	INP_39	INN_39	AVDDI	INP_41	INN_41	VSS	INP_11	INN_11	AVDDI	MF10
P	INP_55	INN_55	AVDDI	INP_45	INN_45	VSS	INP_53	INN_53	AVDDI	INP_23	INN_23	VSS	A1
R	INP_61	INN_61	VSS	INP_51	INN_51	AVDDI	INP_65	INN_65	VSS	INP_35	INN_35	AVDDI	XSET0
T	INP_67	INN_67	AVDDI	INP_57	INN_57	VSS	INP_77	INN_77	AVDDI	INP_47	INN_47	VSS	XSET1
U	INP_73	INN_73	VSS	INP_63	INN_63	AVDDI	INP_89	INN_89	VSS	INP_59	INN_59	AVDDI	A4
V	INP_79	INN_79	AVDDI	INP_75	INN_75	VSS	INP_101	INN_101	AVDDI	INP_71	INN_71	VSS	A6
W	INP_85	INN_85	VSS	INP_87	INN_87	AVDDI	INP_69	INN_69	VSS	INP_83	INN_83	AVDDI	VSS
Y	INP_91	INN_91	AVDDI	INP_99	INN_99	VSS	INP_81	INN_81	AVDDI	INP_95	INN_95	VSS	VSS
AA	INP_97	INN_97	VSS	INP_111	INN_111	AVDDI	INP_93	INN_93	VSS	INP_107	INN_107	AVDDI	AVDDI
AB	INP_103	INN_103	AVDDI	INP_123	INN_123	VSS	INP_105	INN_105	AVDDI	INP_113	INN_113	VSS	VSS
AC	INP_109	INN_109	VSS	INP_115	INN_115	AVDDI	INP_117	INN_117	VSS	INP_119	INN_119	AVDDI	AVDDI
AD	INP_121	INN_121	AVDDI	INP_127	INN_127	VSS	INP_129	INN_129	AVDDI	INP_125	INN_125	VSS	VSS
AE	INP_133	INN_133	VSS	INP_139	INN_139	AVDDI	INP_135	INN_135	VSS	INP_131	INN_131	AVDDI	AVDDI
AF	INP_145	INN_145	AVDDI	INP_151	INN_151	VSS	INP_141	INN_141	AVDDI	INP_137	INN_137	VSS	VSS
AG	INP_157	INN_157	VSS	INP_163	INN_163	AVDDI	INP_153	INN_153	VSS	INP_143	INN_143	AVDDI	AVDDI

Figure 3-3. M21170 Pinout Diagram (2 of 8)

	1	2	3	4	5	6	7	8	9	10	11	12	13
AH	INP_169	INN_169	AVDDI	INP_175	INN_175	VSS	INP_165	INN_165	AVDDI	INP_149	INN_149	VSS	VSS
AJ	INP_181	INN_181	VSS	INP_147	INN_147	AVDDI	INP_177	INN_177	VSS	INP_155	INN_155	AVDDI	AVDDI
AK	INP_187	INN_187	AVDDI	INP_159	INN_159	VSS	INP_189	INN_189	AVDDI	INP_167	INN_167	VSS	VSS
AL	INP_193	INN_193	VSS	INP_171	INN_171	AVDDI	INP_201	INN_201	VSS	INP_179	INN_179	AVDDI	VSS
AM	INP_199	INN_199	AVDDI	INP_183	INN_183	VSS	INP_213	INN_213	AVDDI	INP_191	INN_191	VSS	VSS
AN	INP_205	INN_205	VSS	INP_195	INN_195	AVDDI	INP_161	INN_161	VSS	INP_203	INN_203	AVDDI	VSS
AP	INP_211	INN_211	AVDDI	INP_207	INN_207	VSS	INP_173	INN_173	AVDDI	INP_215	INN_215	VSS	XINPUTEN
AR	INP_217	INN_217	VSS	INP_219	INN_219	AVDDI	INP_185	INN_185	VSS	INP_227	INN_227	AVDDI	CONFIGSEL
AT	INP_223	INN_223	AVDDI	INP_225	INN_225	VSS	INP_197	INN_197	AVDDI	INP_239	INN_239	VSS	XOVERTEMP
AU	INP_229	INN_229	VSS	INP_231	INN_231	AVDDI	INP_209	INN_209	VSS	INP_251	INN_251	AVDDI	XALARM
AV	INP_235	INN_235	AVDDI	INP_237	INN_237	VSS	INP_221	INN_221	AVDDI	INP_263	INN_263	VSS	AVDDO
AW	INP_241	INN_241	VSS	INP_243	INN_243	AVDDI	INP_233	INN_233	VSS	INP_275	INN_275	VSS	OUTN_281
AY	INP_247	INN_247	AVDDI	INP_249	INN_249	VSS	INP_245	INN_245	AVDDI	INP_287	INN_287	VSS	OUTP_281
BA	INP_253	INN_253	VSS	INP_255	INN_255	AVDDI	INP_257	INN_257	VSS	VSS	VSS	AVDDO	VSS
BB	INP_259	INN_259	AVDDI	INP_261	INN_261	VSS	INP_269	INN_269	VSS	OUTN_287	OUTN_275	OUTN_263	OUTN_251
BC	INP_265	INN_265	VSS	INP_267	INN_267	AVDDI	INP_281	INN_281	VSS	OUTP_287	OUTP_275	OUTP_263	OUTP_251
BD	INP_271	INN_271	AVDDI	INP_273	INN_273	VSS	VSS	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO
BE	INP_277	INN_277	VSS	INP_279	INN_279	VSS	OUTN_285	OUTN_279	OUTN_273	OUTN_267	OUTN_261	OUTN_255	OUTN_249
BF	INP_283	INN_283	AVDDI	INP_285	INN_285	VSS	OUTP_285	OUTP_279	OUTP_273	OUTP_267	OUTP_261	OUTP_255	OUTP_249
BG	VSS	VSS	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS
BH		VSS	VSS	VSS	OUTN_283	OUTN_277	OUTN_271	OUTN_265	OUTN_259	OUTN_253	OUTN_247	OUTN_241	OUTN_235
BJ			VSS	VSS	OUTP_283	OUTP_277	OUTP_271	OUTP_265	OUTP_259	OUTP_253	OUTP_247	OUTP_241	OUTP_235

Figure 3-4. M21170 Pinout Diagram (3 of 8)

	14	15	16	17	18	19	20	21	22	23	24	25	26
A	OUTP_222	OUTP_216	OUTP_210	OUTP_204	OUTP_198	OUTP_192	OUTP_186	OUTP_180	OUTP_168	OUTP_156	OUTP_144	OUTP_132	OUTP_120
B	OUTN_222	OUTN_216	OUTN_210	OUTN_204	OUTN_198	OUTN_192	OUTN_186	OUTN_180	OUTN_168	OUTN_156	OUTN_144	OUTN_132	OUTN_120
C	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO
D	OUTP_224	OUTP_218	OUTP_206	OUTP_194	OUTP_182	OUTP_170	OUTP_158	OUTP_146	OUTP_174	OUTP_162	OUTP_150	OUTP_138	OUTP_126
E	OUTN_224	OUTN_218	OUTN_206	OUTN_194	OUTN_182	OUTN_170	OUTN_158	OUTN_146	OUTN_174	OUTN_162	OUTN_150	OUTN_138	OUTN_126
F	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS
G	OUTP_196	OUTP_184	OUTP_172	OUTP_160	OUTP_212	OUTP_200	OUTP_188	OUTP_176	OUTP_164	OUTP_152	OUTP_140	OUTP_134	OUTP_128
H	OUTN_196	OUTN_184	OUTN_172	OUTN_160	OUTN_212	OUTN_200	OUTN_188	OUTN_176	OUTN_164	OUTN_152	OUTN_140	OUTN_134	OUTN_128
J	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO
K	OUTP_238	OUTP_226	OUTP_214	OUTP_202	OUTP_190	OUTP_178	OUTP_166	OUTP_154	OUTP_148	OUTP_142	OUTP_136	OUTP_130	OUTP_124
L	OUTN_238	OUTN_226	OUTN_214	OUTN_202	OUTN_190	OUTN_178	OUTN_166	OUTN_154	OUTN_148	OUTN_142	OUTN_136	OUTN_130	OUTN_124
M	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS
N	A8	A2	XSET3	A5	MF6	VSS	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS
P	XSET2	MF9	A0	MF2	VSS	VSS	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS
R	MF3	MF0	MF1	MF5	VSS	VSS	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS
T	MF8	MF4	VSS	VSS	VSS	VSS	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS
U	MF7	A3	VSS	VSS	VSS	VSS	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS
V	MF11	A7	VSS	VSS	DVDDIO_1	DVDDIO_1	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS
W	VSS	VSS	VSS	VSS	DVDDIO_1	DVDDIO_1	VSS	VSS	VSS	VSS	VSS	VSS	VSS
Y	VSS	VSS	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
AA	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AB	VSS	VSS	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
AC	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AD	VSS	VSS	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
AE	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AF	VSS	VSS	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
AG	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	VSS	VSS	VSS	VSS	VSS	VSS	VSS

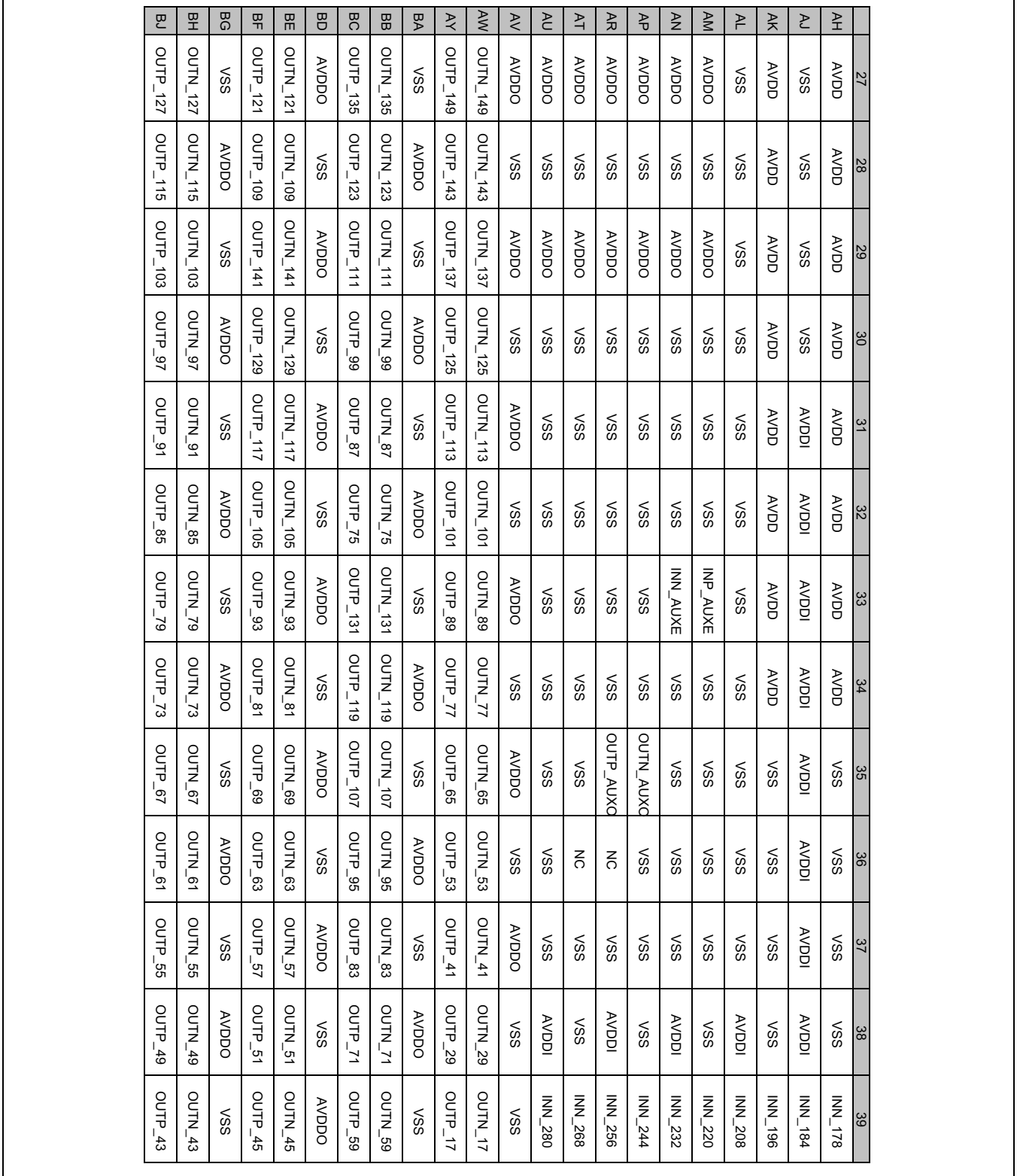
Figure 3-5. M21170 Pinout Diagram (4 of 8)

	14	15	16	17	18	19	20	21	22	23	24	25	26
AH	VSS	VSS	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
AJ	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AK	VSS	VSS	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
AL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AM	VSS	VSS	VSS	VSS	DVDDIO_3	DVDDIO_3	VSS	AVDDO	VSS	AVDDO	AVDDO	AVDDO	VSS
AN	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS
AP	VSS	VSS	INP_AUXO	INN_AUXO	VSS	VSS	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS
AR	DISTEMP	VSS	VSS	VSS	VSS	VSS	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS
AT	TMS	TDI	XOUTPUTEN	VSS	VSS	VSS	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS
AU	TCLK	TDO	XRST	NC	VSS	VSS	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS
AV	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS
AW	OUTN_269	OUTN_257	OUTN_245	OUTN_233	OUTN_221	OUTN_209	OUTN_197	OUTN_185	OUTN_179	OUTN_173	OUTN_167	OUTN_161	OUTN_155
AY	OUTP_269	OUTP_257	OUTP_245	OUTP_233	OUTP_221	OUTP_209	OUTP_197	OUTP_185	OUTP_179	OUTP_173	OUTP_167	OUTP_161	OUTP_155
BA	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO
BB	OUTN_239	OUTN_227	OUTN_215	OUTN_203	OUTN_191	OUTN_219	OUTN_207	OUTN_195	OUTN_183	OUTN_171	OUTN_159	OUTN_153	OUTN_147
BC	OUTP_239	OUTP_227	OUTP_215	OUTP_203	OUTP_191	OUTP_219	OUTP_207	OUTP_195	OUTP_183	OUTP_171	OUTP_159	OUTP_153	OUTP_147
BD	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS
BE	OUTN_243	OUTN_237	OUTN_231	OUTN_225	OUTN_213	OUTN_201	OUTN_189	OUTN_177	OUTN_165	OUTN_169	OUTN_157	OUTN_145	OUTN_133
BF	OUTP_243	OUTP_237	OUTP_231	OUTP_225	OUTP_213	OUTP_201	OUTP_189	OUTP_177	OUTP_165	OUTP_169	OUTP_157	OUTP_145	OUTP_133
BG	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO
BH	OUTN_229	OUTN_223	OUTN_217	OUTN_211	OUTN_205	OUTN_199	OUTN_193	OUTN_187	OUTN_181	OUTN_175	OUTN_163	OUTN_151	OUTN_139
BJ	OUTP_229	OUTP_223	OUTP_217	OUTP_211	OUTP_205	OUTP_199	OUTP_193	OUTP_187	OUTP_181	OUTP_175	OUTP_163	OUTP_151	OUTP_139

Figure 3-6. M21170 Pinout Diagram (5 of 8)

	27	28	29	30	31	32	33	34	35	36	37	38	39
A	OUTP_108	OUTP_102	OUTP_96	OUTP_90	OUTP_84	OUTP_78	OUTP_72	OUTP_66	OUTP_60	OUTP_54	OUTP_48	OUTP_42	OUTP_36
B	OUTN_108	OUTN_102	OUTN_96	OUTN_90	OUTN_84	OUTN_78	OUTN_72	OUTN_66	OUTN_60	OUTN_54	OUTN_48	OUTN_42	OUTN_36
C	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS
D	OUTP_114	OUTP_122	OUTP_110	OUTP_98	OUTP_86	OUTP_74	OUTP_62	OUTP_56	OUTP_50	OUTP_44	OUTP_38	OUTP_32	OUTP_26
E	OUTN_114	OUTN_122	OUTN_110	OUTN_98	OUTN_86	OUTN_74	OUTN_62	OUTN_56	OUTN_50	OUTN_44	OUTN_38	OUTN_32	OUTN_26
F	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO
G	OUTP_116	OUTP_104	OUTP_92	OUTP_80	OUTP_68	OUTP_100	OUTP_88	OUTP_76	OUTP_64	OUTP_52	OUTP_40	OUTP_28	OUTP_16
H	OUTN_116	OUTN_104	OUTN_92	OUTN_80	OUTN_68	OUTN_100	OUTN_88	OUTN_76	OUTN_64	OUTN_52	OUTN_40	OUTN_28	OUTN_16
J	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS
K	OUTP_118	OUTP_112	OUTP_106	OUTP_94	OUTP_82	OUTP_70	OUTP_58	OUTP_46	OUTP_34	OUTP_22	OUTP_10	VSS	INN_4
L	OUTN_118	OUTN_112	OUTN_106	OUTN_94	OUTN_82	OUTN_70	OUTN_58	OUTN_46	OUTN_34	OUTN_22	OUTN_10	VSS	INN_16
M	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	INN_28
N	AVDDO	VSS	AVDDO	VSS	VSS	VSS	VSS	VSS	TEN	TEST0	TEST1	AVDDI	INN_40
P	AVDDO	VSS	AVDDO	VSS	VSS	VSS	VSS	VSS	OUTP_AUXE	VSS	CONFIG0	VSS	INN_52
R	AVDDO	VSS	AVDDO	VSS	VSS	VSS	VSS	VSS	OUTN_AUXE	VSS	CONFIG1	AVDDI	INN_64
T	AVDDO	VSS	AVDDO	VSS	VSS	VSS	NC	NC	VSS	VSS	NC	VSS	INN_76
U	AVDDO	VSS	AVDDO	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AVDDI	INN_88
V	AVDDO	VSS	AVDDO	VSS	VSS	DVDDIO_2	VSS	VSS	VSS	VSS	VSS	VSS	INN_100
W	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	VSS	VSS	AVDD	INN_112
Y	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	VSS	INN_124
AA	VSS	VSS	VSS	VSS	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	INN_136
AB	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	VSS	INN_142
AC	VSS	VSS	VSS	VSS	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	INN_148
AD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	VSS	INN_154
AE	VSS	VSS	VSS	VSS	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	INN_160
AF	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	VSS	INN_166
AG	VSS	VSS	VSS	VSS	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	INN_172

Figure 3-7. M21170 Pinout Diagram (6 of 8)



	27	28	29	30	31	32	33	34	35	36	37	38	39
AH	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	VSS	INN_178
AJ	VSS	VSS	VSS	VSS	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	AVDDI	INN_184
AK	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	VSS	VSS	VSS	VSS	INN_196
AL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AVDDI	INN_208
AM	AVDDO	VSS	AVDDO	VSS	VSS	VSS	INP_AUXE	VSS	VSS	VSS	VSS	VSS	INN_220
AN	AVDDO	VSS	AVDDO	VSS	VSS	VSS	INN_AUXE	VSS	VSS	VSS	VSS	AVDDI	INN_232
AP	AVDDO	VSS	AVDDO	VSS	VSS	VSS	VSS	VSS	OUTN_AUXO	VSS	VSS	VSS	INN_244
AR	AVDDO	VSS	AVDDO	VSS	VSS	VSS	VSS	VSS	OUTP_AUXO	NC	VSS	AVDDI	INN_256
AT	AVDDO	VSS	AVDDO	VSS	VSS	VSS	VSS	VSS	VSS	NC	VSS	VSS	INN_268
AU	AVDDO	VSS	AVDDO	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AVDDI	INN_280
AV	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	VSS
AW	OUTN_149	OUTN_143	OUTN_137	OUTN_125	OUTN_113	OUTN_101	OUTN_89	OUTN_77	OUTN_65	OUTN_53	OUTN_41	OUTN_29	OUTN_17
AY	OUTP_149	OUTP_143	OUTP_137	OUTP_125	OUTP_113	OUTP_101	OUTP_89	OUTP_77	OUTP_65	OUTP_53	OUTP_41	OUTP_29	OUTP_17
BA	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS
BB	OUTN_135	OUTN_123	OUTN_111	OUTN_99	OUTN_87	OUTN_75	OUTN_131	OUTN_119	OUTN_107	OUTN_95	OUTN_83	OUTN_71	OUTN_59
BC	OUTP_135	OUTP_123	OUTP_111	OUTP_99	OUTP_87	OUTP_75	OUTP_131	OUTP_119	OUTP_107	OUTP_95	OUTP_83	OUTP_71	OUTP_59
BD	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO
BE	OUTN_121	OUTN_109	OUTN_141	OUTN_129	OUTN_117	OUTN_105	OUTN_93	OUTN_81	OUTN_69	OUTN_63	OUTN_57	OUTN_51	OUTN_45
BF	OUTP_121	OUTP_109	OUTP_141	OUTP_129	OUTP_117	OUTP_105	OUTP_93	OUTP_81	OUTP_69	OUTP_63	OUTP_57	OUTP_51	OUTP_45
BG	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS
BH	OUTN_127	OUTN_115	OUTN_103	OUTN_97	OUTN_91	OUTN_85	OUTN_79	OUTN_73	OUTN_67	OUTN_61	OUTN_55	OUTN_49	OUTN_43
BJ	OUTP_127	OUTP_115	OUTP_103	OUTP_97	OUTP_91	OUTP_85	OUTP_79	OUTP_73	OUTP_67	OUTP_61	OUTP_55	OUTP_49	OUTP_43

Figure 3-8. M21170 Pinout Diagram (7 of 8)

	40	41	42	43	44	45	46	47	48	49
A	OUTP_30	OUTP_24	OUTP_18	OUTP_12	OUTP_6	OUTP_0	VSS	VSS		
B	OUTN_30	OUTN_24	OUTN_18	OUTN_12	OUTN_6	OUTN_0	VSS	VSS	VSS	
C	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	VSS	VSS
D	OUTP_20	OUTP_14	OUTP_8	OUTP_2	VSS	INN_2	INP_2	AVDDI	INN_0	INP_0
E	OUTN_20	OUTN_14	OUTN_8	OUTN_2	VSS	INN_8	INP_8	VSS	INN_6	INP_6
F	VSS	AVDDO	VSS	VSS	VSS	INN_14	INP_14	AVDDI	INN_12	INP_12
G	OUTP_4	VSS	INN_10	INP_10	AVDDI	INN_20	INP_20	VSS	INN_18	INP_18
H	OUTN_4	VSS	INN_22	INP_22	VSS	INN_26	INP_26	AVDDI	INN_24	INP_24
J	VSS	VSS	INN_34	INP_34	AVDDI	INN_32	INP_32	VSS	INN_30	INP_30
K	INP_4	AVDDI	INN_46	INP_46	VSS	INN_38	INP_38	AVDDI	INN_36	INP_36
L	INP_16	VSS	INN_58	INP_58	AVDDI	INN_44	INP_44	VSS	INN_42	INP_42
M	INP_28	AVDDI	INN_70	INP_70	VSS	INN_50	INP_50	AVDDI	INN_48	INP_48
N	INP_40	VSS	INN_82	INP_82	AVDDI	INN_56	INP_56	VSS	INN_54	INP_54
P	INP_52	AVDDI	INN_94	INP_94	VSS	INN_62	INP_62	AVDDI	INN_60	INP_60
R	INP_64	VSS	INN_106	INP_106	AVDDI	INN_68	INP_68	VSS	INN_66	INP_66
T	INP_76	AVDDI	INN_118	INP_118	VSS	INN_80	INP_80	AVDDI	INN_72	INP_72
U	INP_88	VSS	INN_130	INP_130	AVDDI	INN_92	INP_92	VSS	INN_78	INP_78
V	INP_100	AVDDI	INN_74	INP_74	VSS	INN_104	INP_104	AVDDI	INN_84	INP_84
W	INP_112	VSS	INN_86	INP_86	AVDDI	INN_116	INP_116	VSS	INN_90	INP_90
Y	INP_124	AVDDI	INN_98	INP_98	VSS	INN_128	INP_128	AVDDI	INN_96	INP_96
AA	INP_136	VSS	INN_110	INP_110	AVDDI	INN_140	INP_140	VSS	INN_102	INP_102
AB	INP_142	AVDDI	INN_122	INP_122	VSS	INN_108	INP_108	AVDDI	INN_114	INP_114
AC	INP_148	VSS	INN_134	INP_134	AVDDI	INN_120	INP_120	VSS	INN_126	INP_126
AD	INP_154	AVDDI	INN_146	INP_146	VSS	INN_132	INP_132	AVDDI	INN_138	INP_138
AE	INP_160	VSS	INN_152	INP_152	AVDDI	INN_144	INP_144	VSS	INN_150	INP_150
AF	INP_166	AVDDI	INN_158	INP_158	VSS	INN_156	INP_156	AVDDI	INN_162	INP_162
AG	INP_172	VSS	INN_170	INP_170	AVDDI	INN_168	INP_168	VSS	INN_174	INP_174

Figure 3-9. M21170 Pinout Diagram (8 of 8)

	40	41	42	43	44	45	46	47	48	49
AH	INP_178	AVDDI	INN_182	INP_182	VSS	INN_164	INP_164	AVDDI	INN_180	INP_180
AJ	INP_184	VSS	INN_194	INP_194	AVDDI	INN_176	INP_176	VSS	INN_186	INP_186
AK	INP_196	AVDDI	INN_206	INP_206	VSS	INN_188	INP_188	AVDDI	INN_192	INP_192
AL	INP_208	VSS	INN_218	INP_218	AVDDI	INN_200	INP_200	VSS	INN_198	INP_198
AM	INP_220	AVDDI	INN_190	INP_190	VSS	INN_212	INP_212	AVDDI	INN_204	INP_204
AN	INP_232	VSS	INN_202	INP_202	AVDDI	INN_224	INP_224	VSS	INN_210	INP_210
AP	INP_244	AVDDI	INN_214	INP_214	VSS	INN_230	INP_230	AVDDI	INN_216	INP_216
AR	INP_256	VSS	INN_226	INP_226	AVDDI	INN_236	INP_236	VSS	INN_222	INP_222
AT	INP_268	AVDDI	INN_238	INP_238	VSS	INN_242	INP_242	AVDDI	INN_228	INP_228
AU	INP_280	VSS	INN_250	INP_250	AVDDI	INN_248	INP_248	VSS	INN_234	INP_234
AV	VSS	AVDDI	INN_262	INP_262	VSS	INN_254	INP_254	AVDDI	INN_240	INP_240
AW	OUTN_5	VSS	INN_274	INP_274	AVDDI	INN_260	INP_260	VSS	INN_246	INP_246
AY	OUTP_5	VSS	INN_286	INP_286	VSS	INN_266	INP_266	AVDDI	INN_252	INP_252
BA	AVDDO	VSS	VSS	VSS	AVDDI	INN_272	INP_272	VSS	INN_258	INP_258
BB	OUTN_47	OUTN_35	OUTN_23	OUTN_11	VSS	INN_278	INP_278	AVDDI	INN_264	INP_264
BC	OUTP_47	OUTP_35	OUTP_23	OUTP_11	VSS	INN_284	INP_284	VSS	INN_270	INP_270
BD	VSS	AVDDO	VSS	AVDDO	VSS	VSS	VSS	AVDDI	INN_276	INP_276
BE	OUTN_39	OUTN_33	OUTN_27	OUTN_21	OUTN_15	OUTN_9	OUTN_3	VSS	INN_282	INP_282
BF	OUTP_39	OUTP_33	OUTP_27	OUTP_21	OUTP_15	OUTP_9	OUTP_3	VSS	VSS	VSS
BG	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	AVDDO	VSS	VSS	VSS
BH	OUTN_37	OUTN_31	OUTN_25	OUTN_19	OUTN_13	OUTN_7	OUTN_1	VSS	VSS	
BJ	OUTP_37	OUTP_31	OUTP_25	OUTP_19	OUTP_13	OUTP_7	OUTP_1	VSS		

3.3 M21170 Package Information

The M21170 is packaged in a lead (Pb) free 50 mm x 50 mm 2389-pin Ball Grid Array (BGA) and complies with the temperatures and profiles outlined in the JEDEC standard IPC/JEDEC J-STD-020.

Figure 3-10. M21170 Packaging Drawing (Bottom View)

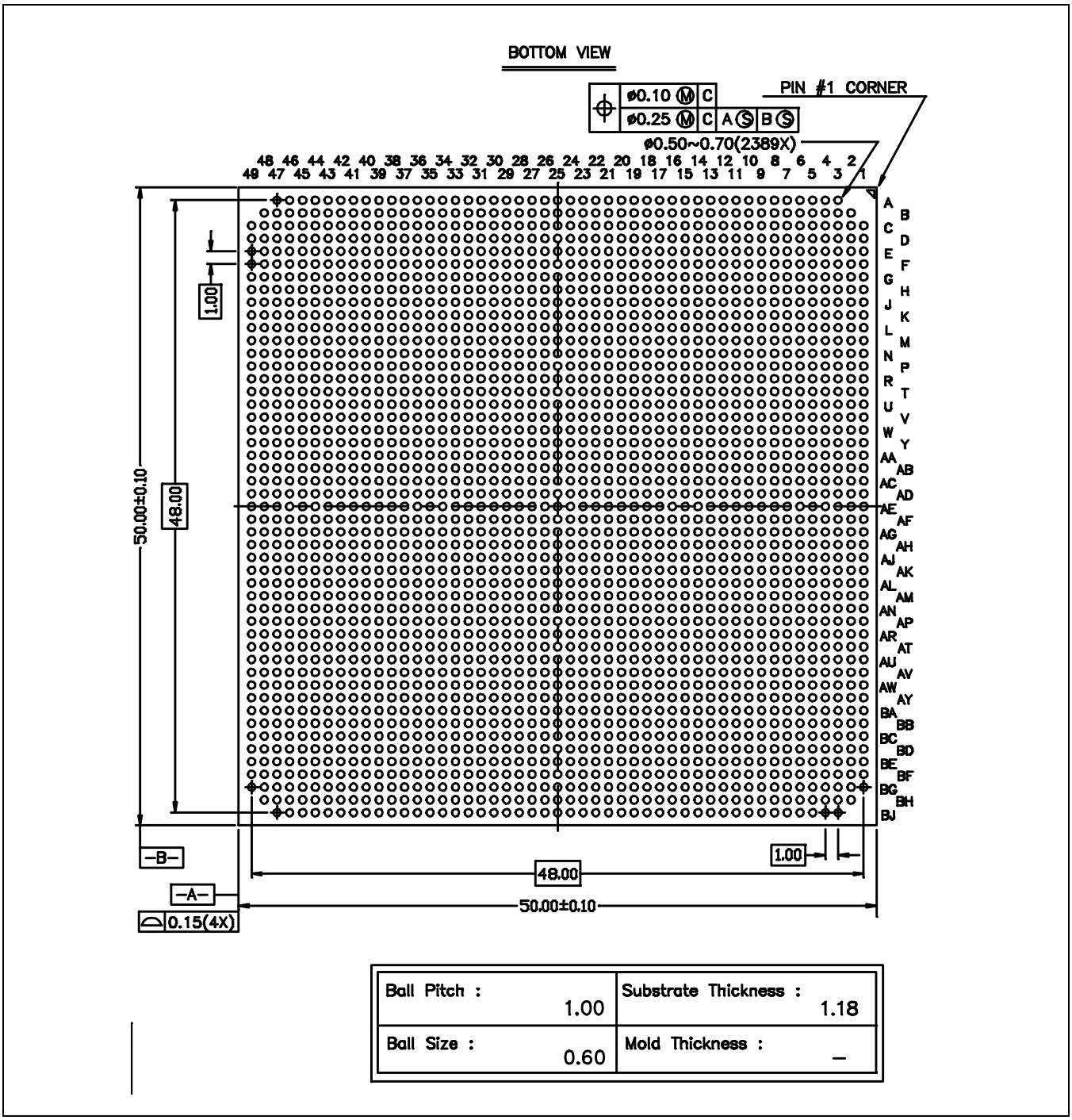
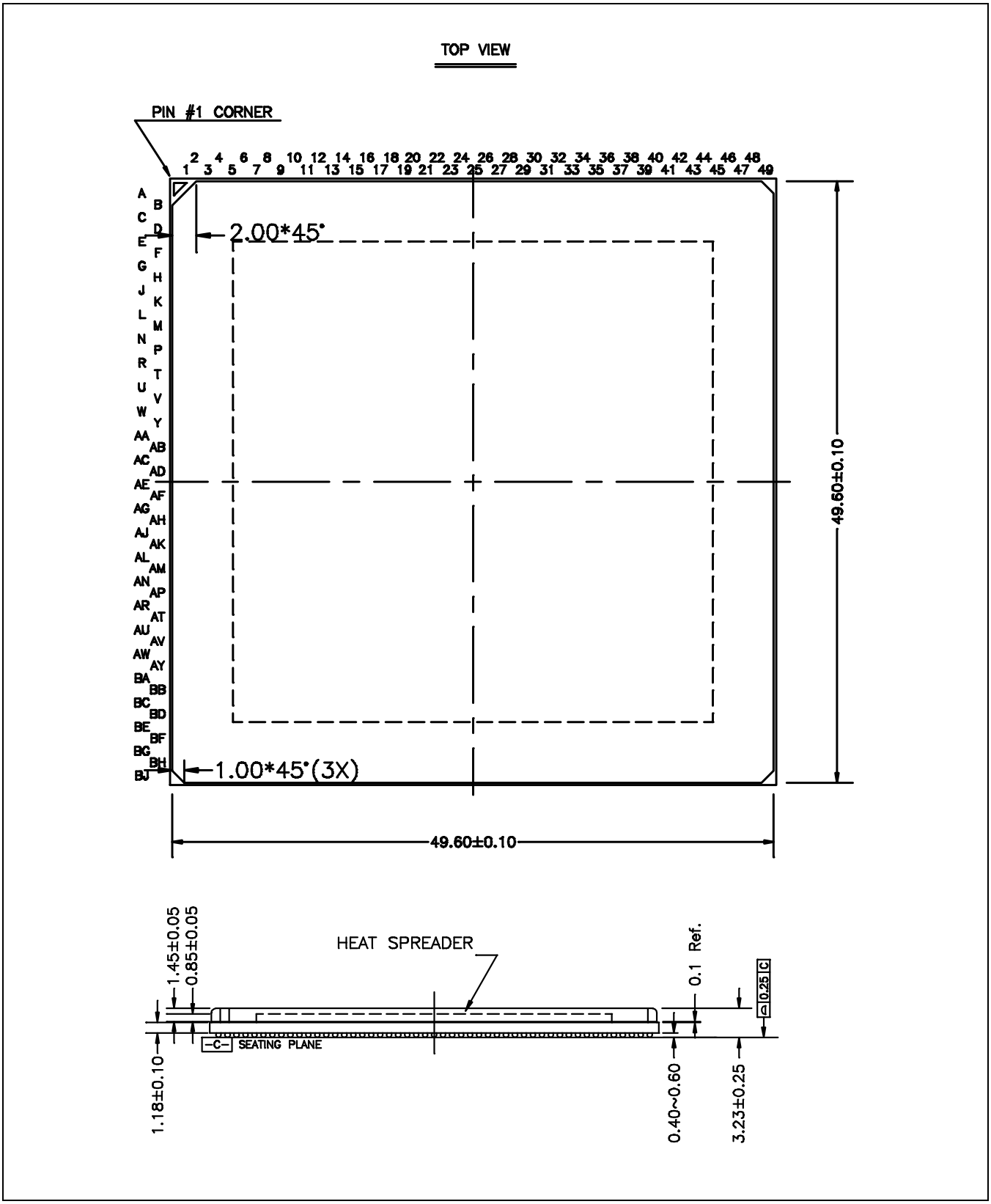


Figure 3-11. M21170 Packaging Drawing (Top and Side Views)



4.0 Functional Description

The M21170 is a 288x288 multi-rate asynchronous crosspoint switch capable of robust operation at data rates up to 3.2 Gbps. In order to allow for synchronous switching, the crosspoint core can be configured by two pre-programmed switch states, or intermediate switch configurations (ISC). Changing the switch state may be triggered using any or all of four strobe ports, or xSETs, via hardware pins or registers bits. Alternatively, the switch may be configured in direct access mode, in which case all states take effect immediately after programming.

Advanced programmable signal conditioning in the form of input equalization and output de-emphasis are provided to improve performance in large, high data rate systems. The M21170 also includes a Loss of Signal (LOS) detector on each input lane that can used to squelch the output preventing unwanted chatter.

The M21170 is designed to be compatible with multiple protocol standards such as Serial Digital Interface (SDI) video, InfiniBand, Fibre Channel, XAUI GbE, parallel 10GbE and SONET. The various options of the device and the switch state can be configured with registers accessed through a 2-wire (I^2C compatible), 4-wire, or parallel interface (9-bits data, 9-bits address).

The following figure depicts the functional block diagram of the M21170. The various functions and blocks are described in detail in the subsequent sections.

Figure 4-1. M21170 Functional Block Diagram

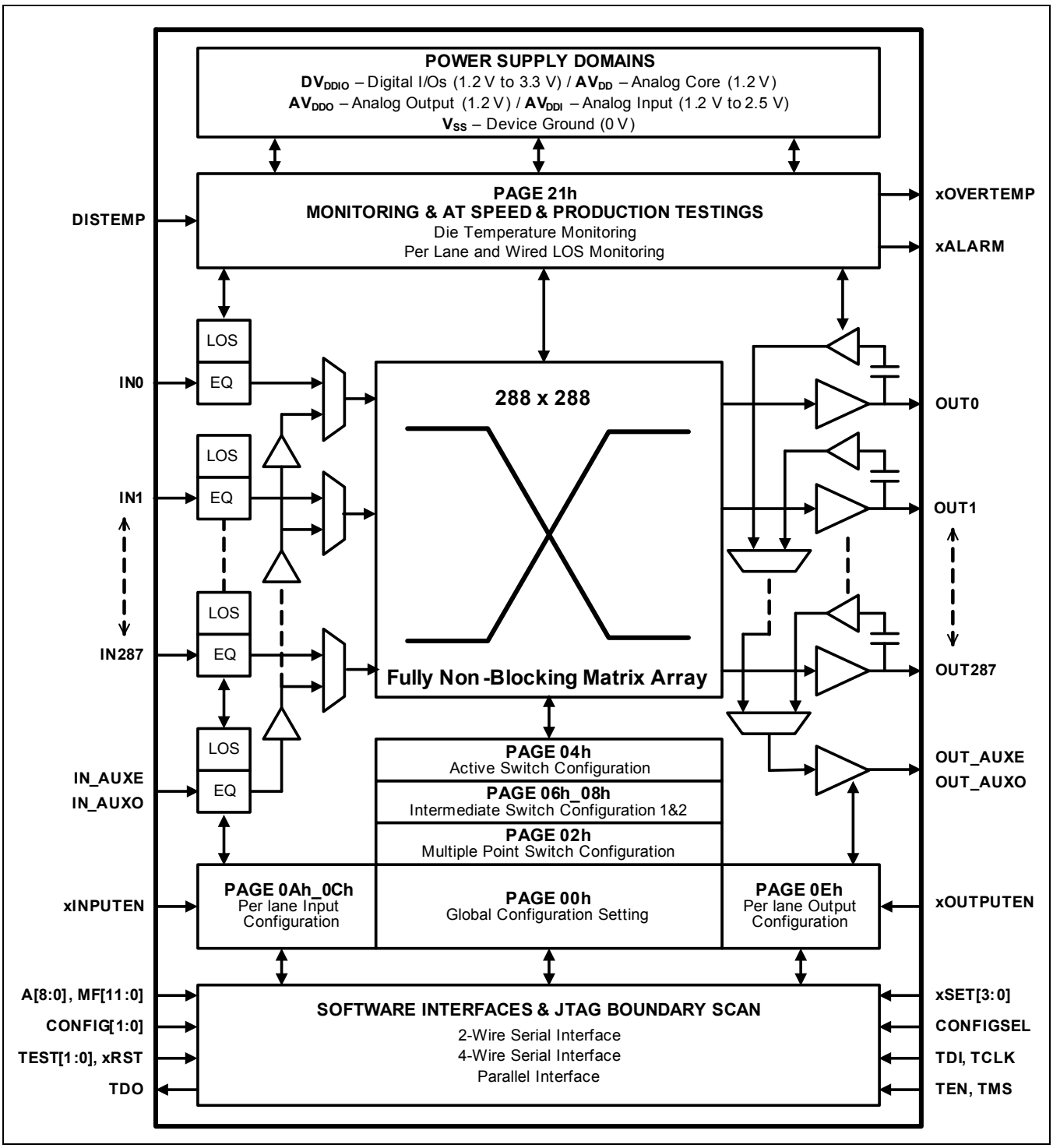


Figure 4-2. High-Speed Differential Input

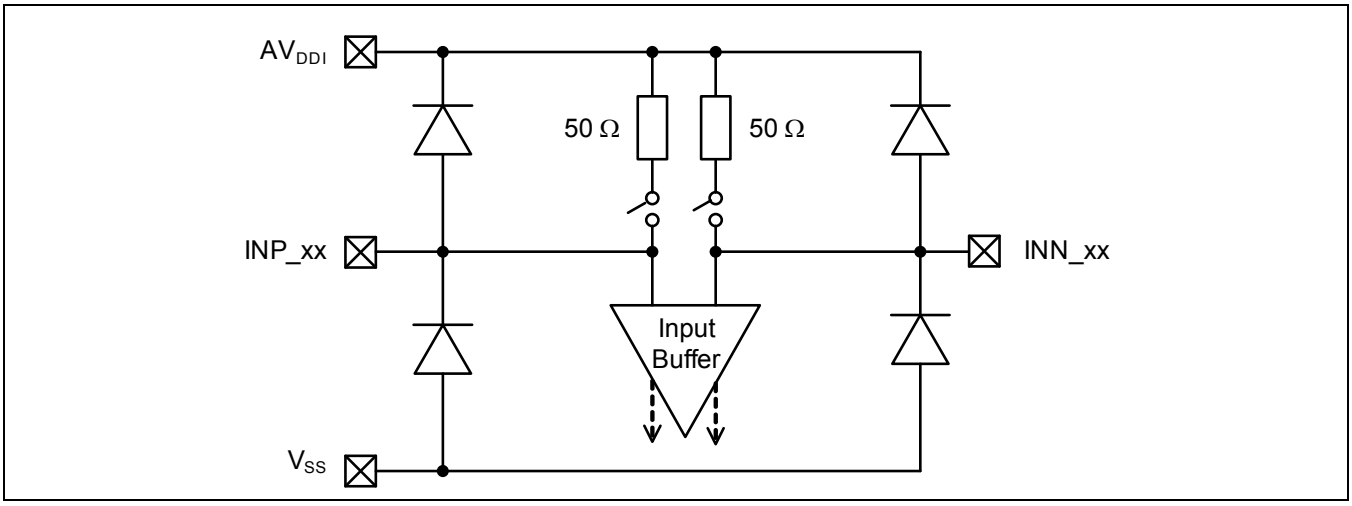


Figure 4-3. High-Speed Differential Output

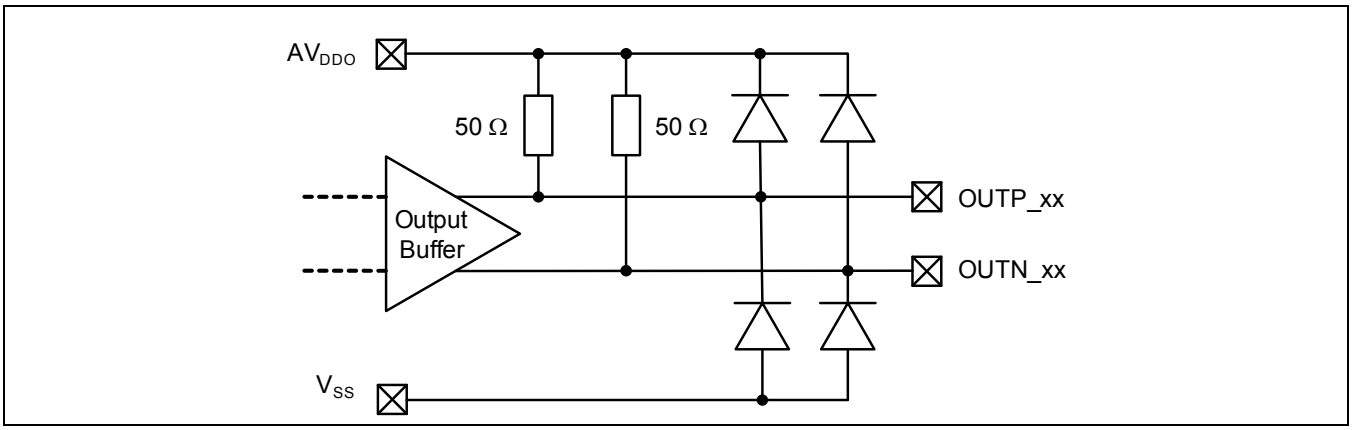


Figure 4-4. Digital Open Drain Logic

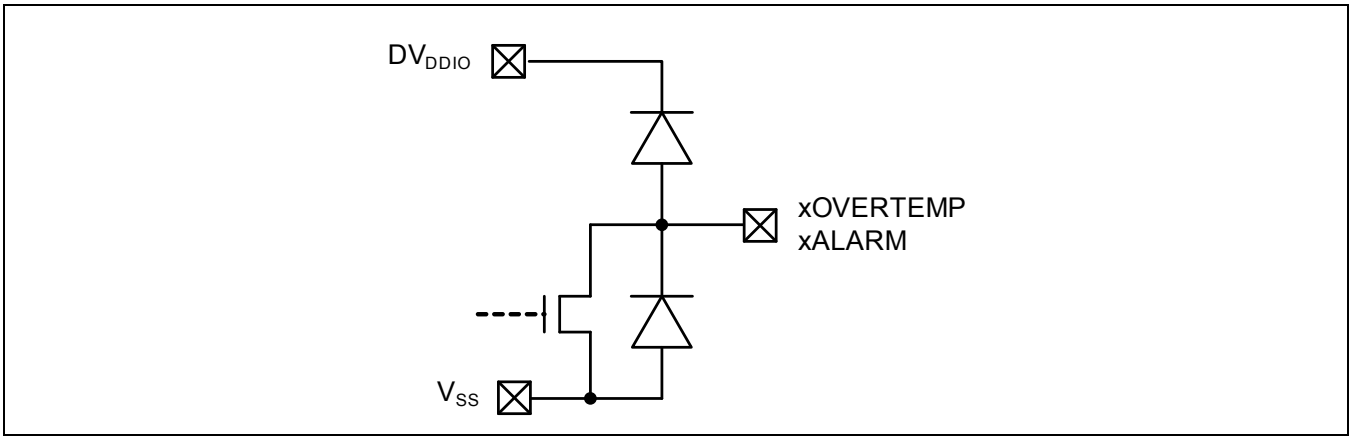


Figure 4-5. Digital CMOS Output

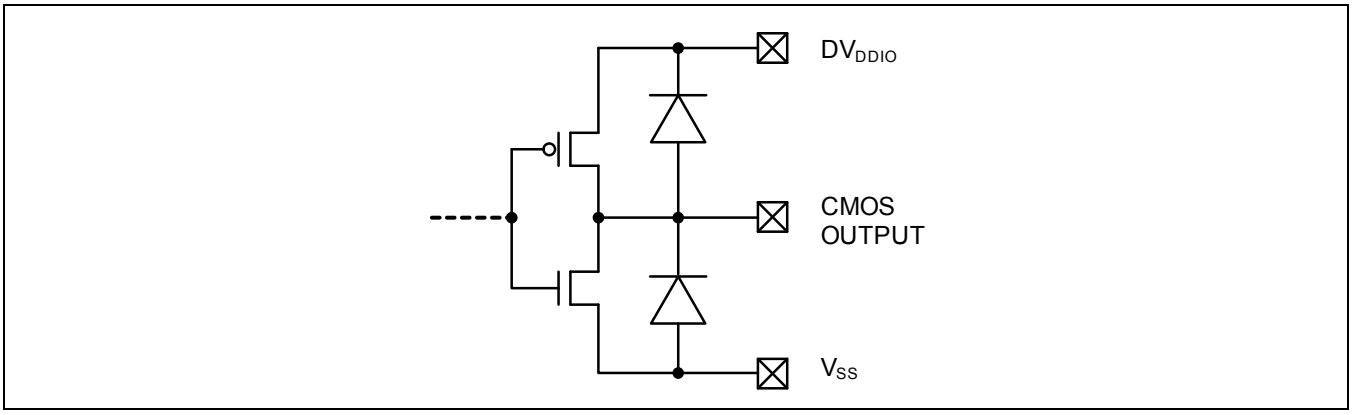


Figure 4-6. Digital CMOS Input

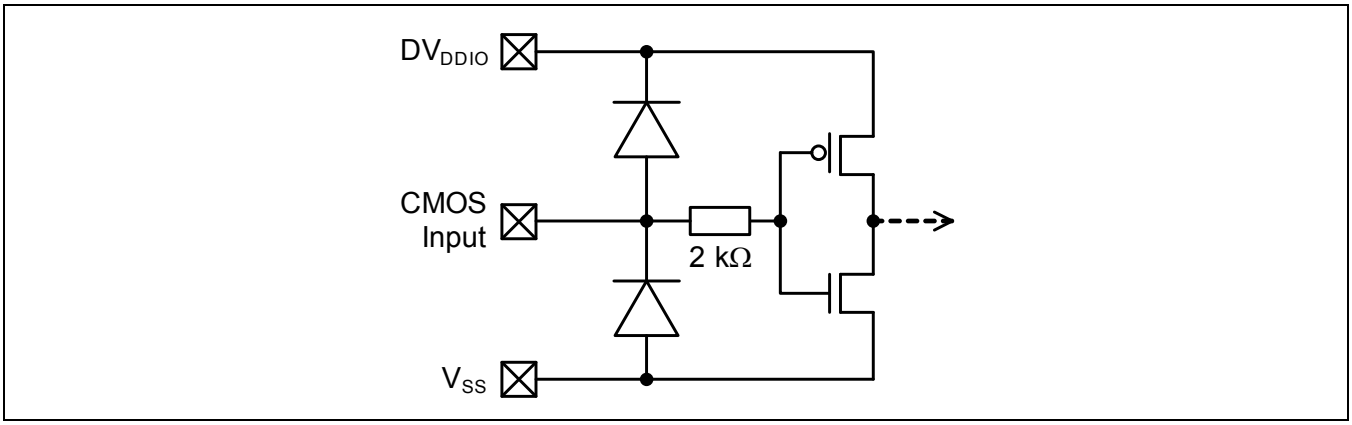


Figure 4-7. Digital CMOS Input with Pull Down

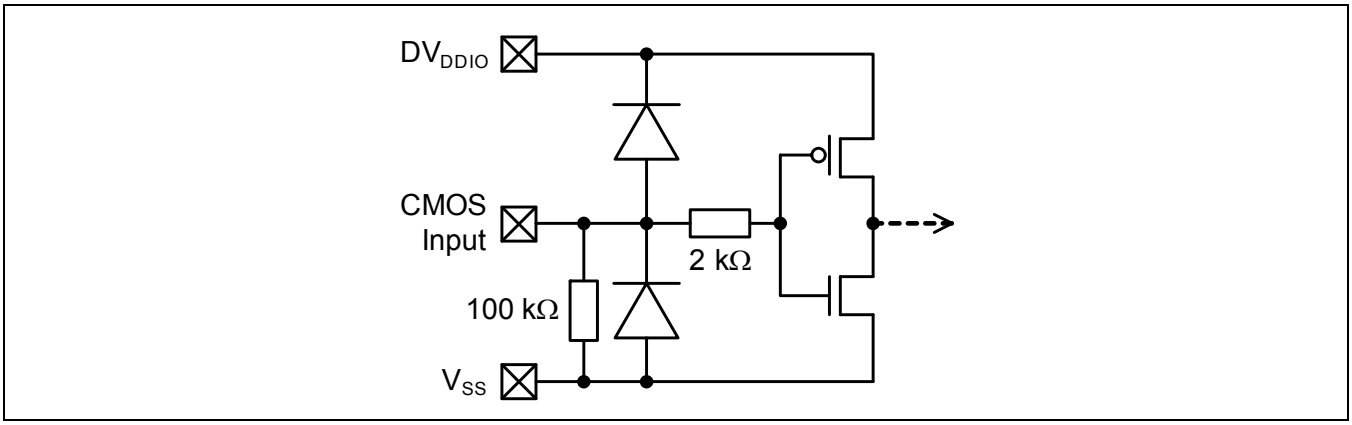
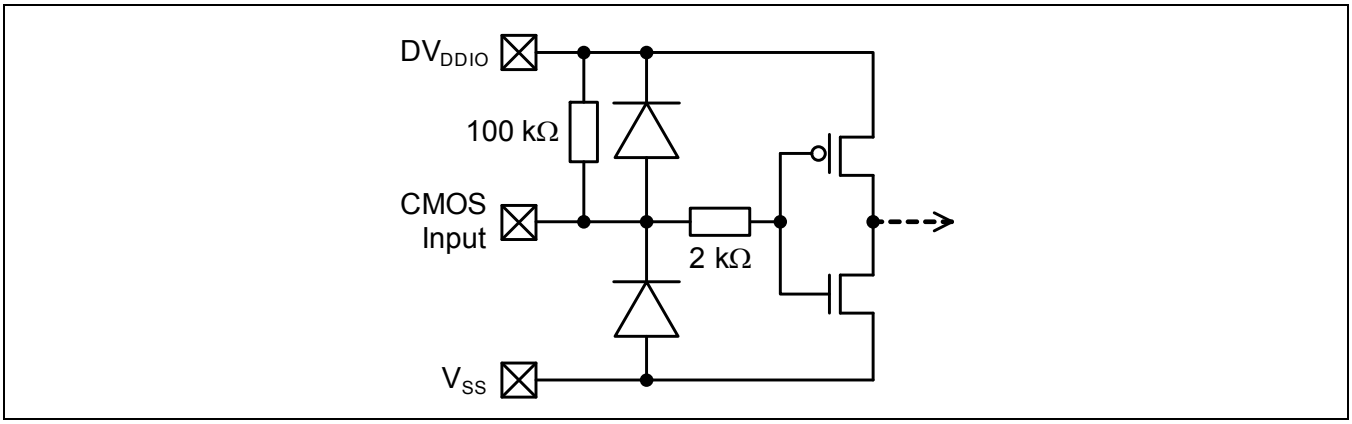


Figure 4-8. Digital CMOS Input with Pull Up



4.1 Power Up

4.1.1 Power on Reset

The M21170 initiates a power-on reset upon application of supply power at pin.**AV_{DD}**. A software reset can also be invoked by writing the value AAh to register.**master reset** (page.000h, address.000h). Alternatively, the device may also be reset manually by asserting a logical LOW on pin.**xRST** (pin active low). The soft reset is functionally equivalent to a hard reset. After a reset event, all registers are set to their default state as described in Chapter 5. A series of hardware pins in conjunction with the default register settings determine the default state of the crosspoint at power up. The hardware pins of interest are described in Chapter 3.

The device is configured after power-up, or a hardware or software reset as defined below:

- The switch configuration is set to multi-cast input lane #0 to all outputs.
- If pin.**xINPUTEN** is set LOW, then all input buffers are enabled with termination set to single-ended 50 Ω termination to pin.**AV_{DDI}** and input equalization is set to minimum.
- If pin.**xINPUTEN** is set HIGH, then all input buffers are powered-down. This includes the LOS detection circuitry. The input termination is set to 50 Ω to pin.**AV_{DDI}**.
- All output buffers are powered-down, regardless of the state of pin.**xOUTPUTEN**. This is to avoid having a large current draw at pin.**AV_{DDO}** on power-up. Pin.**xOUTPUTEN** becomes operational once register.**gboutbuf**.bit[6:5] (page.000h, address.006h) is set to something other than 00b.

4.1.2 Power up Sequence

The M21170 has four different power supplies: AV_{DDI}, AV_{DDO}, AV_{DD}, and DV_{DDIO}.

The recommended procedure is to power up DV_{DDIO} and AV_{DD} at the same time if possible; this is easily implemented if AV_{DD} = DV_{DDIO} = 1.2 V. For DV_{DDIO} voltages greater than 1.2 V, two different power supplies are needed. In this case, Mindspeed recommends having DV_{DDIO} supplied before or with AV_{DD}, to avoid control register corruption. If DV_{DDIO} is supplied after AV_{DD}, a hardware or software reset is needed to make sure all the registers hold their default value. This reset is needed due to the Power-on Reset (POR) being triggered by AV_{DD}, so if AV_{DD} is supplied before DV_{DDIO}, the digital engine does not receive the reset.

There is no power sequence needed for AV_{DDI} and/or AV_{DDO}, they can be supplied shortly after or before AV_{DD} or DV_{DDIO}.

4.2 High-Speed Input Lanes

The 288 primary high-speed input lanes of the M21170 are designed to support both DC interfaces and AC coupled interfaces with external capacitors. For AC coupled configurations, the recommended coupling capacitor is 10 µF for any Serial Digital Interface (SDI) video applications. For correct operation in DC coupled applications the input common mode voltage should match the output common mode voltage set by the transmitting devices driving the M21170. This can be achieved by setting the power supply voltage at pin.**AV_{DDI}** to that of the transmitting devices' output buffers.

After any power up and/or hardware/software reset, all input lanes are enabled with a single-ended on-device 50 Ω termination to pin.**AV_{DDI}** and minimum equalization setting. Alternatively, the input termination can be set to HIGH impedance either individually, by setting register.**gbinbuf**.bit[7] (page.000h, address.005h) to HIGH and programming register.**inputbuf(N)**.bit[5] (page.00Ah, address.hex(N)), or globally by setting register.**gbinbuf**.bit[7] (page.000h, address.005h) to LOW and programming register.**gbinbuf**.bit[5] (page.000h, address.005h).

The input buffers may be globally enabled or powered up with pin.**xINPUTEN**. When pin.**xINPUTEN** is set to LOW, the input buffers may be fully enabled or powered-down, either individually by setting register.**gbinbuf**.bit[7] (page.000h, address.005h) to HIGH and programming register.**inputbuf(N)**.bit[6] (page.00Ah, address.hex(N)), or globally by setting register.**gbinbuf**.bit[7] (page.000h, address.005h) to LOW and programming register.**gbinbuf**.bit[6] (page.000h, address.005h). Note that while the high-speed input buffer is disabled, it is possible to set its termination to 50 Ω or high-impedance through the host interface registers, as long as power is still applied to the whole device.

4.2.1 Input Equalization

Each input lane is equipped with configurable equalization to compensate for the losses that a high-speed signal accumulates after transmission across long copper traces. There are four levels of input equalization provided: minimum equalization, intermediate #1 and #2, and maximum equalization. Input equalization can be configured individually, on a per lane basis, or globally across all input lanes. For global configuration, register.**gbinbuf**.bit[7] (page.000h, address.005h) must be set to LOW and register.**gbinbuf**.bit[2:1] (page.000h, address.005h) programmed to the desired level. Individual equalization control for lane “N” may be achieved by setting register.**gbinbuf**.bit[7] to HIGH and then programming register.**inputbuf(N)**.bit[2:1] (page.00Ah, address.hex(N)) to the desired value.

4.2.2 DCD Correction Loop

All input lanes also feature an automatic offset correction loop to help compensate for DCD (Duty Cycle Distortion) or DC offset. The correction loop is designed to support the video pathological line event seen in SDI applications. The automatic offset correction loop is always globally enabled after any power-up and/or hardware/software reset. For best performance, Mindspeed recommends leaving this feature enabled unless some testing or debug is required or when data rates of 100 Mbps or below are used; then the DCD correction loop must be disabled. The offset correction loop can be disabled individually, on a per lane basis, or globally across all lanes. It can be globally configured by setting register.**gbinbuf**.bit[7] (page.000h, address.005h) to LOW and programming register.**gbinbuf**.bit[3] (page.000h, address.005h) or individually disabled, by setting register.**gbinbuf**.bit[7] to HIGH and then programming register.**inputbuf(N)**.bit[3] (page.00Ah, address.hex(N)).

4.2.3 Input LOS Detection Circuitry

The M21170 features a Loss of Signal (LOS) detection circuitry on each input lane. This circuit can be globally enabled and disabled, or set on an individual lane basis. The LOS detection is globally enabled at power-up. Global LOS configuration is controlled by register.**LOS config** (page.000h, address.007h). Global LOS threshold hysteresis is enabled at power-up and is controlled by register.**gbloshys** (page.021h, address.00Ch). When data

rates below 100 Mbps are used, Mindspeed recommends disabling the LOS circuitry as low data rate signals can falsely trigger an LOS Alarm.

Individual LOS activation for lane N is achieved by setting register.**LOS config**.bit[7] to HIGH and programming register.**input LOS(N)** (page.00Ch, address.hex(N)). Individual per lane setting of the LOS detection threshold is achieved by programming register.**input LOS(N)**.bit[6:4] (page.00Ch, address.hex(N)).

An LOS event on a given input lane is flagged by a bit in two LOS registers: register.**LOS alarm**(0:35) (page.000h, address.040h:063h) and register.**stat alarm**(0:35) (page.000h, address.080h:0A3h). Register.**LOS alarm** (page.000h, address.040h:063h) values are set and held upon an LOS event. A user write is required to clear any event. Alternatively, register.**stat alarm** (page.000h, address.080h:0A3h) values are user read-only and represent dynamic LOS activity. They set and reset based on LOS activity.

4.2.3.1 LOS Monitoring Feature 1, Hardware Pin.xAlarm

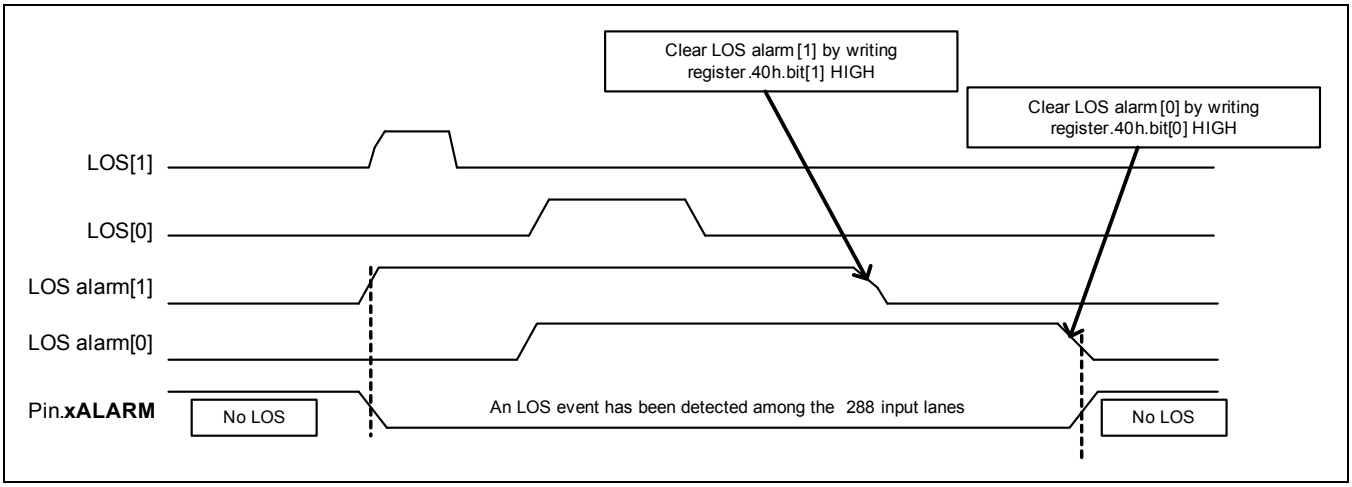
At power-up or after any hardware/software reset, the logical OR of all the values in register.**LOS alarm** (page.000h, address.040h:063h) can be monitored on hardware pin.**xALARM**. An added feature of this mode is the availability of masking the registers of unwanted channels. Bit settings in register.**mask alarm(0:35)** (page.000h, address.0C0h:0E3h) mask out unwanted lanes from the logical OR function permitting individual or group LOS monitoring.

The LOS alarm status from any single lane can be monitored in real-time on pin.**xALARM**. Monitoring the alarm from a single lane is achieved by first setting register.**LOS mon**.bit[0] (page.000h, address.008h) to HIGH, then monitoring the selected lane by programming both register.**LOS mon**.bit[1] (page.000h, address.008h) and register.**monchansel** (page.000h, address.009h).

4.2.3.2 Using xAlarm to Monitor LOS for ALL Input Channels, Application Example

1. After power up, xAlarm is LOW. This is as expected since there are a lot of channels with LOS triggered.
2. All the LOS Alarms need to be cleared (page.000h, addresses[040h:063h] = 00FFh), after pin.**xALARM** goes HIGH.
3. After an LOS alarm is triggered for any of the 288 input lanes, pin.**xALARM** goes LOW. Figure 4-9 shows this example.

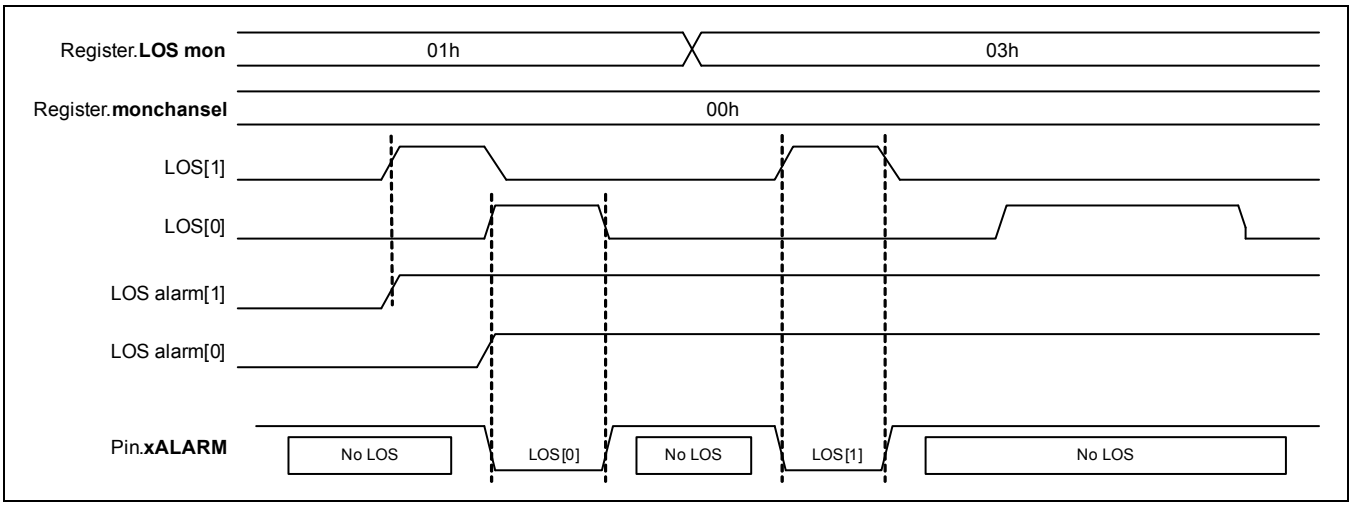
Figure 4-9. Monitoring LOS Globally using Hardware pin.xALARM



4.2.3.3 Using xAlarm to Monitor LOS for Individual Input Channels, Application Example

1. After power up, pin.**xALARM** is LOW. This is as expected since there are a lot of channels with LOS triggered.
2. All of the LOS Alarms need to be cleared (set page.000h, addresses[040h:063h] = 00FFh), after pin.**xALARM** goes HIGH.
3. Mask pin.**xALARM** for all inputs (set page.000h, registers[0C0h:0E3h] = 00FFh).
4. Unmask pin.**xALARM** for **INPUT0** (set page.000h, address.0C0h = FEh).
5. To monitor individual LOS from an even input lane, set register.**LOS mon** (page.000h, address.008h) = 01h.
6. To individually monitor **INPUT0**, set register.**monchansel** (page.000h, address.009h) = 00h.
7. Make the LOS toggle by supplying a signal and removing an input signal.
8. Pin.**xALARM** goes “LOW” when an LOS alarm event is recorded on CH0.
9. Using the same approach, CH1 can be monitored by the value in register.**LOS mon** (page.000h, address.008h) from 01h to 03h and unmasking INPUT1 xAlarm (set page.000h, address.0C0h = FDh), as shown in Figure 4-10 below.

Figure 4-10. Monitoring LOS Individual Lanes using Hardware pin.xALARM



4.2.3.4 LOS Monitoring Feature 2, register.LOS alarm and register.stat alarm

An LOS event on a given input lane is flagged by a bit in two LOS registers: register.**LOS alarm**(0:35) (page.000h, address.040h:063h) and register.**stat alarm**(0:35) (page.000h, address.080h:0A3h). The register.**LOS alarm** (page.000h, address.040h:063h) values are set and held upon an LOS event. A user write is required to clear any event. Alternatively, register.**stat alarm** (page.000h, address.080h:0A3h) values are user read-only and represent dynamic LOS activity. They set and reset based on LOS activity.

4.2.3.5 Using register.LOS alarm to Monitor LOS for Input Channels, Application Example

1. After power up, all of the LOS Alarms need to be cleared (set page.000h, registers[040:063] = 00FFh).
2. After an LOS alarm is triggered for any of the 288 input lanes, the register.**LOS alarm** records the LOS events until this register is cleared. In this example, page.000h, address.040h = 01h when INPUT0 has an LOS.
3. Page.000h, address.040h = 03h when both INPUT0 and INPUT1 have LOS.
    a. Write 01FFh = 0000h to select page.000h.
    b. Write 0040h = 00FFh to clear LOS alarm INPUTS 0 to 7.
    c. …
    d. Write 0063h = 00FFh to clear LOS alarm INPUTS 280 to 287.
    e. Read 0040h = 0001h means LOS on INPUT0.
    f. Read 0040h = 0003h means LOS on INPUTS 0 and 1.

4.2.3.6 Using register.stat alarm to Monitor LOS for Individual Input Channels, Application Example

1. After power up, all of the LOS Alarms need to be cleared, (set page.000h, addresses[040h:063h] = 00FFh).
2. Unmask xAlarm for **INPUT0**, (set page.000h, address.040h = FEh).
3. To monitor individual LOS from an even input lane, set register.**LOS mon** (page.000h, address.008h) = 01h.
4. To individually monitor **INPUT0**, set register.**monchansel** (page.000h, address.009h) = 00h.
5. Make the LOS toggle by supplying a signal and removing an input signal.
6. The register.**stat alarm** records the LOS events in real time, so this register does not need to be cleared. In this example, register page.000h, address.080h = 01h when INPUT0 has an LOS.
    a. Write 01FFh = 0000h to select page.000h.
    b. Write 0040h = 00FFh to clear LOS alarm INPUTS 0 to 7.
    c. …
    d. Write 0063h = 00FFh to clear LOS alarm INPUTS 280 to 287.
    e. Write 00C0h = 00FFh to mask LOS alarm INPUTS 0 to 7.
    f. …
    g. Write 00E3h = 00FFh to mask LOS alarm INPUTS 280 to 287.
    h. Write 00C0h = 00FDh to unmask LOS alarm INPUTS 0 and 1.
    i. Read 0040h = 0001h means LOS on INPUT0.
    j. Read 0040h = 0003h means LOS on INPUTS 0 and 1.

4.2.4 Auxiliary High-Speed Input Lanes

There are two auxiliary input lanes available at pin.**INP_AUXE** / pin.**INN_AUXE** and pin.**INP_AUXO** / pin.**INN_AUXO**. They also feature the same input equalization, LOS and input termination capabilities as any primary high-speed input lane. At power-up or after any hardware/software reset, the two auxiliary inputs are disabled and set in power-down mode. Specifically, their input terminations are automatically set to high impedance and the LOS detection circuitry and the offset compensation circuitry are both disabled.

Any primary input lane can be programmed to propagate the high-speed input data stream seen at the corresponding high speed input pins, or to propagate the high-speed input data stream seen at the two auxiliary input lanes available at pin.**INP_AUXE** / pin.**INN_AUXE** for the even input lanes, and at pin.**INP_AUXO** / pin.**INN_AUXO** for the odd input lanes. At power up or after any hardware/software reset the part will always propagate the primary high-speed data stream seen at the regular input pins. Propagating the auxiliary signal seen at pin.**INP_AUXE** / pin.**INN_AUXE** (respectively at pin.**INP_AUXO** / pin.**INN_AUXO**) to all input even (respectively odd) lanes, is achieved globally by setting register.**gbinbuf**.bit[7] (page.000h, address.005h) to LOW and programming register.**gbinbuf**.bit[4] (page.000h, address.005h). This operation can also be performed on an individual or lane-per-lane basis by setting register.**gbinbuf**.bit[7] (page.000h, address.005h) to HIGH and programming register.**inputbuf(N)**.bit[4] (page.00Ah, address.hex(N)).

The circuitry at pin.**INP_AUXE** / pin.**INN_AUXE** is configured by programming register.**auxine** (page.021h, address.080h) and register.**LOS auxe** (page.021h, address.082h). Similarly the circuitry at pin.**INP_AUXO** / pin.**INN_AUXO** is configured by programming register.**auxino** (page.021h, address.081h) and register.**LOS auxo** (page.021h, address.083h).

The two auxiliary inputs also have the capability to generate and propagate a logical LOW or HIGH without any signal applied at their respective input pins. This feature can be achieved by forcing an LOS event on the auxiliary input, using register.**LOS auxe**.bit[2] and register.**LOS auxo**.bit[2], then squelching the polarity (propagate a logical '1' by squelching HIGH, or a logical '0' by squelching LOW) using respectively register.**LOS auxe**.bit[3] for the even lanes, and register.**LOS auxo**.bit[3] for the odd lanes. Toggling between '1' and '0' values can create a low-speed pattern which may be used during test and debug.

4.3 High-Speed Output Drivers

The 288 primary high-speed output lanes of the M21170 are designed to be AC coupled, using external coupling capacitors, or DC coupled.

All output pins have a single-ended on-device 50 Ω termination connected to pin.**AV_{DDO}**.

DC coupled operation can be supported but may change the common-mode output voltage and differential output swing depending on the input circuitry of the downstream device. Mindspeed recommends consulting your local application resource for any designs requiring DC coupled configuration. All of the figures (output swing and de-emphasis, power at pin.**AV_{DDO}**, etc.) in this document only apply to AC coupled outputs. The recommended coupling capacitor is at least 10 µF for any SDI video applications.

Output drivers can be configured individually, on a per lane basis, or globally across all lanes.

The outputs can be globally disabled and powered down when pin.**xOUTPUTEN** is set to HIGH. When pin.**xOUTPUTEN** is set to LOW, the output driver is configured through the corresponding registers. To control the outputs globally, register.**gboutbuf** (page.000h, address.006h) must be used. To control output driver “N” individually, register.**gboutbuf**.bit[7] must be set HIGH and register.**outputbuf(N)** (page.00Eh, address.hex(N)) must be programmed.

The output buffer is biased using the supply pin.**AV_{DDO}** which can be set to 1.2 V. The differential output swing can be set to any of the three nominal settings of minimum, intermediate, and maximum.

The output swing level can be set globally using register.**gboutbuf**.bit[6:5] (page00h, address.06h) or individually using register.**outputbuf(N)**.bit[6:5] (page.00Eh, address.hex(N)).

The M21170 also has a three-step (approximately 2 dB per step, 6 dB maximum), output de-emphasis capability.

The output de-emphasis is disabled after any power up, hardware or software reset and can be set globally by programming register.**gboutbuf**.bit[4:3] (page00h, address.06h) or individually using register.**outputbuf(N)**.bit[4:3] (page.00Eh, address.hex(N)). The de-emphasis time constant can similarly be set individually or globally using bit[2] from the above mentioned registers.

At power up or after any hardware/software reset the output drivers are all disabled regardless of the state of pin.**xOUTPUTEN**. It is therefore required to enable the output drivers either globally using register.**gboutbuf** (page.000h, address.006h) or individually by setting register.**gboutbuf**.bit[7] to HIGH and programming register.**outputbuf(N)** (page.00Eh, address.hex(N)). Mindspeed recommends enabling the output drivers individually, one at a time, to minimize current surge at pin.$\mathbf{AV_{DDO}}$ and get a smoother power ramp-up.

There are two modes for enabling and disabling the output drivers; these modes are selected by programming register.**gboutbuf**.bit[1] (page00h, address.06h).

The first mode used to power down an output buffer is by powering off the lane that the output buffer is connected to. By default, register.**gboutbuf**.bit[1] is set to “0b”, this would disable not only the output driver but the lane connected to that particular driver, namely the lane specified on the ASC registers (page.004h). To power down both the output driver and its corresponding lane, a “1FFh” must be written to the desired lane on the ASC register (page.004h).

The second mode used to power down only a particular output driver is achieved by setting register.**gboutbuf**.bit[1] to “1b” and writing “00h” for the corresponding address in the individual output driver configuration registers on page.00Eh.

4.3.1 Auxiliary High-Speed Output Lanes

The M21170 features two auxiliary output drivers available at pin.**OUTP_AUXE** / pin.**OUTN_AUXE** and pin.**OUTP_AUXO** / pin.**OUTN_AUXO**. They are equipped with the same output swing and de-emphasis capabilities as the primary high-speed output drivers. At power up or after any hardware/software reset, the two auxiliary drivers are disabled and set in power down mode.

The auxiliary driver at pin.**OUTP_AUXE**, pin.**OUTN_AUXE** is configured by programming register.**auxoute** (page.021h, address.02Fh). Similarly the auxiliary driver at pin.**OUTP_AUXO** / pin.**OUTN_AUXO** is configured by programming register.**auxouto** (page.021h, address.03Fh).

Each driver has the capability to monitor 144 individual output lanes to facilitate testing and debugging. Any of the even primary output lanes can be routed to the driver at pin.**OUTP_AUXE** / pin.**OUTN_AUXE**. This is done by programming register.**outmone** (page.021h, address.008h). Similarly, the driver at pin.**OUTP_AUXO** / pin.**OUTN_AUXO** can be used to monitor any of the 144 odd primary output lanes by programming register.**outmono** (page.021h, address.009h).

NOTE: When using the auxiliary output to monitor the signal at the other outputs, both the auxiliary channel and the output to be monitored need to be terminated. If left unterminated, reflection at the unterminated output will propagate at the auxiliary output.

4.4 Active Switch Configuration (ASC)

The M21170 features a fully non-blocking 288x288 switching matrix, allowing a total of 82,944 possible switching paths.

There are three modes for changing and/or updating the switching matrix configuration:

- The direct ASC mode by programming the desired switching path registers at page.004h.
- The hardware strobe mode, using pin.**xSET**[3:0] and selectively loading one of two pre-determined switching maps.
- The software strobe mode, using register.**strobe** (page.000h, address.004h) and selectively loading one of two pre-determined switching maps.

After power-up or any hardware/software reset, the M21170 is by default in hardware strobe ASC mode. The selection of the switching matrix mode is always determined by programming register.**gen config**.bit[5:4].

4.4.1 Direct ASC Mode

The device is put in direct ASC mode by setting pin.**xSET**[3:0] to LOW and programming register.**gen config**.bit[5:4] (page.000h, address.003h, bit[5:4]) to 00b.

In this mode, any input lane can be independently and asynchronously routed to a specific output lane “N”. Upon a direct write to the appropriate register.**ascout(N)** (page.004h, address.hex(N)) the new ASC register contents and the new switching configuration map will be immediately asserted, without requiring a hardware or software strobe event.

4.4.2 Hardware Strobe Mode

The device is put in hardware strobe mode by programming register.**gen config**.bit[5:4] (page.000h, address.003h) to 01b. This is also the default setting after any power-up and/or hardware/software reset.

The M21170 features four independent, external, switch configuration strobe inputs at hardware pin.**xSET0**, pin.**xSET1**, pin.**xSET2**, and pin.**xSET3**. The hardware strobe pins may be used to synchronously trigger updating the active switch configuration register.

The user may define the strobe signal for each switching lane independently by programming the corresponding switching lane register at page.002h. Any or all switching lanes may be assigned to any or all of the strobe signals.

At power-up, or after any hardware/software reset, all of the 288 switching lanes are assigned to switch with the hardware strobe pin.**xSET0**.

The active switching matrix configuration (ASC) may be loaded from any of the two pre-defined configuration registers ISC1 and ISC2 (Intermediate Switch Configuration #1 and #2) located at page.006h and page.008h, respectively, by setting the hardware pin.**CONFIGSEL**.

Setting pin.**CONFIGSEL** to LOW will transfer the contents of the ISC1 to the ASC upon any hardware strobe event.

Similarly, setting pin.**CONFIGSEL** to HIGH will transfer the content of the ISC2 to the ASC upon any hardware strobe event.

4.4.3 Software Strobe Mode

The device is put in software strobe mode by programming register.**gen config**.bit[5:4] (page.000h, address.003h) to 10b.

The M21170 features four independent switch configuration software strobes in register.**strobe** at page.000h, address.04h (bit[1:0] for xSET0 map, bit[3:2] for xSET1 map, bit[5:4] for xSET2 map and bit[7:6] for xSET3 map). The software strobe signals may be used to synchronously trigger updating the active switch configuration register. The user may define the software strobe for each switching lane independently by programming the corresponding switching lane register at page.002h. Any or all switching lanes may be assigned to any or all of the strobe signals.

The active switching matrix configuration (ASC) may be loaded from any of the two pre-defined configuration registers ISC1 and ISC2 (Intermediate Switch Configuration #1 and #2) located at page.006h and page.008h, respectively, by programming register.**gen config**.bit[7].

Setting register.**gen config**.bit[7] to LOW will transfer the content of the ISC1 to the ASC upon any software strobe event.

Similarly, setting register.**gen config**.bit[7] to HIGH will transfer the content of the ISC2 to the ASC upon any software strobe event.

4.5 Junction Temperature Monitor

The M21170 features four embedded, integrated temperature sensors, one at each corner of the die. Each sensor has an effective range from approximately -45 °C to +130 °C, stepped in 10 °C increments. The sensors can be configured using register.**tempmon** (page.021h, address.000h). The temperature sensors are enabled after power-up or any hardware/software reset.

The readings for the temperature sensors located in the top-right and top-left corners of the die are available in register.**tempmont** (page.021h, address.001h). Similarly, the readings from temperature sensors in the bottom-right and bottom-left corners of the die are available in register.**tempmonb** (page.021h, address.002h). A user provided digital strobe is required to load the temperature values into the two registers. This is accomplished by issuing a rising edge on the strobe signal located at register.**tempmon**.bit[1] (page.021h, address.000h).

For increased accuracy of the readings, Mindspeed recommends calibrating the readings within the specific environment of the application. Please consult your local application resource for the methodology of calibration.

Sensor configuration allows for activating an alarm at pin.**xOVERTEMP** to indicate when the device temperature has exceeded a certain level as detected by any of the four temperature sensors. By default, the alarm is activated and set to active LOW. The alarm can be disabled and its polarity inverted (active HIGH) by programming register.**tempmon**.bit[7] and register.**tempmon**.bit[5] (page.021h, address.000h) respectively. The temperature threshold for asserting the alarm can be set to a value between 80 °C to 130 °C by programming register.**tempmon**.bit[4:2]. Note that the device can sustain permanent damage at a temperature of 130 °C, so setting the alarm to that threshold is not recommended.

To prevent overheating and possibly damaging the device, the temperature monitor can also be used to automatically power down the output drivers or the entire device. This feature is controlled through hardware pin.**DISTEMP**. When this pin is set to HIGH, the device will be powered down (put in standby) upon an over temperature alarm. When both pin.**DISTEMP** and register.**tempmon**.bit[6] (page.021h, address.000h) are set to LOW, all output drivers will be automatically powered down upon a temperature alarm.

4.6 Software Interfaces

The registers of the M21170 can be configured through three different control interfaces:

- A 2-wire serial interface operational at the standard data rates of 100 kHz, 400 kHz, and 3.4 MHz.
- A four-wire serial interface operational up to 100 MHz for register writes and up to 25 MHz for register reads.
- A parallel 9-bit address, 9-bit data interface operational up to 100 MHz for register writes and up to 15 MHz for register reads.

Both serial modes support sequential block writes within a page in burst mode. After the first register write, each additional byte of data is automatically written into the next consecutive register address. Burst mode allows all register pages including ISC#1 or ISC#2 pages to be programmed rapidly without the need to precede each data field with an address field.

In general, pin.**DV_{DDIO}** should share the same power supply as the host controller. The M21170 can support host controller voltages from 1.2 V to 3.3 V. The M21170 registers are defined to allow a select number of parameters to be configured individually or globally. With the global option, selection of a feature will apply to all lanes of the part. If the individual option is selected, then each lane or group can be configured individually. Global configuration is faster but individual configuration allows for more flexibility and customization.

Two hardware pins, pin.**CONFIG0** and pin.**CONFIG1**, allow the user to select the control interface and define the function of the multi-function pins pin.**MF[11:0]** and pin.**A[8:0]** as summarized in Table 4-1 below.

The interface selection is latched upon the power-on reset of the part, or after a hardware reset, and can not be changed during operation. This means that assertion of the software reset will not reset the interface selection. The physical logic level of the control interface (and all low-speed digital I/O pins in general) is determined by the supply voltage seen at pin.**DV_{DDIO}**.

In the following sections, the pins of the selected interface will be referred to by the assigned name in quotes. For example, pin.**MF0** for the 2-wire interface will be called “**SCL**”.

Table 4-1. Digital Mode Control

Control Pins	Multi-function Pin Name	Pin Location	Control Selected Interface				Termination/Type
			2-wire	4-wire	Parallel	JTAG	
CONFIG0		P37	0	1	0	X	Pull-down[1] / Input
CONFIG1		R37	0	0	1	X	Pull-down[1] / Input
TEN		N35	0	0	0	1	Pull-down[1] / Input
TEST1, TEST0		N36 N37	0 0	0 0	0 0	0 0	Pull-down[1] / Input Pull-down[1] / Input
	TCLK	AU14				TCLK	Pull-up[1] / Input
	MF11	V14			R_xW		High-Z / Input
	MF10	N13		xCS	xCS		High-Z / Input
	MF9	P15			D8		High-Z / I_O
	MF8	T14	addr6		D7		High-Z / I_O
	MF7	U14	addr5		D6		High-Z / I_O
	MF6	N18	addr4		D5		High-Z / I_O
	MF5	R17	addr3		D4		High-Z / I_O
	MF4	T15	addr2		D3		High-Z / I_O
	MF3	R14	addr1		D2		High-Z / I_O
	MF2	P17	addr0	SI	D1		High-Z / I_O
	MF1	R16	SDA	SO	D0		High-Z / I_O
	A8	N14			A8		High-Z / Input
	A7	V15			A7		High-Z / Input
	A6	V13			A6		High-Z / Input
	A5	N17			A5		High-Z / Input
	A4	U13			A4		High-Z / Input
	A3	U15			A3		High-Z / Input
	A2	N15			A2		High-Z / Input
	A1	P13			A1		High-Z / Input
	A0	P16			A0		High-Z / Input
	MF0	R15	SCL	SCLK	CLOCK		High-Z / Input

NOTES:

1. Pull-up / pull-down resistance is an internal 100 kΩ to DV_{DDIO} or V_{SS}

4.6.1 2-wire Serial Digital Interface

The 2-wire slave mode is selected with pin.**TEN**=L, pin.**TEST1**=L, pin.**TEST0**=L, pin.**CONFIG0**=L and pin.**CONFIG1**=L.

The M21170 is an I²C-compatible slave device that can operate at 100 kHz, 400 kHz, and 3.4 MHz for all allowed voltages seen at pin.**DV_{DDIO}**. The pins can drive 500 pF at 100 kHz and 400 kHz, also 40 pF at 3.4 MHz. Figure 4-11 illustrates typical waveforms and timing seen at "**SCL**" and "**SDA**" for a read and write operation. In write mode, the standard I²C interface protocol sends two bytes of data for address/data. The M21170 uses the first LSB of the first byte as bit 8 and ignores the other seven bits within the second byte. In read mode, the M21170 provides two bytes of data to the master host.

An example of a random write through the 2-wire interface is depicted below. Note that regardless of whether 9 or 8 bits of data are used, two bytes of data need to be provided for the write process to complete. Likewise, two bytes of data are provided in read mode.

Figure 4-11. 2-wire Bit Operations

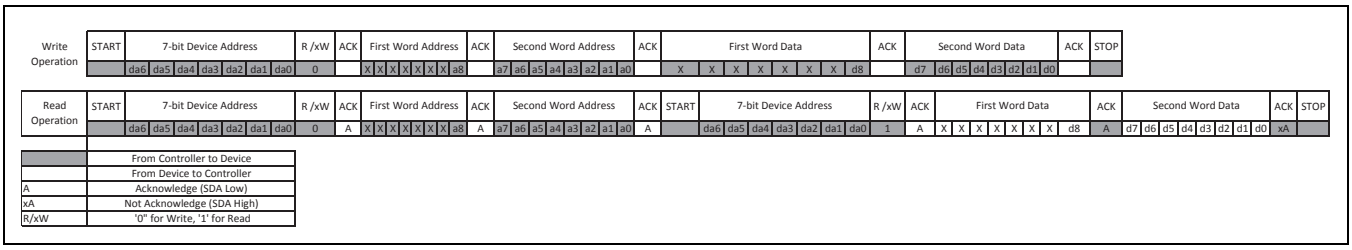


Figure 4-12. 2-wire Read and Write Operation Timing Diagram

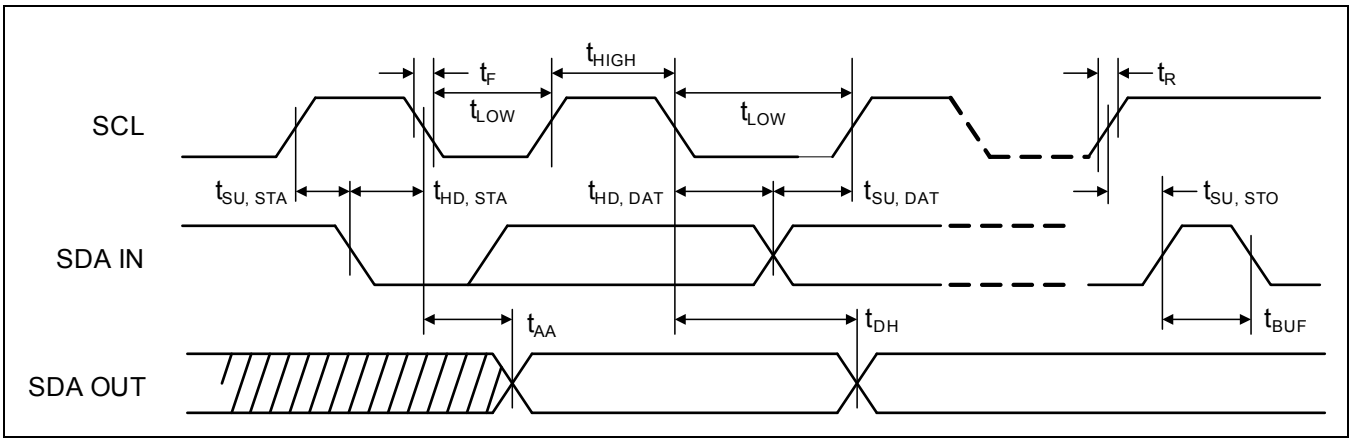


Table 4-2. Two-wire Slave Timing Specifications (Standard Mode / Fast Mode)

Symbol	Parameter	Min	Typ	Max	Units
f_{SCL}	Clock frequency, SCL	—	—	400	kHz
t_{LOW}	Clock pulse width low	1.3	—	—	µs
t_{HIGH}	Clock pulse width high	0.6	—	—	µs
t_{AA}	Clock low to data out valid	0.05	—	0.9	µs
$t_{HD, STA}$	Start hold time	200	—	—	ns
$t_{SU, STA}$	Start set-up time	200	—	—	ns
$t_{HD, DAT}$	Data in hold time	0	—	—	ns
$t_{SU, DAT}$	Data in set-up time	100	—	—	ns
$t_{SU, STO}$	Stop set-up time	200	—	—	ns
t_{DH}	Data out hold time	50	—	—	ns

Table 4-3. Two-wire Slave Timing Specifications (High Speed Mode)

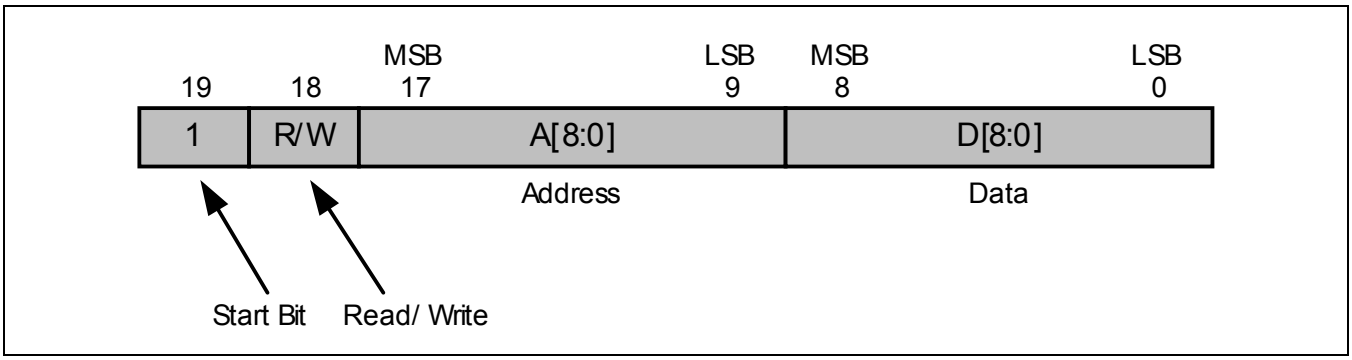
Symbol	Parameter	Min	Typ	Max	Units
f_{SCL}	Clock frequency, SCL	—	—	3.4*	MHz
t_{LOW}	Clock pulse width low	160	—	—	ns
t_{HIGH}	Clock pulse width high	60	—	—	ns
t_{AA}	Clock low to data out valid	0	—	70	ns
$t_{HD, STA}$	Start (repeated) hold time	160	—	—	ns
$t_{SU, STA}$	Start (repeated) set-up time	160	—	—	ns
$t_{HD, DAT}$	Data in hold time	0	—	—	ns
$t_{SU, DAT}$	Data in set-up time	10	—	—	ns
$t_{SU, STO}$	Stop set-up time	160	—	—	ns
t_{DH}	Data out hold time	5	—	—	ns
(*) Max capacitive load at SDA (pin.**MF1**) is 40 pF					

4.6.2 4-wire Serial Digital Interface

The 4-wire slave mode is selected with pin.**TEN**=L, pin.**TEST1**=L, pin.**TEST0**=L, pin.**CONFIG0**=H and pin.**CONFIG1**=L.

The interface shifts data in from the external controller on the rising edge of "**SCLK**". The serial I/O operation is gated by "**xCS**". Data is shifted to M21170 from the Host (Master) on "**SI**" on the falling edge of "**SCLK**", and shifted out through "**SO**" on the rising edge of "**SCLK**". To address a register, an 11-bit input needs to be shifted, consisting of the first bit (Start Bit, SB = 1), the second bit (Operation Bit, OP = 1 for read, = 0 for write), and the 9-bit address (MSB first).

Figure 4-13. 4-wire Serial Digital Interface



Instruction	Instruction Format	xCS at End of Current R/W Operation	Operation
R-Read	11	H	Random read
R-Write	10	H	Random write
S-Read	11	L	Sequence read
S-Write	10	L	Sequence write
Non-Operate	0X		Non-operate (SO remain tristate), reset to new operation after xCS transitioning HIGH to LOW

NOTES:

1. There are no different instructions for random R/W and sequential R/W. When slave select xCS is extended by n*(9 clock cycles), random R/W becomes sequential R/W (see the timing diagram below).
2. A minimum of one clock cycle pulse width is required for slave select xCS to deselect between read-write, write-read, read-read or write-write cycles.
3. At least one clock (SCLK) is required after slave select xCS is deasserted.
4. The sequential R/W continues to roll over the 512 byte addresses if the xCS is extended low (i.e. in sequential write, the page select at address 1FFh could be overwritten to extend to the next page address. It is up to the user to decide when to deselect xCS in the sequential write).
5. After POR, a minimum of three clock cycles is required to get the device "out of reset" before any read/write operation will work (i.e. a first dummy read after POR can be performed for this purpose).

Figure 4-14. 4-wire Sequential WRITE

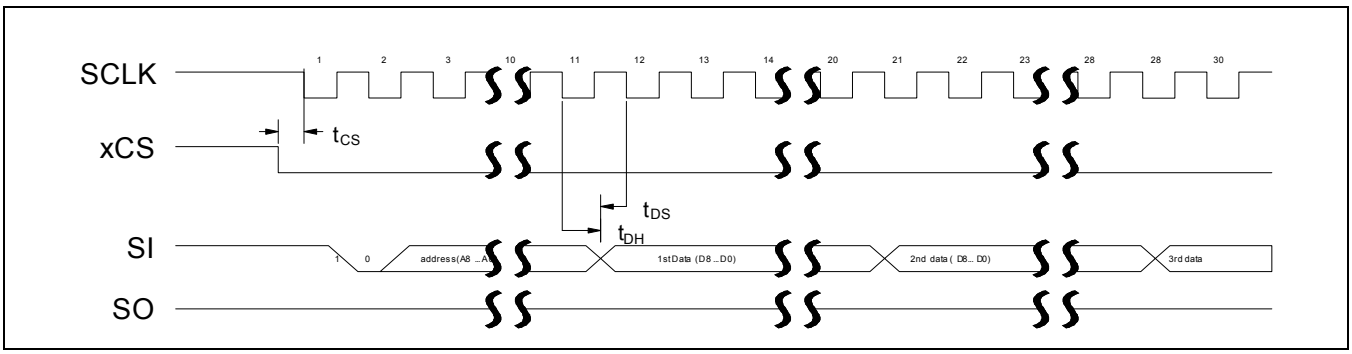


Figure 4-15. 4-wire Random WRITE

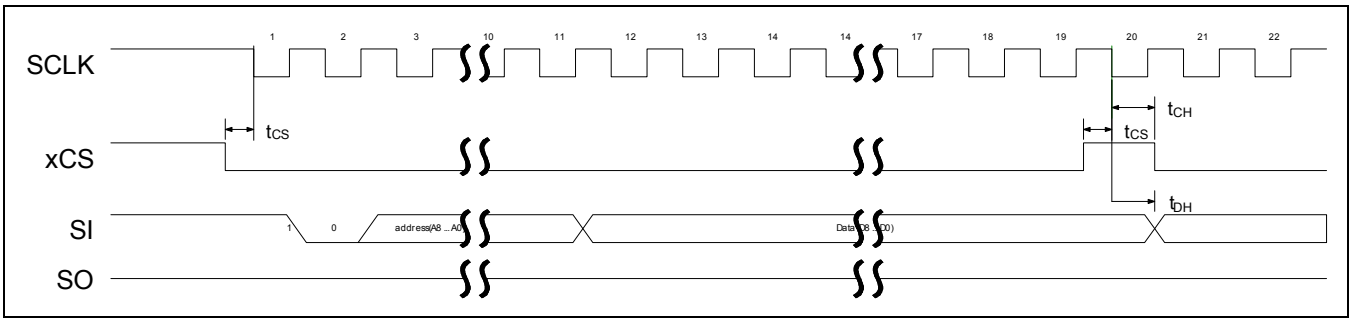


Figure 4-16. 4-wire Sequential READ

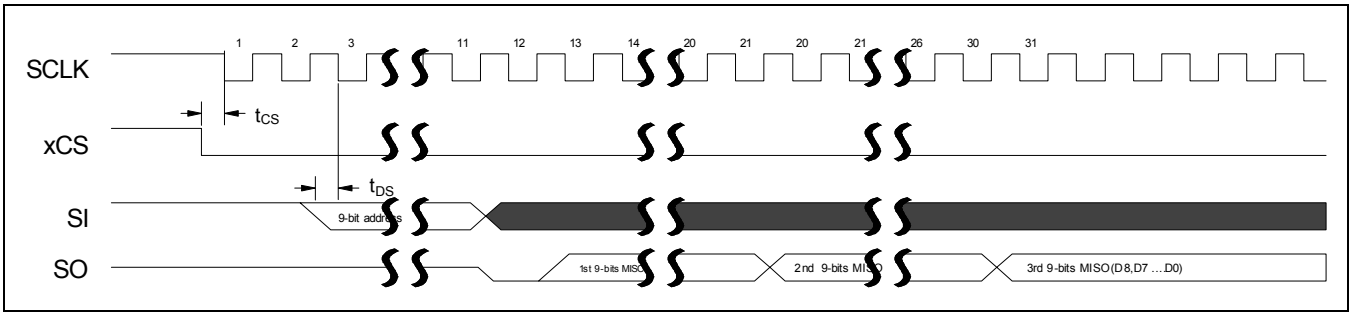


Figure 4-17. 4-wire Random READ

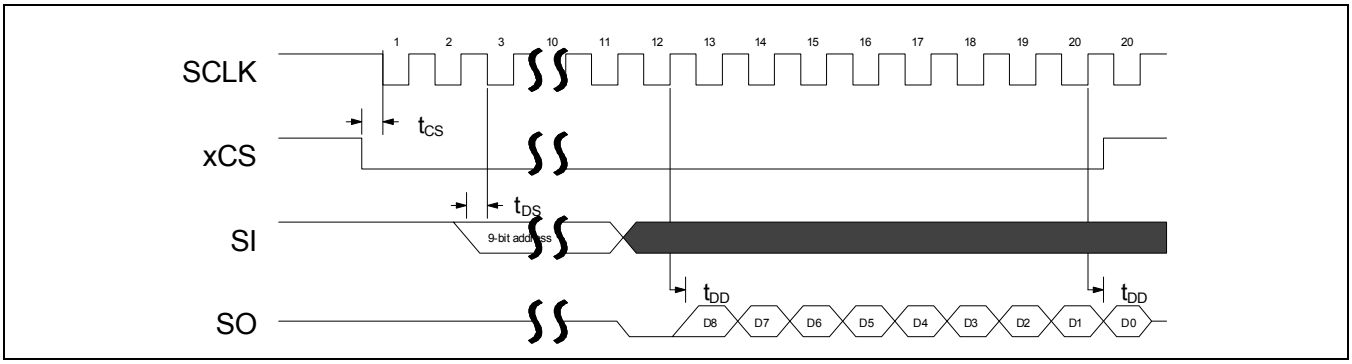


Table 4-4. 4-wire Timing Specification

Symbol	Description	Min	Typ	Max	Units
t_{DS}	Data set-up time	2.5			ns
t_{DH}	Data hold time	2.5			ns
t_{CS}	Enable xCS set-up time	2.5			ns
t_{CH}	xCS hold time	2.5			ns
t_{FREQ}	Write 4-wire clock frequency			100	MHz
	Read 4-wire clock frequency			25	MHz
t_{DCD}	SCLK pulse width	45		55	%
t_{DD}	Read data output delay following rising edge of SCLK	2		16	ns

4.6.3 Parallel Digital Interface

The 9-bit data and 9-bit address parallel interface is selected with pin.**TEN**=L, pin.**TEST1**=L, pin.**TEST0**=L, pin.**CONFIG0**=L and pin.**CONFIG1**=H.

The slave parallel interface has two different write modes of operations: single-write and multiple-write. It also has a single-read mode as seen in the following timing diagrams. Once a multiple write sequence is completed, a read sequence should be initiated only after a certain amount of time (the necessary wait time depends on the application and the read frequency and can vary from a few microseconds to a few 100 microseconds). After "**xCS**" (pin.**MF10**) transitioned from HIGH to LOW, in a single write, 9 input addresses and 9 input datas are sampled by the first rising edge of signal "**CLOCK**" (pin.**MF0**) and the "**xCS**" is deasserted. If the "**xCS**" is extended by n * CLOCK cycles, the interface enters its multiple-write mode (a multiple of 9 address and 9 data are sampled by each rising edge of the "**CLOCK**" signal).

After POR, minimum of three CLOCK cycles is required to get the device initialized after reset before any read or write operation to be valid (a first dummy read after POR can be performed for this purpose).

Figure 4-18. Parallel Single Write

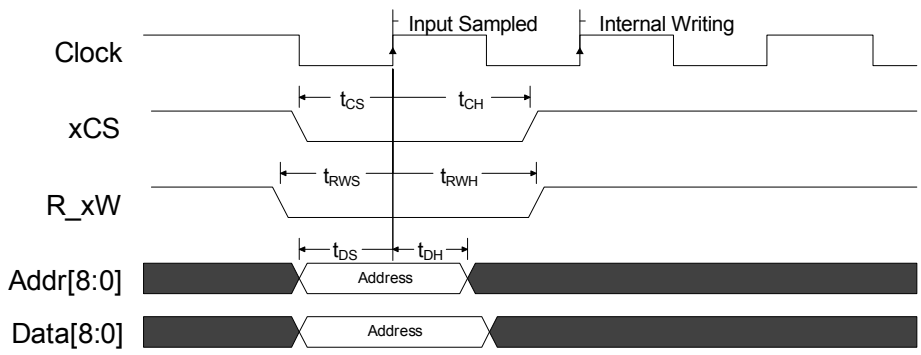


Figure 4-19. Parallel Multiple Write

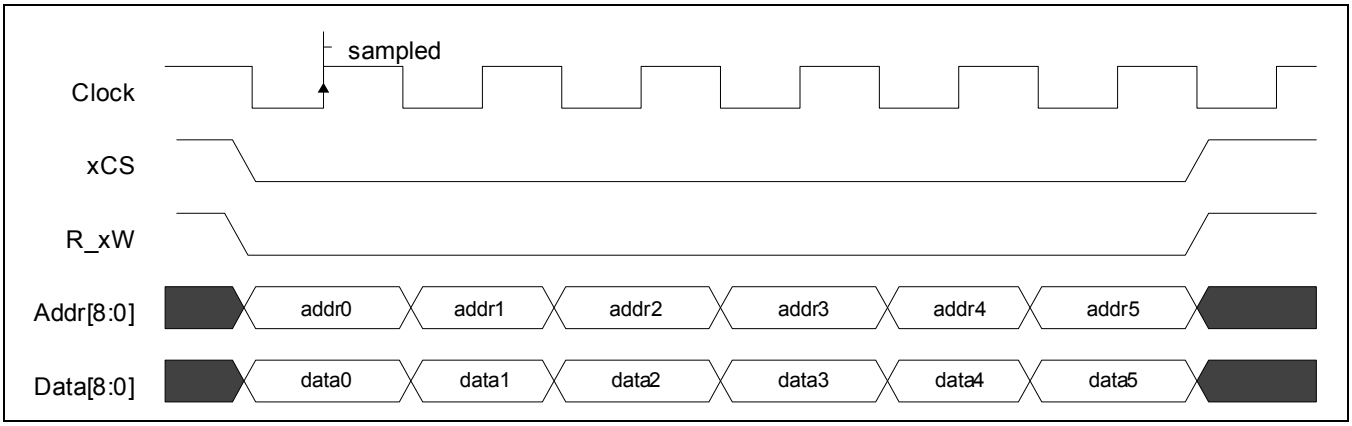


Figure 4-20. Parallel Single Read

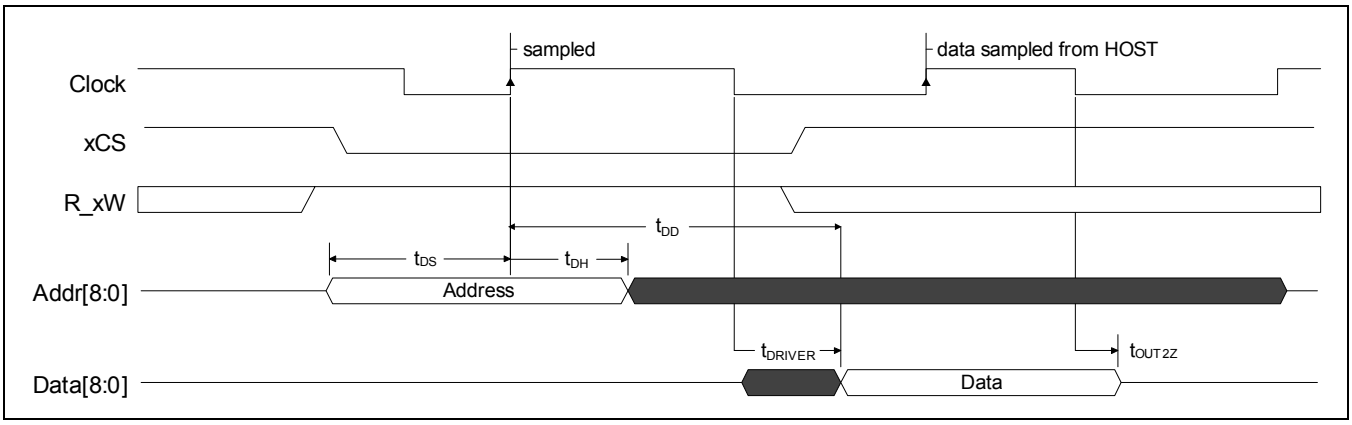


Figure 4-21. Parallel Interface Multiple Single Read Timing Configuration

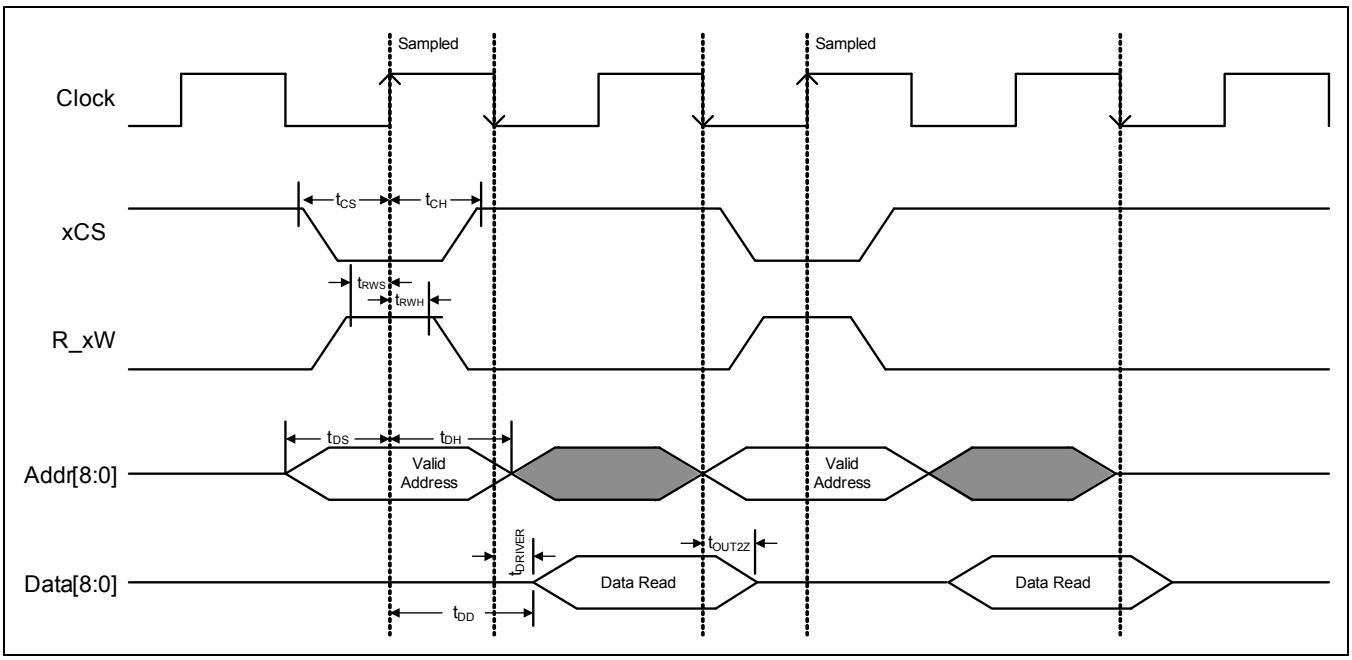


Figure 4-22. Parallel Interface Single Read, Single Write Timing Configuration

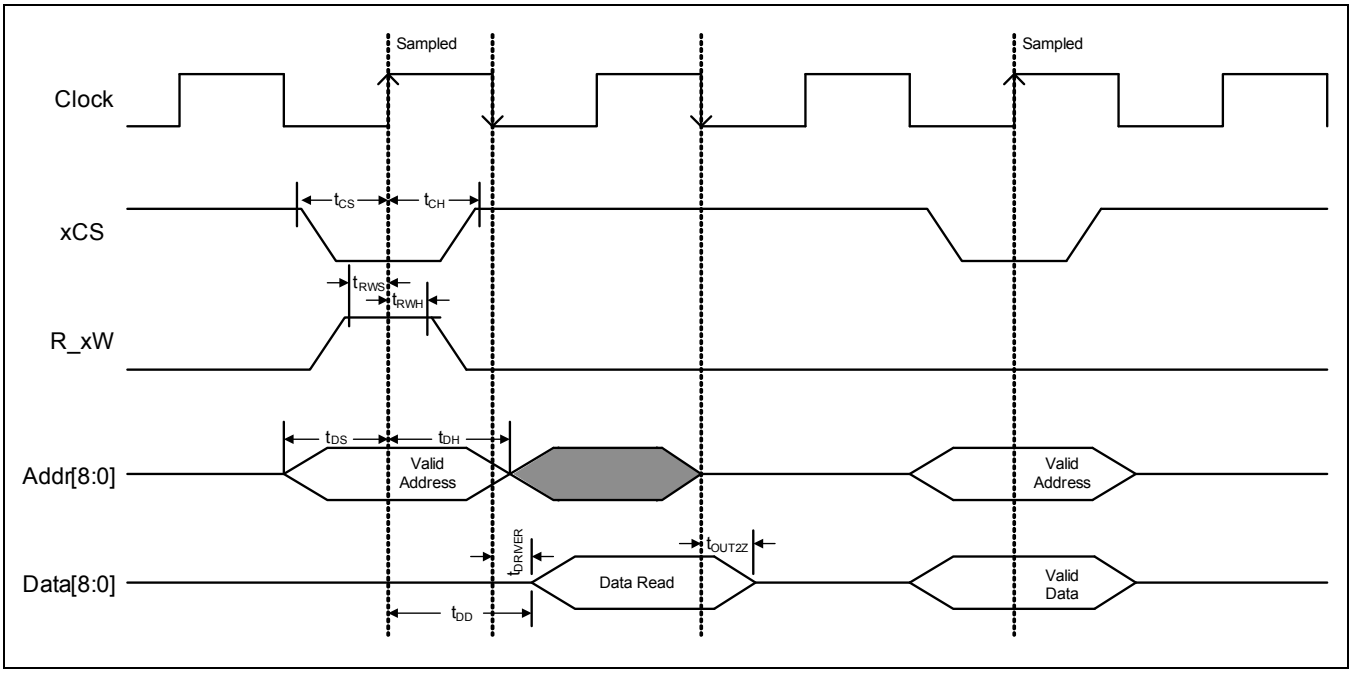


Table 4-5. Parallel Interface Specifications

Symbol	Description	Min	Typ	Max	Units
t_{DS}	Data/address set-up time	1.5			ns
t_{DH}	Data/address hold time	3.5			ns
t_{CS}	xCS set-up time	2			ns
t_{CH}	xCS hold time	3			ns
t_{RWS}	R_xW set up time	1.5			
t_{RWH}	R_xW hold time	3.5			
t_{FREQ}	Write clock frequency			100	MHz
	Read clock frequency			15	MHz
t_{DCD}	Clock pulse width	45		55	%
t_{DD}	Read data output delay following falling edge of CLOCK			60	ns
t_{OUT2Z}	Read data output to float following CLOCK falling edge	1		10	ns
t_{DRIVER}	Read data output driver enable	1			ns
t_{XD}	Output switching delay following falling edge of hardware xSET switching	10			ns
C_{LOAD}	Capacitive loading on the parallel output in READ mode DV_{DDIO} = 3.3 V DV_{DDIO} = 1.2 V			 30 10	 pF pF

4.7 Power Down and Standby Mode

The M21170 has individual, selective, power-up and power-down modes for any lane in the switch matrix (programming page.004h), any input (programming page.00Ah) and any output driver (programming page.00Eh) to assist in power management.

For instructions on how to power down the inputs and output lanes please see Section 4.2, “High-Speed Input Lanes”, and Section 4.3, “High-Speed Output Drivers”.

Disabling any individual lane in the core is achieved by writing a value of 1FFh in the corresponding lane register from the Active Switch Configuration (page.004h). Note that disabling any individual lane in the switch also automatically disables the corresponding output driver, unless register.**gboutbuf**.bit[1] (page.000h, address.006h) is set to HIGH.

The entire device may be put in standby mode by setting register.**gen config**.bit[0] (page.000h, address.003h) to HIGH. In this mode the analog sections including the switching matrix, auxiliary lanes, input and output sections will be disabled and powered-down. However, in this mode the software interfaces will still remain active, allowing the device to be configured in standby mode.

4.8 JTAG

The M21170 may be set to scan mode (supporting JTAG). This mode is enabled by setting pin.**TEN** to HIGH.

Typical JTAG operation can be performed using pin.**TDI**, pin.**TDO** and pin.**TMS**. The JTAG clock can be applied to pin.**TCLK**.

When JTAG mode is enabled, the M21170 automatically bypasses the software registers enabling all output drivers. It also overrides the hardware pin.**xINPUTEN** and pin.**xOUTPUTEN**.

The JTAG boundary scan includes all 288 inputs and outputs. The default for the Active Switch Configuration (ASC) register in JTAG mode is a 1-to-1 configuration.

For further information, please consult your local application resource.

5.0 Control Registers Map and Descriptions

Table 5-1. Register Summary

Page	Address	Register	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
Global Page Selection Register													
000h	1FFh	pagesel	*RSVD*	pagedef								000'h	R/W
Page 000h: Global Configuration													
000h	000h	master reset	*RSVD*	master reset								000'h	R/W
000h	001h	chip code	*RSVD*	chip code								00E'h	R
000h	002h	rev code	*RSVD*	revcode								001'h	R
000h	003h	gen config	*RSVD*	iscsel	*RSVD*	ascsel		*RSVD*			standby	018'h	R/W
000h	004h	strobe	*RSVD*	xset3		xstet2		xset1		xset0		000'h	R/W
000h	005h	gbinbuf	*RSVD*	ind	dis	term	aux	dcoff	eq		polflip	000'h	R/W
000h	006h	gboutbuf	*RSVD*	ind	swing		de		T_{CASE}	disdrv	*RSVD*	000'h	R/W
000h	007h	LOS config	*RSVD*	ind	threshold			sqstate	force	sq	*RSVD*	000'h	R/W
000h	008h	LOS mon	*RSVD*							ind	ored	000'h	R/W
000h	009h	monchansel	*RSVD*	lanesel								000'h	R/W
000h	040h-063h : 001h	LOS alarm(N)	*RSVD*	lane(8*N+7)	lane(8*N+6)	lane(8*N+5)	lane(8*N+4)	lane98*N+3)	lane(8*N+2)	lane(8*N+1)	lane(8*N+0)	000'h	R/W
000h	080h-0A3h : 001h	stat alarm(N)	*RSVD*	lane(8*N+7)	lane(8*N+6)	lane(8*N+5)	lane(8*N+4)	lane98*N+3)	lane(8*N+2)	lane(8*N+1)	lane(8*N+0)	na	R
000h	0C0h-0E3h : 001h	mask alarm(N)	*RSVD*	lane(8*N+7)	lane(8*N+6)	lane(8*N+5)	lane(8*N+4)	lane98*N+3)	lane(8*N+2)	lane(8*N+1)	lane(8*N+0)	000'h	R/W
Page 002h: Multiple Point Switch Configuration													
002h	000h-047h : 001h	xset_group(N)	*RSVD*	lane(4*N+3)		lane(4*N+2)		lane(4*N+1)		lane(4*N+0)		000'h	R/W
Page 004h: Crosspoint Active Switch Configuration (ASC)													
004h	000h-11Fh : 001h	ascout(N)	ascout									000'h	R/W
Page 006h: Crosspoint Intermediate Switch Configuration #1 (ISC1)													
006h	000h-11Fh : 001h	iscout1(N)	iscout1									HEX(N)	R/W
Page 008h: Crosspoint Intermediate Switch Configuration #2 (ISC2)													
008h	000h-11Fh : 001h	iscout2(N)	iscout2									000'h	R/W
Page 00Ah: Individual Input Buffer Configuration													
00Ah	000h-11Fh : 001h	inputbuf(N)	*RSVD*	dis	term	aux	dcoff	eq			polflip	000'h	R/W

Table 5-1. Register Summary

Page	Address	Register	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
Page 00Ch: Individual Input LOS Configuration													
00Ch	000h-11Fh : 001h	input LOS(N)	*RSVD*		threshold			sqstate	force	sq	*RSVD*	000'h	R/W
Page 00Eh: Individual Output Driver Configuration													
00Eh	000h-11Fh : 001h	outputbuf(N)	*RSVD*		enable		de		T_{CASE}	*RSVD*		000'h	R/W
Page 021h: Temperature Monitoring, Diagnostics and Auxiliary lanes Configuration													
021h	000h	tempmon	*RSVD*	dis	drven	alarmst	thresh			str	dis	041'h	R/W
021h	001h	tempmont	*RSVD*	tl				t_R				na	R
021h	002h	tempmonb	*RSVD*	bl				br				na	R
021h	008h	outmone	*RSVD*	lanesele								0FF'h	R/W
021h	009h	outmono	*RSVD*	laneselo								0FF'h	R/W
021h	00Ah	*Reserved*	*RSVD (set to default)*									0FF'h	R/W
021h	00Bh	*Reserved*	*RSVD (set to default)*									0FF'h	R/W
021h	00Ch	gbloshys	*RSVD*								dishys	000'h	R/W
021h	00Dh	*Reserved*	*RSVD (set to default)*									000'h	R/W
021h	00Eh	*Reserved*	*RSVD (set to default)*									000'h	R/W
021h	00Fh	*Reserved*	*RSVD (set to default)*									001'h	R/W
021h	01Fh	*Reserved*	*RSVD (set to default)*									000'h	R/W
021h	02Fh	auxoute	*RSVD*		enable		de		T_{CASE}	*RSVD*		000'h	R/W
021h	03Fh	auxouto	*RSVD*		enable		de		T_{CASE}	*RSVD*		000'h	R/W
021h	04Fh	*Reserved*	*RSVD (set to default)*									000'h	R/W
021h	080h	auxine	*RSVD*		dise	terme	ddcoffe	*RSVD*	eqe		polflipe	058'h	R/W
021h	081h	auxino	*RSVD*		diso	termo	ddcoffo	*RSVD*	eqo		polflipo	058'h	R/W
021h	082h	LOS auxe	*RSVD*		thresholde			sqstatee	forcee	sqe	loshyse	071'h	R/W
021h	083h	LOS auxo	*RSVD*		thresholdo			sqstateo	forceo	sqo	loshyso	071'h	R/W
021h	0CFh	LOS aux	*RSVD*							losauxe	losauxo	na	R
021h	0D0h	*Reserved*	*RSVD (set to default)*									na	R

5.1 Global Page Selection Register

Page: 000h
Address: 1FFh
Register Name: pagesel
Default Value: 000'h
Description: Determines the active register page selection. The 1FFh address is unique and references the same register, irrespective of page selection

Bit(s)	Name	Description	Default	Type
[8]	*RSVD*	*Reserved (set to default)*	0b	R/W
[7:0]	pagedef	0000 0000b: Global configuration 0000 0010b: Multiple point switch configuration 0000 0100b: Crosspoint active switch configuration (ASC) 0000 0110b: Crosspoint intermediate switch configuration #1 (ISC1) 0000 1000b: Crosspoint intermediate switch configuration #2 (ISC2) 0000 1010b: Individual input front-end configuration 0000 1100b: Individual input LOS configuration 0000 1110b: Individual output driver configuration 0010 0001b: Temperature monitoring, diagnostics and auxiliary lanes configuration	0000 0000b	R/W

5.2 Page 000h: Global Configuration

Page: 000h
Address: 000h
Register Name: master reset
Default Value: 000'h
Description: Generate a software reset. Reset all registers to default value

Bit(s)	Name	Description	Default	Type
[8]	*RSVD*	*Reserved (set to default)*		R/W
[7:0]	master reset	0000 0000b: Normal operation 1010 1010b: Assert global reset	0000 0000b	R/W

Page: 000h
Address: 001h
Register Name: chip code
Default Value: 00E'h
Description: Product identification code

Bit(s)	Name	Description	Default	Type
[8]	*RSVD*	*Reserved*		R
[7:0]	chip code	0000 1110b: M21170 identification code	0000 1110b	R

Page: 000h
Address: 002h
Register Name: rev code
Default Value: 001'h
Description: Product revision code

Bit(s)	Name	Description	Default	Type
[8]	*RSVD*	*Reserved*		R
[7:0]	revcode	0000 0001b: M21170-12	0000 0001b	R

Page: 000h
Address: 003h
Register Name: gen config
Default Value: 018'h
Description: General configuration register

Bit(s)	Name	Description	Default	Type
[8]	*RSVD*	*Reserved (set to default)*	0b	R/W
[7]	iscsel	0b: Select ISC1 as the active state to become ASC upon strobe 1b: Select ISC2 as the active state to become ASC upon strobe	0b	R/W
[6]	*RSVD*	*Reserved (set to default)*	0b	R/W
[5:4]	ascsel	00b: Direct ASC mode. Update switch configuration on each ASC register write 01b: Strobe ASC mode (hardware mode). Update switch configuration with pin.**xSET[3:0]** and choosing ISC via pin.**CONFIGSEL** 10b: Strobe ASC mode (software mode). Update switch configuration on write to register.**strobe**.bit[6:0], address.04h, page.00h 11b: Undefined	01b	R/W
[3:1]	*RSVD*	*Reserved (set to default)*	100b	R/W
[0]	standby	0b: Power up the device 1b: Power down and enter the device in standby mode	0b	R/W

Page: 000h
Address: 004h
Register Name: strobe
Default Value: 000'h
Description: Register strobe (synchronously change the switch state, enabled with register.**gen config**.bit[5]=1b)

Bit(s)	Name	Description	Default	Type
[8]	*RSVD*	*Reserved (set to default)*	0b	R/W
[7:6]	xset3	00b: Normal operation 01b: Undefined 10b: Select ISC1 (if register.**gen config**.bit[7]=0) or ISC#2 (if register.**gen config**.bit[7]=1) as the source state for the ASC upon strobe with pin.**xSET3** 11b: Undefined	00b	R/W
[5:4]	xstet2	00b: Normal operation 01b: Undefined 10b: Select ISC1 (if register.**gen config**.bit[7]=0) or ISC#2 (if register.**gen config**.bit[7]=1) as the source state for the ASC upon strobe with pin.**xSET2** 11b: Undefined	00b	R/W
[3:2]	xset1	00b: Normal operation 01b: Undefined 10b: Select ISC1 (if register.**gen config**.bit[7]=0) or ISC#2 (if register.**gen config**.bit[7]=1) as the source state for the ASC upon strobe with pin.**xSET1** 11b: Undefined	00b	R/W
[1:0]	xset0	00b: Normal operation 01b: Undefined 10b: Select ISC1 (if register.**gen config**.bit[7]=0) or ISC#2 (if register.**gen config**.bit[7]=1) as the source state for the ASC upon strobe with pin.**xSET1** 11b: Undefined	00b	R/W

Page: 000h
Address: 005h
Register Name: gbinbuf
Default Value: 000'h
Description: Input front-end configuration register

Bit(s)	Name	Description	Default	Type
[8]	*RSVD*	*Reserved (set to default)*	0b	R/W
[7]	ind	0b: Set all input buffer configurations globally according to bit [6:0] below 1b: Set individual input buffer configurations using register.**inbufctrl(N)**, address.hex(N), page.00Ah	0b	R/W
[6]	dis	0b: Enable the complete input buffer 1b: Disable and power-down the complete input buffer	0b	R/W
[5]	term	0b: Enable 50 Ω input termination 1b: Disable 50 Ω input termination	0b	R/W
[4]	aux	0b: Select regular high speed input lane 1b: Bypass regular high speed input lane and, - select auxiliary high speed lane at pin.**INP_AUXE** and pin.**INN_AUXE** to be sent to the even input lane - select auxiliary high speed lane at pin.**INP_AUXO** and pin.**INN_AUXO** to be sent to the odd input lane	0b	R/W
[3]	dcoff	0b: Enable DCS (dc-servo) offset control loop 1b: Disable DCS (dc-servo) offset control loop	0b	R/W
[2:1]	eq	00b: Minimum eq setting (~3 dB of boosting at Nyquist 1.26 GHz) 01b: Intermediate eq setting 1 (~6 dB of boosting at Nyquist 1.26 GHz) 10b: Intermediate eq setting 2 (~9 dB of boosting at Nyquist 1.26 GHz) 11b: Maximum eq setting (~12.5 dB of boosting at Nyquist 1.26 GHz)	00b	R/W
[0]	polflip	0b: Normal signal polarity 1b: Invert signal polarity	0b	R/W

NOTES:

If input termination is set to high-impedance (setting bit[5] = 1b) the eq setting must be kept at minimum eq setting (bit[2:1] = 00b) whenever AV_{DDI} is equal to 2.5 V.

Page: 000h
Address: 006h
Register Name: gboutbuf
Default Value: 000'h
Description: Output driver configuration register

Bit(s)	Name	Description	Default	Type
[8]	*RSVD*	*Reserved (set to default)*	0b	R/W
[7]	ind	0b: Set all output buffer configurations globally according to bit [6:0] below 1b: Set individual output buffer configurations using register.**outputbuf(N)**, address.hex(N), page.00Eh	0b	R/W
[6:5]	swing	00b: Disable and power down output driver 01b: 500 mV_{PPD} output swing 10b: 900 mV_{PPD} output swing 11b: 1200 mV_{PPD} output swing	00b	R/W
[4:3]	de	00b: Disable de-emphasis 01b: ~2 dB 10b: ~4 dB 11b: ~6 dB	00b	R/W
[2]	T_{CASE}	0b: Nominal time constant for de-emphasis 1b: 2x time constant for de-emphasis	0b	R/W
[1]	disdrv	0b: Disabling an individual core output lane (by writing 1FFh in the ASC, page.004h), also disable automatically the corresponding individual output driver 1b: Disabling an individual core output lane (by writing 1FFh in the ASC, page.004h), does not disable automatically the corresponding individual output driver. To further disable the corresponding individual output driver it is required to write 00h for the corresponding address at page.00Eh	0b	R/W
[0]	*RSVD*	*Reserved (set to default)*	0b	R/W

Page: 000h
Address: 007h
Register Name: LOS config
Default Value: 000'h
Description: LOS alarm configuration register

Bit(s)	Name	Description	Default	Type
[8]	*RSVD*	*Reserved (set to default)*	0b	R/W
[7]	ind	0b: Set LOS configurations globally according to bit [6:0] below 1b: Set individual individual LOS configurations using register.**input LOS(N)**, address.hex(N), page.00Ch	0b	R/W
[6:4]	threshold	000b: 100 mV_{PPD} threshold 001b: 130 mV_{PPD} threshold 010b: 120 mV_{PPD} threshold 011b: 110 mV_{PPD} threshold 100b: 90 mV_{PPD} threshold 101b: 80 mV_{PPD} threshold 110b: 70 mV_{PPD} threshold 111b: LOS power down	000b	R/W
[3]	sqstate	0b: Output '0' on squelch or LOS event 1b: Output '1' on squelch or LOS event	0b	R/W
[2]	force	0b: Do not force a LOS event 1b: Force a LOS event regardless of the input signal	0b	R/W
[1]	sq	0b: Squelch on LOS event, to level as defined at bit[3] 1b: Never squelch on LOS event	0b	R/W
[0]	*RSVD*	*Reserved (set to default)*	0b	R/W

Page: 000h
Address: 008h
Register Name: LOS mon
Default Value: 000'h
Description: LOS monitoring at pin.**xALARM** configuration register
[individual lane selection is done using register.**monchansel**, address.09h, page.00h and register.**LOS mon**, address.08h, page.00h]

Bit(s)	Name	Description	Default	Type
[8:2]	*RSVD*	*Reserved (set to default)*	000 0000b	R/W
[1]	ind	0b: Monitor individual LOS for even lane at pin.**xALARM** 1b: Monitor individual LOS for odd lane at pin.**xALARM**	0b	R/W
[0]	ored	0b: Monitor or'ed status of LOS alarm at pin.**xALARM** 1b: Monitor individual LOS alarm at pin.**xALARM**	0b	R/W

NOTES:
1. Individual lane selection is done using register.**monchansel,** address.09h, page.00h and register.**LOS mon**, address.08h, page.00h.

Page: 000h
Address: 009h
Register Name: monchansel
Default Value: 000'h
Description: Individual LOS monitoring at pin.**xALARM** selection register
[individual lane selection is done using register.**monchansel**, address.09h, page.00h and register.**LOS mon**, address.08h, page.00h]

Bit(s)	Name	Description	Default	Type
[8]	*RSVD*	*Reserved (set to default)*	0b	R/W
[7:0]	lanesel	0000 0000b: Monitor individual LOS for input lane 0 (register.**LOS mon**.bit[1]=0), lane 1 (register.**LOS mon**.bit[1]=1) 0000 0001b: Monitor individual LOS for input lane 2 (register.**LOS mon**.bit[1]=0), lane 3 (register.**LOS mon**.bit[1]=1) 0000 0010b: Monitor individual LOS for input lane 4 (register.**LOS mon**.bit[1]=0), lane 5 (register.**LOS mon**.bit[1]=1) 1000 1110b: Monitor individual LOS for input lane 284 (register.**LOS mon**.bit[1]=0), lane 285 (register.**LOS mon**.bit[1]=1) 1000 1111b: Monitor individual LOS for input lane 286 (register.**LOS mon**.bit[1]=0), lane 287 (register.**LOS mon**.bit[1]=1)	0000 0000b	R/W

NOTES:

1. Individual lane selection is done using register.**monchansel,** address.09h, page.00h and register.**LOS mon**, address.08h, page.00h.

Page: 000h

Address: HEX(64 + n*1) n=0...35
040h 041h 042h 043h 044h 045h 046h 047h 048h 049h 04Ah 04Bh 04Ch 04Dh 04Eh 04Fh 050h 051h 052h 053h 054h 055h 056h 057h 058h 059h 05Ah 05Bh 05Ch 05Dh 05Eh 05Fh 060h 061h 062h 063h

Register Name: LOS alarm(N)

Default Value: 000'h

Description: N=[0..35]
LOS alarm register for lane [8*N+7: 8*N+0]
[The register values are set upon LOS detection. Values are NOT automatically cleared when the LOS condition discontinues. Any set bit persists until reset by the appropriate user write or a global reset]
[Default values depends on the status seen at the LOS detector. These will be all "zero" assuming a regular signal is detected on all input lanes]

Bit(s)	Name	Description	Default	Type
[8]	*RSVD*	*Reserved (set to default)*	0b	R/W
[7]	lane(8*N+7)	Read 0b: No LOS detected Read 1b: LOS flag Write 1b = clear	0b	R/W
[6]	lane(8*N+6)	Read 0b: No LOS detected Read 1b: LOS flag Write 1b = clear	0b	R/W
[5]	lane(8*N+5)	Read 0b: No LOS detected Read 1b: LOS flag Write 1b = clear	0b	R/W
[4]	lane(8*N+4)	Read 0b: No LOS detected Read 1b: LOS flag Write 1b = clear	0b	R/W
[3]	lane98*N+3)	Read 0b: No LOS detected Read 1b: LOS flag Write 1b = clear	0b	R/W
[2]	lane(8*N+2)	Read 0b: No LOS detected Read 1b: LOS flag Write 1b = clear	0b	R/W
[1]	lane(8*N+1)	Read 0b: No LOS detected Read 1b: LOS flag Write 1b = clear	0b	R/W
[0]	lane(8*N+0)	Read 0b: No LOS detected Read 1b: LOS flag Write 1b = clear	0b	R/W

NOTES:

1. The register values are set upon LOS detection. Values are NOT automatically cleared when the LOS condition discontinues. Any set bit persists until reset by the appropriate user write or a global reset.
2. Default values depends on the status seen at the LOS detector. These will be all "zero" assuming a regular signal is detected on all input lanes.

Page: 000h

Address: HEX(128 + n*1) n=0...35
080h 081h 082h 083h 084h 085h 086h 087h 088h 089h 08Ah 08Bh 08Ch 08Dh 08Eh 08Fh 090h 091h 092h 093h 094h 095h 096h 097h 098h 099h 09Ah 09Bh 09Ch 09Dh 09Eh 09Fh 0A0h 0A1h 0A2h 0A3h

Register Name: stat alarm(N)

Default Value: na

Description: N=[0..35]
STAT alarm register for lane [8*N+7: 8*N+0]
[the register values are actively set and re-set upon any detected change in LOS status]

Bit(s)	Name	Description	Default	Type
[8]	*RSVD*	*Reserved*		R
[7]	lane(8*N+7)	0b: No LOS detected 1b: LOS flag		R
[6]	lane(8*N+6)	0b: No LOS detected 1b: LOS flag		R
[5]	lane(8*N+5)	0b: No LOS detected 1b: LOS flag		R
[4]	lane(8*N+4)	0b: No LOS detected 1b: LOS flag		R
[3]	lane98*N+3)	0b: No LOS detected 1b: LOS flag		R
[2]	lane(8*N+2)	0b: No LOS detected 1b: LOS flag		R
[1]	lane(8*N+1)	0b: No LOS detected 1b: LOS flag		R
[0]	lane(8*N+0)	0b: No LOS detected 1b: LOS flag		R

NOTES:

1. Default value is 000h if the LOS features get globally disabled prior the hardware/software reset.

The register values are actively set and re-set upon any detected change in LOS status.

Page: 000h

Address: HEX(192 + n*1) n=0...35
0C0h 0C1h 0C2h 0C3h 0C4h 0C5h 0C6h 0C7h 0C8h 0C9h 0CAh 0CBh 0CCh 0CDh 0CEh 0CFh 0D0h 0D1h 0D2h 0D3h 0D4h 0D5h 0D6h 0D7h 0D8h 0D9h 0DAh 0DBh 0DCh 0DDh 0DEh 0DFh 0E0h 0E1h 0E2h 0E3h

Register Name: mask alarm(N)

Default Value: 000'h

Description: N=[0..35]
MASK alarm register for lane [8*N+7: 8*N+0]
[the register masks the individual lanes that are wired' OR to the pin.**xALARM**. Any set bit persists until reset by the appropriate user or a global reset]

Bit(s)	Name	Description	Default	Type
[8]	*RSVD*	*Reserved (set to default)*	0b	R/W
[7]	lane(8*N+7)	0b: Include this lane 1b: Mask out this lane	0b	R/W
[6]	lane(8*N+6)	0b: Include this lane 1b: Mask out this lane	0b	R/W
[5]	lane(8*N+5)	0b: Include this lane 1b: Mask out this lane	0b	R/W
[4]	lane(8*N+4)	0b: Include this lane 1b: Mask out this lane	0b	R/W
[3]	lane98*N+3)	0b: Include this lane 1b: Mask out this lane	0b	R/W
[2]	lane(8*N+2)	0b: Include this lane 1b: Mask out this lane	0b	R/W
[1]	lane(8*N+1)	0b: Include this lane 1b: Mask out this lane	0b	R/W
[0]	lane(8*N+0)	0b: Include this lane 1b: Mask out this lane	0b	R/W

NOTES:

1. The register masks the individual lanes that are wired' OR to the pin.**xALARM**. Any set bit persists until reset by the appropriate user or a global reset.

5.3 Page 002h: Multiple Point Switch Configuration

Page: 002h

Address: HEX(0 + n*1) n=0...71
000h 001h 002h 003h 004h 005h 006h 007h 008h 009h 00Ah 00Bh 00Ch 00Dh 00Eh 00Fh 010h 011h 012h 013h 014h 015h 016h 017h 018h 019h 01Ah 01Bh 01Ch 01Dh 01Eh 01Fh 020h 021h 022h 023h 024h 025h 026h 027h 028h 029h 02Ah 02Bh 02Ch 02Dh 02Eh 02Fh 030h 031h 032h 033h 034h 035h 036h 037h 038h 039h 03Ah 03Bh 03Ch 03Dh 03Eh 03Fh 040h 041h 042h 043h 044h 045h 046h 047h

Register Name: xset_group(N)

Default Value: 000'h

Description: N=[0..71]
xSET output switch selection and control for lane N
[group(N) N=[0...71], is defined as a group of 4 lanes and mapping to the following definition,
group(0).ch{3.2.1.0} = lane{3.2.1.0}
group(1).ch{3.2.1.0} = lane{7.6.5.4}
…
group(70).ch{3.2.1.0} = lane{283.282.281.280}
group(71).ch{3.2.1.0} = lane{287.286,285.284}]

Bit(s)	Name	Description	Default	Type
[8]	*RSVD*	*Reserved (set to default)*	0b	R/W
[7:6]	lane(4*N+3)	00b: Use pin.**xSET0** (or register.**strobe**.bit[1:0], page.00h, when register.**gen config**.bit[5:4]=10b) to switch lane 3 from group(N) 01b: Use pin.**xSET1** (or register.**strobe**.bit[3:2], page.00h, when register.**gen config**.bit[5:4]=10b) to switch lane 3 from group(N) 10b: Use pin.**xSET2** (or register.**strobe**.bit[5:4], page.00h, when register.**genconfig**.bit[5:4]=10b) to switch lane 3 from group(N) 11b: Use pin.**xSET3** (or register.**strobe**.bit[7:6], page.00h, when register.**gen config**.bit[5:4]=10b) to switch lane 3 from group(N)	00b	R/W
[5:4]	lane(4*N+2)	00b: Use pin.**xSET0** (or register.**strobe**.bit[1:0], page.00h, when register.**gen config**.bit[5:4]=10b) to switch lane 2 from group(N) 01b: Use pin.**xSET1** (or register.**strobe**.bit[3:2], page.00h, when register.**gen config**.bit[5:4]=10b) to switch lane 2 from group(N) 10b: Use pin.**xSET2** (or register.**strobe**.bit[5:4], page.00h, when register.**genconfig**.bit[5:4]=10b) to switch lane 2 from group(N) 11b: Use pin.**xSET3** (or register.**strobe**.bit[7:6], page.00h, when register.**gen config**.bit[5:4]=10b) to switch lane 2 from group(N)	00b	R/W
[3:2]	lane(4*N+1)	00b: Use pin.**xSET0** (or register.**strobe**.bit[1:0], page.00h, when register.**gen config**.bit[5:4]=10b) to switch lane 1 from group(N) 01b: Use pin.**xSET1** (or register.**strobe**.bit[3:2], page.00h, when register.**gen config**.bit[5:4]=10b) to switch lane 1 from group(N) 10b: Use pin.**xSET2** (or register.**strobe**.bit[5:4], page.00h, when register.**genconfig**.bit[5:4]=10b) to switch lane 1 from group(N) 11b: Use pin.**xSET3** (or register.**strobe**.bit[7:6], page.00h, when register.**gen config**.bit[5:4]=10b) to switch lane 1 from group(N)	00b	R/W

Bit(s)	Name	Description	Default	Type
[1:0]	lane(4*N+0)	00b: Use pin.**xSET0** (or register.**strobe**.bit[1:0], page.00h, when register.**gen config**.bit[5:4]=10b) to switch lane 0 from group(N) 01b: Use pin.**xSET1** (or register.**strobe**.bit[3:2], page.00h, when register.**gen config**.bit[5:4]=10b) to switch lane 0 from group(N) 10b: Use pin.**xSET2** (or register.**strobe**.bit[5:4], page.00h, when register.**genconfig**.bit[5:4]=10b) to switch lane 0 from group(N) 11b: Use pin.**xSET3** (or register.**strobe**.bit[7:6], page.00h, when register.**gen config**.bit[5:4]=10b) to switch lane 0 from group(N)	00b	R/W

NOTES:

1.Group(N) N=[0...71], is defined as a group of 4 lanes and mapping to the following definition,.

Group(0).ch{3.2.1.0} = lane{3.2.1.0}.

Group(1).ch{3.2.1.0} = lane{7.6.5.4}.

….

Group(70).ch{3.2.1.0} = lane{283.282.281.280}.

Group(71).ch{3.2.1.0} = lane{287.286,285.284}.

5.4 Page 004h: Crosspoint Active Switch Configuration (ASC)

Page: 004h

Address: HEX(0 + n*1) n=0...287
000h 001h 002h 003h 004h 005h 006h 007h 008h 009h 00Ah 00Bh 00Ch 00Dh 00Eh 00Fh 010h 011h 012h 013h 014h 015h 016h 017h 018h 019h 01Ah 01Bh 01Ch 01Dh 01Eh 01Fh 020h 021h 022h 023h 024h 025h 026h 027h 028h 029h 02Ah 02Bh 02Ch 02Dh 02Eh 02Fh 030h 031h 032h 033h 034h 035h 036h 037h 038h 039h 03Ah 03Bh 03Ch 03Dh 03Eh 03Fh 040h 041h 042h 043h 044h 045h 046h 047h 048h 049h 04Ah 04Bh 04Ch 04Dh 04Eh 04Fh 050h 051h 052h 053h 054h 055h 056h 057h 058h 059h 05Ah 05Bh 05Ch 05Dh 05Eh 05Fh 060h 061h 062h 063h 064h 065h 066h 067h 068h 069h 06Ah 06Bh 06Ch 06Dh 06Eh 06Fh 070h 071h 072h 073h 074h 075h 076h 077h 078h 079h 07Ah 07Bh 07Ch 07Dh 07Eh 07Fh 080h 081h 082h 083h 084h 085h 086h 087h 088h 089h 08Ah 08Bh 08Ch 08Dh 08Eh 08Fh 090h 091h 092h 093h 094h 095h 096h 097h 098h 099h 09Ah 09Bh 09Ch 09Dh 09Eh 09Fh 0A0h 0A1h 0A2h 0A3h 0A4h 0A5h 0A6h 0A7h 0A8h 0A9h 0AAh 0ABh 0ACh 0ADh 0AEh 0AFh 0B0h 0B1h 0B2h 0B3h 0B4h 0B5h 0B6h 0B7h 0B8h 0B9h 0BAh 0BBh 0BCh 0BDh 0BEh 0BFh 0C0h 0C1h 0C2h 0C3h 0C4h 0C5h 0C6h 0C7h 0C8h 0C9h 0CAh 0CBh 0CCh 0CDh 0CEh 0CFh 0D0h 0D1h 0D2h 0D3h 0D4h 0D5h 0D6h 0D7h 0D8h 0D9h 0DAh 0DBh 0DCh 0DDh 0DEh 0DFh 0E0h 0E1h 0E2h 0E3h 0E4h 0E5h 0E6h 0E7h 0E8h 0E9h 0EAh 0EBh 0ECh 0EDh 0EEh 0EFh 0F0h 0F1h 0F2h 0F3h 0F4h 0F5h 0F6h 0F7h 0F8h 0F9h 0FAh 0FBh 0FCh 0FDh 0FEh 0FFh 100h 101h 102h 103h 104h 105h 106h 107h 108h 109h 10Ah 10Bh 10Ch 10Dh 10Eh 10Fh 110h 111h 112h 113h 114h 115h 116h 117h 118h 119h 11Ah 11Bh 11Ch 11Dh 11Eh 11Fh

Register Name: ascout(N)

Default Value: 000'h

Description: N=[0..287]
Active Switch Configuration (ASC) state for output lane N
[writing to this register may cause the switch state to change immediately in an asynchronous manner. Behavior is dependant on the content of register.**gen config**.bit[5:4], address.03h, page.00h]

Bit(s)	Name	Description	Default	Type
[8:0]	ascout	0 0000 0000b: Route input lane 0 to output lane N 0 0000 0001b: Route input lane 1 to output lane N 1 0001 1111b: Route input lane 287 to output lane N 1 1111 1111b: Disable core output lane N and output driver N, if register.**gboutbuf**.bit[1]=0b, address.06h, page.00h Only disable core output lane N, if register.**gboutbuf**.bit[1]=1b, address.06h, page.00h	0 0000 0000b	R/W

NOTES:

1. Writing to this register may cause the switch state to change immediately in an asynchronous manner. Behaviour is dependant on the content of register.**gen config**.bit[5:4], address.03h, page.00h.

5.5 Page 006h: Crosspoint Intermediate Switch Configuration #1 (ISC1)

Page: 006h

Address: HEX(0 + n*1) n=0...287
000h 001h 002h 003h 004h 005h 006h 007h 008h 009h 00Ah 00Bh 00Ch 00Dh 00Eh 00Fh 010h 011h 012h 013h 014h 015h 016h 017h 018h 019h 01Ah 01Bh 01Ch 01Dh 01Eh 01Fh 020h 021h 022h 023h 024h 025h 026h 027h 028h 029h 02Ah 02Bh 02Ch 02Dh 02Eh 02Fh 030h 031h 032h 033h 034h 035h 036h 037h 038h 039h 03Ah 03Bh 03Ch 03Dh 03Eh 03Fh 040h 041h 042h 043h 044h 045h 046h 047h 048h 049h 04Ah 04Bh 04Ch 04Dh 04Eh 04Fh 050h 051h 052h 053h 054h 055h 056h 057h 058h 059h 05Ah 05Bh 05Ch 05Dh 05Eh 05Fh 060h 061h 062h 063h 064h 065h 066h 067h 068h 069h 06Ah 06Bh 06Ch 06Dh 06Eh 06Fh 070h 071h 072h 073h 074h 075h 076h 077h 078h 079h 07Ah 07Bh 07Ch 07Dh 07Eh 07Fh 080h 081h 082h 083h 084h 085h 086h 087h 088h 089h 08Ah 08Bh 08Ch 08Dh 08Eh 08Fh 090h 091h 092h 093h 094h 095h 096h 097h 098h 099h 09Ah 09Bh 09Ch 09Dh 09Eh 09Fh 0A0h 0A1h 0A2h 0A3h 0A4h 0A5h 0A6h 0A7h 0A8h 0A9h 0AAh 0ABh 0ACh 0ADh 0AEh 0AFh 0B0h 0B1h 0B2h 0B3h 0B4h 0B5h 0B6h 0B7h 0B8h 0B9h 0BAh 0BBh 0BCh 0BDh 0BEh 0BFh 0C0h 0C1h 0C2h 0C3h 0C4h 0C5h 0C6h 0C7h 0C8h 0C9h 0CAh 0CBh 0CCh 0CDh 0CEh 0CFh 0D0h 0D1h 0D2h 0D3h 0D4h 0D5h 0D6h 0D7h 0D8h 0D9h 0DAh 0DBh 0DCh 0DDh 0DEh 0DFh 0E0h 0E1h 0E2h 0E3h 0E4h 0E5h 0E6h 0E7h 0E8h 0E9h 0EAh 0EBh 0ECh 0EDh 0EEh 0EFh 0F0h 0F1h 0F2h 0F3h 0F4h 0F5h 0F6h 0F7h 0F8h 0F9h 0FAh 0FBh 0FCh 0FDh 0FEh 0FFh 100h 101h 102h 103h 104h 105h 106h 107h 108h 109h 10Ah 10Bh 10Ch 10Dh 10Eh 10Fh 110h 111h 112h 113h 114h 115h 116h 117h 118h 119h 11Ah 11Bh 11Ch 11Dh 11Eh 11Fh

Register Name: iscout1(N)

Default Value: HEX(N)

Description: N=[0..287]
Intermediate Switch Configuration #1 (ISC1) state for output lane N

Bit(s)	Name	Description	Default	Type
[8:0]	iscout1	0 0000 0000b: Route input lane 0 to output lane N 0 0000 0001b: Route input lane 1 to output lane N 1 0001 1111b: Route input lane 287 to output lane N 1 1111 1111b: Disable core output lane N and output driver N, if register.**gboutbuf**.bit[1]=0b, address.06h, page.00h Only disable core output lane N, if register.**gboutbuf**.bit[1]=1b, address.06h, page.00h		R/W

5.6 Page 008h: Crosspoint Intermediate Switch Configuration #2 (ISC2)

Page: 008h

Address: HEX(0 + n*1) n=0...287
000h 001h 002h 003h 004h 005h 006h 007h 008h 009h 00Ah 00Bh 00Ch 00Dh 00Eh 00Fh 010h 011h 012h 013h 014h 015h 016h 017h 018h 019h 01Ah 01Bh 01Ch 01Dh 01Eh 01Fh 020h 021h 022h 023h 024h 025h 026h 027h 028h 029h 02Ah 02Bh 02Ch 02Dh 02Eh 02Fh 030h 031h 032h 033h 034h 035h 036h 037h 038h 039h 03Ah 03Bh 03Ch 03Dh 03Eh 03Fh 040h 041h 042h 043h 044h 045h 046h 047h 048h 049h 04Ah 04Bh 04Ch 04Dh 04Eh 04Fh 050h 051h 052h 053h 054h 055h 056h 057h 058h 059h 05Ah 05Bh 05Ch 05Dh 05Eh 05Fh 060h 061h 062h 063h 064h 065h 066h 067h 068h 069h 06Ah 06Bh 06Ch 06Dh 06Eh 06Fh 070h 071h 072h 073h 074h 075h 076h 077h 078h 079h 07Ah 07Bh 07Ch 07Dh 07Eh 07Fh 080h 081h 082h 083h 084h 085h 086h 087h 088h 089h 08Ah 08Bh 08Ch 08Dh 08Eh 08Fh 090h 091h 092h 093h 094h 095h 096h 097h 098h 099h 09Ah 09Bh 09Ch 09Dh 09Eh 09Fh 0A0h 0A1h 0A2h 0A3h 0A4h 0A5h 0A6h 0A7h 0A8h 0A9h 0AAh 0ABh 0ACh 0ADh 0AEh 0AFh 0B0h 0B1h 0B2h 0B3h 0B4h 0B5h 0B6h 0B7h 0B8h 0B9h 0BAh 0BBh 0BCh 0BDh 0BEh 0BFh 0C0h 0C1h 0C2h 0C3h 0C4h 0C5h 0C6h 0C7h 0C8h 0C9h 0CAh 0CBh 0CCh 0CDh 0CEh 0CFh 0D0h 0D1h 0D2h 0D3h 0D4h 0D5h 0D6h 0D7h 0D8h 0D9h 0DAh 0DBh 0DCh 0DDh 0DEh 0DFh 0E0h 0E1h 0E2h 0E3h 0E4h 0E5h 0E6h 0E7h 0E8h 0E9h 0EAh 0EBh 0ECh 0EDh 0EEh 0EFh 0F0h 0F1h 0F2h 0F3h 0F4h 0F5h 0F6h 0F7h 0F8h 0F9h 0FAh 0FBh 0FCh 0FDh 0FEh 0FFh 100h 101h 102h 103h 104h 105h 106h 107h 108h 109h 10Ah 10Bh 10Ch 10Dh 10Eh 10Fh 110h 111h 112h 113h 114h 115h 116h 117h 118h 119h 11Ah 11Bh 11Ch 11Dh 11Eh 11Fh

Register Name: iscout2(N)

Default Value: 000'h

Description: N=[0..287]
Intermediate Switch Configuration #2 (ISC2) state for output lane N

Bit(s)	Name	Description	Default	Type
[8:0]	iscout2	0 0000 0000b: Route input lane 0 to output lane N 0 0000 0001b: Route input lane 1 to output lane N 1 0001 1111b: Route input lane 287 to output lane N 1 1111 1111b: Disable core output lane N and output driver N, if register.**gboutbuf**.bit[1]=0b, address.06h, page.00h Only disable core output lane N, if register.**gboutbuf**.bit[1]=1b, address.06h, page.00h	0 0000 0000b	R/W

5.7 Page 00Ah: Individual Input Buffer Configuration

Page: 00Ah

Address: HEX(0 + n*1) n=0...287
000h 001h 002h 003h 004h 005h 006h 007h 008h 009h 00Ah 00Bh 00Ch 00Dh 00Eh 00Fh 010h 011h 012h 013h 014h 015h 016h 017h 018h 019h 01Ah 01Bh 01Ch 01Dh 01Eh 01Fh 020h 021h 022h 023h 024h 025h 026h 027h 028h 029h 02Ah 02Bh 02Ch 02Dh 02Eh 02Fh 030h 031h 032h 033h 034h 035h 036h 037h 038h 039h 03Ah 03Bh 03Ch 03Dh 03Eh 03Fh 040h 041h 042h 043h 044h 045h 046h 047h 048h 049h 04Ah 04Bh 04Ch 04Dh 04Eh 04Fh 050h 051h 052h 053h 054h 055h 056h 057h 058h 059h 05Ah 05Bh 05Ch 05Dh 05Eh 05Fh 060h 061h 062h 063h 064h 065h 066h 067h 068h 069h 06Ah 06Bh 06Ch 06Dh 06Eh 06Fh 070h 071h 072h 073h 074h 075h 076h 077h 078h 079h 07Ah 07Bh 07Ch 07Dh 07Eh 07Fh 080h 081h 082h 083h 084h 085h 086h 087h 088h 089h 08Ah 08Bh 08Ch 08Dh 08Eh 08Fh 090h 091h 092h 093h 094h 095h 096h 097h 098h 099h 09Ah 09Bh 09Ch 09Dh 09Eh 09Fh 0A0h 0A1h 0A2h 0A3h 0A4h 0A5h 0A6h 0A7h 0A8h 0A9h 0AAh 0ABh 0ACh 0ADh 0AEh 0AFh 0B0h 0B1h 0B2h 0B3h 0B4h 0B5h 0B6h 0B7h 0B8h 0B9h 0BAh 0BBh 0BCh 0BDh 0BEh 0BFh 0C0h 0C1h 0C2h 0C3h 0C4h 0C5h 0C6h 0C7h 0C8h 0C9h 0CAh 0CBh 0CCh 0CDh 0CEh 0CFh 0D0h 0D1h 0D2h 0D3h 0D4h 0D5h 0D6h 0D7h 0D8h 0D9h 0DAh 0DBh 0DCh 0DDh 0DEh 0DFh 0E0h 0E1h 0E2h 0E3h 0E4h 0E5h 0E6h 0E7h 0E8h 0E9h 0EAh 0EBh 0ECh 0EDh 0EEh 0EFh 0F0h 0F1h 0F2h 0F3h 0F4h 0F5h 0F6h 0F7h 0F8h 0F9h 0FAh 0FBh 0FCh 0FDh 0FEh 0FFh 100h 101h 102h 103h 104h 105h 106h 107h 108h 109h 10Ah 10Bh 10Ch 10Dh 10Eh 10Fh 110h 111h 112h 113h 114h 115h 116h 117h 118h 119h 11Ah 11Bh 11Ch 11Dh 11Eh 11Fh

Register Name: inputbuf(N)

Default Value: 000'h

Description: N=[0..287]
Individual input front-end configuration lane N

Bit(s)	Name	Description	Default	Type
[8:7]	*RSVD*	*Reserved (set to default)*	00b	R/W
[6]	dis	0b: Enable the complete input buffer 1b: Disable and power-down the complete input buffer	0b	R/W
[5]	term	0b: Enable 50 Ω input termination 1b: Disable 50 Ω input termination	0b	R/W
[4]	aux	0b: Select regular high speed input lane 1b: Bypass regular high speed input lane and, - select auxiliary high speed lane at pin.**INP_AUXE** and pin.**INN_AUXE** to be sent to the even input lane - select auxiliary high speed lane at pin.**INP_AUXO** and pin.**INN_AUXO** to be sent to the odd input lane	0b	R/W
[3]	dcoff	0b: Enable DC-servo offset control loop 1b: Disable DC-servo offset control loop	0b	R/W
[2:1]	eq	00b: Minimum eq setting (~3 dB of boosting at Nyquist 1.26 GHz) 01b: Intermediate eq setting 1 (~6 dB of boosting at Nyquist 1.26 GHz) 10b: Intermediate eq setting 2 (~9 dB of boosting at Nyquist 1.26 GHz) 11b: Maximum eq setting (~12.5 dB of boosting at Nyquist 1.26 GHz)	00b	R/W
[0]	polflip	0b: Normal signal polarity 1b: Invert signal polarity	0b	R/W

NOTES:
If input termination is set to high-impedance (setting bit[5] = 1b) the eq setting must be kept at minimum eq setting (bit[2:1] = 00b) whenever AV_{DDI} is equal to 2.5 V.

5.8 Page 00Ch: Individual Input LOS Configuration

Page: 00Ch

Address: HEX(0 + n*1) n=0...287
000h 001h 002h 003h 004h 005h 006h 007h 008h 009h 00Ah 00Bh 00Ch 00Dh 00Eh 00Fh 010h 011h 012h 013h 014h 015h 016h 017h 018h 019h 01Ah 01Bh 01Ch 01Dh 01Eh 01Fh 020h 021h 022h 023h 024h 025h 026h 027h 028h 029h 02Ah 02Bh 02Ch 02Dh 02Eh 02Fh 030h 031h 032h 033h 034h 035h 036h 037h 038h 039h 03Ah 03Bh 03Ch 03Dh 03Eh 03Fh 040h 041h 042h 043h 044h 045h 046h 047h 048h 049h 04Ah 04Bh 04Ch 04Dh 04Eh 04Fh 050h 051h 052h 053h 054h 055h 056h 057h 058h 059h 05Ah 05Bh 05Ch 05Dh 05Eh 05Fh 060h 061h 062h 063h 064h 065h 066h 067h 068h 069h 06Ah 06Bh 06Ch 06Dh 06Eh 06Fh 070h 071h 072h 073h 074h 075h 076h 077h 078h 079h 07Ah 07Bh 07Ch 07Dh 07Eh 07Fh 080h 081h 082h 083h 084h 085h 086h 087h 088h 089h 08Ah 08Bh 08Ch 08Dh 08Eh 08Fh 090h 091h 092h 093h 094h 095h 096h 097h 098h 099h 09Ah 09Bh 09Ch 09Dh 09Eh 09Fh 0A0h 0A1h 0A2h 0A3h 0A4h 0A5h 0A6h 0A7h 0A8h 0A9h 0AAh 0ABh 0ACh 0ADh 0AEh 0AFh 0B0h 0B1h 0B2h 0B3h 0B4h 0B5h 0B6h 0B7h 0B8h 0B9h 0BAh 0BBh 0BCh 0BDh 0BEh 0BFh 0C0h 0C1h 0C2h 0C3h 0C4h 0C5h 0C6h 0C7h 0C8h 0C9h 0CAh 0CBh 0CCh 0CDh 0CEh 0CFh 0D0h 0D1h 0D2h 0D3h 0D4h 0D5h 0D6h 0D7h 0D8h 0D9h 0DAh 0DBh 0DCh 0DDh 0DEh 0DFh 0E0h 0E1h 0E2h 0E3h 0E4h 0E5h 0E6h 0E7h 0E8h 0E9h 0EAh 0EBh 0ECh 0EDh 0EEh 0EFh 0F0h 0F1h 0F2h 0F3h 0F4h 0F5h 0F6h 0F7h 0F8h 0F9h 0FAh 0FBh 0FCh 0FDh 0FEh 0FFh 100h 101h 102h 103h 104h 105h 106h 107h 108h 109h 10Ah 10Bh 10Ch 10Dh 10Eh 10Fh 110h 111h 112h 113h 114h 115h 116h 117h 118h 119h 11Ah 11Bh 11Ch 11Dh 11Eh 11Fh

Register Name: input LOS(N)

Default Value: 000'h

Description: N=[0..287]
Individual input LOS control at lane N

Bit(s)	Name	Description	Default	Type
[8:7]	*RSVD*	*Reserved (set to default)*	00b	R/W
[6:4]	threshold	000b: 100 mV_{PPD} threshold 001b: 130 mV_{PPD} threshold 010b: 120 mV_{PPD} threshold 011b: 110 mV_{PPD} threshold 100b: 90 mV_{PPD} threshold 101b: 80 mV_{PPD} threshold 110b: 70 mV_{PPD} threshold 111b: LOS power down	000b	R/W
[3]	sqstate	0b: Output '0' on squelch or LOS event 1b: Output '1' on squelch or LOS event	0b	R/W
[2]	force	0b: Do not force a LOS event 1b: Force a LOS event regardless of the input signal	0b	R/W
[1]	sq	0b: Squelch on LOS event, to level as defined at bit[3] 1b: Never squelch on LOS event	0b	R/W
[0]	*RSVD*	*Reserved (set to default)*		R/W

5.9 Page 00Eh: Individual Output Driver Configuration

Page: 00Eh

Address: HEX(0 + n*1) n=0...287
000h 001h 002h 003h 004h 005h 006h 007h 008h 009h 00Ah 00Bh 00Ch 00Dh 00Eh 00Fh 010h 011h 012h 013h 014h 015h 016h 017h 018h 019h 01Ah 01Bh 01Ch 01Dh 01Eh 01Fh 020h 021h 022h 023h 024h 025h 026h 027h 028h 029h 02Ah 02Bh 02Ch 02Dh 02Eh 02Fh 030h 031h 032h 033h 034h 035h 036h 037h 038h 039h 03Ah 03Bh 03Ch 03Dh 03Eh 03Fh 040h 041h 042h 043h 044h 045h 046h 047h 048h 049h 04Ah 04Bh 04Ch 04Dh 04Eh 04Fh 050h 051h 052h 053h 054h 055h 056h 057h 058h 059h 05Ah 05Bh 05Ch 05Dh 05Eh 05Fh 060h 061h 062h 063h 064h 065h 066h 067h 068h 069h 06Ah 06Bh 06Ch 06Dh 06Eh 06Fh 070h 071h 072h 073h 074h 075h 076h 077h 078h 079h 07Ah 07Bh 07Ch 07Dh 07Eh 07Fh 080h 081h 082h 083h 084h 085h 086h 087h 088h 089h 08Ah 08Bh 08Ch 08Dh 08Eh 08Fh 090h 091h 092h 093h 094h 095h 096h 097h 098h 099h 09Ah 09Bh 09Ch 09Dh 09Eh 09Fh 0A0h 0A1h 0A2h 0A3h 0A4h 0A5h 0A6h 0A7h 0A8h 0A9h 0AAh 0ABh 0ACh 0ADh 0AEh 0AFh 0B0h 0B1h 0B2h 0B3h 0B4h 0B5h 0B6h 0B7h 0B8h 0B9h 0BAh 0BBh 0BCh 0BDh 0BEh 0BFh 0C0h 0C1h 0C2h 0C3h 0C4h 0C5h 0C6h 0C7h 0C8h 0C9h 0CAh 0CBh 0CCh 0CDh 0CEh 0CFh 0D0h 0D1h 0D2h 0D3h 0D4h 0D5h 0D6h 0D7h 0D8h 0D9h 0DAh 0DBh 0DCh 0DDh 0DEh 0DFh 0E0h 0E1h 0E2h 0E3h 0E4h 0E5h 0E6h 0E7h 0E8h 0E9h 0EAh 0EBh 0ECh 0EDh 0EEh 0EFh 0F0h 0F1h 0F2h 0F3h 0F4h 0F5h 0F6h 0F7h 0F8h 0F9h 0FAh 0FBh 0FCh 0FDh 0FEh 0FFh 100h 101h 102h 103h 104h 105h 106h 107h 108h 109h 10Ah 10Bh 10Ch 10Dh 10Eh 10Fh 110h 111h 112h 113h 114h 115h 116h 117h 118h 119h 11Ah 11Bh 11Ch 11Dh 11Eh 11Fh

Register Name: outputbuf(N)

Default Value: 000'h

Description: N=[0..287]
Individual output driver control N

Bit(s)	Name	Description	Default	Type
[8:7]	*RSVD*	*Reserved (set to default)*	00b	R/W
[6:5]	enable	00b: Disable and power down output driver 01b: 500 mV_{PPD} output swing 10b: 900 mV_{PPD} output swing 11b: 1200 mV_{PPD} output swing	00b	R/W
[4:3]	de	00b: Disable de-emphasis 01b: Enable ~2 dB of output de-emphasis 10b: Enable ~4 dB of output de-emphasis 11b: Enable ~6 dB of output de-emphasis	00b	R/W
[2]	T_{CASE}	0b: Nominal time constant for de-emphasis 1b: 2x time constant for de-emphasis	0b	R/W
[1:0]	*RSVD*	*Reserved (set to default)*	00b	R/W

5.10 Page 021h: Temperature Monitoring, Diagnostics and Auxiliary lanes Configuration

Page: 021h
Address: 000h
Register Name: tempmon
Default Value: 041'h
Description: Control for the four on-die temperature monitors
[temperature thresholds for asserting pin.**xOVERTEMP** alarm are approximate and are not guaranteed (1-sigma value = ~1.6 °C)]

Bit(s)	Name	Description	Default	Type
[8]	*RSVD*	*Reserved (set to default)*	0b	R/W
[7]	dis	0b: Pin.**xOVERTEMP** alarm active 1b: Pin.**xOVERTEMP** alarm disabled	0b	R/W
[6]	drven	0b: Disable output drivers on over temperature alarm 1b: Do not disable output drivers on over temperature alarm	1b	R/W
[5]	alarmst	0b: Pin.**xOVERTEMP** alarm is set to low whenever T_{JUNC} exceeds the threshold as defined at bit[4:2] 1b: Pin.**xOVERTEMP** alarm is set to high whenever T_{JUNC} exceeds the threshold as defined at bit[4:2]	0b	R/W
[4:2]	thresh	000b: Select mean alarm threshold T_{JUNC} = 130 °C 001b: Select mean alarm threshold T_{JUNC} = 120 °C 010b: Select mean alarm threshold T_{JUNC} = 110 °C 011b: Select mean alarm threshold T_{JUNC} = 100 °C 100b: Select mean alarm threshold T_{JUNC} = 90 °C 101b: Select mean alarm threshold T_{JUNC} = 80 °C	000b	R/W
[1]	str	0b: Hold last read temperature values at register.tempmont and register.**tempmonb** 1b: On rising edge of this bit, strobe and load the temperature values into register.**tempmont** and register.**tempmonb**	0b	R/W
[0]	dis	0b: Disable temperature monitor 1b: Enable temperature monitor	1b	R/W

NOTES:

1. Temperature thresholds for asserting pin.**xOVERTEMP** alarm. These thresholds values are approximate and are not guaranteed (1-sigma value = ~1.6 °C).

Page: 021h
Address: 001h
Register Name: tempmont
Default Value: na
Description: Die top left and right temperature monitor readings
[temperature values are approximate, and are not guaranteed]

Bit(s)	Name	Description	Default	Type
[8]	*RSVD*	*Reserved*		R
[7:4]	tl	0000b: T_{JUNC} < -45 °C 0001b: Range T_{JUNC} [-40 : -30] °C 0010b: Range T_{JUNC} [-30 : -20] °C 0011b: Range T_{JUNC} [-20 : -10] °C 0100b: Range T_{JUNC} [-10 : 0] °C 0101b: Range T_{JUNC} [0 : 10] °C 0110b: Range T_{JUNC} [10 : 80] °C 0111b: Range T_{JUNC} [80 : 90] °C 1000b: Range T_{JUNC} [90 : 100] °C 1001b: Range T_{JUNC} [100 : 110] °C 1010b: Range T_{JUNC} [110 : 120] °C 1011b: Range T_{JUNC} [120 : 130] °C 1100b: T_{JUNC} > 130 °C		R
[3:0]	t_R	0000b: T_{JUNC} < -45 °C 0001b: Range T_{JUNC} [-40 : -30] °C 0010b: Range T_{JUNC} [-30 : -20] °C 0011b: Range T_{JUNC} [-20 : -10] °C 0100b: Range T_{JUNC} [-10 : 0] °C 0101b: Range T_{JUNC} [0 : 10] °C 0110b: Range T_{JUNC} [10 : 80] °C 0111b: Range T_{JUNC} [80 : 90] °C 1000b: Range T_{JUNC} [90 : 100] °C 1001b: Range T_{JUNC} [100 : 110] °C 1010b: Range T_{JUNC} [110 : 120] °C 1011b: Range T_{JUNC} [120 : 130] °C 1100b: T_{JUNC} > 130 °C		R

NOTES:

1. Temperature values are approximate, and are not guaranteed.

Page: 021h
Address: 002h
Register Name: tempmonb
Default Value: na
Description: Die bottom left and right temperature monitor readings
[temperature values are approximate, and are not guaranteed]

Bit(s)	Name	Description	Default	Type
[8]	*RSVD*	*Reserved*		R
[7:4]	bl	0000b: T_{JUNC} < -45 °C 0001b: Range T_{JUNC} [-40 : -30] °C 0010b: Range T_{JUNC} [-30 : -20] °C 0011b: Range T_{JUNC} [-20 : -10] °C 0100b: Range T_{JUNC} [-10 : 0] °C 0101b: Range T_{JUNC} [0 : 10] °C 0110b: Range T_{JUNC} [10 : 80] °C 0111b: Range T_{JUNC} [80 : 90] °C 1000b: Range T_{JUNC} [90 : 100] °C 1001b: Range T_{JUNC} [100 : 110] °C 1010b: Range T_{JUNC} [110 : 120] °C 1011b: Range T_{JUNC} [120 : 130] °C 1100b: T_{JUNC} > 130 °C		R
[3:0]	br	0000b: T_{JUNC} < -45 °C 0001b: Range T_{JUNC} [-40 : -30] °C 0010b: Range T_{JUNC} [-30 : -20] °C 0011b: Range T_{JUNC} [-20 : -10] °C 0100b: Range T_{JUNC} [-10 : 0] °C 0101b: Range T_{JUNC} [0 : 10] °C 0110b: Range T_{JUNC} [10 : 80] °C 0111b: Range T_{JUNC} [80 : 90] °C 1000b: Range T_{JUNC} [90 : 100] °C 1001b: Range T_{JUNC} [100 : 110] °C 1010b: Range T_{JUNC} [110 : 120] °C 1011b: Range T_{JUNC} [120 : 130] °C 1100b: T_{JUNC} > 130 °C		R

NOTES:

1. Temperature values are approximate, and are not guaranteed.

Page: 021h
Address: 008h
Register Name: outmone
Default Value: 0FF'h
Description: Even output lane monitoring at pin.**OUTP_AUXE** and pin.**OUTN_AUXE**

Bit(s)	Name	Description	Default	Type
[8]	*RSVD*	*Reserved (set to default)*	0b	R/W
[7:0]	lanesele	0000 0000b: Monitor lane0 0000 0001b: Monitor lane2 0000 0010b: Monitor lane4 … 1000 1101b: Monitor lane282 1000 1110b: Monitor lane284 1000 1111b: Monitor lane286 1111 1111b: Disable even output lane monitoring	1111 1111b	R/W

Page: 021h
Address: 009h
Register Name: outmono
Default Value: 0FF'h
Description: Odd output lane monitoring at pin.**OUTP_AUXO** and pin.**OUTN_AUXO**

Bit(s)	Name	Description	Default	Type
[8]	*RSVD*	*Reserved (set to default)*	0b	R/W
[7:0]	laneselo	0000 0000b: Monitor lane1 0000 0001b: Monitor lane3 0000 0010b: Monitor lane5 ….. 1000 1101b: Monitor lane283 1000 1110b: Monitor lane285 1000 1111b: Monitor lane287 1111 1111b: Disable odd output lane monitoring	1111 1111b	R/W

Page: 021h
Address: 00Ch
Register Name: gbloshys
Default Value: 000'h
Description: Global LOS hysteresis setting

Bit(s)	Name	Description	Default	Type
[8:1]	*RSVD*	*Reserved (set to default)*	0000 0000b	R/W
[0]	dishys	0b: Enable globally LOS hysteresis 1b: Disable globally LOS hysteresis	0b	R/W

NOTES:
Mindspeed recommends enabling the hysteresis feature whenever the LOS is being used. Whenever bit[0] is set low, the hysteresis is enabled globally for all 288 input channels.

Page: 021h
Address: 02Fh
Register Name: auxoute
Default Value: 000'h
Description: Auxiliary even output test

Bit(s)	Name	Description	Default	Type
[8:7]	*RSVD*	*Reserved (set to default)*	00b	R/W
[6:5]	enable	00b: Disable and power down output driver 01b: 500 mV_{PPD} output swing 10b: 900 mV_{PPD} output swing 11b: 1200 mV_{PPD} output swing	00b	R/W
[4:3]	de	00b: Disable de-emphasis 01b: Enable ~2 dB of output de-emphasis 10b: Enable ~4 dB of output de-emphasis 11b: Enable ~6 dB of output de-emphasis	00b	R/W
[2]	T_{CASE}	0b: Nominal time constant for de-emphasis 1b: 2x time constant for de-emphasis	0b	R/W
[1:0]	*RSVD*	*Reserved (set to default)*	00b	R/W

Page: 021h
Address: 03Fh
Register Name: auxouto
Default Value: 000'h
Description: Auxiliary odd output test

Bit(s)	Name	Description	Default	Type
[8:7]	*RSVD*	*Reserved (set to default)*	00b	R/W
[6:5]	enable	00b: Disable and power down output driver 01b: 500 mV_{PPD} output swing 10b: 900 mV_{PPD} output swing 11b: 1200 mV_{PPD} output swing	00b	R/W
[4:3]	de	00b: Disable de-emphasis 01b: Enable ~2 dB of output de-emphasis 10b: Enable ~4 dB of output de-emphasis 11b: Enable ~6 dB of output de-emphasis	00b	R/W
[2]	T_{CASE}	0b: Nominal time constant for de-emphasis 1b: 2x time constant for de-emphasis	0b	R/W
[1:0]	*RSVD*	*Reserved (set to default)*	00b	R/W

Page: 021h
Address: 080h
Register Name: auxine
Default Value: 058'h
Description: Auxiliary even input test

Bit(s)	Name	Description	Default	Type
[8:7]	*RSVD*	*Reserved (set to default)*	00b	R/W
[6]	dise	0b: Enable the complete input buffer 1b: Disable and power-down the complete input buffer	1b	R/W
[5]	terme	0b: Enable 50 Ω input termination at pin.**INP_AUXE** and pin.**INN_AUXE** 1b: Disable 50 Ω input termination at pin.**INP_AUXE** and pin.**INN_AUXE**	0b	R/W
[4]	ddcoffe	0b: Enable DCS (dc-servo) offset control loop with digital engine 1b: Disable DCS (dc-servo) offset control loop with digital engine	1b	R/W
[3]	*RSVD*	*Reserved (set to default)*	1b	R/W
[2:1]	eqe	00b: Minimum eq setting (~3 dB of boosting at Nyquist 1.26 GHz) 01b: Intermediate eq setting 1 (~6 dB of boosting at Nyquist 1.26 GHz) 10b: Intermediate eq setting 2 (~9 dB of boosting at Nyquist 1.26 GHz) 11b: Maximum eq setting (~12.5 dB of boosting at Nyquist 1.26 GHz)	00b	R/W
[0]	polflipe	0b: Normal signal polarity 1b: Invert signal polarity	0b	R/W

NOTES:

If input termination is set to high-impedance (setting bit[5] = 1b) the eq setting must be kept at minimum eq setting (bit[2:1] = 00b) whenever AV_{DDI} is equal to 2.5 V.

Page: 021h
Address: 081h
Register Name: auxino
Default Value: 058'h
Description: Auxiliary odd input test

Bit(s)	Name	Description	Default	Type
[8:7]	*RSVD*	*Reserved (set to default)*	00b	R/W
[6]	diso	0b: Enable the complete input buffer 1b: Disable and power-down the complete input buffer	1b	R/W
[5]	termo	0b: Enable 50 Ω input termination at pin.**INP_AUXE** and pin.**INN_AUXE** 1b: Disable 50 Ω input termination at pin.**INP_AUXE** and pin.**INN_AUXE**	0b	R/W
[4]	ddcoffo	0b: Enable DCS (dc-servo) offset control loop with digital engine 1b: Disable DCS (dc-servo) offset control loop with digital engine	1b	R/W
[3]	*RSVD*	*Reserved (set to default)*	1b	R/W
[2:1]	eqo	00b: Minimum eq setting (~3 dB of boosting at Nyquist 1.26 GHz) 01b: Intermediate eq setting 1 (~6 dB of boosting at Nyquist 1.26 GHz) 10b: Intermediate eq setting 2 (~9 dB of boosting at Nyquist 1.26 GHz) 11b: Maximum eq setting (~12.5 dB of boosting at Nyquist 1.26 GHz)	00b	R/W
[0]	polflipo	0b: Normal signal polarity 1b: Invert signal polarity	0b	R/W

NOTES:

If input termination is set to high-impedance (setting bit[5] = 1b) the eq setting must be kept at minimum eq setting (bit[2:1] = 00b) whenever AV_{DDI} is equal to 2.5 V.

Page: 021h
Address: 082h
Register Name: LOS auxe
Default Value: 071'h
Description: Auxiliary even LOS configuration

Bit(s)	Name	Description	Default	Type
[8:7]	*RSVD*	*Reserved (set to default)*	00b	R/W
[6:4]	thresholde	000b: 70 mV_{PPD} threshold 001b: 80 mV_{PPD} threshold 010b: 90 mV_{PPD} threshold 011b: 100 mV_{PPD} threshold 100b: 110 mV_{PPD} threshold 101b: 120 mV_{PPD} threshold 110b: 130 mV_{PPD} threshold 111b: LOS power down	111b	R/W
[3]	sqstatee	0b: Output '0' on squelch or LOS event 1b: Output '1' on squelch or LOS event	0b	R/W
[2]	forcee	0b: Do not force a LOS event 1b: Force a LOS event regardless of the input signal	0b	R/W
[1]	sqe	0b: Squelch on LOS event, to level as defined at bit[3] 1b: Never squelch on LOS event	0b	R/W
[0]	loshyse	0b: Enable LOS hysteresis 1b: Disable LOS hysteresis	1b	R/W

Page: 021h
Address: 083h
Register Name: LOS auxo
Default Value: 071'h
Description: Auxiliary odd LOS configuration

Bit(s)	Name	Description	Default	Type
[8:7]	*RSVD*	*Reserved (set to default)*	00b	R/W
[6:4]	thresholdo	000b: 70 mV_{PPD} threshold 001b: 80 mV_{PPD} threshold 010b: 90 mV_{PPD} threshold 011b: 100 mV_{PPD} threshold 100b: 110 mV_{PPD} threshold 101b: 120 mV_{PPD} threshold 110b: 130 mV_{PPD} threshold 111b: LOS power down	111b	R/W
[3]	sqstateo	0b: Output '0' on squelch or LOS event 1b: Output '1' on squelch or LOS event	0b	R/W
[2]	forceo	0b: Do not force a LOS event 1b: Force a LOS event regardless of the input signal	0b	R/W
[1]	sqo	0b: Squelch on LOS event, to level as defined at bit[3] 1b: Never squelch on LOS event	0b	R/W
[0]	loshyso	0b: Enable LOS hysteresis 1b: Disable LOS hysteresis	1b	R/W

Page: 021h
Address: 0CFh
Register Name: LOS aux
Default Value: na
Description: Auxiliary odd and even LOS check

Bit(s)	Name	Description	Default	Type
[8:2]	*RSVD*	*Reserved (set to default)*	b	R
[1]	losauxe	0b: Reading '0' indicated the even auxiliary input channel did not generate any LOS event 1b: Reading '1' indicated the even auxiliary input channel had a LOS event		R
[0]	losauxo	0b: Reading '0' indicated the odd auxiliary input channel did not generate any LOS event 1b: Reading '1' indicated the odd auxiliary input channel had a LOS event		R

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