M21350-15/M21355-15

3G/HD/SD-SDI Multi-rate Video Quad Reclocker

Rev V6

Applications

- 3G/HD/SD-SDI Video Switchers
- 3G/HD/SD-SDI Video Routers
- 3G/HD/SD-SDI Video Distribution Amplifiers
- DVB-ASI Equipment

Features

- Independent, quad channel, multi-rate reclocker
- SMPTE 259M-C, 292, 424M, and DVB ASI Compliant
- Greater than 0.6 UI Input Jitter Tolerance
- Integrated 50 Ω input termination
- 16x4 Input Crosspoint (M21355)
- Quad 4:1 Mux (M21350)
- Common reference clock for all channels
- Input equalization and output de-emphasis for 40" of FR4 trace
- 135 mW power consumption per channel (1.2 V operation)
- Integrated regulators for multi-voltage operation (1.2 V - 3.3 V)
- Electrically independent input, output, and core supply rails
- Recovered serial clock output option
- Output enable/disable and configurable auto or manual bypass mode
- Automatic and manual modes for rate indication and selection
- Loss of Lock (LOL), Loss of Signal (LOS) and data rate indication
- Two-wire and four-wire serial control interfaces
- Industrial operating temperature range (-40 °C to +85 °C)

The M21350 and M21355 are quad serial digital video reclockers with integrated trace equalization, and automatic rate detect (ARD) circuitry. The M21350 has a 4:1 mux on the input of each reclocker channel whereas the M21355 has a common 16x4 crosspoint switch at the input to all four channels. It operates at SDI data rates ranging from 270 Mbps to 2970 Mbps and is compliant to SMPTE 424M, SMPTE292, and SMPTE 259M-C. At 270 Mbps, it also supports DVB-ASI.

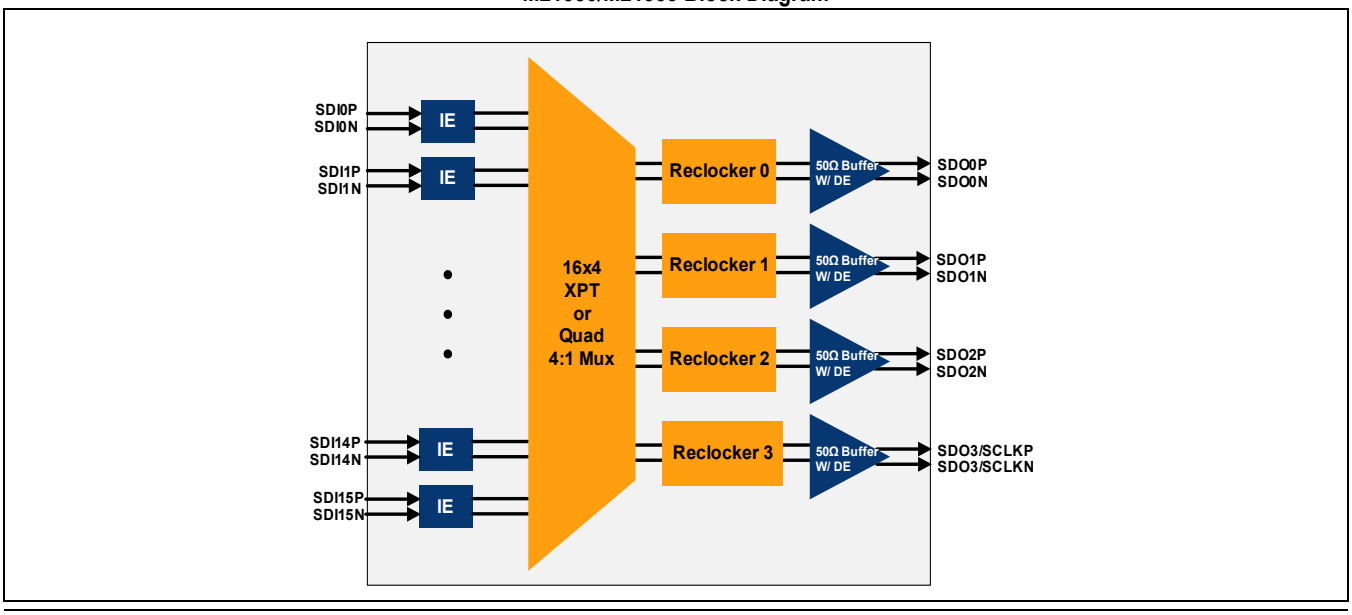
The M21350 and M21355 have an input jitter tolerance (IJT) of greater than 0.6 unit intervals (UI) and can provide retimed serial data outputs with very low alignment jitter. The quad reclockers require a single, external, 27 MHz crystal, which is used as the reference clock for all four channels. The devices also include per lane analog input equalization for up to 40" of FR4 trace and two connectors in addition to output de-emphasis.

These devices feature integrated supply regulators, allowing it to be powered from 1.2 V, 1.8 V, 2.5 V, or 3.3 V supply voltages. When operating at 1.2 V, it consumes only 135 mW per channel at 3G-SDI. Furthermore, the power rails for the core, input, and output circuitry are electrically independent and as such may be connected to different voltage rails on the board. This feature enables the M21350/M21355 to be DC coupled to any upstream or downstream device regardless of its input/output voltage level.

Each of the M21350's quad input MUXes allow any of the four inputs to be switched to the respective reclocker channel. The M21355's 16x4 input crosspoint allows any of the 16 inputs to be routed to any of the four integrated reclockers. The devices can be configured by setting the internal registers though standard two-wire and four-wire interfaces. Limited configuration is also possible through hardware pin settings.

The M21350 and M21355 are offered in a green and RoHS-compliant, 10 mm x 10 mm, 72-pin QFN packaging.

M21350/M21355 Block Diagram



Ordering Information

Part Number	Package	Operating Temperature
M21350G-15*	10 x 10 mm, 72-pin QFN package	-40 °C to 85 °C
M21355G-15*	10 x 10 mm, 72-pin QFN package	-40 °C to 85 °C
* The letter "G" designator after the part number indicates that the device is RoHS compliant. The RoHS compliant devices are backwards compatible with 225 °C reflow profiles.		

Revision History

Revision	Level	Date	Description
V6	Release	December 2015	Updated package drawing, Figure 3-12 and Figure 3-13. Package effective as of August 2014.
V5	Release	June 2015	Updated logos and page layout. No content changes.
I (V4)	Release	June 2012	Section 4.6.2: Revised 4 wire interface. Revised register address 0Bh default to 08h.
H (V3)	Release	December 2011	Figure 3-1: Typo fixed in Pin 66, Pin 11 changed from DIN2P to SDI2P, Pin 12 changed from DIN2N to SDI2N. Table 4-2: Function description for pins MF4 and MF5 modified to make *low* equivalent to *floating*. Table 1-8: Added 2-state input to VIH and VIL. Section 4.7.1: Renamed SDOA to SDO0. Section 4.9.2: Inserted a note to add a 10 kΩ pull to AV_{DDIO}.

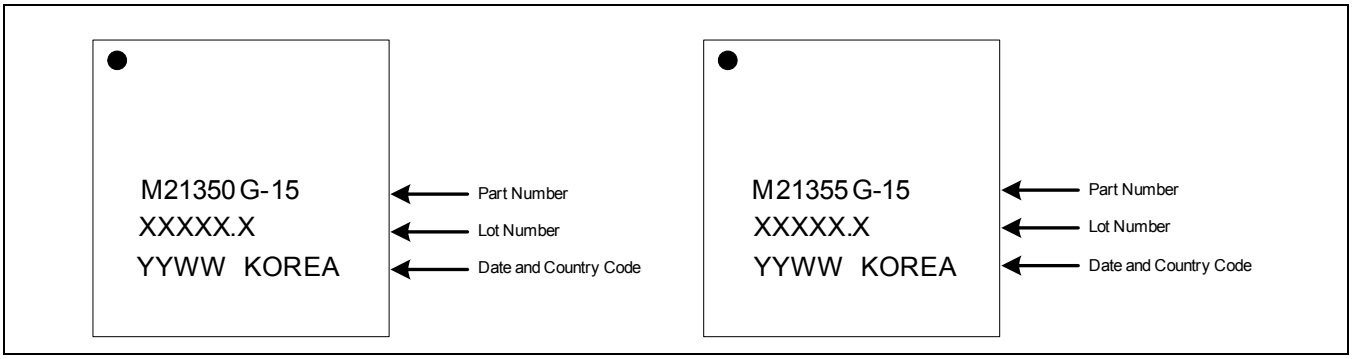
Revision History

Revision	Level	Date	Description
G (V2)	Released	February 2011	In the previous revision of this device, M21355/50G-14, the Loss of Lock (LOL) alarm would be erroneously triggered when pathological signals were used. As a workaround, MACOM recommended masking the faulty LOL alarm by setting register 96h bit[6] to 1b. In the latest version, M21355/50G-15, the faulty algorithm has been corrected. Therefore, the requirement to mask the LOL alarm has been removed from this data sheet. Please note that this change has been made to be fully backwards compatible, so setting register 96h bit[6] to 1b, while unnecessary, will not affect the function or performance of the device. Ordering Information: Updated part number from -14 to 15. Table 1-7: Updated XTAL and reference clock electrical specifications, input Impedance typical from to 400 kΩ to 200 Ω, input amplitude range from 1.6 V-2.0 V to 0.8 V to 1.2 V and max rise/fall times from 1 ns max to 2 ns typical and 6 ns max. Table 1-8: Updated V_{OH} from 0.75 to 0.80 x DV_{DDIO} and I_{OL} from 24 mA to 3 mA. Figure 3-1: Updated the pinout diagram to reflect new pin naming convention. Table 3-1: Updated table to reflect new pin naming convention. Table 5-1: Updated register map table. Added all registers needed to perform EEPROM checksum. Register 0Eh: Modified Interrupt mode xAlarm pulse widths to reflect their true value with respect to a 10K Ω pull up resistor. Register 82h: Updated chip version from 03h to 04h. Section 4.2: Included conditions necessary for self biased mode. Figure 4-4: Updated self bias diagram to reflect conditions necessary for self biased mode. Section 4.6.2: Updated to include the detailed timing description for four-wire interface when conducting a write operation followed by a read operation. Table 4-6: Updated the EEPROM addresses. Table 4-7: Updated the EEPROM addresses. Section 4.7.1: Clock Recovery: Updated the data to clock delay to 60 ps. Status for floating logic state for pin MF4 changed from reclocker bypass to normal operation in Table 3-1 and Table 4-2. Status for floating logic state for pin MF5 changed from reclocker bypass to normal operation in Table 3-1 and Table 4-2. Corrected pins 59, 58 to SDO3/SCLKP/N in Table 3-1. Changed MF4 and MF5 levels in Table 3-1. Added note to Figure 4-4. Changed MF4 and MF5 levels in Table 4-2. Changed MF3 function description in Table 4-5.
F (V1)	Released	May 2010	Revised all power consumption specifications in Table 1-3. Revised minimum and maximum values for V_{OUT} in Table 1-5. Revised typical and maximum values for t_R/t_F in Table 1-5. Revised typical and maximum values for J_{OUT} in Table 1-6. Revised bit values for 11h (Group Rate CTRL) register in Table 5-1. Revised bit values for 88h (Reclocker ALARMS) register in Table 5-1. Revised description field in Section 4.2. Revised bit 4 description for 11h (Reclocker Configuration). Revised description field 83h (LOS Status 0). Revised description field 84h (LOS Status 1). Revised description field 85h (Alarm Clear). Revised description field 88h (Reclocker Status Register). Revised bit 4 and 5 descriptions for 88h (Reclocker Status Register).
E (V1P)	Preliminary	March 2010	Refer to prior revision for details.
D (V4A)	Advance	November 2009	Combined M21350 and M21355 data sheets. Added M21350 register details in Section 5.0. Minimum input swing increased to 300 mV.
C (V3A)	Advance	May 2009	Removed M21350 and updated all sections.
B (V2A)	Advance	October 2008	Added chip outline and crystal capacitance.

Revision History

Revision	Level	Date	Description
A (V1A)	Advance	August 2008	Initial release.

M21350/M21355 Marking Diagram



1.0 Electrical Characteristics

Unless noted otherwise, specifications apply for typical recommended operating conditions shown in Table 1-2, with DV_{DDO} = 1.2 V, AV_{DDCORE} = 1.2 V, DV_{DDCORE} = 1.2 V, AV_{DDI} = 1.2 V, CML inputs/outputs at 800 mV differential (R_{LOAD} = 50 Ω), and PRBS 2^{10} – 1 test pattern at 2.97 Gbps.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Note	Minimum	Maximum	Unit
AV_{DDI}	Analog supply for input circuitry	1, 3	-0.5	3.6	V
AV_{DDO}	Analog supply for output circuitry	1, 3	-0.5	3.6	V
DV_{DDIO}	Digital supply for input/output circuitry	1, 3	-0.5	3.6	V
DV_{DDCORE}	Digital core positive supply	1, 3	-0.5	1.5	V
AV_{DDCORE}	Analog core positive supply	1, 3	-0.5	1.5	V
T_{STORE}	Storage Temperature	1, 3	-65	150	°C
$V_{IN, CMOS}$	DC input voltage (CMOS)	1, 3	-0.5	DV_{DDIO}+0.5	V
V_{IN}	DC input voltage (PCML)	1, 3	-0.5	AV_{DDI}+0.5	V
$V_{ESD, HBM}$	Human Body Model (HBM)	1, 2, 3	-2	2	kV
$V_{ESD, CDM}$	Charge Device Model (CDM)	1, 2, 3	-500	500	V
LU	Latch Up @ 85 °C	1, 3	-150	150	mA
V_{IN}	Maximum High-speed input current	1, 3	-100	100	mA
$I_{OUT, PCML}$	Maximum High-speed output short circuit current	1, 3	-0.5	100	mA

NOTES:

1. Exposure of the device beyond the minimum/maximum limits may cause permanent damage. Limits listed in the above table are stress limits only, and do not imply functional operation within these limits.
2. HBM and CDM per JEDEC Class 2 (JESD22-A114-B).
3. Limits listed in the above table are stress limits only and do not imply functional operation within these limits.

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
DV_{DDIO}	Digital I/O positive supply	—	1.14	1.2, 1.8, 2.5, or 3.3	3.47	V
AV_{DDI}	Analog input positive supply	—	1.14	1.2, 1.8, 2.5, or 3.3	3.47	V
AV_{DDO}	Analog output positive supply	—	1.14	1.2, 1.8, 2.5, or 3.3	3.47	V
AV_{DDCORE}	Analog core positive supply	—	1.14	1.2	1.26	V
DV_{DDCORE}	Digital core positive supply	—	1.14	1.2	1.26	V
T_{CASE}	Case Temperature	—	-40	25	+85	°C

Table 1-3. Power Consumption Specifications

Symbol	Parameter	Conditions	Note	Typical	Maximum	Unit
P_{TOTAL}	Total power consumption	AV_{DDI} = AV_{DDO}=DV_{DDIO}=DV_{DDCORE} = AV_{DDCORE}= 1.2 V SDO Swing Level 1	1	540	750	mW
		AV_{DDI} = AV_{DDO}=DV_{DDIO}=DV_{DDCORE} = 1.2V AV_{DDCORE}= 1.2 V SDO Swing Level 2	1	550	780	mW
		AV_{DDI} = AV_{DDO}=DV_{DDIO}=DV_{DDCORE} = 1.2V AV_{DDCORE}= 1.2 V AV_{DDO}= 1.8 V SDO Swing Level 3	1	650	880	mW
		AV_{DDI} = DV_{DDIO}= AV_{DDO}= 3.3 V AV_{DDCORE}/DV_{DDCORE} = N/A Internal regulators enabled SDO Swing Level 3	2	1740	2130	mW
θ_{JA}	Junction to Ambient Thermal Resistance		3	25	—	°C/W

NOTE:

1. Internal regulators disabled.
2. Internal regulators enabled.
3. Airflow = 0 m/s.

Table 1-4. SDI High Speed (Positive Current Mode Logic) Input Electrical Specifications

Symbol	Parameter	Conditions	Note	Minimum	Typical	Maximum	Unit
DR	SDI input data rate	SD Operation (SMPTE 259M-C)		—	270	—	Mbps
		HD Operation (SMPTE 292)		—	1485, 1483.5	—	Mbps
		3G Operation (SMPTE 424M)		—	2970, 2967	—	Mbps
		Reclocker bypassed		18	—	3400	Mbps
V_{IN}	Differential input voltage	At the chip input (point blank) Input equalization disabled LOS enabled (80/90 setting)	1, 3	300	800	1600	mV_{PPD}
V_{ICM}	Input common mode voltage	At the chip input (point blank) Input equalization disabled LOS enabled		AV_{DDI}-0.6	—	AV_{DDI}+0.1	V
R_{IN}	Input Termination to AV_{DDI}			40	50	60	Ω
IE	Input Equalization		2	—	0, 2, 4, 6	—	dB

NOTE:

1. For example, 1200 mV_{PP} differential = 600 mV_{PP} for each single-ended terminal.
2. These values correspond to: off, small, medium, and large respectively. The small setting is not available in hardware mode.
3. When using long traces and input equalization enabled, MACOM recommends a minimum input swing of 400 mV_{PPD}. With pathological patterns, DC coupling produces the best results.

Table 1-5. SDO High Speed (Positive Current Mode Logic) Output Electrical Specifications

Symbol	Parameter	Conditions	Note	Minimum	Typical	Maximum	Unit
DR	SDO output data rate	SD Operation (SMPTE 259M-C)		—	270	—	Mbps
		HD Operation (SMPTE 292)		—	1485, 1483.5	—	
		3G Operation (SMPTE 424M)		—	2970, 2967	—	
		Reclocker bypassed		18	—	3400	
F_{CLOCK}	Serial clock output frequency	SD Operation (SMPTE 259M-C)	1, 6	—	270	—	MHz
		HD Operation (SMPTE 292)		—	1485, 1483.5	—	
		3G Operation (SMPTE 424M)		—	2970, 2967	—	
V_{OUT}	Differential Output Swing (peak to peak, differential)	Swing Level 1	2	470	600	720	mV_{PPD}
		Swing Level 2	2	600	800	970	
		Swing Level 3	2,3	960	1200	1500	
V_{OCM}	Output common mode voltage	DC coupled	2	—	AV_{DDO}-V_{OUT}/4	—	
t_R/t_F	SDO output Rise/Fall Time	From 20%-80% of the swing for all levels		—	85	130	ps
$t_R/t_{F\ DIFF}$	Rise/Fall Time Mismatch	From 20%-80% of the swing for all levels		—	—	30	ps
DCD_{DATA}	Output duty cycle distortion	For all data rates	4	—	—	15	ps
R_{OUT}	Output Termination to AV_{DDO}			40	50	60	Ω
DE	Output De-Emphasis		5	—	0, 2, 4, 6	—	dB

NOTE:

1. Serial clock output enabled.
2. Differential swing is maximum output level (De-emphasis is disabled or max level when de-emphasis is enabled), max level includes overshoot.
3. 1200 mV swing level requires AV_{DDO} to be 1.8 V or higher.
4. Measured in reclocked mode.
5. These values correspond to: off, small, medium, and large respectively. The small setting is not available in hardware mode.
6. See Section 4.7 for information on clock data alignment.

Table 1-6. Reclocker Specifications *(See note below for Level B format)*

Symbol	Parameter	Conditions	Note	Minimum	Typical	Maximum	Unit
t_{LOCK}	Lock time (asynchronous)	Automatic rate detection enabled	1	—	—	6	ms
$F_{LBWPEAK}$	Loop bandwidth peaking		1	—	0.1	—	dB
F_{LBW}	Loop bandwidth (nominal setting)	3G operation (2.97 Gbps)	1	—	1.7	—	MHz
		HD operation (1.485 Gbps)	1	—	0.85	—	
		SD operation (270 Mbps)	1	—	0.17	—	
J_{TOL}	Input jitter tolerance	3G, HD, and SD operation	2	>0.6	—	—	UI p-p
J_{GEN}	Total Output jitter	3G operation (2.97 Gbps)	2, 3	—	0.07	0.11	UI p-p
		HD operation (1.485 Gbps)	2, 3	—	0.04	0.06	
		SD operation (270 Mbps)	2, 3	—	0.02	0.05	

NOTE:

1. 0.2 UI input jitter applied at SDI input.
2. Measured with $PRBS2^{10}$-1.
3. Input jitter = 20 ps p-p.

Table 1-7. XTALP/N and Reference Clock Electrical Specifications

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
F_{REF}	XTAL/Ref clock frequency	3	—	27	—	MHz
$F_{REF, PPM}$	XTAL/Ref clock frequency accuracy	—	-100	0	100	ppm
C_{LOAD}	XTAL load capacitance	1	—	20	25	pF
$CLOCK_{JITT}$	Jitter (RMS)	2, 4	—	—	1	ps
$CLOCK_{DCT}$	Reference clock duty cycle tolerance	2	40	—	60	%
R_{IN}	Input impedance	2, 5	0.2	0.75	1.2	kΩ
V_{IN}	Input amplitude	2	0.8	—	1.2	V
t_R/t_F	Rise/Fall time	2, 6	—	2	6	ns

NOTE:

1. This capacitance is supplied internally (no external cap is required).
2. When using an external reference clock source, this should be AC coupled through a 0.1 µF capacitor.
3. When using an external clock a small increase in jitter may be seen. For best performance a crystal is recommended.
4. Jitter Bandwidth 12 kHz to 20 MHz.
5. Measured with Agilent TDR module.
6. 10% to 90% rise and fall times.

Table 1-8. Digital Input/Output Electrical Characteristics

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
V_{OH}	Output Logic High	1	0.80 x DV_{DDIO}	DV_{DDIO}	—	V
V_{OL}	Output Logic Low	2	—	—	0.2 x DV_{DDIO}	V
V_{IH}	Input Logic High	3, 5	0.85 x DV_{DDIO}	—	DV_{DDIO} + 0.5	V
V_{IF}	Input Logic Floating	3, 5	0.25 x DV_{DDIO}	—	0.75 x DV_{DDIO}	V
V_{IL}	Input Logic Low	3, 5	0	—	0.15 x DV_{DDIO}	V
V_{IH}	Input Logic High	4, 5	0.75 x DV_{DDIO}	—	DV_{DDIO} + 0.5	V
V_{IL}	Input Logic Low	4, 5	0	—	0.25 x DV_{DDIO}	V

NOTE:

1. I_{OH} = -3 mA
2. I_{OL} = 3 mA
3. 3- state input
4. 2- state input
5. Some inputs can be 2 or 3 state. Depending on which mode is selected the threshold levels will change accordingly.

2.0 Typical Performance Characteristics

Figure 2-1. Eye Diagram at Reclocker Input PRBS15 pattern@ 3 Gbps

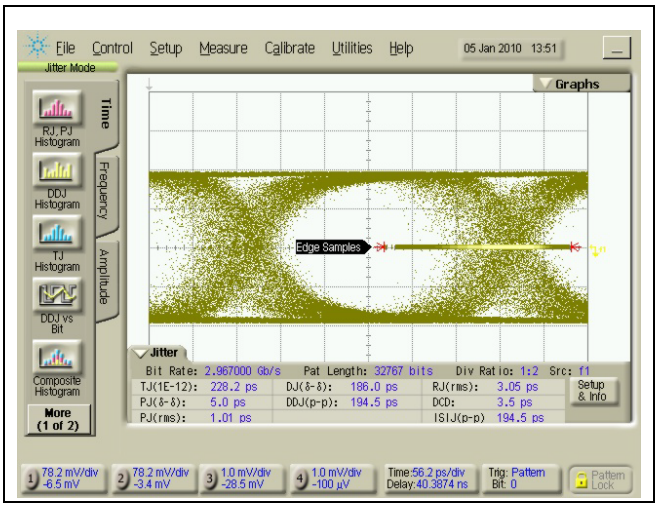
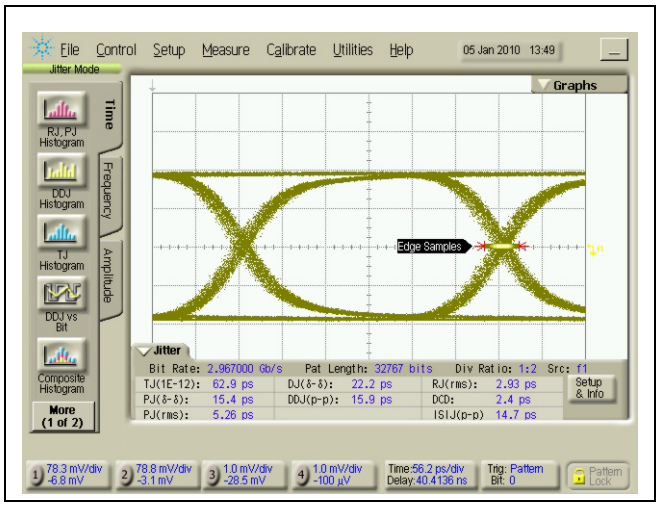


Figure 2-2. Eye Diagram at Reclocker Output PRBS15 pattern@ 3 Gbps



3.0 Pinout Diagram, Pin Descriptions, and Package Outline Drawing

Figure 3-1. M21350/M21355 Pinout Diagram

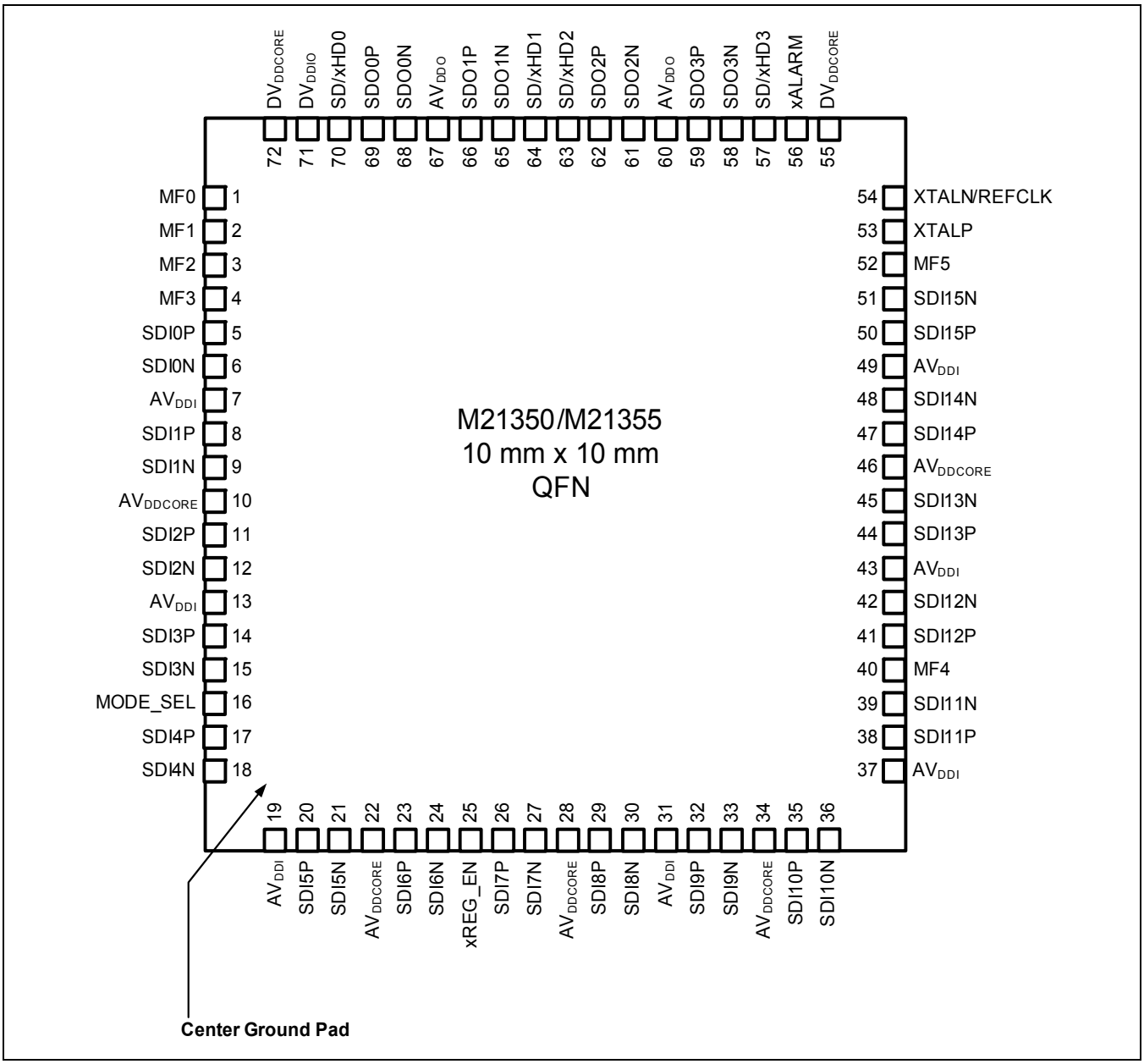


Table 3-1. M21350/M21355 Pin Description

Pin Name	Pin Number	Type	Description
AV_{DDCORE}	10, 22, 28, 34, 46	Power	Analog positive supply
AV_{DDI}	7, 13, 19, 31, 37, 43, 49	Power	Analog positive supply
AV_{DDO}	60, 67	Power	Analog positive supply
DV_{DDCORE}	55, 72	Power	Digital Core Positive Supply
DV_{DDIO}	71	Power	Digital Core Positive Supply
AV_{SS}	Center Ground Pad	Power	Ground
SDI0P, SDI0N	5, 6	PCML input	Data Input Lane0; true/complement
SDI1P, SDI1N	8, 9	PCML input	Data Input Lane1; true/complement
SDI2P, SDI2N	11, 12	PCML input	Data Input Lane2; true/complement
SDI3P, SDI3N	14, 15	PCML input	Data Input Lane3; true/complement
SDI4P, SDI4N	17, 18	PCML input	Data Input Lane4; true/complement
SDI5P, SDI5N	20, 21	PCML input	Data Input Lane5; true/complement
SDI6P, SDI6N	23, 24	PCML input	Data Input Lane6; true/complement
SDI7P, SDI7N	26, 27	PCML input	Data Input Lane7; true/complement
SDI8P, SDI8N	29, 30	PCML input	Data Input Lane8; true/complement
SDI9P, SDI9N	32, 33	PCML input	Data Input Lane9; true/complement
SDI10P, SDI10N	35, 36	PCML input	Data Input Lane10; true/complement
SDI11P, SDI11N	38, 39	PCML input	Data Input Lane11; true/complement
SDI12P, SDI12N	41, 42	PCML input	Data Input Lane12; true/complement
SDI12P, SDI13N	44, 45	PCML input	Data Input Lane12; true/complement
SDI14P, SDI14N	47, 48	PCML input	Data Input Lane14; true/complement
SDI15P, SDI15N	50, 51	PCML input	Data Input Lane15; true/complement
SDO0P, SDO0N	69, 68	PCML output	Data Output Lane0; true/complement
SDO1P, SDO1N	66, 65	PCML output	Data Output Lane1; true/complement
SDO2P, SDO2N	62, 61	PCML output	Data Output Lane2; true/complement
SDO3P/SCLKP, SDO3N/ SCLKN	59, 58	PCML output	Data Output Lane3; true/complement
XTALP	53	Reference Clock	27 MHz reference XTAL connection
XTALN/REFCLK	54	Reference Clock	27 MHz reference XTAL connection or 27 MHz reference clock input

Table 3-1. M21350/M21355 Pin Description

Pin Name	Pin Number	Type	Description
MODE_SEL	16	CMOS Control Input	Sets the device control/configuration mode: L = Device is in register access mode with two-wire serial control (SIC2) F = Device is in hardware control mode (Hardware Mode) H = Device is in register access mode with four-wire serial control (SIC4) Termination - F
xREG_EN	25	CMOS Control Input	Regulator enable control, as in Figure 3-6, but pull up resistor is to AV_{DDI}. L = Integrated regulators enabled F = Integrated regulators disabled Termination - H, 100 kΩ pull up to AV_{DDI}
SD/xHD0	70	CMOS Output	CMOS SD/xHD rate indicator L = HD/3G Data rate H = SD Rate
SD/xHD1	64	CMOS Output	CMOS SD/xHD rate indicator L = HD/3G Data rate H = SD Rate
SD/xHD2	63	CMOS Output	CMOS SD/xHD rate indicator L = HD/3G Data rate H = SD Rate
SD/xHD3	57	CMOS Output	CMOS SD/xHD rate indicator L = HD/3G Data rate H = SD Rate
xALARM	56	Output (Open Drain)	Alarm indicator for all channels (Logical OR of all individual channel alarms). Termination - Open L = Alarm asserted H = Normal operation Serial Control Mode (two-wire/four-wire) Mode: Reg0E = 00h, xALARM in interrupt mode Reg0Eh=08b, xALARM in status mode Hardware Mode: xALARM is in status mode
MF0	1	CMOS Control Input	Four-wire serial control Mode: Serial clock input (SCLK) Two-wire serial control Mode: Clock input from master host (SCL) Hardware Mode: Unused
MF1	2	CMOS Control Input	Four-wire serial control Mode: Serial data output (SO) Two-wire serial control Mode: Serial data I/O (SDA) Hardware Mode: Unused

Table 3-1. M21350/M21355 Pin Description

Pin Name	Pin Number	Type	Description
MF2	3	CMOS Control Input	Four-wire serial control Mode: Serial data in (SI) Two-wire serial control Mode: Address bit 0 (ADD0) Hardware Mode: Input trace equalization control for all SDI inputs (IE_CTRL) H = Large Input EQ F = Medium Input EQ L = Input EQ disabled
MF3	4	CMOS Control Input	Four-wire serial control Mode: Active low chip select (xCS) Two-wire serial control Mode: Address bit 1 (ADD1) Hardware Mode: Output de-emphasis (DE) control for SDO outputs (DE_CTRL) H = Large Output DE F = Medium Output DE L = DE disabled
MF4	40	CMOS Control Input	Four-wire serial control Mode: Not used. Tie to DV_{DDIO} or leave floating Two-wire serial control Mode: Address bit 2 (ADD2) Hardware Mode: Reclocker bypass control (RC_BYPASS) L/F = Normal operation, Reclocker not bypassed H = Reclocker bypassed
MF5	52	CMOS Control Input	Four-wire serial control Mode: Not used. Tie to AVSS or leave floating Two-wire serial control Mode: Address bit 3 (ADD3) Hardware Mode: SDO disable control for all outputs (SDO_DIS) H = SDO disabled output logic high L/F = SDO enabled

Figure 3-2. I-Analog

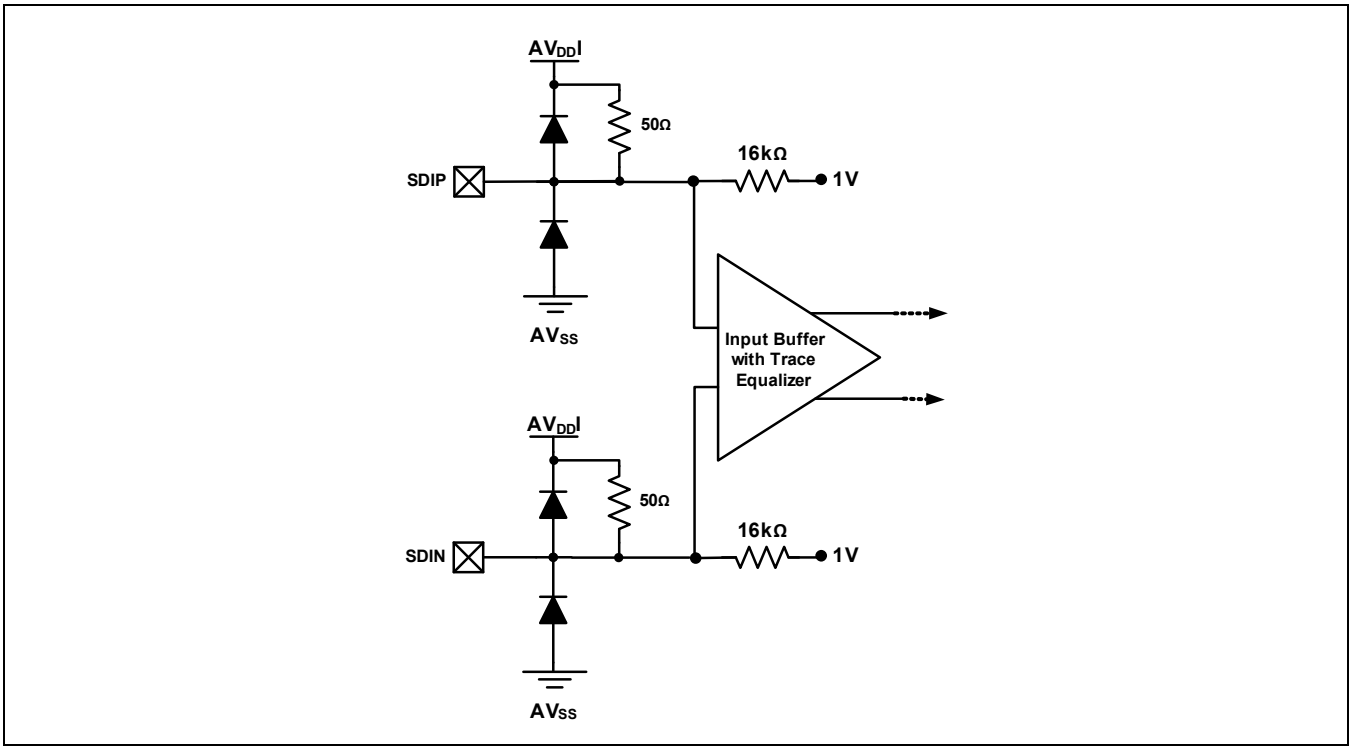


Figure 3-3. O-Analog

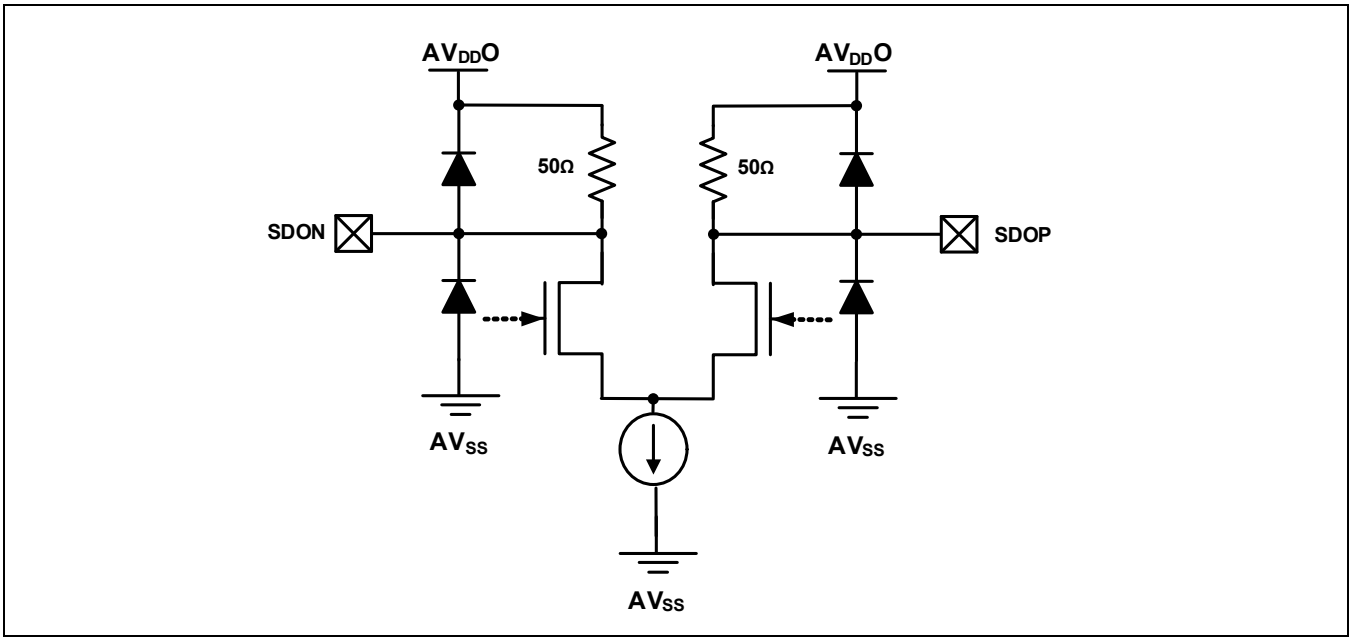


Figure 3-4. Ref Clock

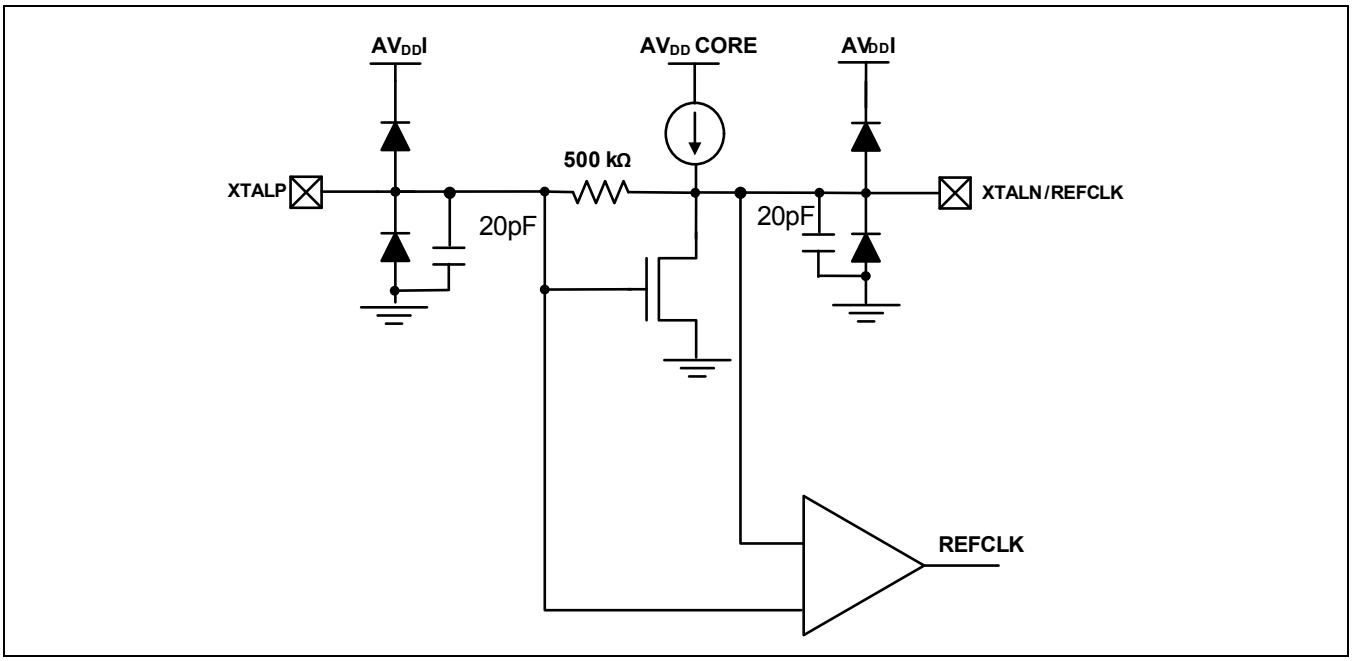


Figure 3-5. I-Digital With No Pull-up

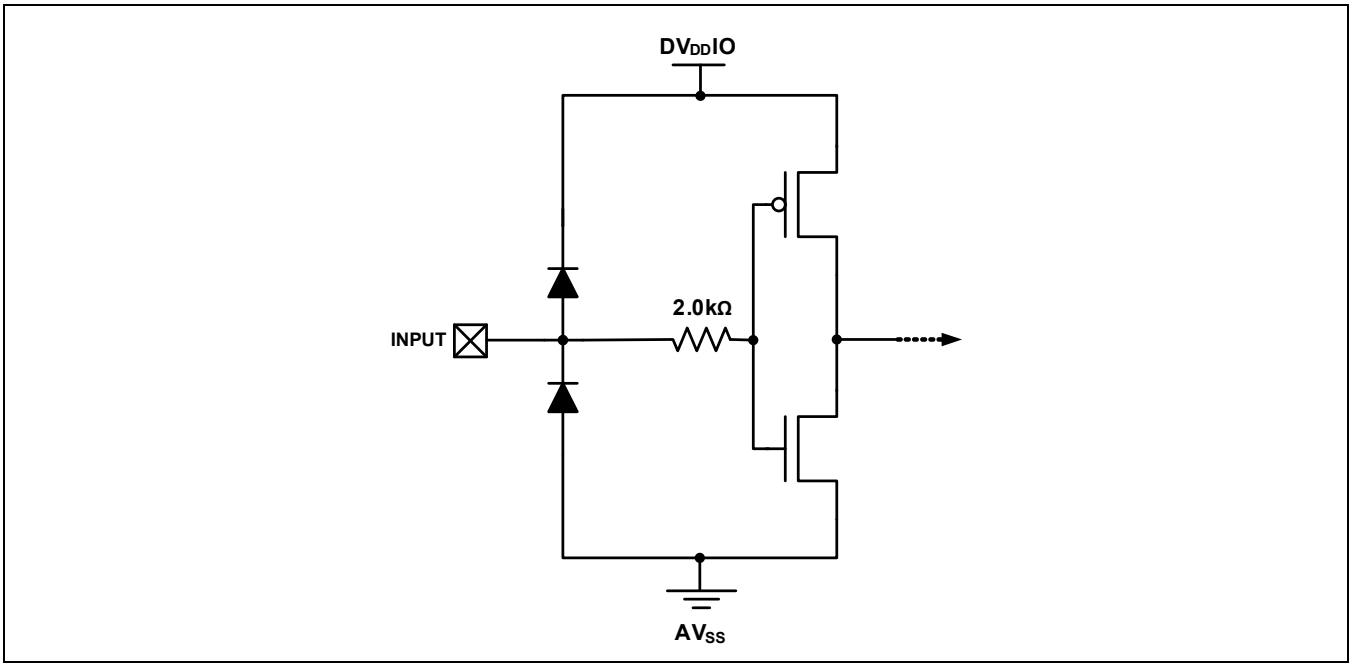


Figure 3-6. I-Digital With Pull-up

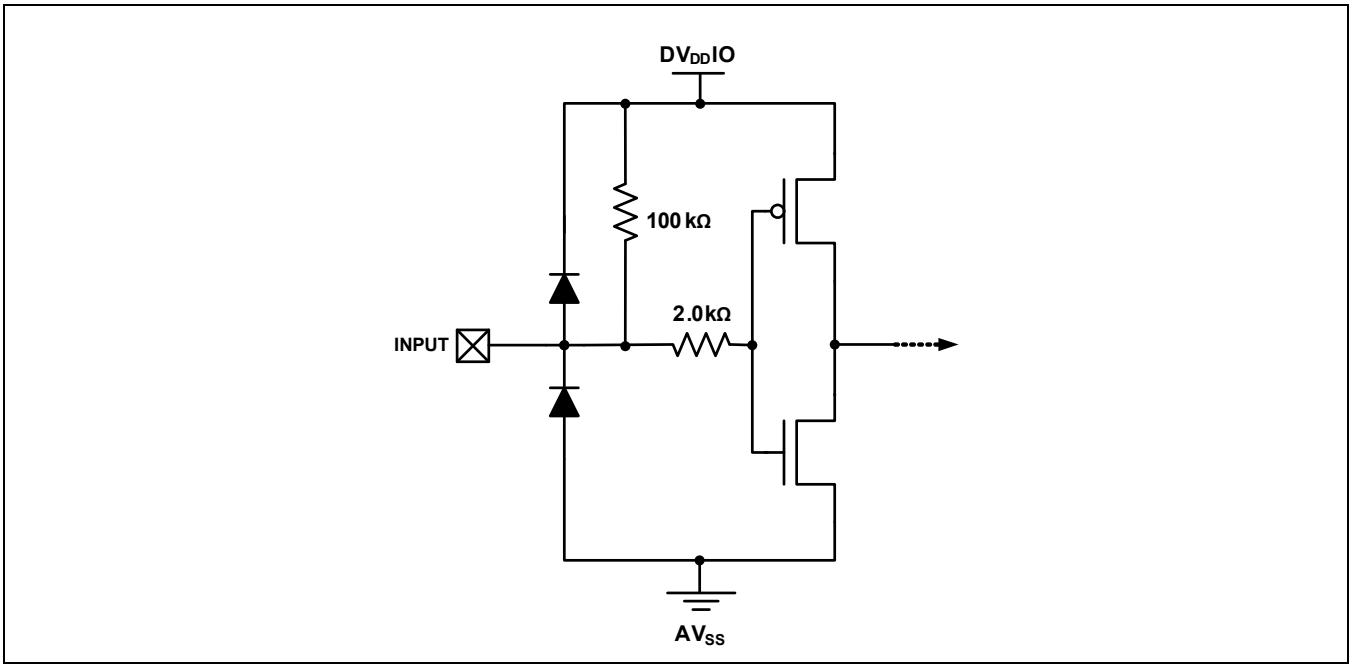


Figure 3-7. I-Digital With Pull-down

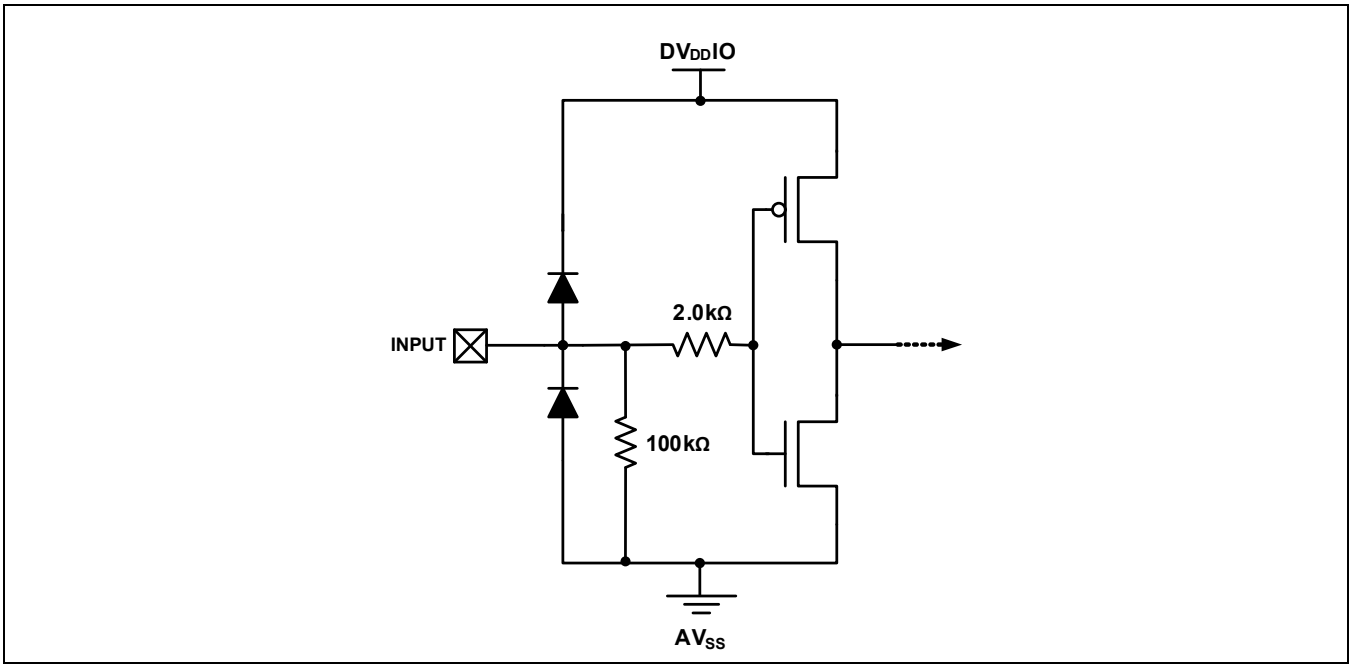


Figure 3-8. 3-State/I-Digital

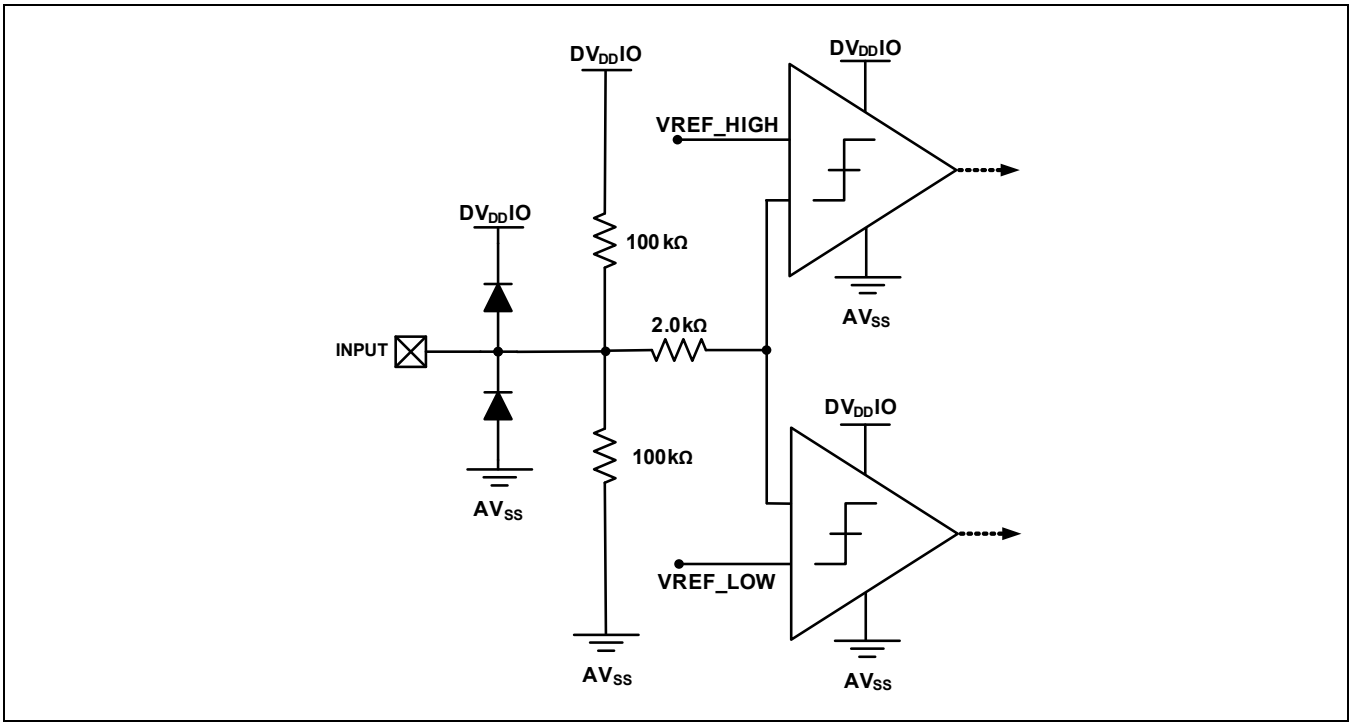


Figure 3-9. O-Digital

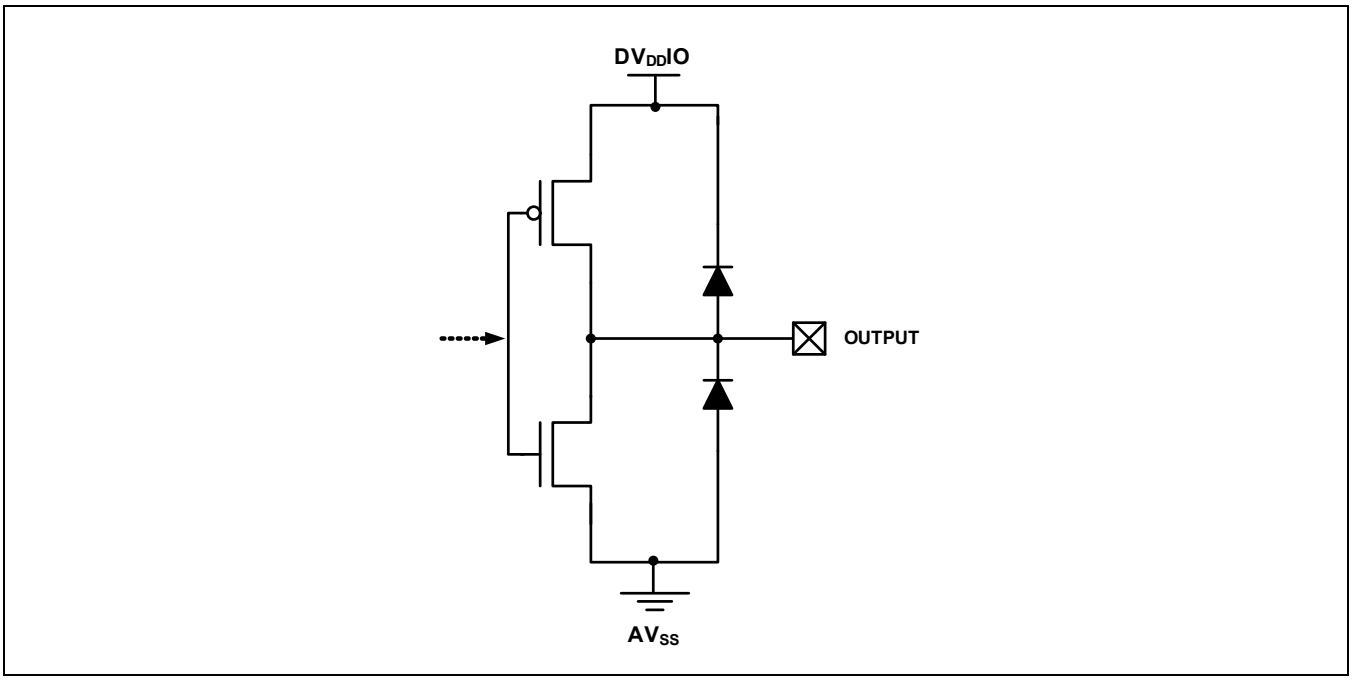
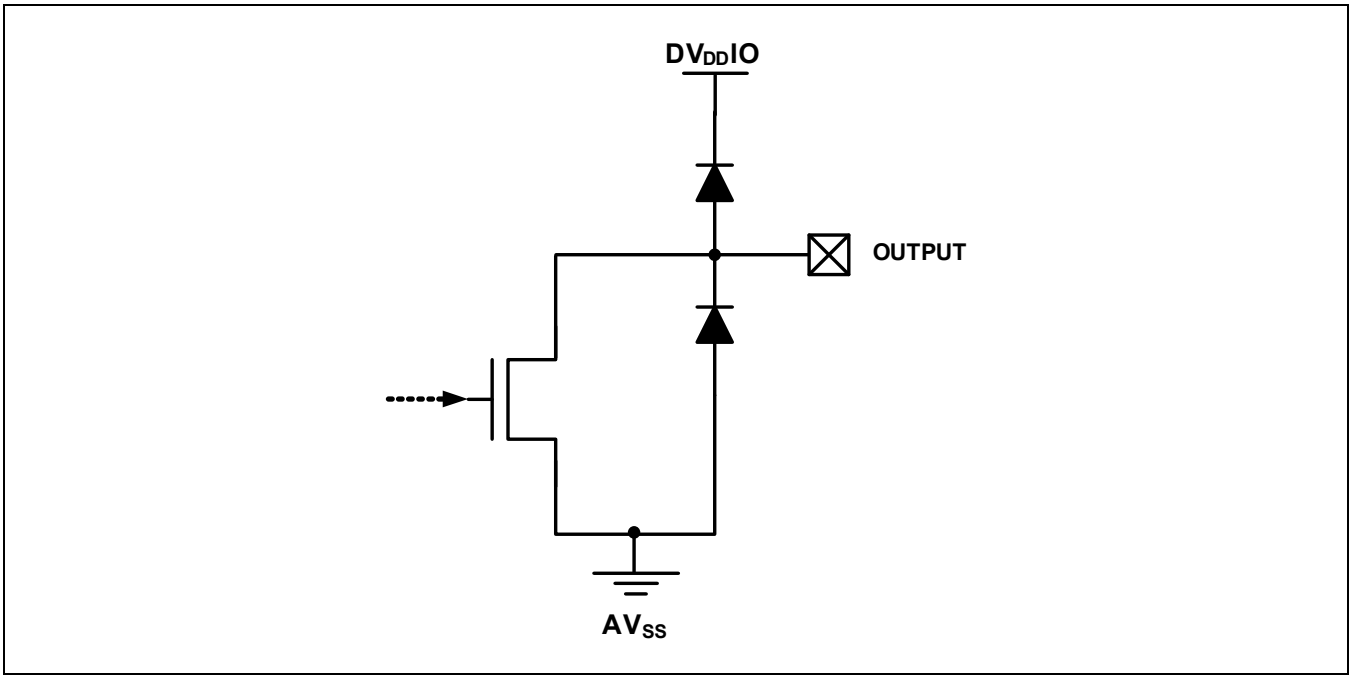


Figure 3-10. O-Open Drain



The M21350/M21355 is assembled in a 72-pin, 10 mm x 10 mm Quad Flat No-Lead (QFN) package. The exposed paddle serves as the IC ground (AV_{SS}), and the primary means of thermal dissipation. This paddle should be soldered to the PCB. A cross-section of the QFN package is shown below.

Figure 3-11. QFN Package Cross Section

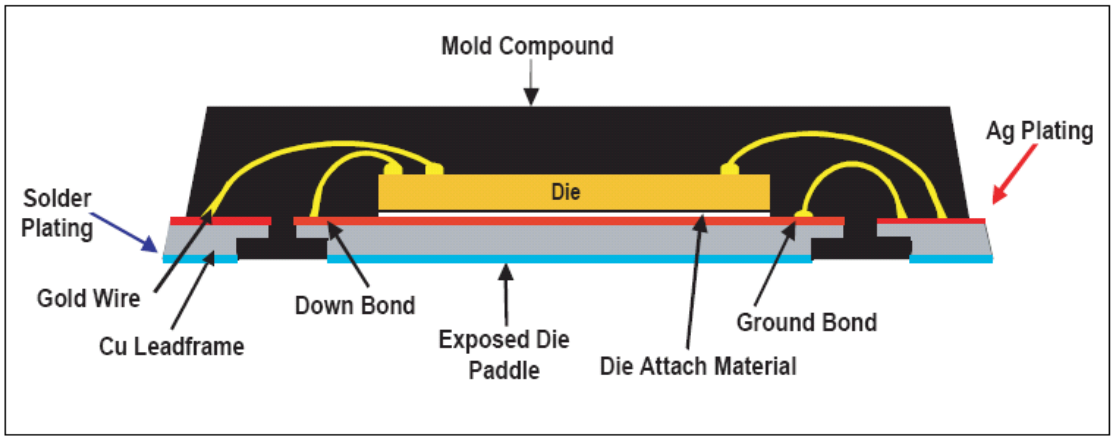
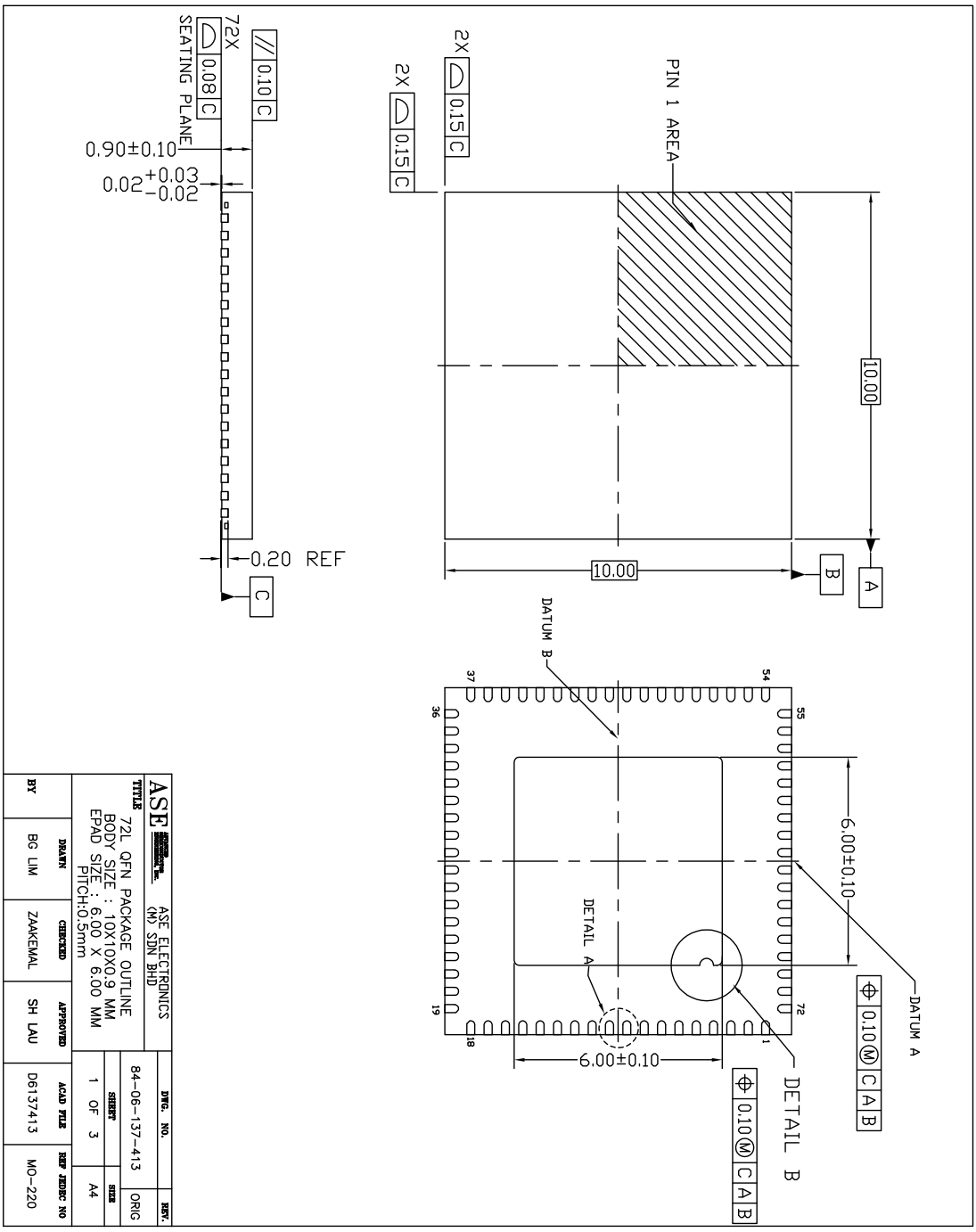
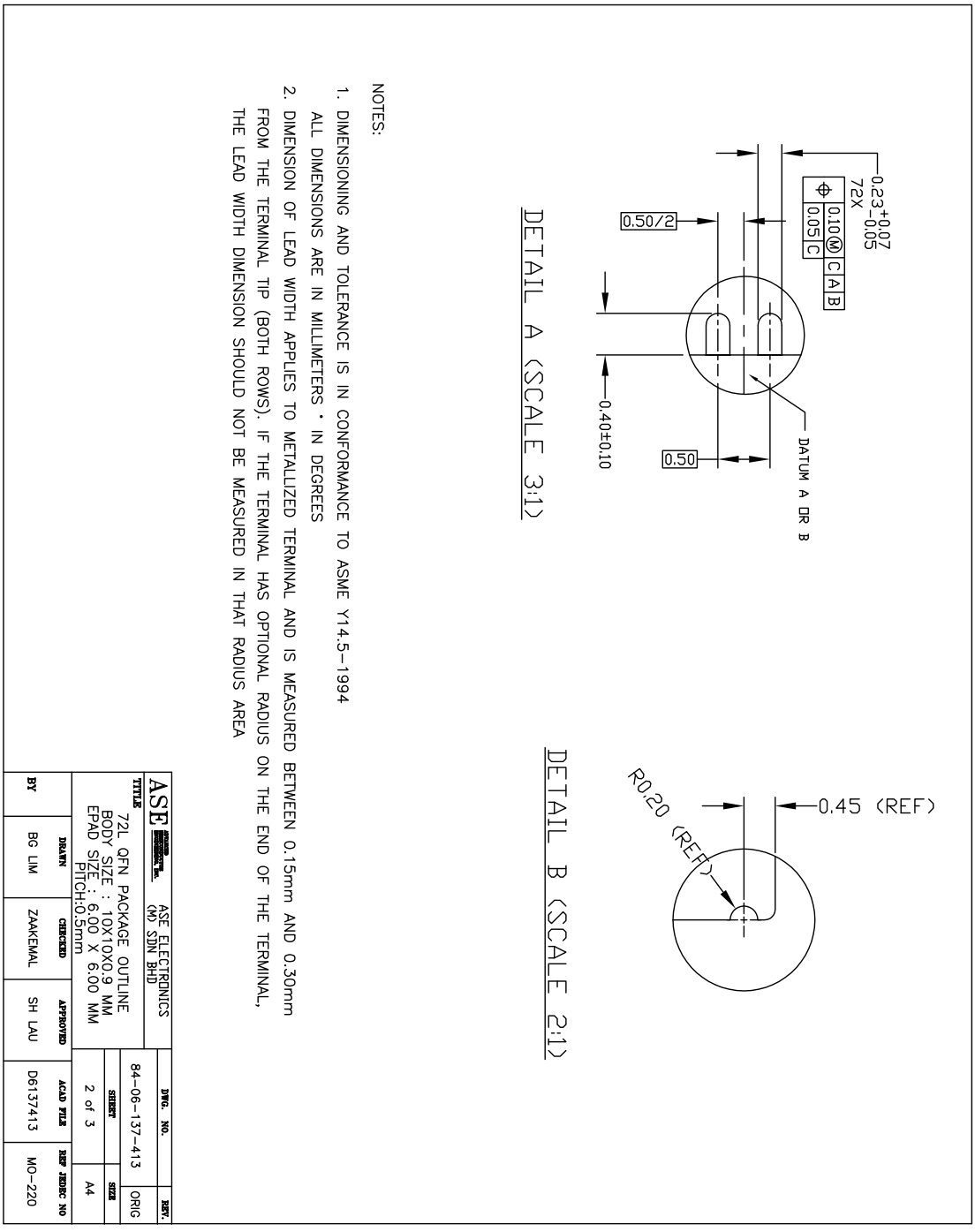


Figure 3-12. Package Outline Drawing



1. New Unisem package and old Amkor package have the same footprint dimensions.

Figure 3-13. 72-Pin QFN Package Dimensions



1. New Unisem package and old Amkor package have the same footprint dimensions.

4.0 Functional Description

4.1 Functional Block Diagram

Figure 4-1and Figure 4-2 illustrate the M21350 and M21355 block diagrams respectively. The subsequent sections provide additional detail on the operation of the devices.

Figure 4-1. M21350 Block Diagram

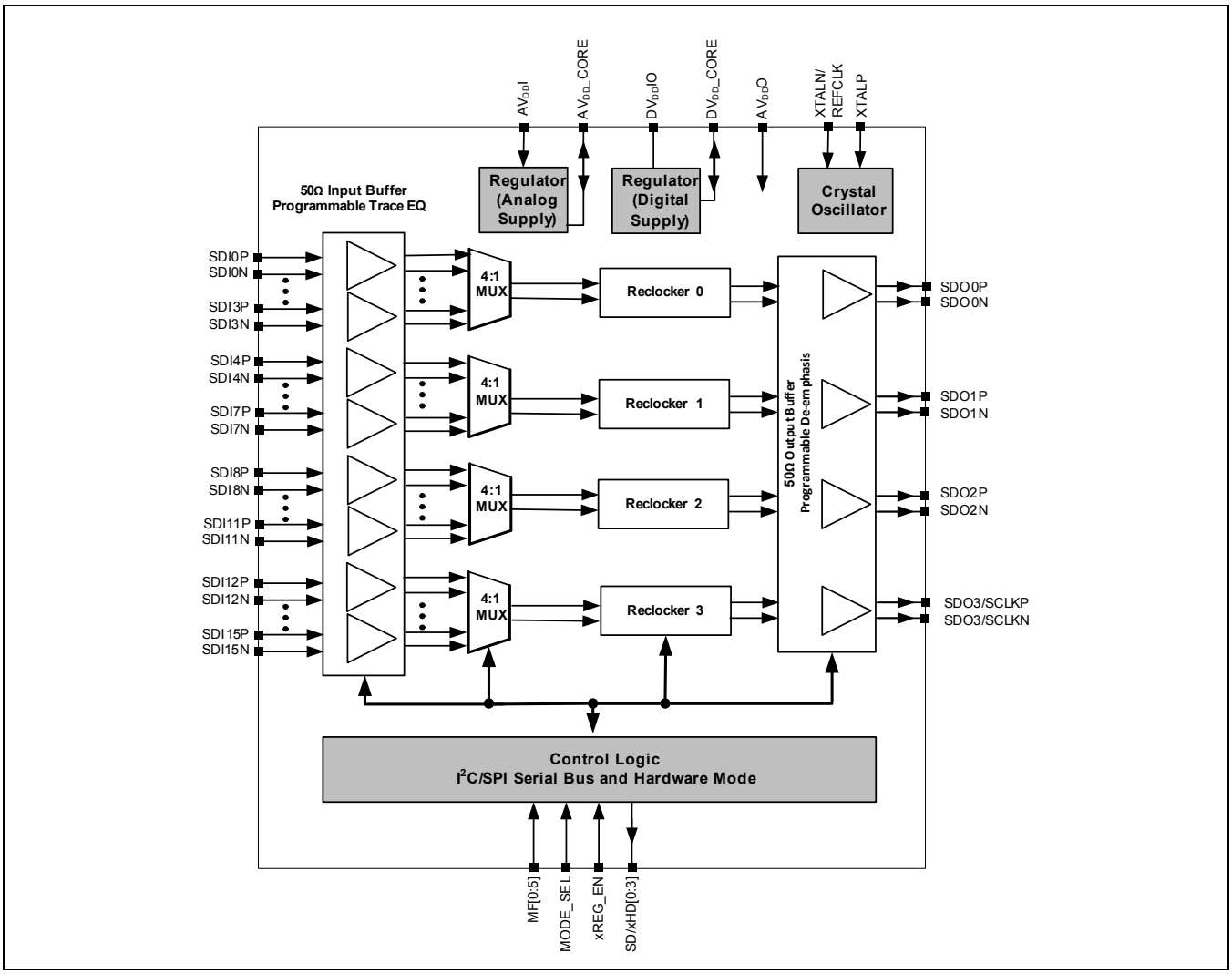
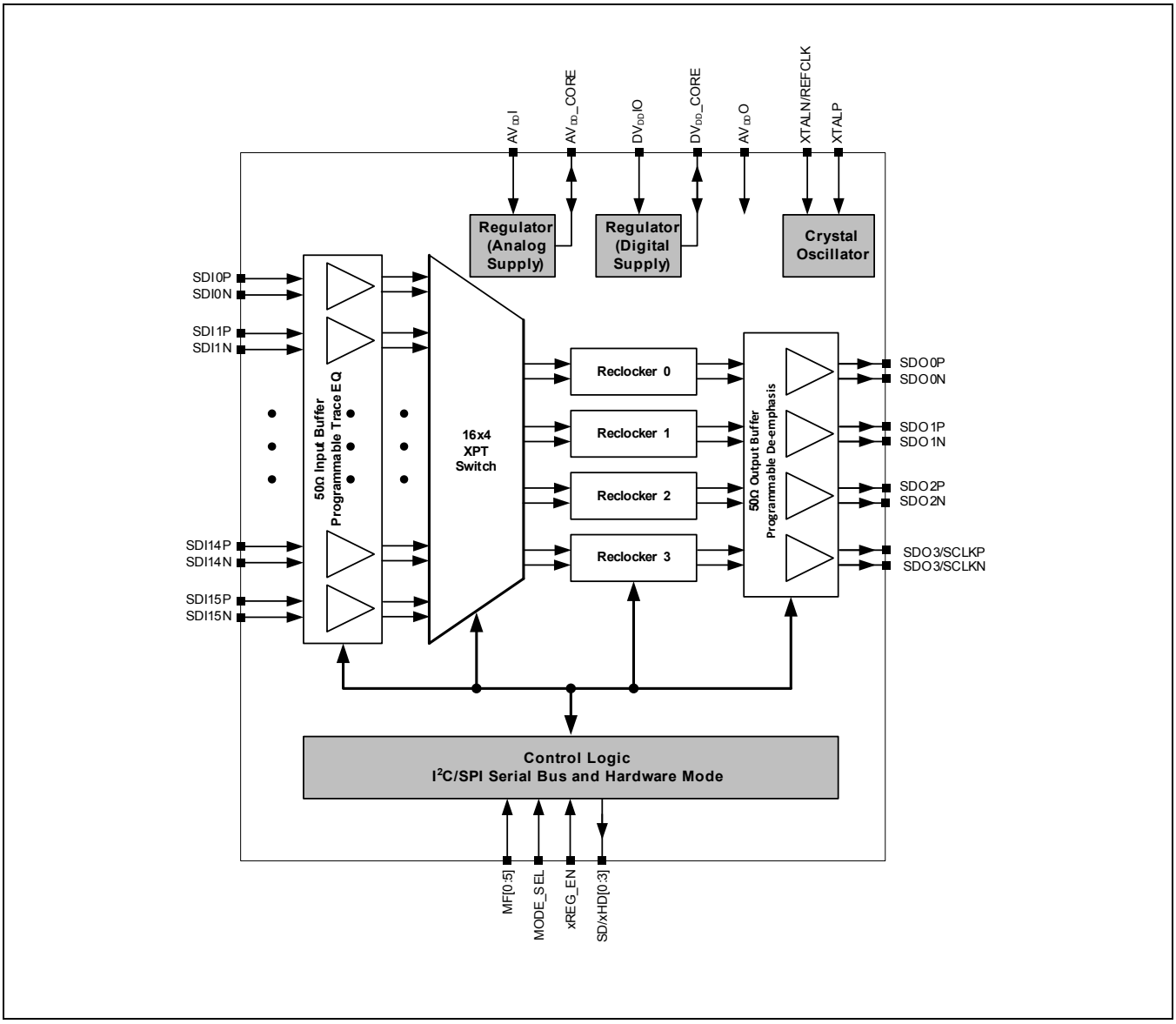


Figure 4-2. M21355 Block Diagram



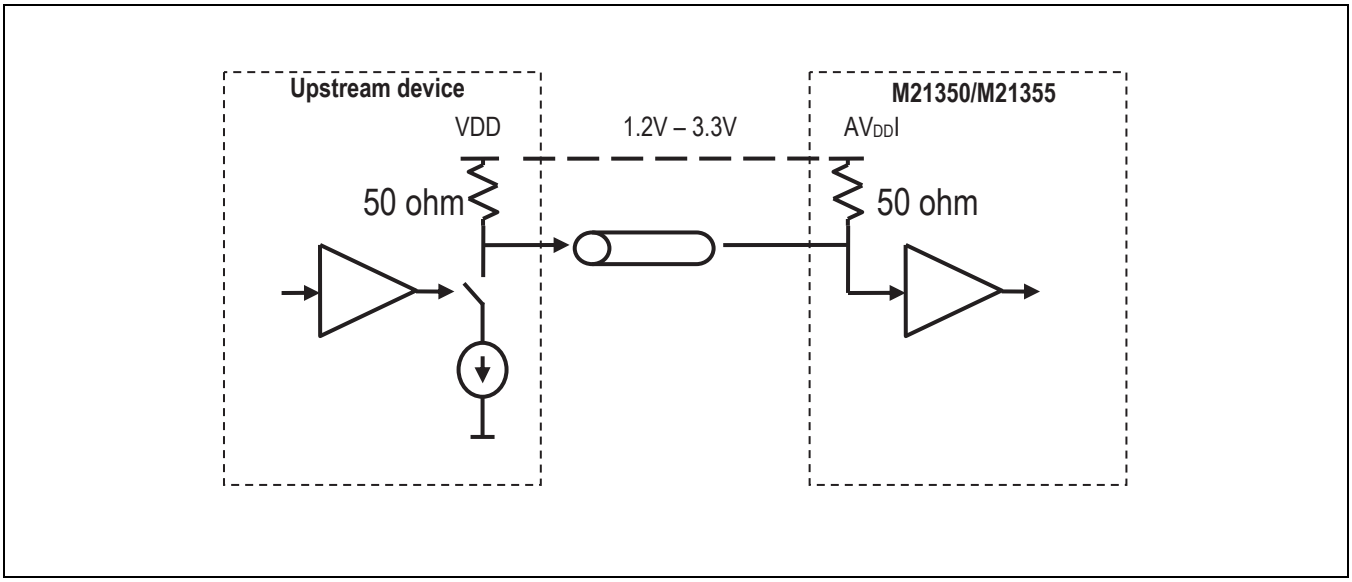
4.2 High-Speed Differential Inputs

The M21350/M21355 features 16 differential, PCML-compatible inputs. LVDS and LVPECL signal levels are also accommodated. Serial data to be retimed is presented to these 16 inputs. Each input is terminated with an internal 50 Ω termination to AV_{DDI}. AV_{DDI} can be supplied from any voltage ranging from 1.2 V to 3.3 V.

In order to improve signal integrity when used in large systems, each input also comes equipped with programmable input equalization (IE) for FR4 trace. There are four settings for input equalization: 0 dB (or no equalization), 2 dB, 4 dB, and 6 dB. In serial control mode, the input equalization level for each input may be set by programming the desired value to reg00h-reg03h. Alternatively, in hardware mode, the input equalization for all of the inputs may be set globally through the IE_CTRL (MF2) pin. In hardware mode only the three settings of 0 dB, 4 dB, and 6 dB are available.

In most SDI applications, it is important to avoid AC coupled data interfaces between devices wherever possible. In addition to reducing the number of components, DC coupling will result in more system jitter margin. In order to accommodate DC coupling with the upstream device, the AV_{DDI} power domain of the M21350/M21355 is electrically independent from all other power domains therefore allowing it to be tied to the V_{DD} of the upstream device. This is demonstrated in Figure 4-3 below.

Figure 4-3. M21350/M21355 AV_{DDI} Connected to the V_{DD} of the Upstream Device

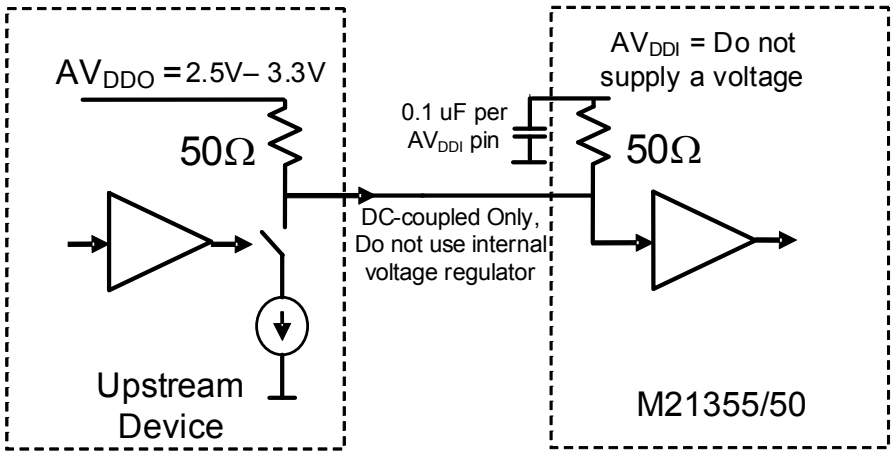


Alternatively and under certain conditions, the M21350/M21355 allows for the inputs to be self biased eliminating the need for an electrical connection between the supply voltages of the upstream device and M21350/M21355. This configuration offers the benefit of keeping the supply of the previous device and the power domain(s) of the M21350/M21355 completely isolated, while using DC coupling. AC coupling should not be used with the self bias interface. This self biasing scheme is demonstrated in Figure 4-4 below.

When using the M21350/M21355 in self biased mode, specific conditions must be met:

1. The self biased inputs must be DC coupled. No AC coupling is supported in self biased mode.
2. The AV_{DDO} of the upstream device must be 2.5 V or greater. AV_{DDO} levels 1.2 V and 1.8 V are not supported in this mode.
3. The common mode of the upstream signals must be greater than 600 mV.
4. Internal voltage regulators are disabled.
5. All inputs are configured in self biased mode. Combination of self biased and non-self biased is not supported.

Figure 4-4. Self Biasing the Input of M21350/M21355



NOTE:
1. For self-bias applications, AV_{DDI} is not to be supplied with any voltage level. The common mode voltage will be generated internally, please add a 0.1 µF capacitor per AV_{DDI} pin as shown in Figure 4-4.

A Loss of Signal (LOS) detector monitors each input and issues an alarm when the input signal level dips below the detection threshold set in register 06h. See Section 4.3 for more information on the LOS circuit.

In order to correct any duty cycle distortion (DCD) in the input signal, or any DC offset buildup in the internal signal path, a DC correction loop has been added. Programming reg0Dh bit 1 to a '1' will disable the DC correction loop for all inputs.

The M21350 includes four 4:1 multiplexers. These allow any one of the four input signals for each mux to be routed to its respective reclocker. By default, SDI0 is routed to SDO0, SDI4 is routed to SDO1, SDI8 is routed to SDO2 and SDI12 is routed to SDO3. The input to each reclocker channel can be set independently of any of the other channels using MUX control registers 07h and 08h.

Following the input buffers, the M21355 includes a 16x4 crosspoint switch. This switch allows any or all of the 16 input signals to be routed to any or all of the four reclocker channels. By default, SDI0 is routed to SDO0, SDI4 is routed to SDO1, SDI8 is routed to SDO2, and SDI12 is routed to SDO3. The input to each reclocker channel can be set independently of any of the other channels using Xpoint control registers 07h and 08h.

By default, only the selected inputs are powered up, with all other inputs powered down. When an input is powered down, its associated LOS circuitry is disabled. If required, all the other inputs can also be powered up by setting bit[3] in reg0Dh. This will allow a faster response if rapid input switching is required as there is no delay waiting for the circuitry to power-up and adjust to the input signal, but has the disadvantage of consuming more power.

4.3 LOS (Loss of Signal)

The M21350/M21355 has an integrated LOS circuit on each of its 16 high-speed inputs. This circuit monitors the input amplitude and if it falls below the detection threshold it asserts the corresponding LOS alarm bit in reg83h and 84h by setting this to a logic high. The alarm bits are latched and will need to be reset with the CLR_ALARMS, reg85h, by setting bit 0 to a high and back to a low. Hysteresis is built into the LOS circuit to avoid chattering. The LOS threshold can be set to a different level by using the bits[7:5] in reg06h, this changes the level on all 16 inputs.

By default, the LOS alarm mutes the signal from that particular input. Setting bit7 reg06h to a high will disable this feature.

4.4 High-Speed Output Description

There are four high-speed outputs available on the M21350/M21355. By default, each output provides the reclocked serial data from the associated reclocker channel. However, if desired, SDO3/SCLK may be configured to output the recovered serial clock from any of the other three reclocker channels by programming reg06h, bit 0 to '1'. The reclocker channel that is used for the recovered serial clock output is selected with bits [1:0] of reg0Bh.

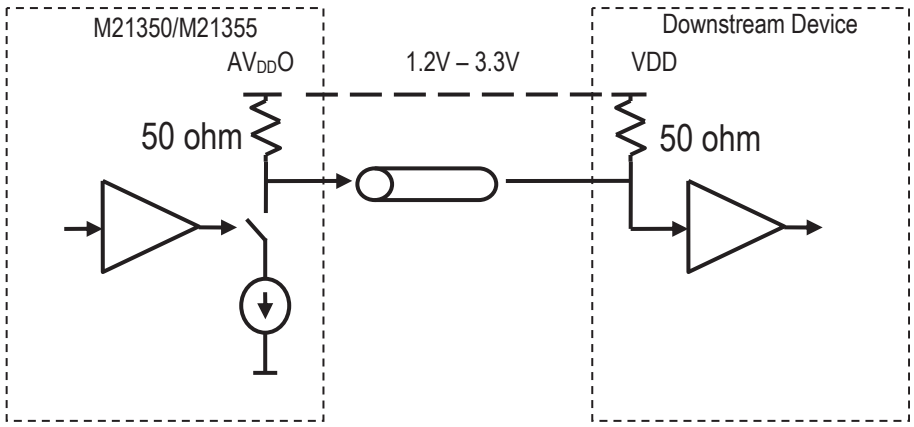
The M21350/M21355 features differential current mode logic (CML) drivers with integrated 50 Ω pull ups to AV_{DDO} for the output of each reclocker channel. AV_{DDO} may be supplied from any voltage ranging from 1.2 V to 3.3 V.

The differential, peak-to-peak, output swing for each CML driver is programmable and may be set to 600 mV_{PPD}, 800 mV_{PPD}, or 1200 mV_{PPD}. Please note that the 1200 mV_{PPD} output swing setting is only available when AV_{DDO} is supplied from a voltage of 1.8 V or greater. The swing setting may be programmed by writing to reg09h-reg0Bh.

In order to improve signal integrity when used in large systems, each output also comes equipped with programmable de-emphasis (DE) for FR4 trace. There are four settings for output de-emphasis: 0 dB (or no DE), 2 dB, 4 dB, and 6 dB. In serial control mode, the output de-emphasis level for each input may be set by programming the desired value to reg09h-reg0Bh. Alternatively, in hardware mode, the de-emphasis level for all of the outputs may be globally set through pin DE_CTRL (MF3). In hardware mode only the three settings of 0 dB, 4 dB, and 6 dB are available.

In most SDI applications, it is important to avoid AC coupled data interfaces between devices wherever possible. In addition to reducing the number of components, DC coupling will result in more system jitter margin. In order to accommodate DC coupling with the upstream device, the AV_{DDO} power domain of the M21350/M21355 is electrically independent from all other power domains therefore allowing it to be tied to the V_{DD} of the downstream device. This is demonstrated in Figure 4-5 below.

Figure 4-5. M21350/M21355 AV_{DDO} Connected to the V_{DD} of the Downstream Device



If AC coupling is desired or necessary, then the capacitor should be at least 10 µF.

4.5 Logic Signals

To allow interfacing to logic levels other than the 1.2 V core voltage, or any of the analog input and output supplies, the digital interface signals are referenced to DV_{DDIO} which is an isolated power domain. DV_{DDIO} may be supplied from any voltage ranging from 1.2 V to 3.3 V. Many digital control pins have three states, high (H), low (L), or floating, (F). In order to assert the F or floating state, the pin must be left unconnected or undriven.

4.6 Control Modes

The M21350/M21355 may be configured in four separate control modes. The control mode is determined by the setting of the MODE_SEL pin as shown in Table 4-1 below.

Table 4-1. Control Mode Setting

MODE_SEL	Control Mode
MODE_SEL = F	Hardware Control Mode (HIC)
MODE_SEL = H	Four-wire Serial Interface Control Mode (SIC4 or SPI)
MODE_SEL = L	Two-wire Serial Interface control Mode (SIC2 or I^2C)
	Memory Interface Configuration Mode (MIC) When the reclocker is configured through an external EEPROM

The MIC mode is a subset of the two-wire Interface mode and is initiated by writing to special reserved address when the device is set in two-wire Interface mode.

4.6.1 HIC Mode

Configuring the M21350/M21355 in hardware mode avoids the complication of adding a micro controller, but offers limited control options. When in hardware mode, the MF (Multi Function IO) pins are configured as shown in Table 4-2 below.

Table 4-2. MF Pin Configuration in Hardware Mode

MF	HIC Mode Pin Name	Function
MF2	IE_CTRL	Input trace equalization control for all SDI inputs H = 6 dB Input EQ F = 2 dB Input EQ L = 0 dB Input EQ
MF3	DE_CTRL	Output de-emphasis (DE) control for all SDO outputs H = 6 dB of output DE F = 4 dB of output DE L = 0 dB output DE
MF4	RC_BYPASS	Reclockers bypass control for all outputs L/F = Normal operation, Reclocker not bypassed H = Reclocker bypassed
MF5	SDO_DIS	SDO disable control for all outputs H = SDO disabled output logic high L/F = SDO enabled

In this mode, the xALARM pin is in status mode. In hardware mode, only the default routing of input SDI0 to the reclocker is available.

4.6.2 Four-Wire Digital Interface

In this mode, a four-wire serial interface is used to program the device's internal registers, configuring the operation of the M21350/M21355. When in SIC4 mode, **MF**[0:3] pins comprise the four-wire bus as shown in Table 4-3 below.

Table 4-3. MF Pin Configuration in Four-wire Interface Mode

MF	SIC4 Mode Pin Name	Function
MF0	SCLK	Serial clock input
MF1	SO	Serial data output
MF2	SI	Serial Data input
MF3	xCS	Chip Select (active low)

The interface shifts data in from the external controller on the rising edge of SCLK. The serial I/O operation is gated by xCS. Data is shifted in to M2135x from the Host (Master) to SI on the falling edge of SCLK, and shifted out through SO on the rising edge of SCLK. To write to a register, an 18-bit input needs to be shifted on SI, consisting of the first bit (Start Bit, SB = 1), the second bit (Operation Bit, OP = 0 for write), the 8-bit address (MSB first) and the 8-bit data (MSB first).

Figure 4-6. 4-wire Serial Digital Interface

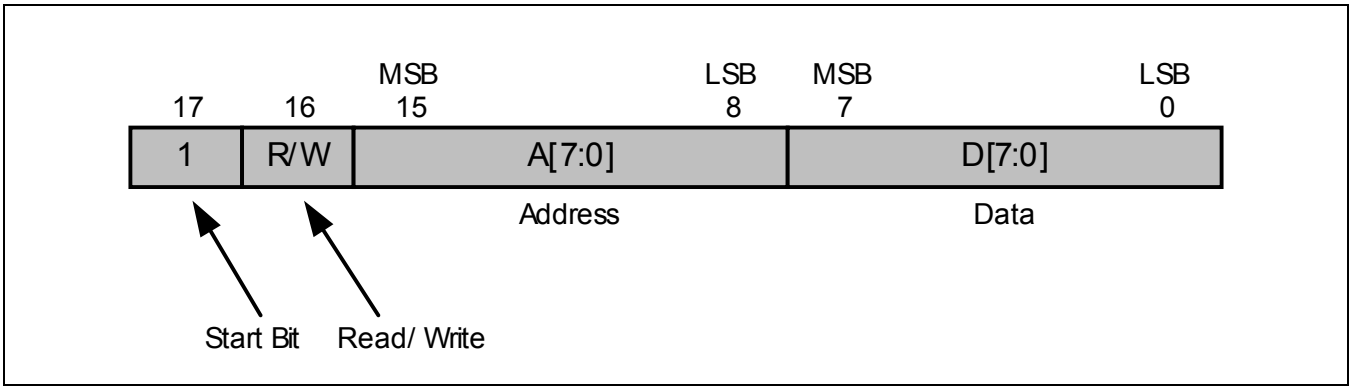


Figure 4-7 and Figure 4-8 illustrate the Serial Write Mode. To initiate a Write sequence, "**xCS**" goes low before the falling edge of "**SCLK.**" On each falling edge of the clock, the 18 bits consisting of the SB = 1, OP = 0, ADDR, and DATA, are latched into the input shift register through "**SI.**" The rising edge of "**xCS**" must occur before the falling edge of "**SCLK**" for the last bit. Upon receipt of the last bit, one additional cycle of "**SCLK**" is necessary before DATA transfers from the input shift register to the addressed register.

The 4-wire serial interface supports multiple consecutive writes. In this case, the address header is not needed and each additional 8 bits of data will be written into consecutive addresses. If consecutive read/write cycles are being performed, it is not necessary to insert an extra clock cycle between read/write cycles, however one extra clock cycle is needed after the last data bit of the last read/write cycle.

Figure 4-9 and Figure 4-10 illustrate the Serial Read mode to initiate a read sequence. "**xCS**" goes low before the falling edge of "**SCLK.**" On each falling edge of "**SCLK**", the 10 bits consisting of SB = 1, OP = 1, and the 8-bit ADDR are written to the serial input shift register and copied to the serial output shift register. Data is then read back to the master, through pin SO on the next rising edge after the address LSB. SO is initially forced to 0 by the M2135x, for one bit period, the 8 bits data are then shifted out. On a Write cycle, any bits that follow the expected number of bits are ignored, and only the first 16 bits following SB and OP are used. An invalid SB or OP renders the operation undefined. The falling edge of "**xCS**" always resets the serial operation for a new Read or Write cycle.

Figure 4-7. 4-wire Serial Sequential WRITE Timing Diagram

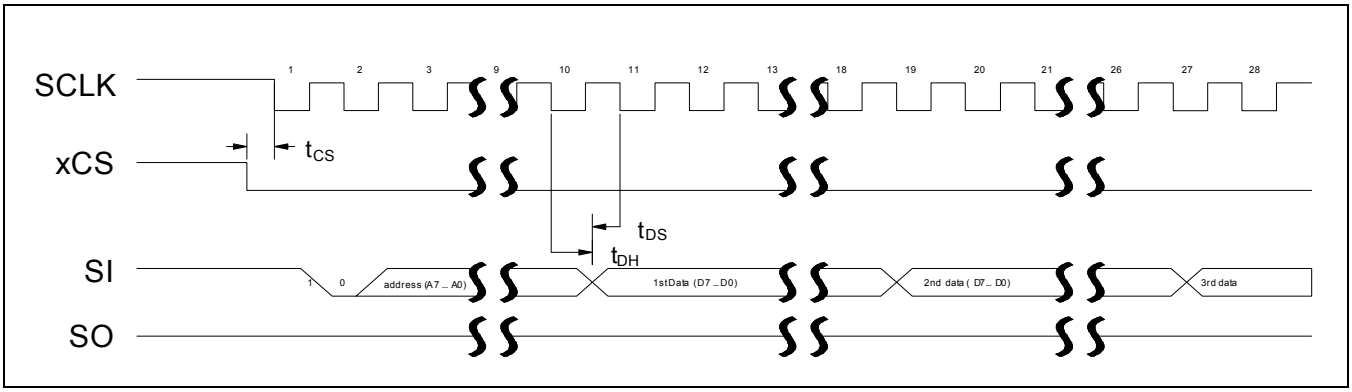


Figure 4-8. 4-wire Random WRITE Timing Diagram

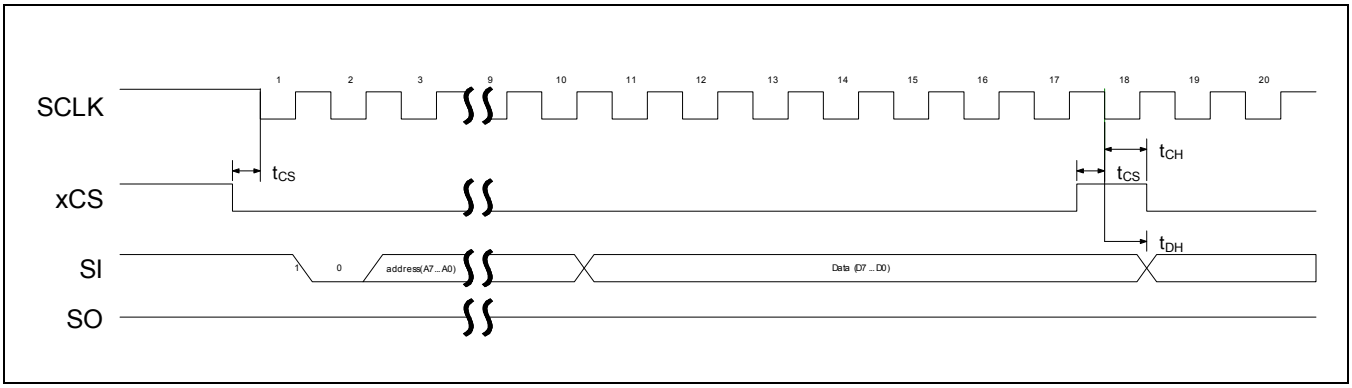


Figure 4-9. 4-wire Sequential READ Timing Diagram

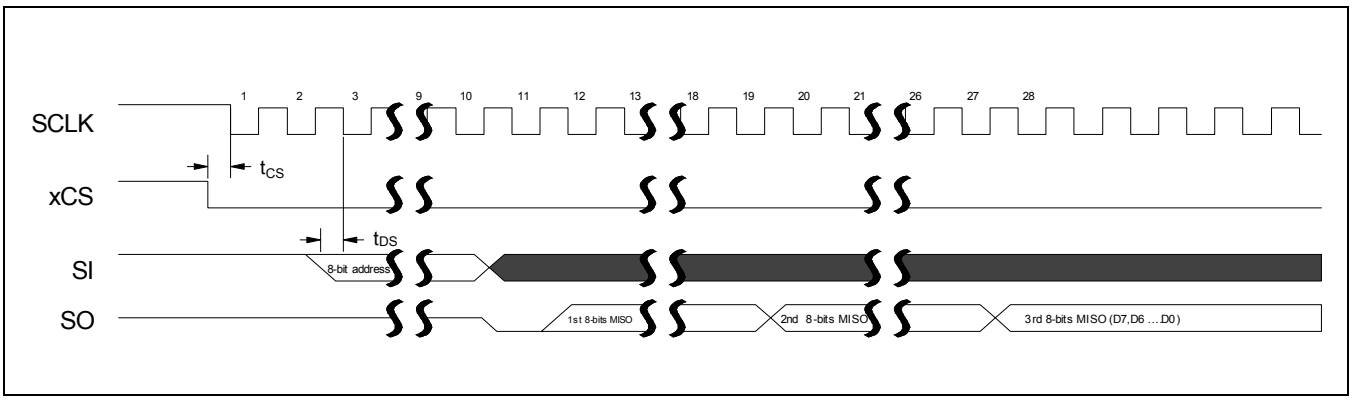


Figure 4-10. 4-wire Random READ Timing Diagram

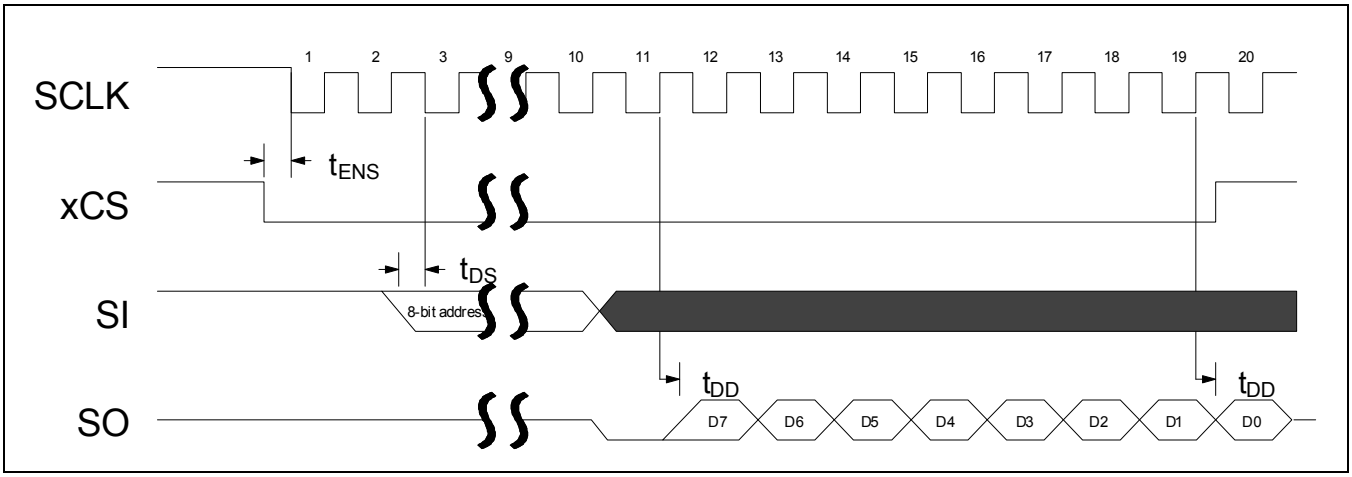


Table 4-4. Four-wire Interface Timing

Timing Symbol	Description	Min	Max	Unit
Tds	Data set-up time	2.5	—	ns
Tdh	Data hold time	2.5	—	ns
Tcs	xCS set-up time	2.5	—	ns
Tch	xCS hold time	2.5	—	ns
Tfreq, write	Four-wire interface write clock frequency	—	100	MHz
Tfreq, read	Four-wire interface read clock frequency DV_{DDIO}=1.2 V, 1.8 V Maximum load capacitance 10 pF	—	25	MHz
	Four-wire interface read clock frequency DV_{DDIO}=2.5 V, 3.3 V Maximum load capacitance 30 pF	—	50	MHz
T_{DUTY}	SCLK duty cycle	40	60	%
Tdd	Four-wire interface read data output delay DV_{DDIO}=1.2 V, 1.8 V Maximum load capacitance 10 pF	2	17	ns
	Four-wire interface read data output delay DV_{DDIO}=2.5 V, 3.3 V Maximum load capacitance 30 pF	2	9	ns

4.6.3 Two-wire Interface Mode (SIC2)

In this mode a two-wire serial interface is used to program the device's internal registers, configuring the operation of the M21350/M21355. When in SIC2 mode, MF[0:5] pins are configured as shown below.

Table 4-5. MF Pin Configuration in Two-wire Interface Mode

MF	SIC4 Mode Pin Name	Function
MF0	SCL	Clock input from master host
MF1	SDA	Serial data input/output
MF2	ADD0	Address bit 0
MF3	ADD1	Address bit 1
MF4	ADD2	Address bit 2
MF5	ADD3	Address bit 3

Each device has an individual address and is addressed using an address byte, which is latched upon Power-On-Reset (POR). In this mode, the M21350/M21355 is an I^2C-compatible slave device that can operate at 100 kHz and 400 kHz for all allowed voltages seen at the DV_{DDIO} pin.

The M21350/M21355 allows for forty different addresses to be programmed using the inputs ADD[3:0]; these inputs have three states, low (L), high (H) and floating (F). The slave addresses are from 21h to 48h.

Table 4-6. M21350/M21355 2-Wire Interface Address Map

Dec Add	Hex Add	Bin Add	Pin Setting				Function
			ADD3	ADD2	ADD1	ADD0	
32	20	010 0000b	L	L	L	L	EEPROM only, Address 50h
32	20	010 0000b	L	L	L	H	EEPROM only, Address 51h
32	20	010 0000b	L	L	H	L	EEPROM only, Address 52h
32	20	010 0000b	L	L	H	H	EEPROM only, Address 53h
33	21	010 0001b	L	H	L	L	Slave 1
34	22	010 0010b	L	H	L	H	Slave 2
35	23	010 0011b	L	H	L	F	Slave 3
36	24	010 0100 b	L	H	H	L	Slave 4
37	25	010 0101b	L	H	H	H	Slave 5
38	26	010 0110b	L	H	H	F	Slave 6
39	27	010 0111b	L	H	F	L	Slave 7
40	28	010 1000 b	L	H	F	H	Slave 8
41	29	010 1001b	L	H	F	F	Slave 9
42	2A	010 1010b	L	F	L	L	Slave 10

Table 4-6. M21350/M21355 2-Wire Interface Address Map

Dec Add	Hex Add	Bin Add	Pin Setting				Function
			ADD3	ADD2	ADD1	ADD0	
43	2B	010 1011b	L	F	L	H	Slave 11
44	2C	010 1100b	L	F	L	F	Slave 12
45	2D	010 1101b	L	F	H	L	Slave 13
46	2E	010 1110b	L	F	H	H	Slave 14
47	2F	010 1111b	L	F	H	F	Slave 15
48	30	011 0000 b	L	F	F	L	Slave 16
49	31	011 0001 b	L	F	F	H	Slave 17
50	32	011 0010 b	L	F	F	F	Slave 18
51	33	011 0011 b	F	L	L	L	Slave 19
52	34	011 0100 b	F	L	L	H	Slave 20
53	35	011 0101 b	F	L	L	F	Slave 21
54	36	011 0110 b	F	L	H	L	Slave 22
55	37	011 0111 b	F	L	H	H	Slave 23
56	38	011 1000 b	F	L	H	F	Slave 24
57	39	011 1001b	F	L	F	L	Slave 25
58	3A	011 1010b	F	L	F	H	Slave 26
59	3B	011 1011b	F	L	F	F	Slave 27
60	3C	011 1100b	F	H	L	L	Slave 28
61	3D	011 1101b	F	H	L	H	Slave 29
62	3E	011 1110b	F	H	L	F	Slave 30
63	3F	011 1111b	F	H	H	L	Slave 31
64	40	100 0000b	F	H	H	H	Slave 32
65	41	100 0001b	F	H	H	F	Slave 33
66	42	100 0010b	F	H	F	L	Slave 34
67	43	100 0011b	F	H	F	H	Slave 35
68	44	100 0100 b	F	H	F	F	Slave 36
69	45	100 0101b	F	F	L	L	Slave 37
70	46	100 0110b	F	F	L	H	Slave 38
71	47	100 0111b	F	F	L	F	Slave 39
72	48	100 1000 b	F	F	H	L	Slave 40

Table 4-7. Supported AT24C01 EEPROM Addresses

Dec Add	Hex Add	Bin Add	Fixed by EEPROM				Address Pin Setting		
			ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
80	50	010 0000b	H	L	H	L	L	L	L
81	51	010 0001b	H	L	H	L	L	L	H
82	52	010 0010b	H	L	H	L	L	H	L
83	53	010 0011b	H	L	H	L	L	H	H

Figure 4-11 illustrates typical waveforms and timing seen at SCL and SDA for a read and write operation.

Figure 4-11. Two-wire Interface Timing Diagram

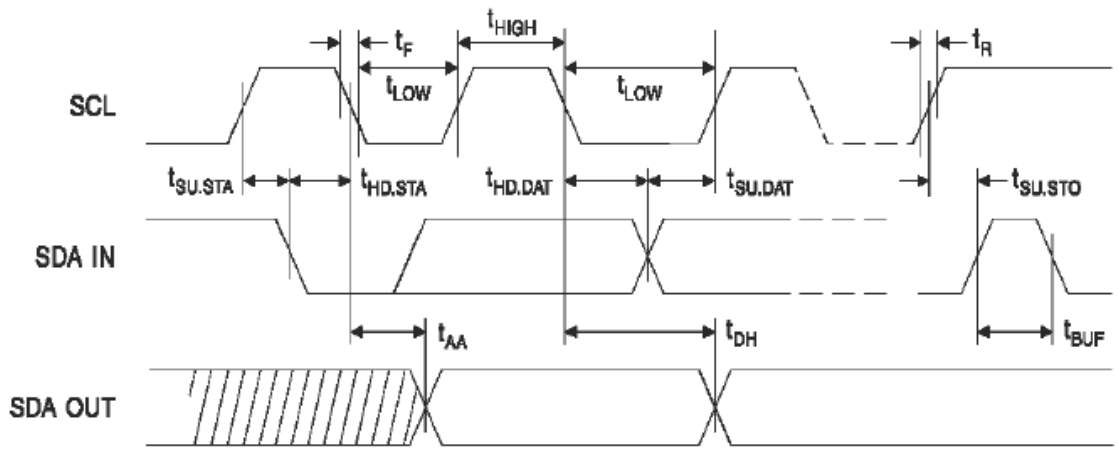


Table 4-8. Two-wire Interface Timing Specifications (Standard Mode or Fast Mode)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_{SCL}	Clock Frequency, SCL	—	—	400	kHz
t_{LOW}	Clock Pulse Width Low	1.3	—	—	µs
t_{HIGH}	Clock Pulse Width High	1	—	—	µs
t_{AA}	Clock Low to Data Out Valid	0.05	—	0.9	µs
t_{HDSTA}	Start Hold Time	200	—	—	ns
t_{SUSTA}	Start Set-up Time	200	—	—	ns
t_{HDDAT}	Data In Hold Time	0	—	—	ns
t_{SUDAT}	Data In Set-up Time	100	—	—	ns

Table 4-8. Two-wire Interface Timing Specifications (Standard Mode or Fast Mode)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{SUSTO}	Stop Set-up Time	200	—	—	ns
t_{DH}	Data Out Hold Time	50	—	—	ns

Notes:

For the two-wire interface both SDA and SCL are able to drive 500 pF at 100 kHz and 250 pF at 400 kHz with 1 kΩ pull-up resistor.

4.6.4 MIC Mode Operation

In this mode, the reclocker is initialized from an EEPROM. To use this mode, the EEPROM must be programmed with the register data required. The I^2C address of the memory can be 50h, 51h, 52h or 53h; the reclocker loads its register contents from this address.

This mode is enabled when the I^2C mode is set and address 20h has been hardwired on the address pins. When the reclocker locates the memory at one of the above addresses, it sets itself into I^2C quasi-master mode. It will then load its registers from the EEPROM. Addresses 00h to 19h should be used when only one reclocker is used. Register 0Fh contains the number of slave reclockers, if there are none this is set to 0, the maximum number of slaves is 39 (40 including the master).

Once the master has finished the task of downloading the registers, it will revert to slave mode at address 20h and can be accessed for debugging purposes.

Note that when using MIC power mode supply, ramp time is important. The EEPROM should be powered from the same supply as DV_{DDIO} and the ramp up of the supply should be < 100 ms. If the ramp time is not met, the reclocker I^2C will time-out before the EEPROM is ready to receive serial data.

The target EEPROM is the AT24C01 or equivalent.

If there is more than one reclocker to be programmed, a checksum is used to confirm that the data is correct. This works as follows:

1. The slave reclocker sums all registers from 00 to 1Ah, then truncates this to leave the 8 LSB bits. This is then compared with the value 2Eh. If it is not equal, then the registers are not loaded and it returns to the default value. It will then try up to 512 times before timing out. When the checksum is equal to 2Eh, the registers are loaded with the EEPROM settings.

2. To make the checksum = 2Eh, register 1Ah must be programmed with the 8 LSBs from the following calculation:

Reg 1Ah = 2Eh - (sum of registers 0 to 19h)

4.7 Reclocker Operation

4.7.1 Clock Recovery

This block generates a serial clock signal at a frequency close to the data rate. The clock signal is generated by a phased locked loop (PLL) which uses the 27 MHz input clock as a reference.

The presence of the reference clock is monitored by the device. An alarm bit (NOREF) in reg88h is set to '1' when a suitable reference clock is not present. Once the PLL has locked to the reference clock, the REFLOL bit in the same register, will be set to '0'. A value of '1' in this bit indicates that the PLL has not locked to the input reference clock.

The frequency locked clock signal is supplied to the phase lock block. In this block, a bang-bang phase comparator is used to make fine adjustments to the phase and frequency of the clock, aligning it with the incoming serial data.

Once the clock signal is phase and frequency aligned with the serial data stream, it is used to re-time the data, producing a clean data signal that is provided at the output of the device. The phase lock block uses an integrated, programmable loop filter. The bandwidth of the phase lock block may be programmed using the BW[2:0] bits in register 16h. A wide bandwidth allows more jitter from the input serial data stream to be transferred to the output. Alternatively, a low bandwidth setting causes the loop to reject more of the incoming data stream's jitter.

Furthermore, since the phase lock block uses a non-linear, bang-bang loop, the bandwidth of the system is inversely proportional to the incoming data stream's jitter. This offers several advantages over linear PLLs. With higher input jitter, the loop automatically reduces the bandwidth, causing higher jitter attenuation. Conversely, a data stream with lower jitter will cause the loop bandwidth to be widened allowing it to correct for small variations correctly. Note that bandwidth settings greater than 2x will increase output jitter.

When the recovered serial clock output is enabled, the clock alignment to the SDO0 data output will be typically 60 ps, where the falling edge of the clock lags the transition edge of the SDO0 signal.

4.7.2 Automatic Rate Detection

Each reclocker channel features an Automatic Rate Detector (ARD) circuit that monitors the input signal rate and automatically sets the reclocker to the correct video rate. The data rate determined by the ARD block may be read from bits 1:0 in register 89h as shown in Table 4-9.

Table 4-9. Reclocker Rate Detection

Reg 89h Bits RATEn [1:0] *	Function
00b	Reclocker unlocked
01b	SD rate detected
10b	HD rate detected
11b	3G rate detected
NOTES: * where n = channel number	

As an alternative to the ARD, the user may manually set the reclocker to the desired data rate by programming bits 3:2 in registers 12h and 13h to the desired values as shown in Table 4-10.

Table 4-10. Reclocker Data Rate Selection

Reg12h, Reg13h Bits RATEn [1:0]	Function
00b	ARD Enabled
01b	Manual SD rate programmed
10b	Manual HD rate programmed
11b	Manual 3G rate programmed
NOTES: 1. n = Reclocker channel being programmed.	

When in auto-bypass mode, if the ARD cannot determine the rate of the input data stream, it will switch the reclocker into bypass mode. This allows a data rate other than those specified to be passed through the reclocker. The auto-bypass mode may be disabled for each reclocker independently, through reg14h.

4.7.3 Lock Detection

Several circuits monitor each reclocker for Loss of Lock. One in particular compares the recovered serial clock to one derived from the reference clock. If the clock frequency is within ±2000 ppm of the serial data frequency, the Loss of Lock (LOL) alarm will be set to '0'. If the clock is outside of this window, then the LOL alarm will be asserted to '1'.

The LOL bit for each reclocker channel can be read in bits [3:0] in reg88h.

4.7.4 Reference Clock

The M21350/M21355 can operate from a crystal or an external reference clock, but better jitter results are obtained with a crystal. If using an external reference clock then this should be a 27 MHz clock with a frequency accuracy of ±100 ppm or better. Reference clock jitter is important and care must be taken to supply a low jitter reference clock to the reclocker of 1 ps RMS or less. The reference clock may either be from an external CMOS clock oscillator or an external parallel resonance crystal. If a low jitter 27 MHz signal is already available on the board then it may be used. Due to the higher jitter, a genlocked 27 MHz clock is likely not suitable for this device. When supplying an external clock signal, it is recommended to use AC coupling, through a 0.1 µF capacitor. Refer to Table 1-6 for recommended input levels.

4.8 SD/xHD[0:3] Outputs

When any of the reclocker channels is locked to the input data, the associated SD/xHD output indicates whether an SD or HD rate is detected. When a 3G rate is being received, the output will indicate HD. This output is designed to be connected to the slew rate control on a downstream cable driver.

The SD/xHD pins have two available modes as shown in Table 4-11. These are controlled by the SDALG bit, reg 18h[5], by default this is a 0 and only goes high when the reclocker is locked to a 270 Mbps input signal. This mode

sets the fast edge on the cable driver and allows for any signal in the reclockers data range to be bypassed. If the slow edge is set, any signal above 540 Mbps would be distorted by the slow edge on the cable driver.

When SDALG is high it also sets the SD/xHD pin high when the reclocker is unlocked. This is used when the user requires other SD rates such as 143 Mbps and 360 Mbps to be output from the cable driver with the slow SD edge when the reclocker is not locked.

Table 4-11. SD/xHD Output Algorithm

Rate (Gbps)	SD/xHD Pin	
	SDALG Bit = 0	SDALG Bit = 1
0.270	H	H
1485/1483.5	L	L
2.97/2.967	L	L
unlocked	L	H

4.9 xALARM

The xALARM output pin is provided so the user can monitor alarm activity on the reclocker. The output is open drain as shown in Figure 3-10. The xALARM output has two modes of operation, set by the ST/xINT bit (bit3, reg 0Eh): status mode and interrupt mode. Table 4-12 shows the reclocker alarms and their function. The assertion of any of the alarms in Table 4-12 on any of the four reclocker channels, will trigger xALARM.

Table 4-12. Reclocker Alarm Function

Alarm	Function
LOS	Asserted when input signal goes below LOS threshold as set in register 06h
LOL	Asserted when reclocker cannot lock to the incoming data
NOREF	Asserted when no input reference is present at the reference clock inputs
REFLOL	Asserted when frequency lock block cannot lock to the reference clock input

4.9.1 Status Mode

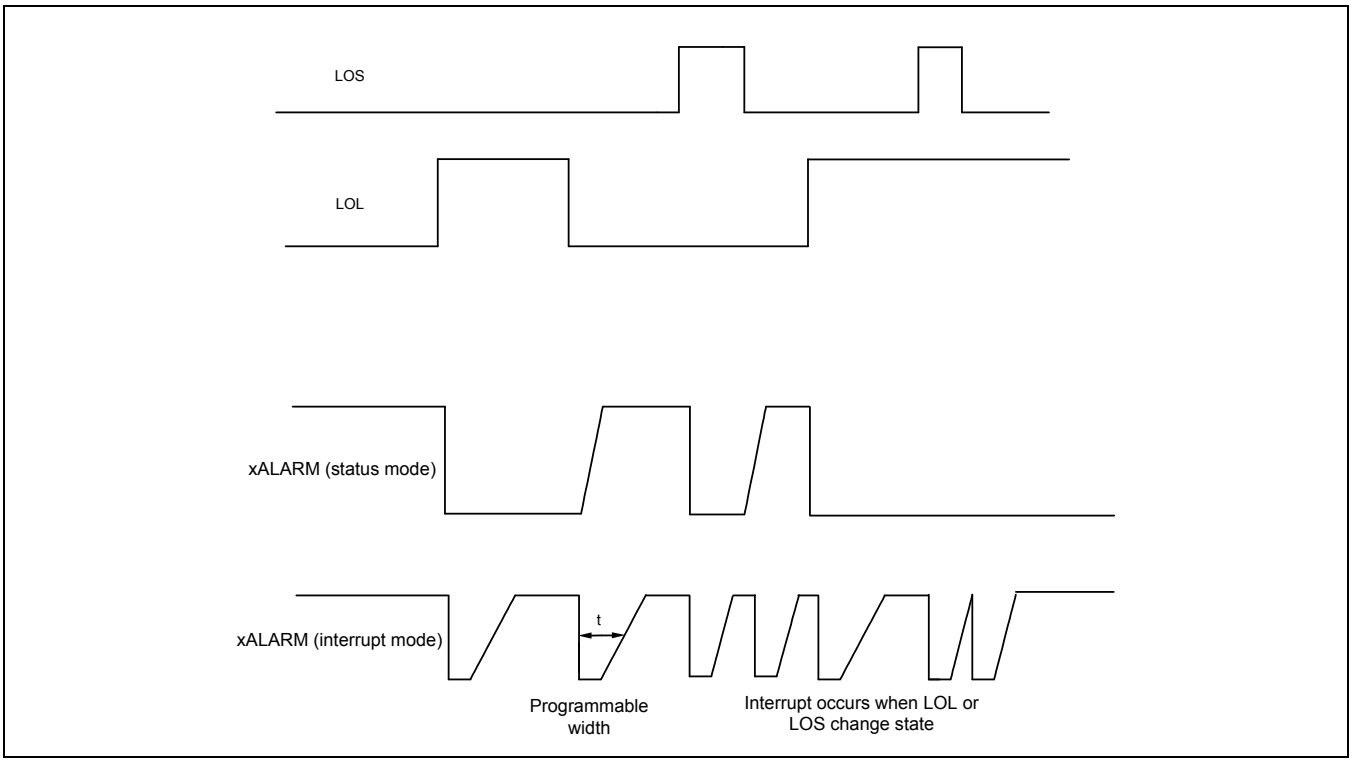
In this mode the xAlarm pin goes low if any of the internal alarm flags are asserted. The xALARM will only go back to high low when the offending alarm is de-asserted, see Figure 4-12. This mode is useful for driving an LED alarm indicator.

4.9.2 Interrupt Mode

In this mode the Alarm goes low on assertion of any of the internal alarm flags, as with Status, but the output only stays low for a fixed period (see Figure 4-12). This period is set by the Interrupt Control register (0Eh) by default this is 0 and that corresponds to 20 ns, the maximum period is 2.560 µs, when INT[3:0] is set to Fh. This mode is designed to be connected to a microprocessor's interrupt pin. After the interrupt occurs, the microprocessor can

read the reclocker's alarm registers to determine which alarm was asserted. A 10 kΩ pull up to DV_{DDIO} should be added to the xALARM output to achieve the correct pulse widths.

Figure 4-12. xALARM-Output Status and Interrupt Modes



4.9.3 Reading Register Alarm Bits

The LOS and LOL alarm bits are latched when asserted, after reading they should be cleared using the CLRALRM bit in register 85h. This bit needs to be set to '1' to reset the alarms, it should then be reset to a '0' to re-enable normal alarm operation.

4.10 Internal Regulator

If a 1.2 V supply is not available locally, then the internal regulator can be used to create this domain from AV_{DDI} and DV_{DDIO}. Setting the xREG_EN pin LOW, enables the internal regulator. This regulator generates a 1.2 V domain at pins AV_{DD} and DV_{DD}. See Figures Figure 4-13 to Figure 4-15 for the three different supply configurations. Note that unless specified, the decoupling capacitors should be at least 100 nF.

Figure 4-13. All Power Pins Connected to 1.2 V; Internal Regulators Not Used

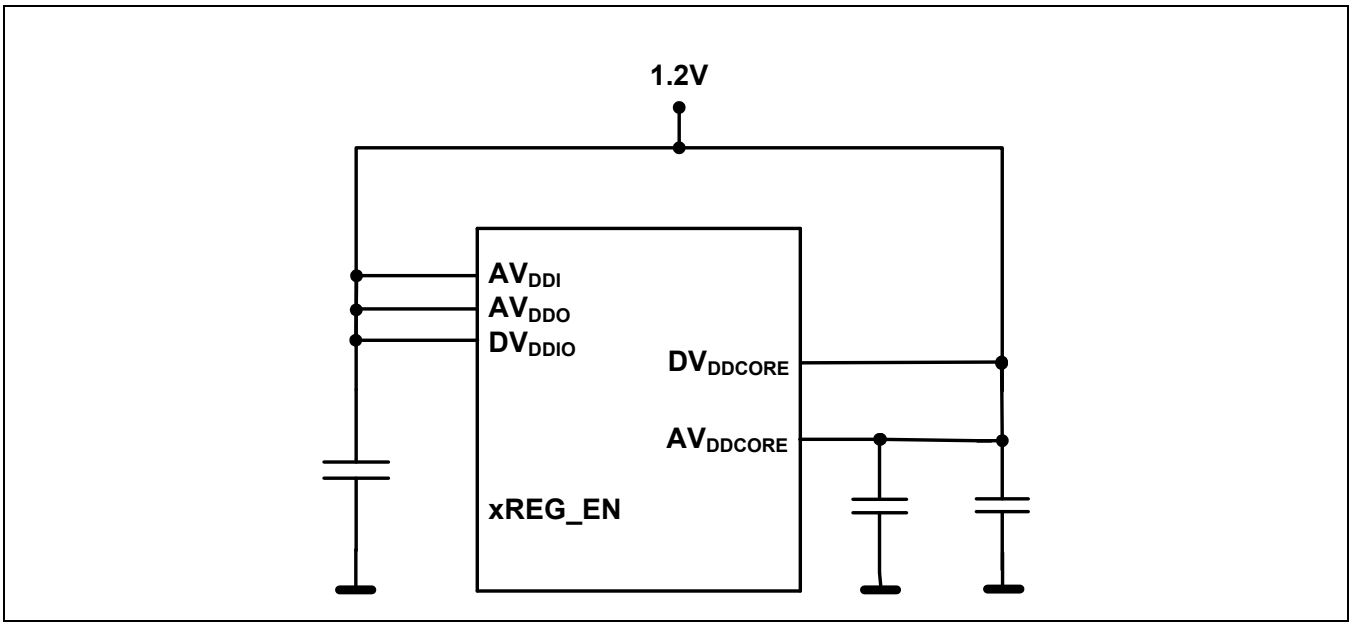


Figure 4-14. AV_{DDI}, AV_{DDO}, and DV_{DDIO} Connected to a Supply at 1.8 V or 3.3 V; 1.2 V is Supplied to AV_{DD} and DV_{DD};Internal Regulator not Used

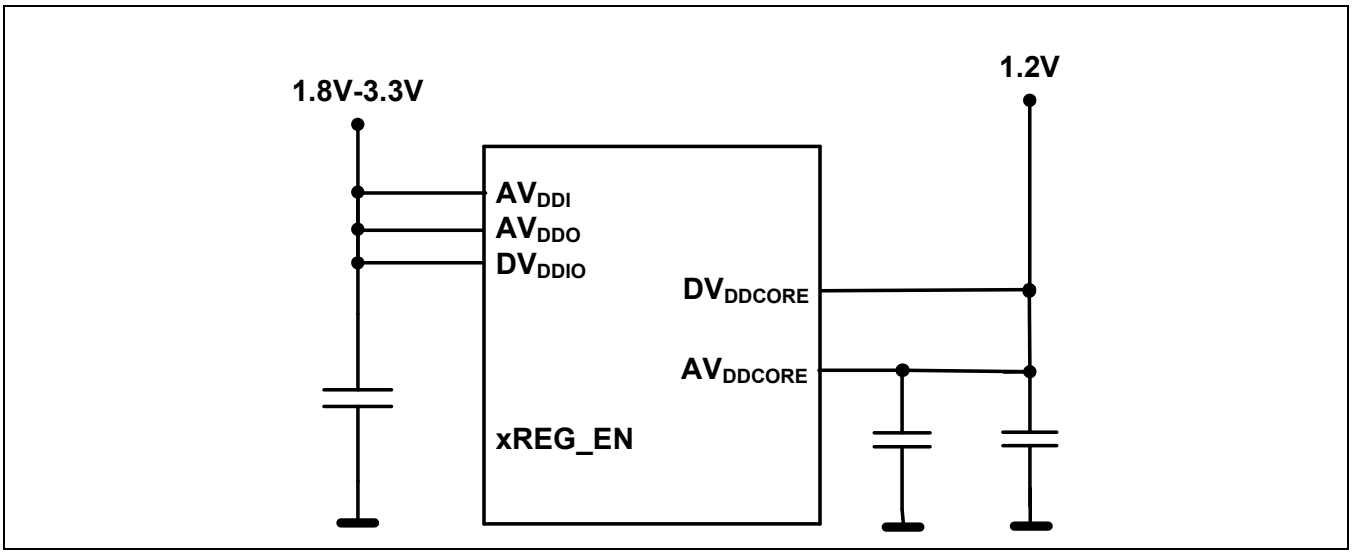
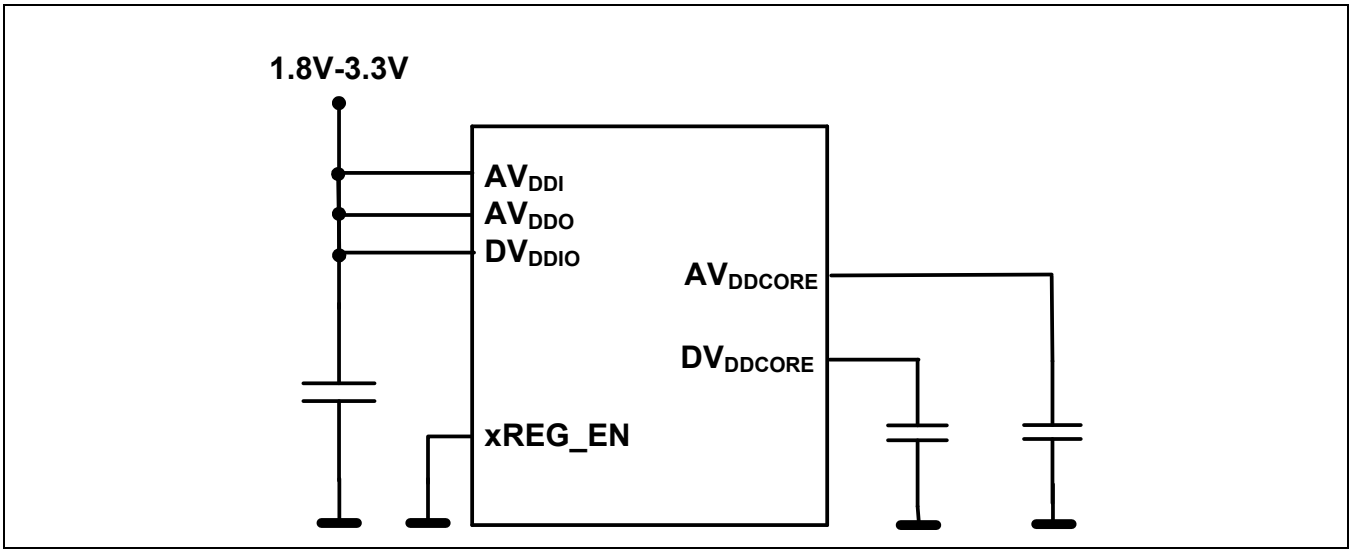


Figure 4-15. AV_{DDI}, AV_{DDO}, and DV_{DDIO} Connected to a Supply at 1.8 V or 3.3 V; Internal Regulator Generates On-Chip 1.2 V



Note: In order to simplify the diagrams, AV_{DDI}, AV_{DDO}, and DV_{DDIO} are shown to be shorted together. In practice, they may all be separated and connected to different supply domains if desired.

AV_{DDO} is sensitive to noise and therefore should be filtered through a ferrite bead, with a 10 nF ceramic capacitor adjacent to each AV_{DDO} pin.

5.0 Control Registers Map and Descriptions

Table 5-1. Register Map

Addr	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
Input Configuration											
00h	Input EQ Config 0	IE3[1]	IE3[0]	IE2[1]	IE2[0]	IE1[1]	IE1[0]	IE0[1]	IE0[0]	00h	R/W
01h	Input EQ Config 1	IE7[1]	IE7[0]	IE6[1]	IE6[0]	IE5[1]	IE5[0]	IE4[1]	IE4[0]	00h	R/W
02h	Input EQ Config 2	IE11[1]	IE11[0]	IE10[1]	IE10[0]	IE9[1]	IE9[0]	IE8[1]	IE8[0]	00h	R/W
03h	Input EQ Config 3	IE15[1]	IE15[0]	IE14[1]	IE14[0]	IE13[1]	IE13[0]	IE12[1]	IE12[0]	00h	R/W
04h	Input Polarity Flip 0	POL7	POL6	POL5	POL4	POL3	POL2	POL1	POL0	00h	R/W
05h	Input Polarity Flip 1	POL15	POL14	POL13	POL12	POL11	POL10	POL9	POL8	00h	R/W
06h	LOS Config	LVL[2]	LVL[1]	LVL[0]	F_LOS	NVRSQ	SQPOL	RSVD	CLK_EN	20h	R/W
07h	MUX CTRL 0 (M21350)	RSVD	RSVD	MUX1[1]	MUX 1[0]	RSVD	RSVD	MUX 0[1]	MUX 0[0]	40h	R/W
07h	XPT CTRL 0 (M21355)	XPTOUT1[3]	XPTOUT1[2]	XPTOUT1[1]	XPTOUT1[0]	XPTOUT0[3]	XPTOUT0[2]	XPTOUT0[1]	XPTOUT0[0]	40h	R/W
08h	MUX CTRL 1 (M21350)	RSVD	RSVD	MUX 3[1]	MUX 3[0]	RSVD	RSVD	MUX 2[1]	MUX 2[0]	C8h	R/W
08h	XPT CTRL1 (M21355)	XPTOUT3[3]	XPTOUT3[2]	XPTOUT3[1]	XPTOUT3[0]	XPTOUT2[3]	XPTOUT2[2]	XPTOUT2[1]	XPTOUT2[0]	C8h	R/W
Output Configuration											
09h	Output CTRL 0	LVL1[1]	LVVL1[0]	DE1[1]	DE1[0]	LVL0[1]	LVL0[0]	DE0[1]	DE0[0]	88h	R/W
0Ah	Output CTRL 1	LVL3[1]	LVL3[0]	DE3[1]	DE3[0]	LVL2[1]	LVLI2[0]	DE2[1]	DE2[0]	88h	R/W
0Bh	CLK_Out and Output_Mute	MUTE[3]	MUTE[2]	MUTE[1]	MUTE[0]	CLK_LVL[1]	CLK_LVL[0]	CLK_SEL[1]	CLK_SEL[0]	08h	R/W
0Ch	Reserved	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	02h	R/W
0Dh	GBL CTRL	RSVD	RSVD	RSVD	RSVD	FORCESDION	RSVD	OFFLOOP	PDALL	00h	R/W
0Eh	Interrupt CTRL	RSVD	RSVD	RSVD	RSVD	INT[3]	INT[2]	INT[1]	INT[0]	00h	R/W
0Fh	MicReg	RSVD	RSVD	MICDEV	MICDEV	MICDEV	MICDEV	MICDEV	MICDEV	00h	R/W
Reclocker Configuration											
10h	Reserved	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	30h	R/W
11h	Group Rate CTRL	RSVD	RSVD	RSVD	RSVD	GPMODE	GRATE[1]	GRATE[0]	GBYPASS GPD	00h	R/W
12h	Indv Rate CTRL 0	RATE1[1]	RATE1[0]	BYPASS1	PDOWN1	RATE0[1]	RATE0[0]	BYPASS0	PDOWN0	00h	R/W
13h	Indv Rate CTRL 1	RATE3[1]	RATE3[0]	BYPASS3	PDOWN3	RATE2[1]	RATE2[0]	BYPASS2	PDOWN2	00h	R/W
14h	AUTOBYPASSDIS	RSVD	RSVD	RSVD	RSVD	BYPDIS3	BYPDIS2	BYPDIS1	BYPDIS0	00h	R/W

Table 5-1. Register Map

Addr	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
15h	Reserved	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	00h	R/W
16h	Reclocker BW CTRL	RSVD	BW[2]	BW[1]	BW[0]	RSVD	RSVD	RSVD	RSVD	20h	R/W
17h	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	C0h	R/W
18h	RSVD	RSVD	RSVD	SDALG	RSVD	RSVD	RSVD	RSVD	RSVD	00h	R/W
19h	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	03h	R/W
Checksum for Memory Interface Configuration											
1Ah	CHECKSUM	CHKSUM	CHKSUM	CHKSUM	CHKSUM	CHKSUM	CHKSUM	CHKSUM	CHKSUM	55h	R/W
Status/Monitoring Registers											
80h	MASTER RESET	RST	RST	RST	RST	RST	RST	RST	RST	00h	R/W
81h	CHIP ID (M21350)	ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	09h	R
81h	CHIP ID (M21355)	ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	08h	R
82h	CHIP REV	REV[7]	REV [6]	REV [5]	REV [4]	REV [3]	REV [2]	REV [1]	REV [0]	03h	R
83h	LOS STATUS 0	LOS7	LOS6	LOS5	LOS4	LOS3	LOS2	LOS1	LOS0	00h	R
84h	LOS STATUS 1	LOS15	LOS14	LOS13	LOS12	LOS11	LOS10	LOS9	LOS8	00h	R
85h	CLEAR	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	SOFTRST	CLRALARMS	00h	R/W
87h	CHECKSUM RESULT	CHKRESULT	CHKRESULT	CHKRESULT	CHKRESULT	CHKRESULT	CHKRESULT	CHKRESULT	CHKRESULT	00h	R/W
88h	Reclocker ALARMS	RSVD	RSVD	NOREF	REFLOL	LOL	LOL	LOL	LOL	00h	R
89h	Reclocker RATE DETECT	RATE3[1]	RATE3[0]	RATE2[1]	RATE2[0]	RATE1[1]	RATE1[0]	RATE0[1]	RATE0[0]	00h	R

NOTE:

1. RSVD are reserved bits that should never be changed from the default level.

5.1 Registers Description

5.1.1 Input/Output Configuration

Register Address: 00h
Default: 00h
Register Name: Input EQ Config 0
Description: Select input equalization level, input 0

Bit	Bit Description	Default	R/W
7:6	00b: SDI 3, Input equalization disabled 01b: SDI 3, Small input equalization level 10b: SDI 3, Medium input equalization level 11b: SDI 3, Large input equalization level	00b	R/W
5:4	00b: SDI 2, Input equalization disabled 01b: SDI 2, Small input equalization level 10b: SDI 2, Medium input equalization level 11b: SDI 2, Large input equalization level	00b	R/W
3:2	00b: SDI 1, Input equalization disabled 01b: SDI 1, Small input equalization level 10b: SDI 1, Medium input equalization level 11b: SDI 1, Large input equalization level	00b	R/W
1:0	00b: SDI 0, Input equalization disabled 01b: SDI 0, Small input equalization level 10b: SDI 0, Medium input equalization level 11b: SDI 0, Large input equalization level	00b	R/W

Register Address: 01h
Default: 00h
Register Name: Input EQ Config 1
Description: Select input equalization level, input 1

Bit	Bit Description	Default	R/W
7:6	00b: SDI 7, Input equalization disabled 01b: SDI 7, Small input equalization level 10b: SDI 7, Medium input equalization level 11b: SDI 7, Large input equalization level	00b	R/W
5:4	00b: SDI 6, Input equalization disabled 01b: SDI 6, Small input equalization level 10b: SDI 6, Medium input equalization level 11b: SDI 6, Large input equalization level	00b	R/W
3:2	00b: SDI 5, Input equalization disabled 01b: SDI 5, Small input equalization level 10b: SDI 5, Medium input equalization level 11b: SDI 5, Large input equalization level	00b	R/W
1:0	00b: SDI 4, Input equalization disabled 01b: SDI 4, Small input equalization level 10b: SDI 4, Medium input equalization level 11b: SDI 4, Large input equalization level	00b	R/W

Register Address: 02h
Default: 00h
Register Name: Input EQ Config 2
Description: Select input equalization level, input 2

Bit	Bit Description	Default	R/W
7:6	00b: SDI 11, Input equalization disabled 01b: SDI 11, Small input equalization level 10b: SDI 11, Medium input equalization level 11b: SDI 11, Large input equalization level	00b	R/W
5:4	00b: SDI 10, Input equalization disabled 01b: SDI 10, Small input equalization level 10b: SDI 10, Medium input equalization level 11b: SDI 10, Large input equalization level	00b	R/W
3:2	00b: SDI 9, input equalization disabled 01b: SDI 9, Small input equalization level 10b: SDI 9, Medium input equalization level 11b: SDI 9, Large input equalization level	00b	R/W
1:0	00b: SDI 8, Input equalization disabled 01b: SDI 8, Small input equalization level 10b: SDI 8, Medium input equalization level 11b: SDI 8, Large input equalization level	00b	R/W

Register Address: 03h
Default: 00h
Register Name: Input EQ Config 3
Description: Select input equalization level, input 3

Bit	Bit Description	Default	R/W
7:6	00b: SDI 15, input equalization disabled 01b: SDI 15, Small input equalization level 10b: SDI 15, Medium input equalization level 11b: SDI 15, Large input equalization level	00b	R/W
5:4	00b: SDI 14, input equalization disabled 01b: SDI 14, Small input equalization level 10b: SDI 14, Medium input equalization level 11b: SDI 14, Large input equalization level	00b	R/W
3:2	00b: SDI 13, input equalization disabled 01b: SDI 13, Small input equalization level 10b: SDI 13, Medium input equalization level 11b: SDI 13, Large input equalization level	00b	R/W
1:0	00b: SDI 12, input equalization disabled 01b: SDI 12, Small input equalization level 10b: SDI 12, Medium input equalization level 11b: SDI 12, Large input equalization level	00b	R/W

Register Address: 04h
Default: 00h
Register Name: Input Polarity Flip 0
Description: Setting to a '1' inverts associated input, inputs 0 to 1

Bit	Bit Description	Default	R/W
7	0b: SDI 7, Input normal 1b: SDI 7, Input inverted	0b	R/W
6	0b: SDI 6, Input normal 1b: SDI 6, Input inverted	0b	R/W
5	0b: SDI 5, Input normal 1b: SDI 5, Input inverted	0b	R/W
4	0b: SDI 4, Input normal 1b: SDI 4, Input inverted	0b	R/W
3	0b: SDI 3, Input normal 1b: SDI 3, Input inverted	0b	R/W
2	0b: SDI 2, Input normal 1b: SDI 2, Input inverted	0b	R/W
1	0b: SDI 1, Input normal 1b: SDI 1, Input inverted	0b	R/W
0	0b: SDI 0, Input normal 1b: SDI 0, Input inverted	0b	R/W

Register Address: 05h
Default: 00h
Register Name: Input Polarity Flip 1
Description: Setting to a '1' inverts associated input, inputs 2 to 3

Bit	Bit Description	Default	R/W
7	0b: SDI 15, Input normal 1b: SDI 15, Input inverted	0b	R/W
6	0b: SDI 14, Input normal 1b: SDI 14, Input inverted	0b	R/W
5	0b: SDI 13, Input normal 1b: SDI 13, Input inverted	0b	R/W
4	0b: SDI 12, Input normal 1b: SDI 12, Input inverted	0b	R/W
3	0b: SDI 11, Input normal 1b: SDI 11, Input inverted	0b	R/W
2	0b: SDI 10, Input normal 1b: SDI 10, Input inverted	0b	R/W
1	0b: SDI 9, Input normal 1b: SDI 9, Input inverted	0b	R/W
0	0b: SDI 8, Input normal 1b: SDI 8, Input inverted	0b	R/W

Register Address: 06h
Default: 20h
Register Name: LOS Config/CLK EN
Description: Sets configuration for Loss of Signal alarm/Enables serial clock output buffer

Bit	Bit Description	Default	R/W
7:5	000b: 70 mV_{PPD} assert, 80 mV_{PPD} de-assert 001b: 80 mV_{PPD} assert, 90 mV_{PPD} de-assert [default] 010b: 90 mV_{PPD} assert, 100 mV_{PPD} de-assert 011b: 100 mV_{PPD} assert, 110 mV_{PPD} de-assert 100b: 110 mV_{PPD} assert, 120 mV_{PPD} de-assert 101b: 120 mV_{PPD} assert, 130 mV_{PPD} de-assert 110b: 130 mV_{PPD} assert, 140 mV_{PPD} de-assert 111b: LOS power down (globally applied for all input channels)	001b	R/W
4	0b: Normal LOS operation 1b: Force LOS to asserted	0b	R/W
3	0b: Squelch input upon LOS assertion 1b: Never squelch input upon LOS assertion	0b	R/W
2	0b: Squelch to logic high state 1b: Squelch to logic low state	0b	R/W
1	RSVD	0b	R/W
0	0b: Serial clock output is disabled 1b: Serial clock output is enabled (output level controlled by reg0Bh[3:2]	0b	R/W

Register Address: 07h
Default: 40h
Register Name: MUX Control 0
Description: MUX control for outputs 0 and 1 (M21350)

Bit	Bit Description	Default	R/W
7:6	Reserved	01b	R/W
5:4	MUX1 00: select input 4 to out1 [default] 01: select input 5 to out1 10: select input 6 to out1 11: select input 7 to out1	00b	R/W
3:2	Reserved	00b	R/W
1:0	MUX0 00: select input 0 to out0 [default] 01: select input 1 to out0 10: select input 2 to out0 11: select input 3 to out0	00b	R/W

Register Address: 07h
Default: 40h
Register Name: Xpoint control for outputs 0 and 1 (M21355)
Description: Selects the input that is selected for the serial data output

Bit	Bit Description	Default	R/W
7:4	0000: select input 0 to out1 0001: select input 1 to out1 0010: select input 2 to out1 0011: select input 3 to out1 0100:select input 4 to out1 [default] .... 1111: select input 15 to out1	0100b	R/W
3:0	0000: select input 0 to out0 [default] 0001: select input 1 to out0 0010: select input 2 to out0 0011: select input 3 to out0 0100:select input 4 to out0 .... 1111: select input 15 to out0	0000b	R/W

Register Address: 08h
Default: C8h
Register Name: MUX Control 1
Description: MUX control for outputs 2 and 3.

Bit	Bit Description	Default	R/W
7:6	Reserved	11b	R/W
[5:4]	MUX3 0: select input 12 to out3 [default] 01: select input 13 to out3 10: select input 14 to out3 11: select input 15 to out3	00b	R/W
3:2	Reserved	10b	R/W
[3:0]	MUX2 00: select input 8 to out2 [default] 01: select input 9 to out2 10: select input 10 to out2 11: select input 11 to out2	00b	R/W

Register Address: 08h
Default: C8h
Register Name: Xpoint control for outputs 2 and 3 (M21355)
Description: Selects the input that is selected for the serial data output

Bit	Bit Description	Default	R/W
7:4	0000: select input 0 to out3 0001: select input 1 to out3 0010: select input 2 to out3 0011: select input 3 to out3 .... 1100: select input 12 to out3 [default] .... 1111: select input 15 to out3	1100b	R/W
3:0	0000: select input 0 to out2 0001: select input 1 to out2 0010: select input 2 to out2 0011: select input 3 to out2 0100:select input 4 to out2 .... 1000:select input 8 to out2 [default] .... 1111: select input 15 to out2	1000b	R/W

Register Address: 09h
Default: 88h
Register Name: Data Output Control
Description: Sets output level and De-emphasis for SDO1 and SDO0

Bit	Bit Description	Default	R/W
7:6	00b: SDO 1 powered down 01b: SDO 1 output swing = 600 mV p-p 10b: SDO 1 output swing = 800 mV p-p 11b: SDO 1 output swing = 1200 mV p-p	10b	R/W
5:4	00b: SDO 1 de-emphasis off 01b: SDO 1 de-emphasis = small 10b: SDO 1 de-emphasis = medium 11b: SDO 1 de-emphasis = large	00b	R/W
3:2	00b: SDO 0 powered down 01b: SDO 0 output swing = 600 mV p-p 10b: SDO 0 output swing = 800 mV p-p 11b: SDO 0 output swing = 1200 mV p-p	10b	R/W
1:0	00b: SDO 0 de-emphasis off 01b: SDO 0 de-emphasis = small 10b: SDO 0 de-emphasis = medium 11b: SDO 0 de-emphasis = large	00b	R/W

Register Address: 0Ah
Default: 88h
Register Name: Data Output Control
Description: Sets output level and De-emphasis for SDO3 and SDO2

Bit	Bit Description	Default	R/W
7:6	00b: SDO 3 powered down 01b: SDO 3 output swing = 600 mV p-p 10b: SDO 3 output swing = 800 mV p-p 11b: SDO 3 output swing = 1200 mV p-p	10b	R/W
5:4	00b: SDO 3 de-emphasis off 01b: SDO 3 de-emphasis = small 10b: SDO 3 de-emphasis = medium 11b: SDO 3 de-emphasis = large	00b	R/W
3:2	00b: SDO 2 powered down 01b: SDO 2 output swing = 600 mV p-p 10b: SDO 2 output swing = 800 mV p-p 11b: SDO 2 output swing = 1200 mV p-p	10b	R/W
1:0	00b: SDO 2 de-emphasis off 01b: SDO 2 de-emphasis = small 10b: SDO 2 de-emphasis = medium 11b: SDO 2 de-emphasis = large	00b	R/W

Register Address: 0Bh
Default: 08h
Register Name: Clock and Data Output Control
Description: SDO mute control/Sets output level for SCO

Bit	Bit Description	Default	R/W
7	0b: SDO 3 output in normal operation 1b: SDO 3 output muted	0b	R/W
6	0b: SDO 2 output in normal operation 1b: SDO 2 output muted	0b	R/W
5	0b: SDO 1 output in normal operation 1b: SDO 1 output muted	0b	R/W
4	0b: SDO 0 output in normal operation 1b: SDO 0 output muted	0b	R/W
3:2	00b: SCO output powered down 01b: SCO output swing = 600 mV p-p 10b: SCO output swing = 800 mV p-p 11b: SCO output swing = 1200 mV p-p	10b	R/W
1:0	Select the recovered clock from Reclocker 0-3 to the SCO pin 00b: select clock from Reclocker 0 [default] 01b: select clock from Reclocker 1 10b: select clock from Reclocker 2 11b: select clock from Reclocker 3	00b	R/W

Register Address: 0Ch
Default: 02h
Register Name: Reserved
Description: Reserved

Bit	Bit Description	Default	R/W
7:0	Reserved	0000010b	R/W

Register Address: 0Dh
Default: 00h
Register Name: Global Control
Description: Controls Global Configuration

Bit	Bit Description	Default	R/W
7:4	Reserved	0000b	R/W
3	0b: Inputs that are not used are powered down 1b: All inputs are forced on; note that this increases power consumption	0b	R/W
2	Reserved	0b	R/W
1	0b: Input offset correction loop On (all inputs) 1b: Input offset correction loop Off (all inputs)	0b	R/W
0	0b: Normal Operation 1b: Global Power Down	0b	R/W

Register Address: 0Eh
Default: 00h
Register Name: Interrupt Control
Description: Sets configuration for xALARM Output pin

Bit	Bit Description	Default	R/W
7:4	Reserved	00000b	R/W
3	0b: xALARM output is used in Interrupt mode 1b: Alarm output is used in Status mode	0b	R/W
2:0	000b: xALARM pulse width = 140 ns 001b: xALARM pulse width = 180 ns 010b: xALARM pulse width = 200 ns 011b: xALARM pulse width = 300 ns 100b: xALARM pulse width = 450 ns 101b: xALARM pulse width = 800 ns 110b: xALARM pulse width = 1.5 µs 111b: xALARM pulse width = 2.8 µs Measured with a 10 kΩ pullup resistor. Actual pulse width varies with the value of the pullup resistor.	000b	R/W

Register Address: 0Fh
Default: 00h
Register Name: Memory Interface Configuration Control
Description: Defines the number of slave RCLK devices, controlled by quasi master/EEPROM (ranging from 0 to 39)

Bit	Bit Description	Default	R/W
7:6		00b	R/W
5:0	000000b: no slave RCLKs 000001b 1 slave RCLK 000010b: 2 slave RCLKs	000000b	R/W

5.2 Reclocker Configuration

Register Address: 11h
Default: 00h
Register Name: Group Reclocker Control 1
Description: Controls all reclockers as a group (Bits[3:0] require bit4=1b to take effect).

Bit	Bit Description	Default	R/W
7:5	Reserved	00b	R/W
4	0b: Normal operation 1b: All CDRs controlled through common “group mode” settings	0b	R/W
3:2	00b: ARD enabled for all Reclockers 01b: SD data rate forced for all Reclockers 10b: HD data rate forced for all Reclockers 11b: 3G data rate forced for all Reclockers	00b	R/W
1	0b: Normal operation for all Reclockers 1b: Bypass mode for all Reclockers	0b	R/W
0	0b: Normal operation for all Reclockers 1b: All Reclockers powered down	0b	R/W

Register Address: 12h
Default: 00h
Register Name: Reclocker Control 0
Description: Controls Reclocker 1/0

Bit	Bit Description	Default	R/W
7:6	00b: ARD enabled for Reclocker 1 01b: SD data rate forced for Reclocker 1 10b: HD data rate forced for Reclocker 1 11b: 3G data rate forced for Reclocker 1	00b	R/W
5	0b: Reclocker 1 Normal operation (Reclocker 1 not bypassed) 1b: Reclocker 1 bypassed	0b	R/W
4	0b: Normal operation 1b: Reclocker 1 powered down	0b	R/W
3:2	00b: ARD enabled for CD R0 01b: SD data rate forced for Reclocker 0 10b: HD data rate forced for Reclocker 0 11b: 3G data rate forced for Reclocker 0	00b	R/W
1	0b: Reclocker 0 Normal operation (Reclocker 0 not bypassed) 1b: Reclocker 0 bypassed	0b	R/W
0	0b: Normal operation 1b: Reclocker 0 powered down	0b	R/W

Register Address: 13h
Default: 00h
Register Name: Reclocker Control 1
Description: Controls Reclocker 3/2

Bit	Bit Description	Default	R/W
7:6	00b: ARD enabled for Reclocker 3 01b: SD data rate forced for Reclocker 3 10b: HD data rate forced for Reclocker 3 11b: 3G data rate forced for Reclocker 3	00b	R/W
5	0b: Reclocker 3 Normal operation (Reclocker 3 not bypassed) 1b: Reclocker 3 bypassed	0b	R/W
4	0b: Normal operation 1b: Reclocker 3 powered down	0b	R/W
3:2	00b: ARD enabled for Reclocker 2 01b: SD data rate forced for Reclocker 2 10b: HD data rate forced for Reclocker 2 11b: 3G data rate forced for Reclocker 2	00b	R/W
1	0b: Reclocker 2 Normal operation (Reclocker 2 not bypassed) 1b: Reclocker 2 bypassed	0b	R/W
0	0b: Normal operation 1b: Reclocker 2 powered down	0b	R/W

Register Address: 14h
Default: 00h
Register Name: Reclocker Control 1
Description: Controls Reclocker

Bit	Bit Description	Default	R/W
7:4	Reserved	0000b	R/W
3	0b: Normal operation 1b: Reclocker 3 auto-bypass feature disabled	0b	R/W
2	0b: Normal operation 1b: Reclocker 2 auto-bypass feature disabled	0b	R/W
1	0b: Normal operation 1b: Reclocker 1 auto-bypass feature disabled	0b	R/W
0	0b: Normal operation 1b: Reclocker 0 auto-bypass feature disabled	0b	R/W

Register Address: 16h
Default: 20h
Register Name: Reclocker BW Control
Description: Controls bandwidth of Reclocker

Bit	Bit Description	Default	R/W
7	Reserved	0b	R/W
6:4	000b: Reserved (do not use) 001b: 0.5 x Nominal LBW 010b: 1 x Nominal LBW 011b: 4 x Nominal LBW 100b: 2 x Nominal LBW 101b: 3 x Nominal LBW 110b: 1.5 x Nominal LBW 111b: 0.875 x Nominal LBW	010b	R/W
3:0	Reserved	0000b	R/W

Register Address: 18h
Default: 00h
Register Name: SD/xHD Algorithm Control
Description: Controls SD/xHD output of Reclocker

Bit	Bit Description	Default	R/W
7:6	Reserved	0b	R/W
5	0b: SD/xHD output conforms to case 1, Table 4-11 1b SD/xHD output conforms to case 2, Table 4-11	0b	R/W
4:0	Reserved	0000b	R/W

5.2.1 Checksum for Memory Interface Configuration

Register Address: 1Ah
Default: 55h
Register Name: Checksum
Description: Checksum value to be added to sum of reg 00h to 19h contents

Bit	Bit Description	Default	R/W
7:0	Checksum value	01010101b	R/W

5.2.2 Status/Monitoring

Register Address: 80h
Default: 00h
Register Name: Reset
Description: Does Master Reset on Device

Bit	Bit Description	Default	R/W
7:0	00h: Normal Operation AAh: Master Reset (must be set back to 00)	00000000b	R/W

Register Address: 81h
Default: 09h (**M21350**)
Register Name: Chip ID
Description: Chip Identification Number

Bit	Bit Description	Default	R/W
7:0	M21350	00001001b	R

Register Address: 81h
Default: 08h (**M21355**)
Register Name: Chip ID
Description: Chip Identification Number

Bit	Bit Description	Default	R/W
7:0	M21355	00001000b	R

Register Address: 82h
Default: 04h
Register Name: Chip Rev
Description: Chip Revision Number

Bit	Bit Description	Default	R/W
7:0	Chip revision	00000100b	R

Register Address: 83h
Default: 00h
Register Name: LOS Status 0
Description: Inputs 0-7, Set to a '1' when LOS asserted (single-event latched operation). Proper status is obtained after clearing all latched alarms by using Register 85h bit 0.

Bit	Bit Description	Default	R/W
7	0b: SDI 7, Input normal 1b: SDI 7, LOS Asserted	0b	R
6	0b: SDI 6, Input normal 1b: SDI 6, LOS Asserted	0b	R
5	0b: SDI 5, Input normal 1b: SDI 5, LOS Asserted	0b	R
4	0b: SDI 4, Input normal 1b: SDI 4, LOS Asserted	0b	R
3	0b: SDI 3, Input normal 1b: SDI 3, LOS Asserted	0b	R
2	0b: SDI 2, Input normal 1b: SDI 2, LOS Asserted	0b	R
1	0b: SDI 1, Input normal 1b: SDI 1, LOS Asserted	0b	R
0	0b: SDI 0, Input normal 1b: SDI 0, LOS Asserted	0b	R

Register Address: 84h
Default: 00h
Register Name: LOS Status 1
Description: Inputs 8-15 Set to a '1' when LOS asserted (single-event latched operation). Proper status is obtained after clearing all latched alarms by using Register 85h bit 0.

Bit	Bit Description	Default	R/W
7	0b: SDI 15, Input normal 1b: SDI 15, LOS Asserted	0b	R
6	0b: SDI 14, Input normal 1b: SDI 14, LOS Asserted	0b	R
5	0b: SDI 13, Input normal 1b: SDI 13, LOS Asserted	0b	R
4	0b: SDI 12, Input normal 1b: SDI 12, LOS Asserted	0b	R
3	0b: SDI 11, Input normal 1b: SDI 11, LOS Asserted	0b	R
2	0b: SDI 10, Input normal 1b: SDI 10, LOS Asserted	0b	R
1	0b: SDI 9, Input normal 1b: SDI 9, LOS Asserted	0b	R
0	0b: SDI 8, Input normal 1b: SDI 8, LOS Asserted	0b	R

Register Address: 85h
Default: 00h
Register Name: Alarm Clear
Description: lears Latched Alarms. To properly clear all alarm bits, write “1” followed by a “0” to bit 0.

Bit	Bit Description	Default	R/W
7:2	Reserved	000000b	R/W
1	0b: Normal operation 1b: Soft reset for CDR	0b	R/W
0	0b: Normal operation 1b: Clears all alarm bits in registers 83h, 84h and 88h (except reg88h[7])	0b	R/W

Register Address: 87h
Default: 00h
Register Name: Checksum result
Description: Shows the result of the checksum calculation

Bit	Bit Description	Default	R/W
7:0	Checksum result	00000000b	R/W

Register Address: 88h
Default: 00h
Register Name: Reclocker Status Register
Description: Reads status of the Reclocker. Proper status is obtained after clearing all latched alarms by using Register 85h bit 0.

Bit	Bit Description	Default	R/W
7:6	Reserved	00b	R
5	0b: Reference clock is present 1b: No reference clock detected	0b	R
4	0b: PLL locked 1b: PLL unlocked	0b	R
3	0b: Reclocker 3, locked 1b: Reclocker 3, un-locked	0b	R
2	0b: Reclocker 2, locked 1b: Reclocker 2, un-locked	0b	R
1	0b: Reclocker 1, locked 1b: Reclocker 1, un-locked	0b	R
0	0b: Reclocker 0, locked 1b: Reclocker 0, un-locked	0b	R

Register Address: 89h
Default: 00h
Register Name: Reclocker Rate Detect
Description: Reads data rate for Reclocker

Bit	Bit Description	Default	R/W
7:6	00b: Reclocker 3: Reclocker un-locked 01b: Reclocker 3: SD data rate detected 10b: Reclocker 3: HD data rate detected 11b: Reclocker 3: 3G data rate detected	00b	R
5:4	00b: Reclocker 2: Reclocker un-locked 01b: Reclocker 2: SD data rate detected 10b: Reclocker 2: HD data rate detected 11b: Reclocker 2: 3G data rate detected	00b	R
3:2	00b: Reclocker 1: Reclocker un-locked 01b: Reclocker 1: SD data rate detected 10b: Reclocker 1: HD data rate detected 11b: Reclocker 1: 3G data rate detected	00b	R
1:0	00b: Reclocker 0: Reclocker un-locked 01b: Reclocker 0: SD data rate detected 10b: Reclocker 0: HD data rate detected 11b: Reclocker 0: 3G data rate detected	00b	R

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