M21450

6.5 Gbps Dual-Channel Backplane Driver and Adaptive Equalizer with 2x2 Crosspoint Switch

The M21450 is a dual channel device designed to enable the transmission of multi gigabit serial data through the most challenging environments. The device features two independent adaptive equalizers that automatically equalize data at rates up to 6.5 Gbps. Control of key functions of the M21450 is provided through hardware pins, and full register control of the M21450 is provided through an I^2C compatible software control interface. The M21450 can also self-configure from an external EEPROM without the need for a host processor. For compatibility with PCI-Express and S-ATA/SAS systems, the M21450 is designed with an electrical idle pass-through function to drive the differential output to the common mode level during OOB signaling. Boundary scan is provided for high-speed input and output pins through a JTAG port, and the device is available in a 6x6 mm, 40-pin, QFN package.

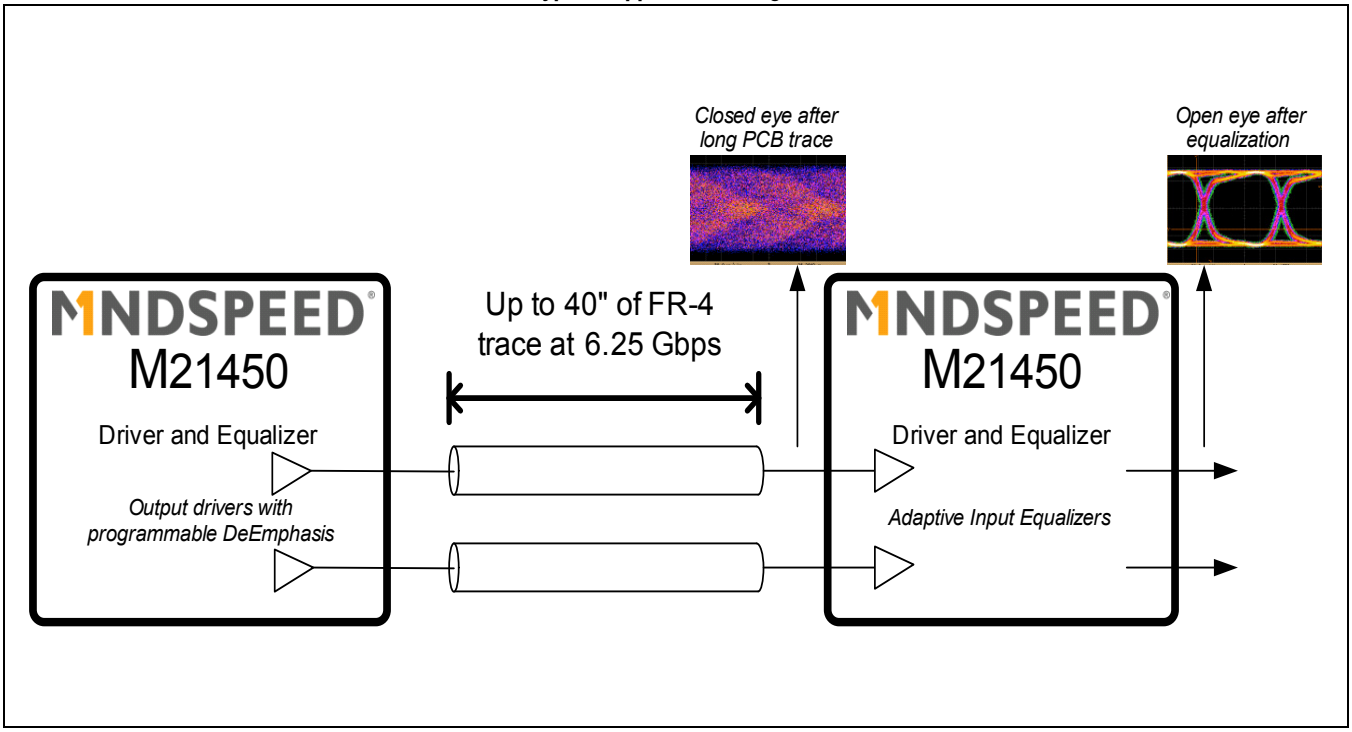
Features

- Adaptive Equalization for up to 40" of FR-4 PCB trace at 6.25 Gbps
- Supports electrical idle signaling for PCIe and OOB signaling for S-ATA/SAS
- Low power dissipation: 155 mW per channel, 310 mW total power at 1.2V
- Up to 40 dB of input equalization and 6 dB of output de-emphasis
- HW, SW, and EEPROM programmable
- 6x6 mm, 40-pin QFN package
- Extended operating case temperature range (-40°C to 85°C)
- Software configurable 2x2 Crosspoint Switch Matrix

Applications

XAUI	3.125 Gbps	6.25 Gbps	—
S-ATA/SAS	1.5 Gbps	3.0 Gbps	6.0 Gbps
PCIe	2.5 Gbps	5.0 Gbps	—
Fibre Channel	1.0625 Gbps	2.125 Gbps	4.25 Gbps
InfiniBand	2.5 Gbps	5.0 Gbps	—
SDI Video	270 Mbps	1.485 Gbps	2.97 Gbps
		1.485/1.001 Gbps	2.97/1.001 Gbps

Typical Application Diagram



Ordering Information

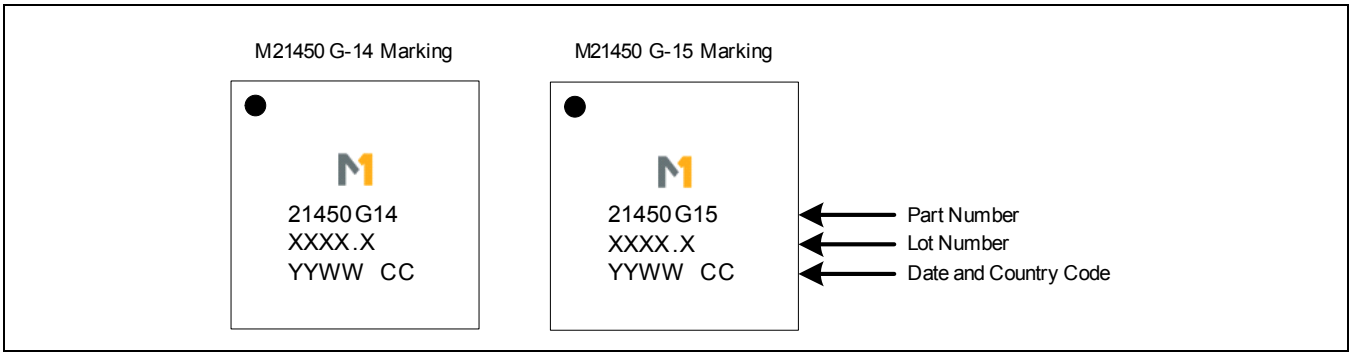
Part Number	Package	Operating Case Temperature
M21450G-14*	6x6 mm, 40-pin QFN package	-40°C to 85°C
M21450G-15*	6x6 mm, 40-pin QFN package	-40°C to 85°C

* The letter “G” designator after the part number indicates that the device is RoHS compliant. Refer to www.mindspeed.com for additional information. The RoHS compliant devices are backwards compatible with 225°C reflow profiles. The M21450G-14 device is optimized for applications that require the best input sensitivity performance, while the M21450G-15 is optimized for applications that require maximum immunity to system noise. Refer to Section 4.1 for additional details.

Revision History

Revision	Level	Date	Description
L	Released	September 2012	Updated power supply description in Section 4.2 to include power supply sequencing recommendation that V_{DDCORE} is powered up last.
K	Released	March 2012	Changed minimum operating case temperature from -20 °C to -40 °C.
J	Released	January 2011	Updated control pin type definitions to define inputs and outputs in Table 3-1.
I	Released	August 2010	Updated marking diagram to add legend. Updated Package Outline Drawing to match new package and height requirements (Figure 3-1). Updated default settings for input equalizer (Register Address 04h [3:0], Address 05h [7:4]). Removed 3.4 MHz I^2C data rate and reduced capacitor bus loading to 100 µF and 400 µF (Section 4.15).
H	Released	May 2010	Refer to prior revision for details on data sheet changes.
G	Released	March 2010	Refer to prior revision for details on data sheet changes.
F	Released	February 2010	Refer to prior revision for details on data sheet changes.
E	Released	November 2009	Refer to prior revision for details on data sheet changes.
D	Released	April 2009	Refer to prior revision for details on data sheet changes.
C	Released	December 2008	Refer to prior revision for details on data sheet changes.
B	Advance	September 2008	Refer to prior revision for details on data sheet changes.
A	Advance	August 2008	Initial release.

M21450 Marking Diagrams



1.0 Electrical Characteristics

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
AV_{DDIO}	Analog I/O power supply voltage	—	2.1	V
V_{DDCORE}	Core power supply voltage	—	1.5	V
DV_{DDIO}	Digital I/O power supply voltage	—	3.6	V
T_{STORE}	Storage Temperature	–65	150	°C
$V_{ESD, HBM}$	Electrostatic discharge voltage (HBM)	—	2000	V
$V_{ESD, CDM}$	Electrostatic discharge voltage (CDM)	—	500	V

NOTES:

Exposure of the device beyond the minimum/maximum limits may cause permanent damage.

Limits listed in the above table are stress limits only, and do not imply functional operation within these limits.

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
AV_{DDIO}	Analog I/O power supply voltage	1.14	1.2, 1.8	1.89	V
V_{DDCORE}	Core power supply voltage	1.14	1.2	1.26	V
DV_{DDIO}	Digital I/O power supply voltage (1)	1.14	1.2, 1.8, 2.5, 3.3	3.47	V
T_{CASE}	Case Temperature	–40	—	85	°C
θ_{JA}	Junction to ambient thermal resistance (no airflow)	—	34.4	—	°C/W
θ_{JA}	Junction to ambient thermal resistance (1.0 m/s airflow)	—	30	—	°C/W
θ_{JC}	Junction to case thermal resistance	—	3.3	—	°C/W

NOTES:

1. DV_{DDIO} must be 2.5V or 3.3V for operation in SIC or MIC mode. In HIC mode, DV_{DDIO} can be 1.2V, 1.8V, or 3.3V.

Table 1-3. Power Consumption Specifications

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
AI_{DDIO}	Analog I/O power supply current (AV_{DDIO} = 1.2V)	1	—	35	45	mA
AI_{DDIO}	Analog I/O power supply current (AV_{DDIO} = 1.8V)	2	—	65	75	mA
AI_{DDCORE}	Core power supply current (AV_{DDIO} = 1.2V)	1	—	220	275	mA
AI_{DDCORE}	Core power supply current (AV_{DDIO} = 1.8V)	2	—	240	290	mA
DI_{DDIO}	Digital I/O power supply current	—	—	2	—	mA
P_{TOTAL}	Total power dissipation (AV_{DDIO}=1.2V)	1, 3	—	310	405	mW
P_{TOTAL}	Total power dissipation (AV_{DDIO}=1.8V)	2, 3	—	360	510	mW

NOTES:

1. Valid with nominal (800 mV_{PPD}) output swing for both channels.
2. Valid with maximum (1500 mV_{PPD}) output swing for both channels.
3. Typical calculated with nominal current and voltage. Maximum calculated with maximum current and 5% over voltage.

Unless noted otherwise, specifications in this section are valid with AV_{DDIO} = 1.8V, 25°C case temperature, 800 mV differential input data swing, nominal (800 mV_{PPD}) output swing level, PRBS 2^{15} – 1 test pattern at 6.5 Gbps, R_{LOAD} = 50Ω, short cables and/or traces.

Table 1-4. Input/Output Electrical Characteristics

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
DR	NRZ Data Rate	—	100	—	6500	Mbps
V_{IN}	Input p-p differential voltage swing (AC-Coupled), voltage measured at the device input	—	200	—	2000	mV
V_L	Input launch amplitude (Voltage used to drive a signal across 40" of FR-4 trace)	—	500	—	—	mV_{PPD}
V_L	Input launch amplitude (Voltage used to drive a signal across 40" of FR-4 trace, pathological video pattern)	—	700	—	—	mV_{PPD}
R_{TERM}	PCML Input differential input impedance termination	—	80	100	120	Ω
V_{OH}	PCML single ended output logic-high	—	AV_{DDIO} - 0.05	—	AV_{DDIO}	V
V_{OD}	PCML p-p differential output swing	1, 2, 3, 6	350	—	1750	mV_{PPD}
t_R/t_F	PCML output rise/fall time (20–80%)	6	—	60	—	ps
t_{DJ}	Deterministic output jitter	4	—	35	200	mUI
t_{RJ}	Random output jitter	4	—	6	9	mUI RMS
t_{PD}	Propagation delay	—	—	1	—	ns
$t_{SKEW, CH}$	Channel to Channel Skew	—	—	100	—	ps
V_{IH}	CMOS Input logic high	—	0.85 x DV_{DDIO}	—	—	V
V_{IF}	CMOS input logic floating state	—	0.25 x DV_{DDIO}	—	0.75 x DV_{DDIO}	V
V_{IL}	CMOS input logic low	—	—	—	0.15 x DV_{DDIO}	V
V_{OH}	CMOS output logic high	5	0.9 x DV_{DDIO}	—	—	V
V_{OL}	CMOS output logic low	5	—	—	0.1 x DV_{DDIO}	V

NOTES:

1. AV_{DDIO} must be 1.8V to achieve higher than 800 mV output swing.
2. Output swing is specified with output de-emphasis disabled.
3. Six output swing levels can be selected. Output swing increases by approximately 200 mV with each setting. Refer to Figure 2-6 for typical performance.
4. Additive output jitter with minimal media length
5. Two-wire serial interface can drive 400 pF @ 100 kHz and 100 pF @ 400 kHz.
6. Measured using a CID pattern with a minimum CID length of 10 bits.

2.0 Typical Performance Characteristics

Unless noted otherwise, test conditions in this section are: AV_{DDIO} = 1.8V, 25°C case temperature, 800 mV differential input data swing, nominal (800 mV_{PPD}) output swing, PRBS 2^{15} - 1 test pattern at 6.5 Gbps, R_{LOAD} = 50Ω, short traces and/or cables.

Figure 2-1. Eye Diagram at 3.125 Gbps

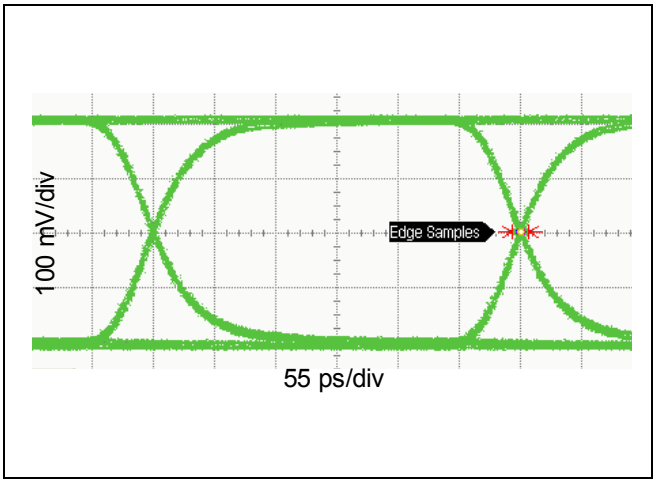


Figure 2-2. Eye Diagram at 6.25 Gbps

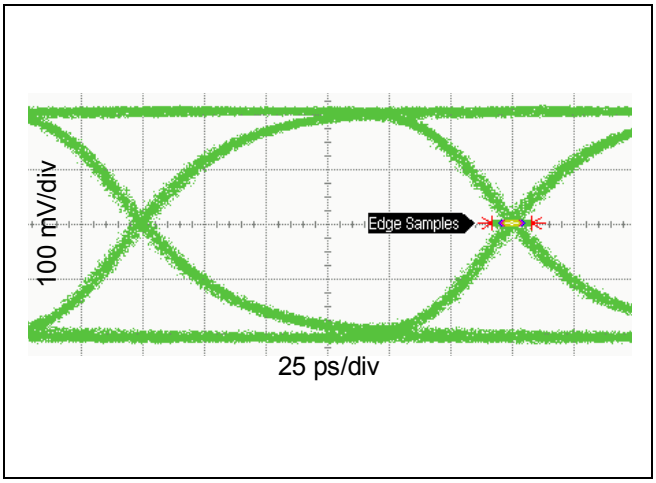


Figure 2-3. Eye Diagram at 5.0 Gbps

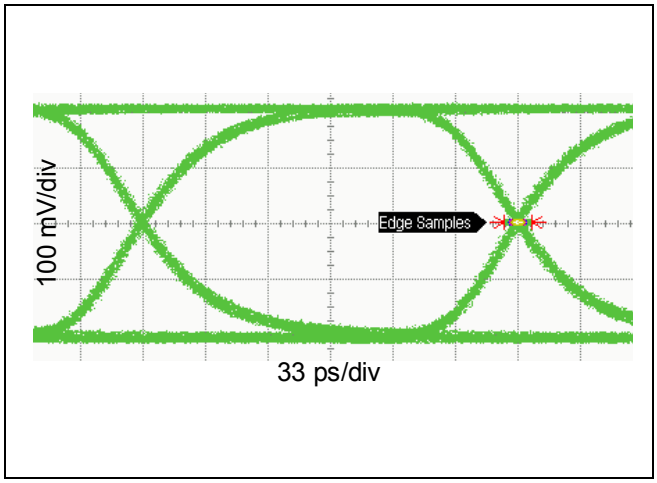


Figure 2-4. Output Waveform With COMWAKE OOB Signal

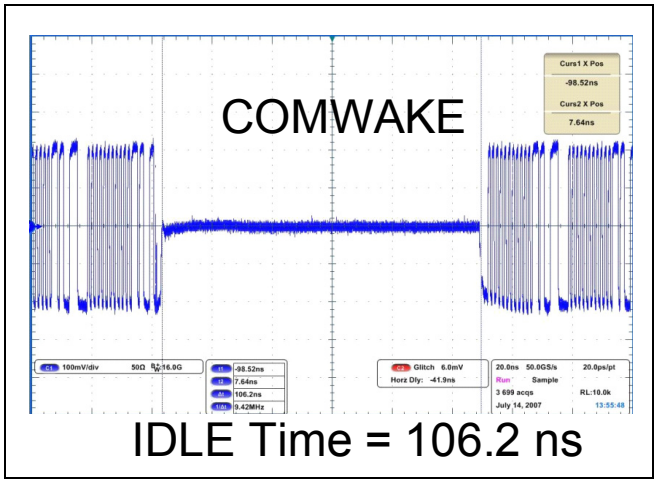


Figure 2-5. Eye Diagram after 40" of FR-4 trace

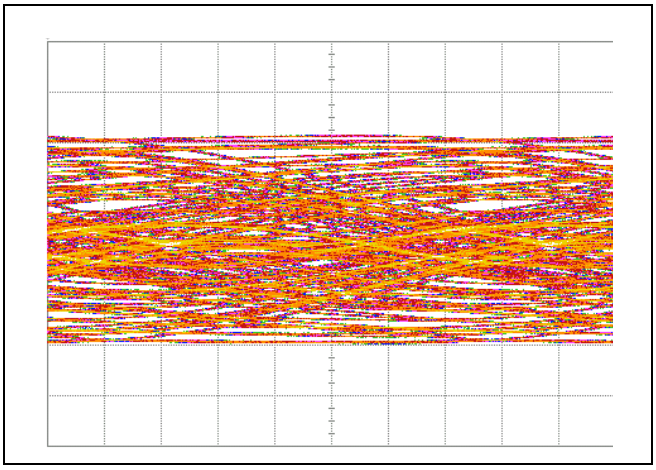


Figure 2-6. Differential Output Swing vs. OutctrlN[7:5] Setting as a Function of AV_{DDIO}

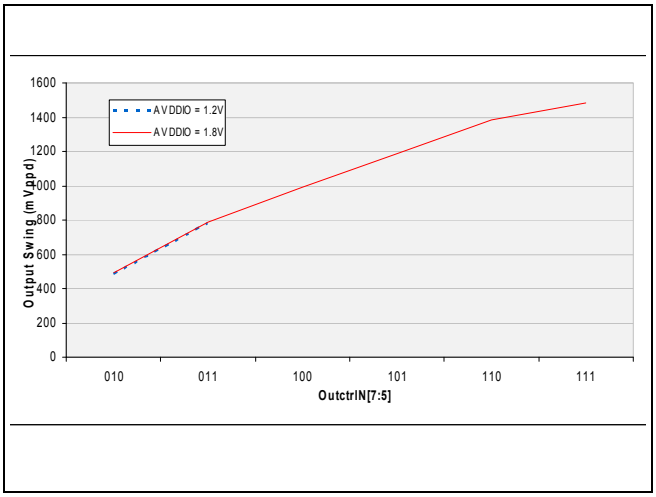


Figure 2-7. Eye Diagram after equalizing 40" of FR-4 trace at 6.0 Gbps

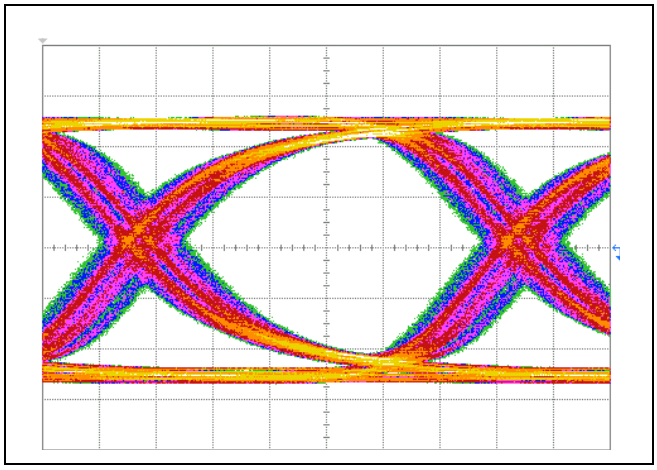


Figure 2-8. Deterministic Jitter vs Data Rate as a Function of FR-4 Trace Length

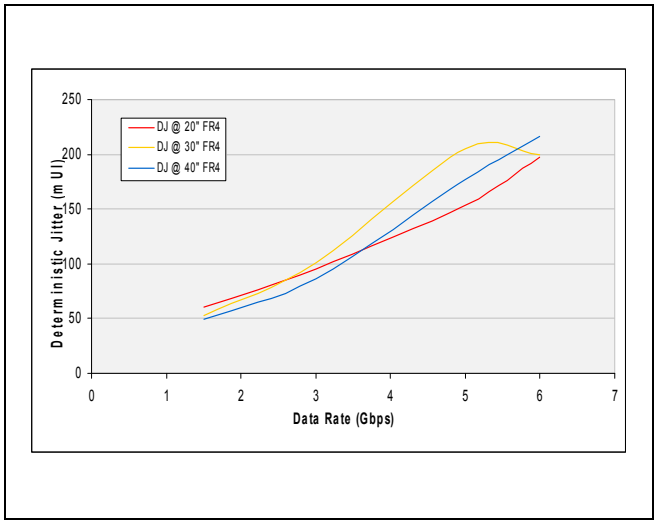


Figure 2-9. Random Jitter Distribution

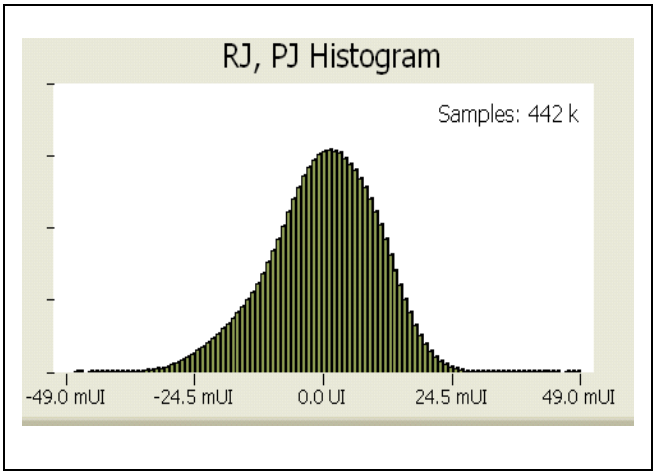


Figure 2-11. Bathtub Curve

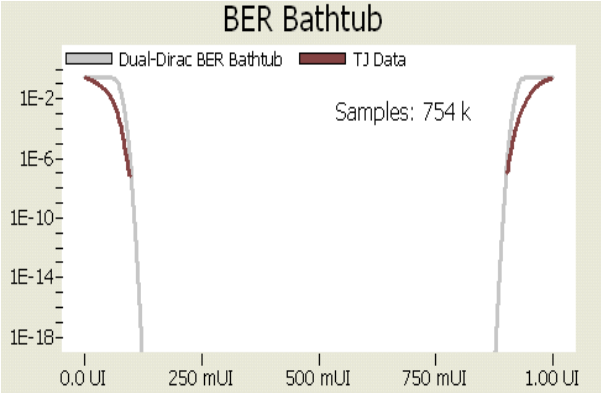


Figure 2-10. Deterministic Jitter vs Launch Amplitude as a Function of Data Rate (After Equalizing for 30" FR-4 trace)

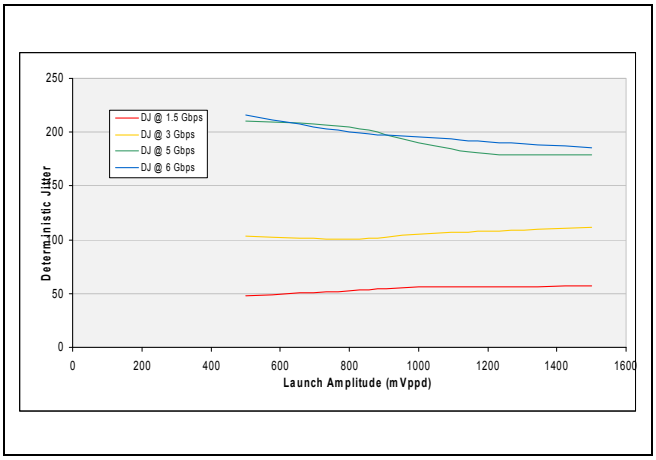
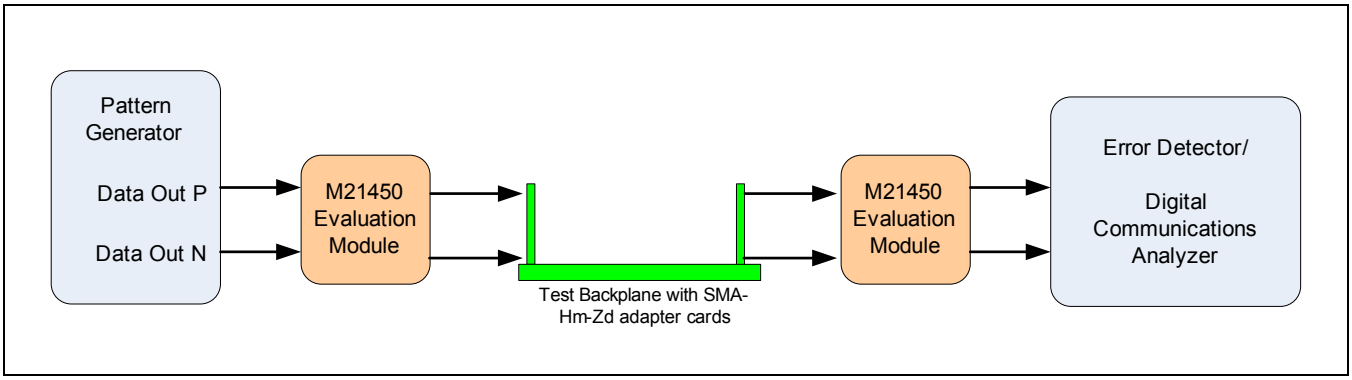


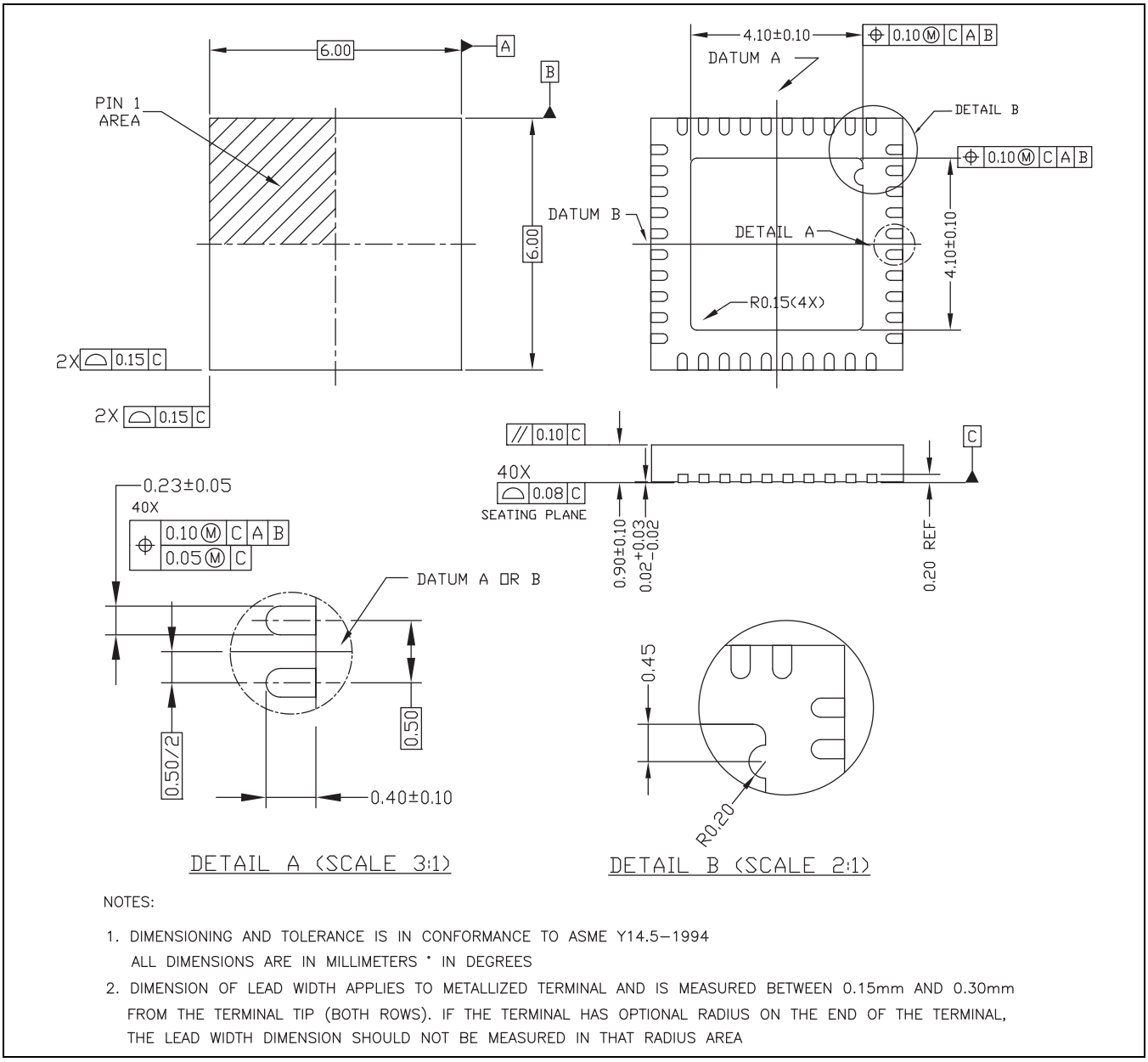
Figure 2-12. Input Equalization Test Setup Test Backplane



3.0 Package Outline Drawing, Pinout Diagram, and Package Description

The M21450 is assembled in 6x6 mm, 40-pin QFN packages. The exposed pad on the bottom of the package is used to provide the device ground connection as well as a thermal path.

Figure 3-1. Package Outline Drawing



NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5–1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

Figure 3-2. Pinout Diagram (Top View Shown)

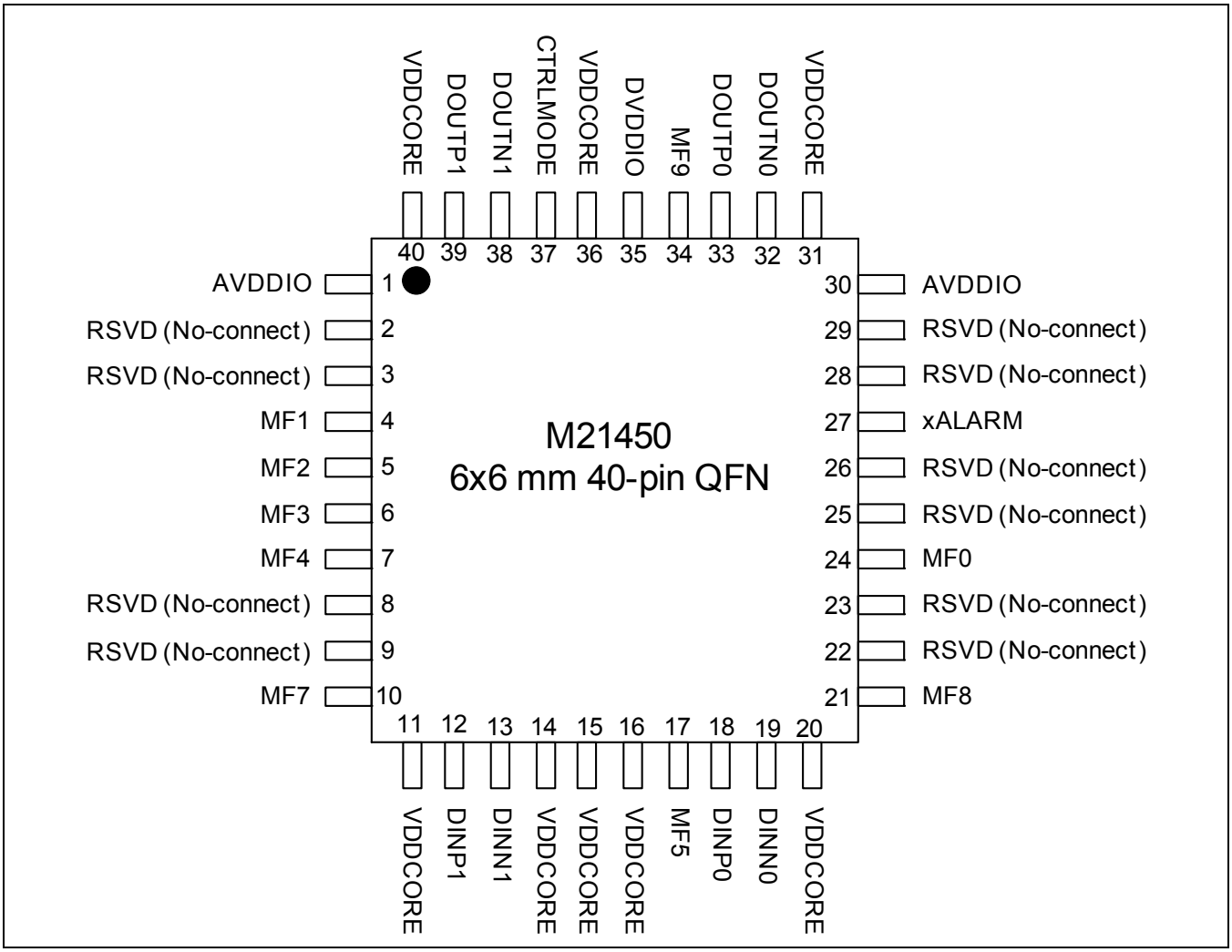


Table 3-1. M21450 Pin Descriptions

Pin Name	Pin Number(s)	Type	Description
AV_{DDIO}	1, 30	Power	Analog positive supply
DV_{DDIO}	35	Power	Digital positive supply
V_{DDCORE}	11, 14, 15, 16, 20, 31, 36, 40	Power	Core positive supply
GND	GND	Ground	Ground
MF0	24	CMOS input	Multifunction pin
MF1	4	CMOS input	Multifunction pin
MF2	5	CMOS input	Multifunction pin
MF3	6	CMOS input	Multifunction pin
MF4	7	CMOS input	Multifunction pin
MF5	17	CMOS input	Multifunction pin
MF7	10	CMOS input	Multifunction pin
MF8	21	CMOS output	Multifunction pin
MF9	34	CMOS output	Multifunction pin
CTRLMODE	37	CMOS input	Control Mode Select
xALARM (1)	27	CMOS output	Alarm output pin (1)
NC	2, 3, 8, 9, 22, 23, 25, 26, 28, 29	No connect	Do not connect
DINP1	12	PCML input	Channel 1 Input P
DINN1	13	PCML input	Channel 1 Input N
DINP0	18	PCML input	Channel 0 Input P
DINN0	19	PCML input	Channel 0 Input N
DOUTP1	39	PCML output	Channel 1 Output P
DOUTN1	38	PCML output	Channel 1 Output N
DOUTP0	33	PCML output	Channel 0 Output P
DOUTN0	32	PCML output	Channel 0 Output N

NOTES:

1. xALARM is an open drain output and should be connected to an external 10 kΩ pull-up resistor in system designs.

4.0 Functional Description

4.1 Device Versions

There are two revisions of the M21450 device available, the M21450G-14 and the M21450G-15. The M21450G-14 offers the highest input sensitivity for improved equalization performance with lossy backplanes. The M21450G-15 device offers increased immunity to system noise during electrical idle signaling with a reduction in input sensitivity. Applications that do not use electrical idle signaling or where the system noise floor is below 50 mV_{PPD} should use the M21450G-14 for increased equalization performance. Applications that use electrical idle signaling and have system noise above 50 mV_{PPD} should use the M21450G-15 for increased noise immunity during electrical idle signal periods.

4.2 Power Supply

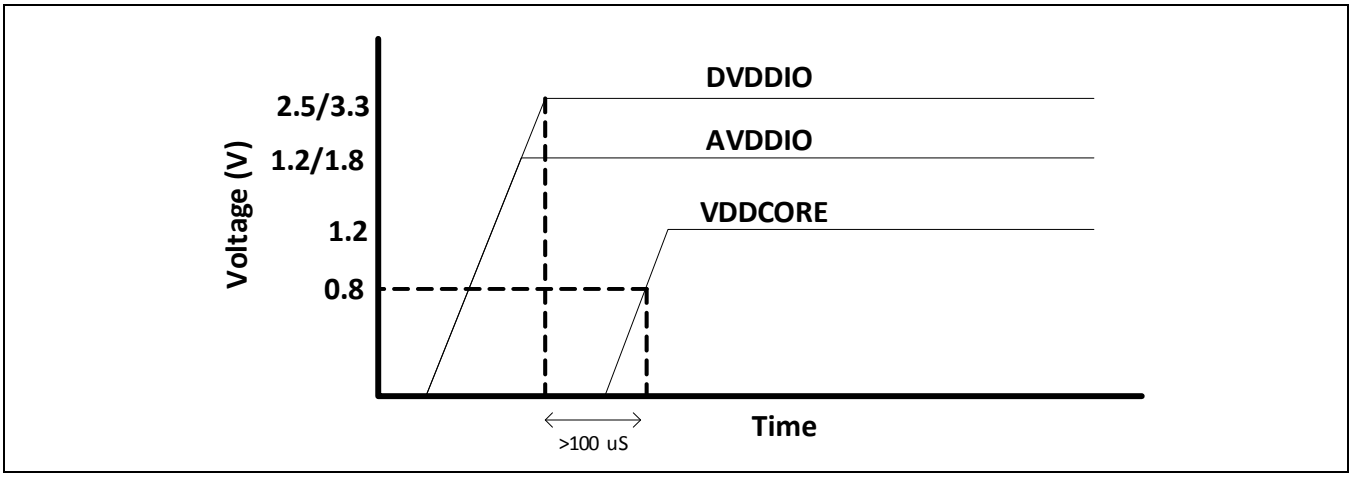
The M21450 includes three distinct power supply domains: V_{DDCORE}, AV_{DDIO}, and DV_{DDIO}.

AV_{DDIO} powers the input/output circuits in the device, and can be set to either 1.2V or 1.8V. Note that to achieve output swing levels higher than 800 mV_{PPD}, AV_{DDIO} must be set to 1.8V.

DV_{DDIO} powers the digital circuitry within the device, and can be set to 1.2V, 1.8V, 2.5V, or 3.3V to allow for interface with various external digital devices. It is recommended that DV_{DDIO} is connected to the same voltage level as any digital devices that are used to control the M21450.

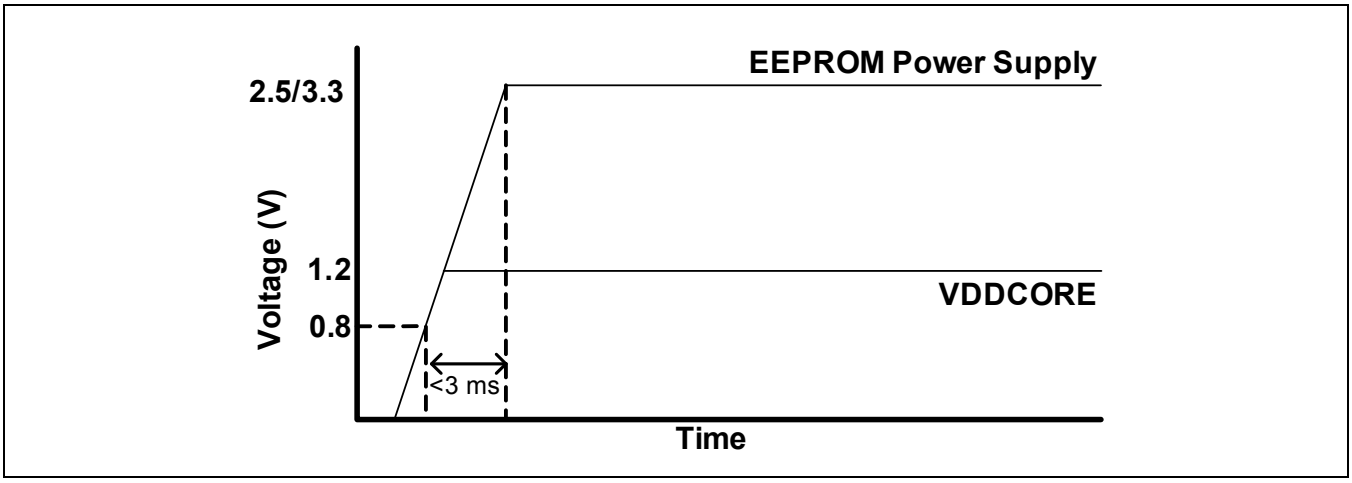
V_{DDCORE} powers the analog and digital core circuitry in the device, and must be set to 1.2V. A power-on reset (POR) is issued when V_{DDCORE} reaches approximately 0.8 V during power up. To eliminate any potential issues related to the POR, the power supplies should be sequenced such that AV_{DDIO} and DV_{DDIO} are powered up and stable a minimum of 100 µs before V_{DDCORE} reaches 0.8 V during power up. Figure 4-1 below shows the recommended power supply ramp sequence for the M21450.

Figure 4-1. Power Supply Timing Sequence



When the M21450 is operated in memory interface control (MIC) mode, the external EEPROM must be powered up and stable before the M21450 is powered up to ensure that the automatic register download occurs without errors. When the M21450 is operated in memory interface control (MIC) mode, the EEPROM must be powered up and stable within 3 ms of V_{DDCORE} reaching approximately 0.8V to ensure that the register download from the EEPROM is robust. Note that in MIC mode, the startup current on DV_{DDIO} could be as high as 50 mA until V_{DDCORE} is powered up. The device will issue a power on reset (POR) when V_{DDCORE} reaches approximately 0.8V during the power supply ramp. After the POR is complete, the device will poll the ADDR pins to determine which control mode the device is configured for. If the device is configured for MIC operation, it will attempt to communicate with the on-board EEPROM for register download immediately after the POR is complete. If the EEPROM does not respond within approximately 3 ms after the POR, the M21450 will stop trying to communicate with the EEPROM and the MIC download will fail. See below for the recommended power supply ramp up timing in MIC mode.

Figure 4-2. Recommended EEPROM Power Supply Ramp up in MIC Mode



4.3 Control Options

There are three control modes available for the M21450. For control without a programming interface, the device can be configured for Hardware Interface Control (HIC) operation. To control using a two wire, I^2C compatible programming interface, the device can be configured for Software Interface Control (SIC). The M21450 can also self configure from an external EEPROM when the Memory Interface Control (MIC) mode is selected. In addition to the three control modes, the M21450 also supports boundary scan.

To select the control mode, configure the CTRLMODE and MF0 pins as shown:

Table 4-1. Control Mode

Operating Mode	CTRLMODE pin	MF0 pin
Hardware Interface Control	L	N/A
Software Interface Control	H	L
Memory Interface Control (EEPROM control)	H	H
Boundary Scan	F	F

4.4 Multifunction Pins

The M21450 contains a series of multifunction pins, whose functionality changes depending on the control mode configuration of the device. Each multifunction pin is designed to support three different logic levels, high, low, and floating state. The floating state logic level is achieved by floating the pin, connecting it to a high impedance source, or driving to a voltage equal to $DV_{DDIO}/2$. The multifunction control pins do not include any on-chip pullup/pulldown resistors in order to support three state logic on these pins. The table below summarizes the functionality of the multifunction pins (MF[9:0]) for each control mode. More details on the functionality of the MF pins are included in the description sections for each control mode.

Table 4-2. Multifunction Pins

Pin	Functionality in Hardware Interface Control mode	Functionality in Software/ Memory Interface Control mode	Functionality in Boundary Scan mode
MF0	Output de-emphasis enable	Memory Interface Control enable	F
MF1	Output swing level	SDA	TMS
MF2	RSVD Must be connected to logic low	SCL	TCLK
MF3	Input Eq (M21450-14 only, MF3 must be tied L when the M21450-15 is used in HIC mode)	ADDR0	Not used
MF4	RSVD Must be connected to logic high	ADDR1	Not used
MF5	RSVD Must be connected to logic high	ADDR2	Not used
MF7	RSVD	RSVD	TDI
MF8	RSVD	RSVD	TDO
MF9	EI/LOS Enable	Strobe (MIC mode)	Not used

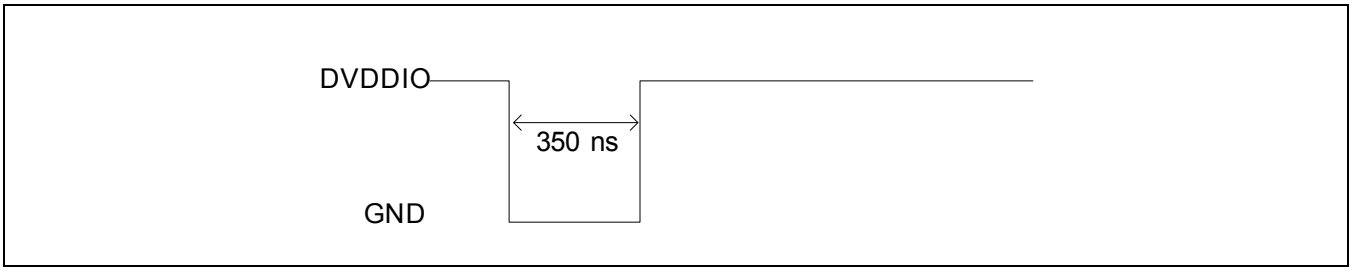
4.5 Input and Output Buffers

The input buffers in the M21450 are designed to work with AC coupled input signals, and support operation with a wide range of AC coupling capacitor values. Applications that use PRBS and/or 8b/10b encoded data will typically use AC coupling capacitors with a value of 0.1 µF. SDI video applications will typically use AC coupling capacitors with a value of 10 µF or larger. The output buffers are designed with PCML logic, and can operate with either AC coupled or DC coupled systems. The input and output buffers include 50Ω internal terminations and support boundary scan. For PCIe applications where support for PCIe receiver detection is needed, an external termination circuit should be designed on the system board. Please refer to the Mindspeed Applications Note titled “PCI Express Receiver Detection with Mindspeed Signal Conditioners” for more details on using this device to support PCIe receiver detection.

4.6 LOS Alarm

There is signal detect circuit that will assert an alarm if the signal level at the input of the device is lower than approximately 100 mV_{PPD}. Once asserted, the alarm will remain asserted until the signal is above approximately 200 mV_{PPD}. There is hysteresis between the assert and de-assert levels to prevent chattering of the LOS alarm. When the input voltage level is between 100 mV_{PPD} and 200 mV_{PPD}, the LOS alarm can be high or low. The LOS circuit should be disabled when used with strings of 1010 data that last for more than approx 3 µs to avoid false LOS alarms. When the M21450 is configured for operation in SIC/MIC mode, the xALARM hardware pin operates as an interrupt signal by default and will generate an interrupt signal with a pulse width of approximately 350 ns when there is an alarm on any input channel. See Figure 4-2 below for an example of the timing of the xALARM interrupt signal.

Figure 4-3. Timing of xALARM Interrupt Signal



To configure the device so that the xALARM pin acts as a status indicator rather than an interrupt signal, register address 87h[2] is used. When the M21450 is used in HIC mode, the xALARM pin acts as a status indicator, and is a static L when there is an alarm condition and static H where all alarms are clear.

4.7 Input Equalization

Each input channel of the M21450 includes an input equalizer, designed to compensate for bandwidth limitations of PCB traces. The equalizer can operate in the adaptive mode or in a manual mode, where a fixed equalization setting is selected. In the adaptive equalization mode, the equalizer will select the optimal equalization setting for the backplane type and length connected to the input. The input equalization is configured using pin MF3 when the device is in HIC mode (M21450-14 only, MF3 must be tied low when using the M21450-15 in HIC mode), and through register addresses 04h and 05h when the device is in SIC/MIC mode.

4.8 Output De-emphasis

Each output buffer of the M21450 includes a de-emphasis circuit that is manually configured by the user. There is approximately 6 dB of de-emphasis available, and the de-emphasis levels are selectable. The output de-emphasis is controlled by pin MF0 when the device is in HIC mode, and register addresses 07h and 08h when the device is in SIC/MIC mode.

4.9 Electrical Idle Pass-through

Some protocols, such as SATA/SAS and PCIe, define a third logic state at the common mode for transmission of an electrical idle level. In SAS/SATA systems, OOB signals such as COMRESET, COMWAKE, and COMSAS utilize burst and idle levels for communication. The M21450 is designed to pass the electrical idle (EI) through the device to support SATA/SAS and PCIe protocol requirements. When the EI feature of the M21450 is enabled, the device

will detect and pass EI signals with minimal distortion of the signal. The EI feature is enabled/disabled through pin MF9 when the device is in HIC mode, and through register address 01h when the device is in SIC/MIC mode.

When the M21450 is used in SIC or MIC mode, register address 2Fh can be used to vary the input voltage threshold when the device is in electrical idle mode. Higher values increase the input voltage threshold (higher immunity to noise), lower values decrease the input voltage threshold for signal detection (less immunity to noise, increased sensitivity to small signals for longer equalizer reach).

4.10 Squelch

To avoid random chattering of the output due to noise when there is no signal present at the inputs, the M21450 includes a squelch feature to automatically inhibit the output when there is a LOS alarm. This feature can be disabled if desired, and there is an option to inhibit to either logic H, logic L, or the electrical idle (common mode) level on squelch. In addition to the automatic squelch feature, a manual squelch can be forced using register 0Bh. When the M21450 is in hardware interface control mode and the EI feature is enabled, the LOS alarm does not squelch the device output when there is a LOS condition. When the M21450 is in software interface control mode or memory interface control mode, LOS should either be disabled or set to “never squelch” when the EI circuit is enabled to allow the device to detect data bursts quickly after electrical idle periods that last longer than approximately 5 µs. LOS can be set to "never squelch" by setting bits [7:6] of register 0Bh to 00h.

4.11 Crosspoint Switch Core

When the M21450 is used in SIC or MIC mode, the 2x2 crosspoint switch is configured using register address 0Dh. Refer to Section 5.0 for details on configuring the crosspoint switch. When the M21450 is used in HIC mode, the crosspoint switch configuration is fixed such that input 0 is routed to output 0, and input 1 is routed to output 1.

4.12 Operation in SDI Video Applications

Pathological data patterns found in SDI digital video applications stress the control circuitry in the adaptive equalization loops of the M21450 and limit the equalization performance of the device. For this reason, the adaptive equalization of the M21450 should be disabled and the manual equalization mode of the device should be used in SDI video applications. With the M21450 in manual equalization mode, the device can pass pathological video data error-free for SD-SDI, HD-SDI, and 3G-SDI data rates. In addition to putting the device into manual equalization mode, the following register settings should be set in applications when the device is used with pathological video data patterns.

Table 4-3. Recommended Register Settings for SDI Video Applications (1 of 2)

Register Name	Address	Default Value	Recommended Value	Description
Equalizer Configuration	02h	C0h	40h	Disable adaptive equalization
Input 1 Manual Equalization Setting	04h	77h	Determined by the system channel	Set manual equalization level
Input 0 Manual Equalization Setting	05h	77h	Determined by the system channel	Set manual equalization level
SDI Video Configuration A, Input 1	25h	00h	F0h	Increase low frequency gain

Table 4-3. Recommended Register Settings for SDI Video Applications (2 of 2)

Register Name	Address	Default Value	Recommended Value	Description
SDI Video Configuration A, Input 0	26h	00h	F0h	Increase low frequency gain
SDI Video Configuration B, Input 1	29h	00h	40h	Enable manual setting of low frequency gain
SDI Video Configuration B, Input 0	2Ah	00h	40h	Enable manual setting of low frequency gain

For optimum performance with long strings of consecutive bits found in pathological patterns, 10 µF or larger value AC coupling capacitors should be used on the inputs of the M21450.

4.13 Boundary Scan Operation

In order to test external connections to and from the M21450, the device includes support for boundary scan through a JTAG port when configured for boundary scan mode. The device is put in this mode by setting MF0 = F and CTRLMODE = F.

When the device is in boundary scan mode, the following pins are used for the JTAG port:

Table 4-4. Boundary Scan Mode Functionality

Pin Name	Pin Number	Functionality in Boundary Scan Mode
MF1	4	TMS
MF2	5	TCLK
MF7	10	TDI
MF8	21	TDO

For the input pins, the M21450 supports AC-coupled interconnects with edge rates faster than 20 ns. The clock rate should be less than 10 MHz. The input scan cells are built as single-ended, self-referenced edge detectors, such that for a differential input two signals are created (allowing for independent testing of p/n connections).

For the output pins, the scan signal is injected into the output signal path and will be driven out differentially (one digital signal is used per differential output). The scan signal is muxed in before the 2x2 crosspoint core, so if a particular crosspoint switch state is being used during the scan test, the scan signal will be switched as well.

4.14 Hardware Interface Control Mode Operation

With the M21450 configured for Hardware Interface Control (HIC) operation, the MF pins are used to control various functions for the device. The table below describes the functionality of the MF pins when the device is configured for HIC operation.

Table 4-5. Functionality of MF pins in Hardware Interface Control mode

Pin	Pin Number	Name	Functionality in Hardware Interface Control mode
MF0	24	OutDe enable	L = Output De-emphasis disabled (0 dB) on all high-speed outputs F = Approximately 3 dB of de-emphasis on all high-speed outputs H = Approximately 6 dB of de-emphasis on all high-speed output
MF1	4	Output level	L = Approximately 800 mV_{PPD} output swing selected for all high-speed output buffers (AV_{DDIO} = 1.2V or 1.8V) F = Approximately 1200 mV_{PPD} output swing selected for all high-speed output buffers (AV_{DDIO} = 1.8V only) H = Approximately 1500 mV_{PPD} output swing selected for all high-speed output buffers (AV_{DDIO} = 1.8V only)
MF2	5	RSVD	Reserved, connect to logic low
MF3	6	Input Eq	Input Eq selects equalization settings for all input channels as follows. **Note**: This applies to the M21450-14 only. MF3 must be tied low when using the M21450-15 in HIC mode. The M21450-15 operates with adaptive equalization only in HIC mode. L = Adaptive equalization mode F = Manual equalization, medium equalization level H = Manual equalization, maximum equalization level
MF4, MF5	7, 17	RSVD	Reserved, connect to logic high
MF7	10	RSVD	Reserved, do not connect
MF8	21	RSVD	Reserved, do not connect
MF9	34	EI/LOS Enable	L = EI Disabled, LOS Disabled F = EI Disabled, LOS Enabled (Output will squelch to common mode when LOS alarm is asserted) H = EI Enabled, LOS Enabled (Output will not squelch when LOS alarm is asserted)

4.15 Software Interface Control Mode Operation

With the M21450 configured for Software Interface Control (SIC) operation, the functionality of the M21450 is controlled through register settings. Refer to Table 5-1 for a full description of the registers available within the M21450. To access the registers, an I^2C compatible, two-wire programming interface is available in the device. SDA is used for data transfer and is mapped to MF1 when the M21450 is configured for SIC operation. SCL is used for the clock signal and is mapped to the pin MF2 when the M21450 is configured for SIC operation. There are no internal pull-up resistors on the SDA and SCL pins of the M21450. External pull-up resistors should be connected to the SDA and SCL pins when using the two-wire programming interface.The two-wire device address is determined by the status of the pins MF[5:3]. The table below shows the address for each combination of settings for MF[5:3]

Table 4-6. Two Wire Serial Device Address List

MF[5:3} Setting	7-bit Device address
LLL	0100000
LLH	0100001
LHL	0100010
LHH	0100011
HLL	0100100
HLH	0100101
HHL	0100110
HHH	0100111
LLF	0101000
LHF	0101001
HLF	0101010
HHF	0101011
LFL	0101100
LFH	0101101
HFL	0101110
HFH	0101111
FLL	0110000
FLH	0110001
FHL	0110010
FHH	0110011
LFF	0110100
HFF	0110101
FLF	0110110
FHF	0110111
FFL	0111000
FFH	0111001
FFF	0111010

The two wire programming interface is designed to drive 400 pF @ 100 kHz and 100 pF @ 400 kHz operation. During a write operation, data is latched into the M21450 registers on the rising edge of SCL during the acknowledge phase (ACK) of communication. Refer to the I^2C bus specification standard for more details on the two wire programming interface.

4.16 Memory Interface Control Mode Operation

With the M21450 configured for Memory Interface Control (MIC) operation, a single M21450 device or an array of M21450 devices can self configure from a single EEPROM with a two wire serial programming interface upon device power-up. After the M21450 has self configured, the device reverts to SIC operation to allow an optional host controller to modify the register settings of the M21450.

If the M21450 is configured for MIC operation at power up, the lead M21450 interface operates as a temporary two wire quasi-master operating at 100 kHz when downloading from external memory and 400 kHz when configuring other M21450 devices. In an array of M21450 devices, only one device should be configured for MIC operation, and subsequent devices in the array should be configured for SIC operation. All devices in an array will receive the same configuration. As a quasi-master, the M21450 will drive pin MICSTROBE low during power up to indicate that the self configuration is in process. When the M21450 device begins to self configure, it will read the contents of an external EEPROM and configure its registers accordingly. The expected EEPROM device address is 1010000b, and the M21450 quasi master device address should be set to 0100000b. The EEPROM should be powered-up and stable before the M21450 is powered-up in MIC mode to ensure that the automatic register download occurs without errors. Please refer to Figure 4-1 for the recommended power supply ramp up timing in MIC mode.

Register 1Fh is used to load the checksum seed value. The checksum seed value should be selected such that the 8 LSB of the sum of the register values from address 00h through 2Fh is equal to 2Eh. After the download from the EEPROM, the checksum value is computed and written into register address FCh. If the checksum value is equal to 2Eh, then this is recognized as a valid checksum and the quasi-master device will continue to program other device on the interface buss. If the checksum value is not equal to 2Eh, the quasi master device will repeat the download process and look for the correct checksum value up to 512 times before timing out. If the correct checksum value is not detected, the quasi-master device will not configure any additional devices on the interface bus, but the quasi-master will be programed with the contents of the EEPROM.

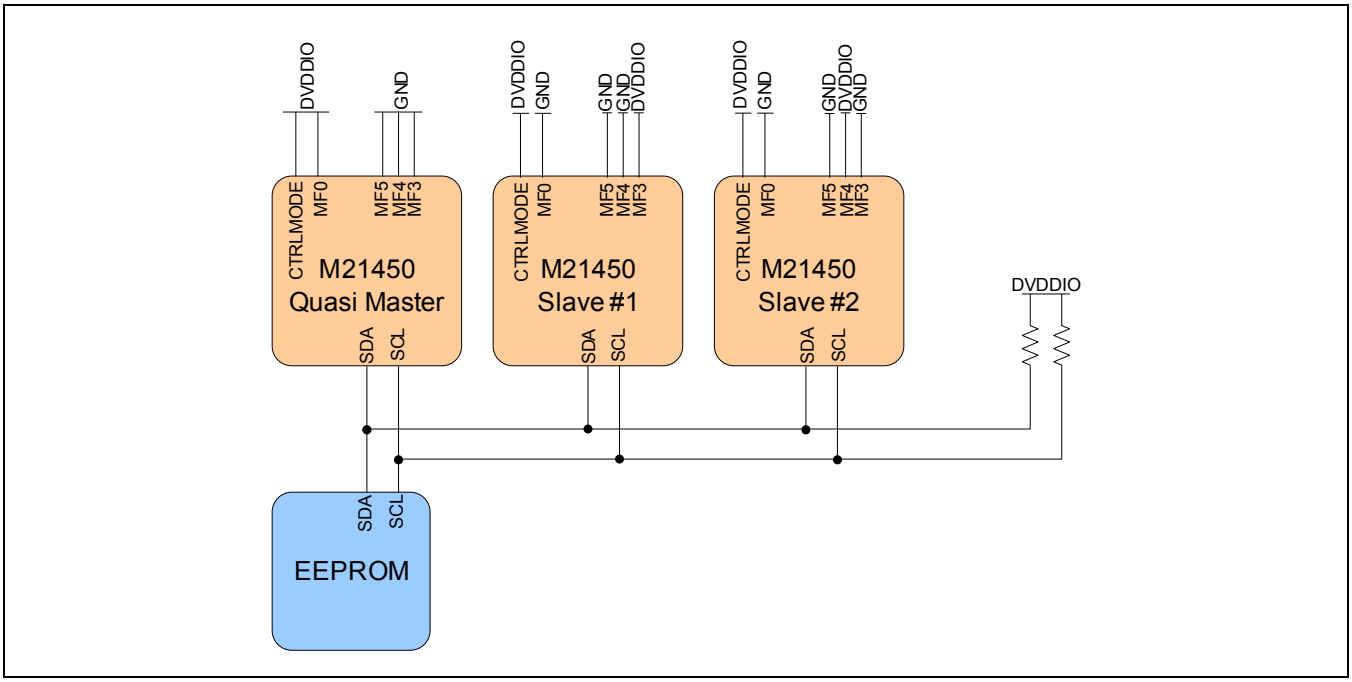
Register address 0Ch is used to identify the number of M21450 that will be self configured by the quasi master in MIC mode. When multiple M21450 devices are self configured in an array, the quasi master M21450 device will copy its register contents into other devices in the array sequentially using a 400 kHz interface bus. The devices in the array must have sequential programming addresses, starting with 0100000b for the quasi master device. After the last device in the M21450 has been configured, the pin MICSTROBE on the quasi master M21450 will be driven high, and the device will revert to SIC operation.

If the MIC mode is used in conjunction with an external host controller, the two wire interface on the host controller must not interrupt the programming buss while self configuration is taking place. This can be ensured by timing out the host controller for N x 0.8 seconds (N= number of M21450 devices in the self configure array), by monitoring the SDA/SCL buss for activity, or by monitoring the MICSTROBE pin on the quasi master device.

The device will issue a power on reset (POR) when V_{DDCORE} reaches approximately 0.8V during the power supply ramp. After the POR is complete, the device will poll the ADDR pins to determine which control mode the device is configured for. If the device is configured for MIC operation, it will attempt to communicate with the onboard EEPROM for register download immediately after the POR is complete. If there is no response from the EEPROM within approximately 3 ms after the POR is complete, the M21450 will stop trying to communicate with the EEPROM and the register download will fail. Please refer to Figure 4-1 for the recommended power supply ramp up timing in MIC mode.

Figure 4-3 below illustrates the connections necessary to self-configure three M21450 devices using MIC mode. The first M21450 device (quasi master) is configured for operation in MIC mode, and the other two devices (Slave #1 and Slave #2) are configured for SIC operation with consecutive programming addresses.

Figure 4-4. M21450 MIC System Diagram



5.0 Control Registers Map and Descriptions

Table 5-1. M21450 Register Summary

Address	Register Name	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0	Default	R/W
00h	Reserved	MSPD								01h	R/W
01h	devctrl1	standby	MSPD			ebi_enable	MSPD			00h (M21450G-14) 08h (M21450G-15)	R/W
02h	eqconfig	eqen		pd_dcoff	MSPD		polflip0	polflip1	MSPD	C0h	R/W
03h	inctrl	MSPD		in0pwr		in1pwr		MSPD		FFh	R/W
04h	maneqlvl1	eqlvl1				MSPD				77h (M21450-14) FFh (M21450-15)	R/W
05h	maneqlvl0	MSPD				eqlvl0				77h (M21450-14) FFh (M21450-15)	R/W
06h	Reserved	MSPD								60h	R/W
07h	outctrl1	outlvl			MSPD	delvl		de_freq	MSPD	60h	R/W
08h	outctrl0	outlvl			MSPD	delvl		de_freq	MSPD	60h	R/W
09h	Reserved	MSPD								60h	R/W
0Ah	alarm configuration	MSPD		xLOS_en	MSPD				clear_alarm	CAh	R/W
0Bh	squelch	sqlevel		squelch	sqtime	MSPD				C0h (M21450G-14) 00h (M21450G-15)	R/W
0Ch	micreg	micdev					MSPD			00h	R/W
0Dh	xpointctrl	MSPD		xstate0		xstate1		MSPD		E4h	R/W
0Eh - 0Fh	Reserved	MSPD								00h	R/W
10h	Reserved	MSPD								30h	R/W
11h - 1Eh	Reserved	MSPD								00h	R/W
1Fh	Checksum	Seed value for MIC checksum								55h	R/W
20h - 24h	Reserved	MSPD								00h	R/W
25h	SDI Video_A 1	SDI Gain Channel 1				MSPD				00h	R/W
26h	SDI Video_A 0	SDI Gain Channel 0				MSPD				00h	R/W
27h - 28h	Reserved	MSPD								00h	R/W

Table 5-1. M21450 Register Summary

Address	Register Name	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0	Default	R/W
29h	SDI Video_B 1	MSPD	SDI_en 1	MSPD						00h	R/W
2Ah	SDI Video_B 0	MSPD	SDI_en 0	MSPD						00h	R/W
2Bh - 2Eh	Reserved	MSPD								00h	R/W
2Fh	ei_threshold	MSPD				EI Threshold adjustment				00h (M21450-14) 07h (M21450-15)	R/W
30h - 7Fh	Reserved	MSPD								00h	R/W
80h	reset	reset								00h	R/W
81h	chip_id	chip_id								B1h	R
82h	chip_rev	chip_rev								—*	R
83h	alarm	MSPD	chan0 LOS	chan1 LOS	MSPD					N/A	R
87h	alarm_int	MSPD				alarm_mode	MSPD			04h	R/W
FCh	MIC Checksum	Computed Checksum Value								00h	R

* See register description for details on contents of the chip revision register (address 82h).

Address 01h—Device Control 1

Bits	Type	Default	Label	Description
7	R/W	0	standby	0: Power Up—Normal operation. 1: Power Down—Standby operation.
6:4	R/W	000	MSPD	Reserved, set to 000.
3	R/W	0 for M21450G-14 1 for M21450G-15	ebi_enable	0: Disable EI state pass through mode. 1: Enable EI state pass through mode.
2:0	RSVD	000	MSPD	Reserved, set to 000

Address 02h—Equalizer Configuration

Bits	Type	Default	Label	Description
[7:6]	R/W	11	eqen	00: Disable input equalization. 01: Enable manual equalization mode. 10: Invalid setting—Do not use. 11: Enable adaptive equalization mode.
5	R/W	0	pd_dcoff	0: DC offset correction loop enabled. 1: DC offset correction loop disabled.
4:3	R/W	00	MSPD	Reserved, set to 00.
2	R/W	0	polflip0	0: Normal polarity for input 0. 1: Invert polarity for input 0 (reverse INP and INN connections).
1	R/W	0	polflip1	0: Normal polarity for input 1. 1: Invert polarity for input 1 (reverse INP and INN connections).
0	R/W	0	MSPD	Reserved, set to 0.

Address 03h—Input Buffer Control

Bits	Type	Default	Label	Description
[7:6]	R/W	11	MSPD	Reserved, set to 11.
[5:4]	R/W	11	in0pwr	00: Power down input 0 with high impedance (>100 kΩ single ended, 100Ω differential) termination. 01: Power down input 0 with source 50Ω single-ended (100Ω differential) termination. 10: Enable input 0 with high impedance (>100 kΩ single ended, 100Ω differential) termination. 11: Enable input 0 with source 50Ω single-ended (100Ω differential) termination.
[3:2]	R/W	11	in1pwr	00: Power down input 1 with high impedance(>100 kΩ single ended, 100Ω differential) termination. 01: Power down input 1 with source 50Ω single-ended (100Ω differential) termination. 10: Enable input 1 with high impedance (>100 kΩ single ended, 100Ω differential) termination. 11: Enable input 1 with source 50Ω single-ended (100Ω differential) termination.
[1:0]	R/W	11	MSPD	Reserved, set to 11.

Address 04h—Input 1 Manual Equalization Setting

Bits	Type	Default	Label	Description
[7:4]	R/W	0111 (M21450-14) 1111 (M21450-15)	eqlvl1	Input equalization settings for input 1 when manual equalization mode is enabled. 1111: Minimum equalization 1110: Low equalization .... 1000: Medium equalization 0000: Medium equalization .... 0110: High equalization 0111: Maximum equalization Input equalization is programmed using sign magnitude encoding, with 1111 being the lowest eq setting and 0111 being the highest eq setting.
[3:0]	R/W	0111 (M21450-14) 1111 (M21450-15)	MSPD	Reserved.

Address 05h—Input 0 Manual Equalization Setting

Bits	Type	Default	Label	Description
[7:4]	R/W	0111 (M21450-14) 1111 (M21450-15)	MSPD	Reserved.
[3:0]	R/W	0111 (M21450-14) 1111 (M21450-15)	eqlvl0	Input equalization settings for input 0 when manual equalization mode is enabled. 1111: Minimum equalization 1110: Low equalization .... 1000: Medium equalization 0000: Medium equalization .... 0110: High equalization 0111: Maximum equalization Input equalization is programmed using sign magnitude encoding, with 1111 being the lowest eq setting and 0111 being the highest eq setting.

Address 07h, 08h —Output Buffer Control (address 07h = output 1, address 08h = output 0)

Bits	Type	Default	Label	Description
[7:5]	R/W	011	outlvl	Sets the output swing level. 00x: Power Down 010: Minimum Output Swing (approximately 500 mV_{PPD}) ... 111: Maximum Output Swing (approximately 1500 mV_{PPD}) **Note:** Refer to Figure 2-6 for typical output swing levels for each register setting.
4	RSVD	0	MSPD	Reserved, set to 0
[3:2]	R/W	00	delvl	Controls output de-emphasis. 00: Output de-emphasis disabled. 01: Approximately 2 dB de-emphasis. 10: Approximately 4 dB de-emphasis. 11: Approximately 6 dB de-emphasis.
1	R/W	0	de_freq	0: Nominal time constant for output de-emphasis. 1: High time constant for output de-emphasis.
0	RSVD	0	MSPD	Reserved, set to 0.

Address 0Ah—Alarm Configuration

Bits	Type	Default	Label	Description
[7:6]	RSVD	11	MSPD	Reserved, set to 11.
5	R/W	0	xLOS_en	0: Enable LOS circuit 1: Disable and power down LOS circuit
[4:1]	RSVD	0101	MSPD	Reserved, set to 0101.
0	R/W	0	clear_alarm	0: Normal operation. 1: Clear alarm registers. (Note: To clear alarms, set this bit to '1', then set back to '0' for normal operation)

Address 0Bh—Squelch Control

Bits	Type	Default	Label	Description
[7:6]	R/W	11 for M21450G-14 00 for M21450G-15	sqlevel	00: Never squelch output. 01: Output H on LOS (recommended for DC coupled outputs). 10: Output L on LOS (recommended for DC coupled outputs). 11: Output EI level on LOS (recommended for AC coupled outputs).
[5]	R/W	0	squelch	0: Normal operation. 1: Force squelch to level determined by sqlevel setting (bits [7:6]).
[4]	R/W	0	sqtime	Squelch enable time. 0: Declare LOS after approx 5 µs of no input data. 1: Declare LOS after approx 1 µs of no input data.
[3:0]	RSVD	0000	MSPD	Reserved, set to 0000.

Address 0Ch—Memory Interface Control Mode Registers

Bits	Type	Default	Label	Description
[7:3]	R/W	00000	micdev	Identifies the number of M21450 devices on the bus for Memory Interface Control mode. 00000: No additional M21450 devices on serial bus. 11010: Maximum number (26) of additional M21450 devices on serial bus.
[2:0]	RSVD	000	MSPD	Reserved, set to 000.

Address 0Dh—Crosspoint Switch Control

Bits	Type	Default	Label	Description
[7:6]	R/W	11	MSPD	Reserved, set to 11.
[5:4]	R/W	10	xstate0	00: Not used. 01: Route input 1 to output 0. 10: Route input 0 to output 0. 11: Not used.
[3:2]	R/W	01	xstate1	00: Not used. 01: Route input 1 to output 1. 10: Route input 0 to output 1. 11: Not used.
[1:0]	R/W	00	MSPD	Reserved, set to 00.

Address 1Fh—Checksum

Bits	Type	Default	Label	Description
[7:0]	R/W	01010101	Checksum seed value	Used with MIC mode. Adjust the value of register 1Fh so that the sum of the value of registers from 00h-2Fh is equal to 2Eh in order to compute a valid checksum after the EEPROM download.

Address 25h, 26h—SDI Video Configuration A (address 25h = channel 1, address 26h = channel 0)

Bits	Type	Default	Label	Description
[7:4]	R/W	0000	SDI Gain	Sets the amount of low frequency gain when bit 6 of register 29h/2Ah is set to 1. If bit 6 of register 29h/2Ah is set to 0, the low frequency gain is automatically determined by the device (for applications that use 8B/10B and PRBS data patterns, this register should be left at it's default value). 0111: Minimum low frequency gain …. 0000: Nominal low frequency gain 1000: Nominal low frequency gain …. 1111: Highest low frequency gain (recommended setting for SDI video for best performance with pathological patterns) The low frequency gain is programmed using sign magnitude encoding, with 1111 being the lowest setting and 0111 being the highest setting.
[3:0]	R/W	0000	MSPD	Reserved, set to 0000

Address 29h, 2Ah—SDI Video Configuration B (address 29h = channel 1, address 2Ah = channel 0)

Bits	Type	Default	Label	Description
[7]	R/W	0	MSPD	Reserved, set to 0
[6]	R/W	0	SDI_en	0: Disable manual low frequency gain setting using SDI Video Configuration A Register 1: Enable manual low frequency gain setting using SDI Video Configuration A Register (recommended for SDI video)
[5:0]	R/W	000000	MSPD	Reserved, set to 000000

Address 2Fh—Electrical Idle Threshold Adjustment

Bits	Type	Default	Label	Description
[7:4]	R/W	0000	MSPD	Reserved, set to 0000
[3:0]	R/W	0000 (M21450-14) 0111 (M21450-15)	EI Thresh	Use these register bits to vary the input voltage threshold when the device is in Electrical Idle mode. Higher values increase the voltage threshold (higher immunity to noise), lower values decrease the voltage threshold for signal detection (less immunity to noise, increased sensitivity to small signals for longer equalizer reach). 1111: Minimum EI threshold 1110: Low EI threshold .... 1000: Medium EI threshold 0000: Medium EI threshold .... 0110: High EI threshold 0111: Maximum EI threshold The EI threshold is programmed using sign magnitude encoding, with 1111 being the lowest setting and 0111 being the highest setting.

Address 80h—Reset

Bits	Type	Default	Label	Description
[7:0]	R/W	00000000	reset	00: Normal operation. AA: Reset mode. (Note, to reset the device, write AAh followed by a second write of 00h)

Address 81h—Chip Identification

Bits	Type	Default	Label	Description
[7:0]	R	10110001	chip_id	Device identification register.

Address 82h—Chip Revision

Bits	Type	Default	Label	Description
[7:0]	R	—	chip_rev	Device revision register. M21450-14 = 05h M21450-15 = 09h

Address 83h—Alarm Status

Bits	Type	Default	Label	Description
7	RSVD	N/A	MSPD	Reserved, may contain undefined values when read.
6	R	N/A	chan0 LOS	0: No alarm for input channel 0. 1: LOS alarm for input channel 0.
5	R	N/A	chan1 LOS	0: No alarm for input channel 1. 1: LOS alarm for input channel 1.
[4:0]	RSVD	N/A	MSPD	Reserved, may contain undefined values when read.

Address 87h—Alarm Interrupt Mode Control

Bits	Type	Default	Label	Description
[7:4]	RSVD	0000	MSPD	Reserved, set to 0000.
3	R/W	0	alarm_mode	0: Interrupt mode while in Software/Memory Interface Control mode. 1: Status mode for alarm output pin while in Software/Memory Interface Control mode.
[2:0]	RSVD	100	MSPD	Reserved, set to 100.

Address FCh—MIC Checksum

Bits	Type	Default	Label	Description
[7:0]	R	00000000	MIC Checksum Calculated Value	After an EEPROM download, this register contains the checksum calculated value. If this value is not equal to 2Eh after the EEPROM download, there was either an issue with the download or the checksum seed value in register 1Fh is not correct.

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